



# THE DATASHEET OF ADSP-21565KSWZ10



# SHARC+ Single Core High Performance DSP (Up to 1 GHz)

**ADSP-21562/21563/21565/21566/21567/21569**

## SYSTEM FEATURES

Enhanced SHARC+ high performance floating-point core

Up to 1 GHz

5 Mb (640 kB) Level 1 (L1) SRAM memory with parity  
(optional ability to configure as cache)

32-bit, 40-bit, and 64-bit floating-point support

32-bit fixed point

Byte, short word, word, long word addressed

Powerful DMA system

On-chip memory protection

Integrated safety features

17 mm × 17 mm, 400-ball CSP\_BGA (0.8 mm pitch), RoHS  
compliant

120-lead LQFP\_EP (0.4 mm pitch), RoHS compliant

Low system power across automotive temperature range

## MEMORY

Large on-chip Level 2 (L2) SRAM with ECC protection, up to  
8 Mb (1 MB)

One Level 3 (L3) interface optimized for low system power,  
providing 16-bit interface to DDR3/DDR3L SDRAM devices

## ADDITIONAL FEATURES

Security and Protection

Crypto hardware accelerators

Fast secure boot with IP protection

Enhanced FIR and IIR accelerators running up to 1 GHz

AEC-Q100 qualified for automotive applications

## APPLICATIONS

Automotive: audio amplifier, head unit, ANC/RNC, rear seat  
entertainment, digital cockpit, ADAS

Consumer: speakers, sound bars, AVRs, conferencing sys-  
tems, mixing consoles, microphone arrays, headphones

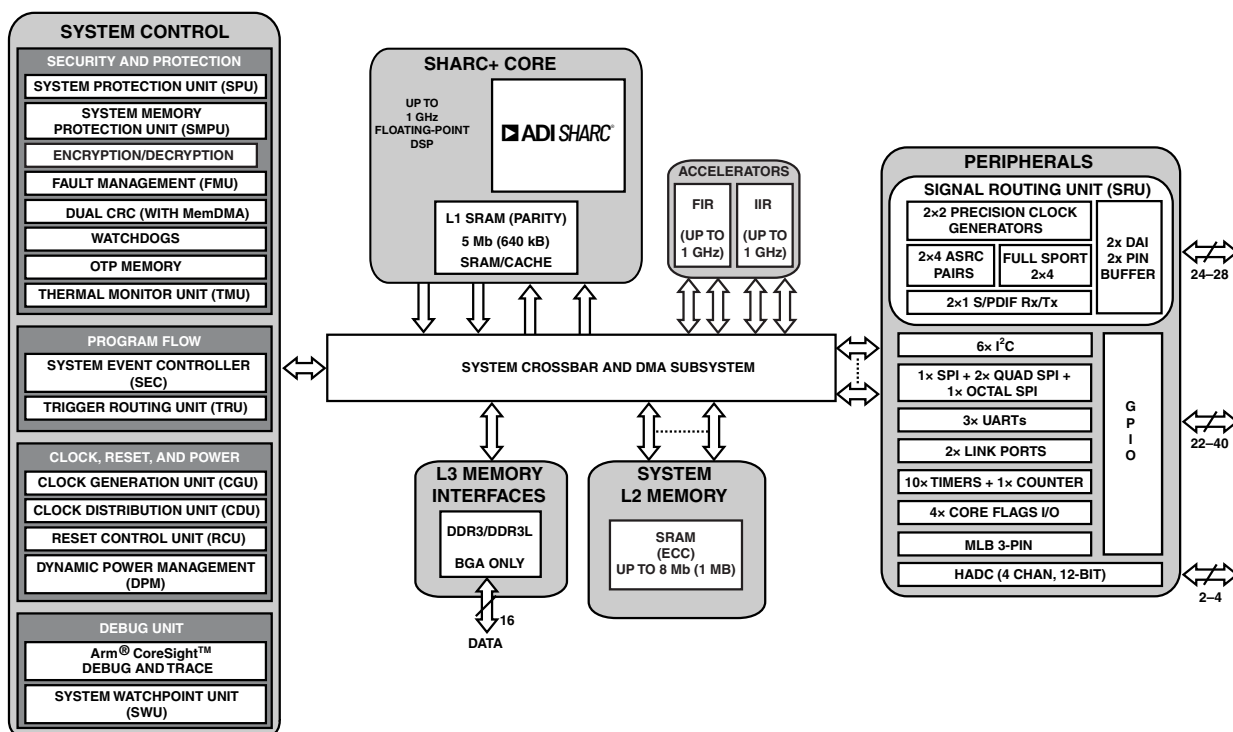


Figure 1. ADSP-21569 (Full-Featured Model) Processor Block Diagram

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## Rev. D

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## REVISION HISTORY

### 6/2023—Rev. C to Rev. D

|                                                                                                                |    |
|----------------------------------------------------------------------------------------------------------------|----|
| Changes to Footnote 2 and Footnote 3 in <a href="#">LPs—Receive ...</a>                                        | 55 |
| Change to coplanarity dimension from 0.12 mm to 0.20 mm for BC-400-3 BGA in <a href="#">Outline Dimensions</a> | 99 |

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## GENERAL DESCRIPTION

Reaching speeds of up to 1 GHz, the ADSP-2156x processors are members of the SHARC<sup>®</sup> family of products. The ADSP-2156x processor is based on the SHARC+<sup>®</sup> single core. The ADSP-2156x SHARC processors are members of the SIMD SHARC family of digital signal processors (DSPs) that feature Analog Devices, Inc., Super Harvard Architecture. These 32-bit/40-bit/64-bit floating-point processors are optimized for high performance audio/floating-point applications with large on-chip static random-access memory (SRAM), multiple internal buses that eliminate input/output (I/O) bottlenecks, and innovative digital audio interfaces (DAI). New additions to the

SHARC+ core include cache enhancements and branch prediction, while maintaining instruction set compatibility to previous SHARC products.

By integrating a rich set of industry-leading system peripherals and memory (see [Table 1](#)), the SHARC+ processor is the platform of choice for applications that require programmability similar to reduced instruction set computing (RISC), multimedia support, and leading edge signal processing in one integrated package. These applications span a wide array of markets, including automotive, professional audio, and industrial-based applications that require high floating-point performance.

**Table 1. Processor Features<sup>1</sup>**

| Processor Feature                      | ADSP-21562             | ADSP-21563 | ADSP-21565 | ADSP-21566       | ADSP-21567 | ADSP-21569 |
|----------------------------------------|------------------------|------------|------------|------------------|------------|------------|
| SHARC+ Core (MHz Maximum) <sup>2</sup> | 400                    | 600, 800   | 800, 1000  | 400              | 600, 800   | 800, 1000  |
| SHARC L1 SRAM (kB)                     | 640                    |            |            |                  |            |            |
| System Memory                          |                        |            |            |                  |            |            |
| L2 SRAM (kB)                           | 256                    | 512        | 1024       | 256              | 512        | 1024       |
| DDR3 and DDR3L Controller (16-Bit)     | N/A                    |            |            | 1                |            |            |
| DAI (Includes SRU)                     | 2                      |            |            |                  |            |            |
| Full SPORTs                            | 2 × 4                  |            |            |                  |            |            |
| S/PDIF Rx/Tx                           | 2 × 1                  |            |            |                  |            |            |
| ASRCs                                  | 2 × 4                  |            |            |                  |            |            |
| Precision Clock Generators             | 2 × 2                  |            |            |                  |            |            |
| Buffers                                | 2 × 12                 |            |            | 2 × 14           |            |            |
| Hardware Accelerators                  |                        |            |            |                  |            |            |
| FIR/IIR                                | Yes                    |            |            |                  |            |            |
| Security Crypto Engine                 | Yes                    |            |            |                  |            |            |
| I <sup>2</sup> C (TWI)                 | 4                      |            |            | 6                |            |            |
| SPI                                    | 1                      |            |            |                  |            |            |
| Quad SPI                               | 2                      |            |            |                  |            |            |
| Octal SPI                              | 1                      |            |            |                  |            |            |
| UARTs                                  | 2                      |            |            | 3                |            |            |
| Link Port                              | 0                      |            |            | 2                |            |            |
| General-Purpose Timer <sup>3</sup>     | 6                      |            |            | 10               |            |            |
| General-Purpose Counter                | 1                      |            |            |                  |            |            |
| Multichannel 12-bit ADC                | 2-ch                   |            |            | 4-ch             |            |            |
| Watchdog Timer                         | 2                      |            |            |                  |            |            |
| MLB 3-pin                              | Automotive models only |            |            |                  |            |            |
| GPIO Ports                             | Port A to Port B       |            |            | Port A to Port C |            |            |
| GPIO + DAI Pins                        | 22 + 24                |            |            | 40 + 28          |            |            |
| Package Options                        | 120-lead LQFP_EP       |            |            | 400-ball CSP_BGA |            |            |

<sup>1</sup> N/A means not applicable.

<sup>2</sup> The values refer to different speed grades.

<sup>3</sup> Refer to [Table 14](#) for internal timer signal routing.

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## SHARC PROCESSOR

The SHARC processor integrates a SHARC+ SIMD core, L1 memory crossbar, I-cache/D-cache controller, L1 memory blocks, and the requester/completer ports, as shown in Figure 2. The SHARC+ SIMD core block diagram is shown in Figure 3.

The SHARC processor supports a modified Harvard architecture in combination with a hierarchical memory structure. L1 memories typically operate at the full processor speed with little or no latency.

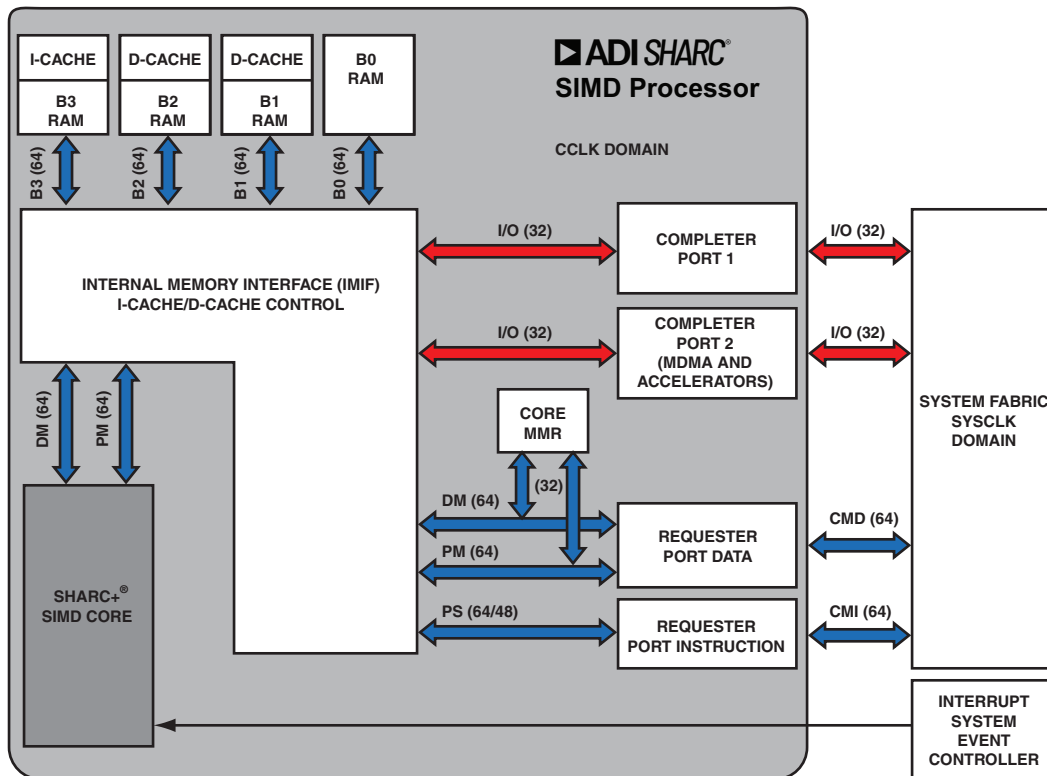


Figure 2. SHARC Processor Block Diagram

## L1 Memory

Figure 4 shows the ADSP-2156x memory map. The SHARC+ core has a tightly coupled 5 Mb L1 SRAM. The SHARC+ core can access code and data in a single cycle from this memory space.

In the SHARC+ core private address space, the core has L1 memory.

SHARC+ core memory-mapped register (CMMR) address space is 0x0000 0000 through 0x0003 FFFF in normal word (32-bit). Each block can be configured for different combinations of code and data storage. Of the 5 Mb SRAM, up to 1 Mb can be configured for data memory (DM), program memory (PM), and instruction cache each. Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The memory architecture, in combination with its separate on-chip buses, allows two data transfers from the core and one from the direct memory access (DMA) engine in a single cycle.

The SRAM of the processor can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5 Mb. All of the memory can be accessed as 8-bit, 16-bit, 32-bit, 48-bit, or 64-bit words. Support of a 16-bit floating-point storage format doubles the amount of data that can be stored on chip.

Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. Whereas each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM and PM buses, with each bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. The system configuration is flexible, but a typical configuration is 512 kb DM, 128 kb PM, and 128 kb of instruction

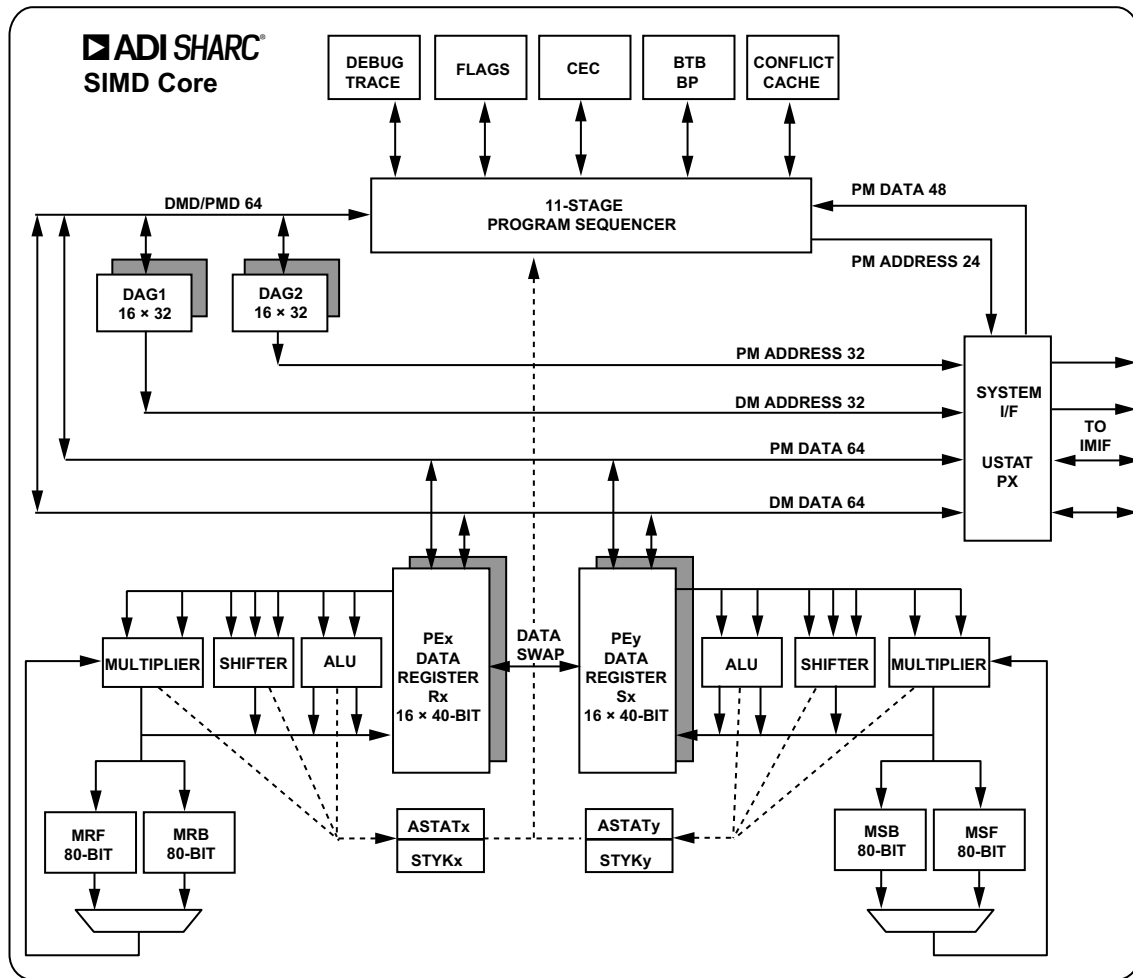


Figure 3. SHARC+ SIMD Core Block Diagram

cache, with the remaining L1 memory configured as SRAM. Each addressable memory space outside the L1 memory can be accessed either directly or via cache.

The memory map in Table 2 gives the L1 memory address space and shows multiple L1 memory blocks offering a configurable mix of SRAM and cache.

### L1 Requester and Completer Ports

The SHARC+ core has two requester/completer ports to and from the system fabric. One requester port fetches instructions. The second requester port drives data to the system world. Completer Port 1 together with Completer Port 2 memory direct memory access (high speed MDMA) run conflict free access to the individual memory blocks. For the completer port addresses, refer to the L1 memory address map in Table 2.

### L1 On-Chip Memory Bandwidth

The internal memory architecture allows programs to have four accesses at the same time to any of the four blocks, assuming no block conflicts. The total bandwidth is realized using both the DMD and PMD buses ( $2 \times 64$ -bits CCLK speed and  $2 \times 32$ -bit SYSCLK speed).

### Instruction and Data Cache

The ADSP-2156x processors also include a traditional instruction cache (I-cache) and two data caches (D-caches, one each for PM/DM) with parity support for all caches. These caches support one instruction access and two data accesses over the DM and PM buses per CCLK cycle. The cache controllers automatically manage the configured L1 memory. The system can configure part of the L1 memory for automatic management by the cache controllers. The sizes of these caches are independently configurable from 0 to 128 kB each. The memory not managed by the cache controllers is directly addressable by the processors. The controllers ensure the data coherence between

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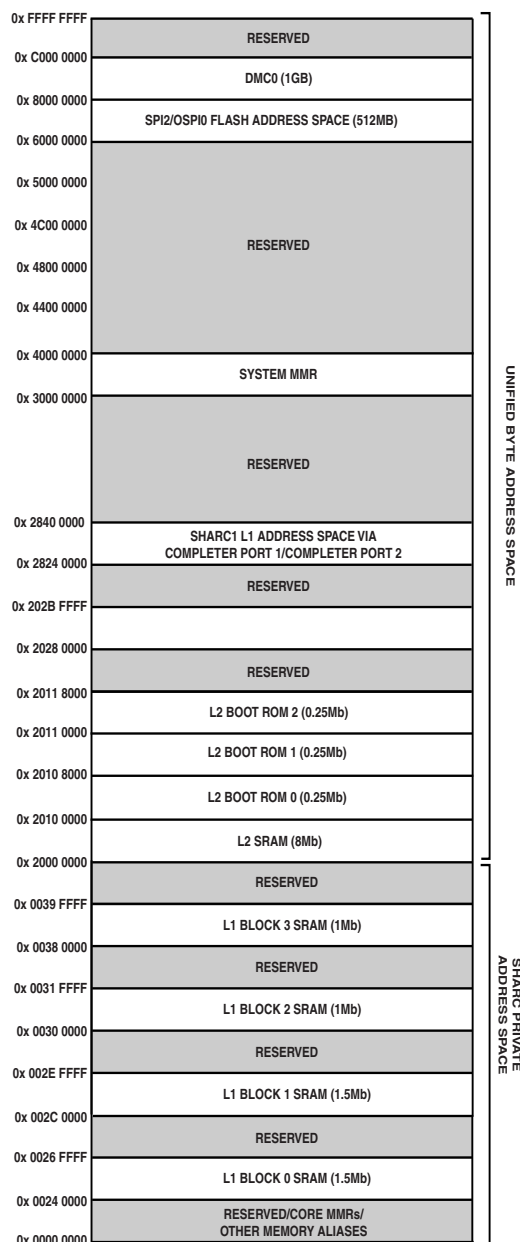


Figure 4. ADSP-2156x Memory Map

the two data caches. The caches provide user controllable features such as full and partial locking, range bound invalidation, and flushing.

## Core Memory-Mapped Registers (CMMR)

The core memory-mapped registers control the L1 instruction and data cache, branch target buffer (BTB), parity error, system control, debug, and monitor functions.

## SHARC+ CORE ARCHITECTURE

The ADSP-2156x processors are assembly code compatible with all previous SHARC processors featuring the SHARC or SHARC+ core, beginning with the first generation ADSP-2106x SHARC processors and including the ADSP-2116x, ADSP-2126x, ADSP-213xx, ADSP-214xx, and ADSP-SC5xx/ADSP-215xx processors.

The SIMD architecture featured on the ADSP-2156x processors is identical to all previous SIMD SHARC processors, namely the ADSP-2116x, ADSP-2126x, ADSP-213xx, ADSP-214xx, and ADSP-SC5xx/ADSP-215xx processors, as shown in Figure 3 and as described in the following sections.

### Single-Instruction, Multiple Data (SIMD) Computational Engine

The SHARC+ core contains two computational processing elements that operate as a single-instruction, multiple data (SIMD) engine.

The processing elements are referred to as PEx and PEy, each containing an arithmetic logic unit (ALU), multiplier, shifter, and register file. PEx is always active, and PEy is enabled by setting the PEYEN mode bit in the mode control register (MODE1).

SIMD mode allows the processors to execute the same instruction in both processing elements, but each processing element operates on different data. This architecture efficiently executes math intensive DSP algorithms. In addition to all the features of previous generation SHARC cores, the SHARC+ core also provides a new and simpler way to execute an instruction only on the PEy data register.

SIMD mode also doubles the bandwidth between memory and the processing elements, as required for sustained computational operation of two processing elements. When using the data address generators (DAGs) to transfer data in SIMD mode, two data values transfer with each memory or register file access.

### Independent Parallel Computation Units

Within each processing element is a set of pipelined computational units. The computational units consist of a multiplier, an ALU, and a shifter. These units are arranged in parallel, maximizing computational throughput. These computational units support IEEE 32-bit single-precision floating-point; 40-bit extended-precision floating-point; IEEE 64-bit double-precision floating-point; and 32-bit fixed-point data formats.

A multifunction instruction set supports parallel execution of ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements per core.

All processing operations take one cycle to complete. For all floating-point operations, the processor takes two cycles to complete in case of data dependency. Double-precision floating-point data take two to six cycles to complete. The processor stalls for the appropriate number of cycles for an interlocked pipeline plus data dependency check.

## Core Timer

The SHARC+ processor core includes an extra timer. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generating periodic operating system interrupts.

## Data Register File

Each processing element contains a general-purpose data register file. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register register files (16 primary, 16 secondary), combined with the enhanced Harvard architecture of the processor, allow unconstrained data flow between computation units and internal memory. The registers in the PEx data register file are referred to as R0–R15 and in the PEy data register file as S0–S15.

## Context Switch

Many of the registers of the processor have secondary registers that can activate during interrupt servicing for a fast context switch. The data, DAG, and multiplier result registers have secondary registers. The primary registers are active at reset, whereas control bits in MODE1 activate the secondary registers.

## Universal Registers

General-purpose tasks use the universal registers. The four universal status (USTAT) registers allow easy bit manipulations (set, clear, toggle, test, XOR) for all control and status peripheral registers.

The data bus exchange register (PX) permits data to pass between the 64-bit PM data bus and the 64-bit DM data bus or between the 40-bit register file and the PM or DM data bus. These registers contain hardware to handle the data width difference.

## Data Address Generators (DAG) With Zero Overhead Hardware Circular Buffer Support

For indirect addressing and implementing circular data buffers in hardware, the ADSP-2156x processor uses two data address generators (DAGs). Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing and are commonly used in digital filters and fast Fourier transforms (FFT). The DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets and 16 secondary sets). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

## Flexible Instruction Set Architecture (ISA)

The flexible instruction set architecture (ISA), a 48-bit instruction word, accommodates various parallel operations for concise programming. For example, the processors can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

Additionally, the double-precision floating-point instruction set is new to the SHARC+ core, as compared with the previous SHARC core.

## Variable Instruction Set Architecture (VISA)

In addition to supporting the standard 48-bit instructions from previous SHARC core processors, the SHARC+ core processors support 16-bit and 32-bit opcodes for many instructions, formerly 48-bit in the ISA. This variable instruction set architecture (VISA) feature drops redundant or unused bits within the 48-bit instruction to create more efficient and compact code. The program sequencer supports fetching these 16-bit and 32-bit instructions from both internal and external memories. VISA is not an operating mode; rather, it is address dependent (refer to the ISA/VISA address spaces in [Table 5](#)). Finally, the processor allows jumps between ISA and VISA instruction fetches.

## Single-Cycle Fetch of Instructional Four Operands

The ADSP-2156x processors feature an enhanced Harvard architecture in which the DM bus transfers data and the PM bus transfers both instructions and data.

With the separate program memory bus, data memory buses, and on-chip instruction conflict cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction from the conflict cache in a single cycle.

## Core Event Controller (CEC)

The SHARC+ core event controller (CEC) can be configured to service various interrupts generated by the core (including arithmetic and circular buffer instruction flow exceptions) and system event controller (SEC) events (peripheral interrupt request, debug or monitor, and software-raised), responding only to interrupts enabled in the IMASK register. The output of the SEC is forwarded to the CEC to respond directly to any enabled system interrupts. For all SEC channels, the processor automatically stacks the arithmetic status (ASTATx and ASTATy) registers and mode (MODE1) register in parallel with interrupt servicing.

## Instruction Conflict Cache

The processors include a 32-entry instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions that require fetches conflict with the PM bus data access cache. This cache allows full speed execution of core looped operations, such as digital filter multiply accumulates and FFT butterfly processing. The conflict cache serves for bus conflicts within the SHARC+ core only.

## Addressing Spaces

In addition to traditionally supported long word, normal word, extended precision word, and short word addressing aliases, the processors support byte addressing for the data and instruction accesses. The enhanced ISA/VISA provides new instructions for accessing all sizes of data from byte space, as well as converting word addresses to byte addresses and byte addresses to word addresses.

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## Branch Target Buffer (BTB)/Branch Predictor (BP)

Implementation of a hardware-based branch predictor (BP) and branch target buffer (BTB) reduce branch delay. The program sequencer supports efficient branching using the BTB for conditional and unconditional instructions.

## SHARC Fabric

The FIR/IIR accelerators on the ADSP-2156x processors are integrated closely with the SHARC+ core with the help of a dedicated SHARC fabric and run at CCLK speed. This allows the FIR/IIR accelerator requester ports to directly access the SHARC L1 memory with reduced latency, as these accesses do not go through the main system fabric. These accesses are arbitrated between both the SHARC+ core completer ports. The SHARC+ core can also access the FIR/IIR accelerator MMR registers directly.

## Additional Features

To enhance the reliability of the application, L1 data RAMs support parity error detection for every byte, and illegal opcodes are also detected (core interrupts flag both errors). Requester ports of the core also detect failed external accesses.

## SYSTEM INFRASTRUCTURE

The following sections describe the system infrastructure of the ADSP-2156x processors.

### System L2 Memory

A system L2 SRAM memory of up to 8 Mb (1 MB) is available to the SHARC+ core and the system DMA channels (see [Table 3](#)). The L2 SRAM block is subdivided into up to eight banks to

support concurrent access to the L2 memory ports. Memory accesses to the L2 memory space are multicycle accesses by the SHARC+ core.

The memory space is used for various situations including

- Accelerator and peripheral sources and destination memory to avoid accessing data in the external memory
- A location for DMA descriptors
- Storage for additional data for the SHARC+ core to avoid external memory latencies and reduce external memory bandwidth
- Storage for data coefficient tables cached by the SHARC+ core

See the [System Memory Protection Unit \(SMPU\)](#) section for options in limiting access by the core and DMA requesters.

## One Time Programmable Memory (OTP)

The processors feature 7 kb of one time programmable (OTP) memory that is memory-map accessible. This memory can be programmed with custom keys and supports secure boot and secure operation.

## I/O Memory Space

Mapped I/Os include SPI2 or OSPI0 memory address spaces (see [Table 5](#)).

## SYSTEM MEMORY MAP

Table 2. L1 Block 0, Block 1, Block 2, and Block 3 SHARC+® Addressing Memory Map (Private Address Space)

| Memory                      | Long Word (64 Bits)       | Extended Precision/<br>ISA Code (48 Bits) | Normal Word (32 Bits)     | Short Word/<br>VISA Code (16 Bits) | Byte Access (8 Bits)      |
|-----------------------------|---------------------------|-------------------------------------------|---------------------------|------------------------------------|---------------------------|
| L1 Block 0 SRAM<br>(1.5 Mb) | 0x00048000–<br>0x0004DFFF | 0x00090000–<br>0x00097FFF                 | 0x00090000–<br>0x0009BFFF | 0x00120000–<br>0x00137FFF          | 0x00240000–<br>0x0026FFFF |
| L1 Block 1 SRAM<br>(1.5 Mb) | 0x00058000–<br>0x0005DFFF | 0x000B0000–<br>0x000B7FFF                 | 0x000B0000–<br>0x000BBFFF | 0x00160000–<br>0x00177FFF          | 0x002C0000–<br>0x002EFFFF |
| L1 Block 2 SRAM<br>(1 Mb)   | 0x00060000–<br>0x00063FFF | 0x000C0000–<br>0x000C5554                 | 0x000C0000–<br>0x000C7FFF | 0x00180000–<br>0x0018FFFF          | 0x00300000–<br>0x0031FFFF |
| L1 Block 3 SRAM<br>(1 Mb)   | 0x00070000–<br>0x00073FFF | 0x000E0000–<br>0x000E5554                 | 0x000E0000–<br>0x000E7FFF | 0x001C0000–<br>0x001CFFFF          | 0x00380000–<br>0x0039FFFF |

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**Table 3. L2 Memory Addressing Map**

| Memory <sup>1</sup> | Byte Address Space<br>SHARC+ Data Access | Normal Word Address Space<br>SHARC+ Data Access | VISA Address Space<br>SHARC+ Instruction Fetch | ISA Address Space<br>SHARC+ Instruction Fetch |
|---------------------|------------------------------------------|-------------------------------------------------|------------------------------------------------|-----------------------------------------------|
| L2 RAM (2 Mb)       | 0x200C0000–<br>0x200FFFFF                | 0x08030000–<br>0x0803FFFF                       | 0x00BE0000–<br>0x00BFFFFF                      | 0x005E0000–<br>0x005EAAAA                     |
| L2 RAM (4 Mb)       | 0x20080000–<br>0x200FFFFF                | 0x08020000–<br>0x0803FFFF                       | 0x00BC0000–<br>0x00BFFFFF                      | 0x005D5556–<br>0x005EAAAA                     |
| L2 RAM (8 Mb)       | 0x20000000–<br>0x200FFFFF                | 0x08000000–<br>0x0803FFFF                       | 0x00B80000–<br>0x00BFFFFF                      | 0x005C0000–<br>0x005EAAAA                     |
| L2 Boot ROM0        | SHARC/DMA:<br>0x20100000–0x20107FFF      | 0x08040000–<br>0x08041FFF                       | 0x00B20000–<br>0x00B23FFF                      | 0x00580000–<br>0x00581555                     |
| L2 Boot ROM1        | 0x20108000–<br>0x2010FFFF                | 0x08042000–<br>0x08043FFF                       | 0x00B00000–<br>0x00B03FFF                      | 0x00500000–<br>0x00501555                     |
| L2 Boot ROM2        | 0x20110000–<br>0x20117FFF                | 0x08044000–<br>0x08045FFF                       | 0x00B40000–<br>0x00B43FFF                      | 0x00540000–<br>0x00541555                     |

<sup>1</sup> The L2 RAM blocks are subdivided into banks—the 8 Mb L2 models have eight banks, the 4 Mb models have four banks, and there are two banks for the 2 Mb models.

**Table 4. SHARC+<sup>®</sup> L1 Memory Space**

|                                                                | Memory<br>Block | Byte Address Space SHARC+ | Normal Word Address Space SHARC+ |
|----------------------------------------------------------------|-----------------|---------------------------|----------------------------------|
| L1 Memory Space Address via Completer1<br>Port/Completer2 Port | Block 0         | 0x28240000–0x2826FFFF     | 0x0A090000–0x0A09BFFF            |
|                                                                | Block 1         | 0x282C0000–0x282EFFFF     | 0x0A0B0000–0x0A0BBFFF            |
|                                                                | Block 2         | 0x28300000–0x2831FFFF     | 0x0A0C0000–0x0A0C7FFF            |
|                                                                | Block 3         | 0x28380000–0x2839FFFF     | 0x0A0E0000–0x0A0E7FFF            |

**Table 5. Memory Map of Mapped I/Os<sup>1</sup>**

|                                  | Byte Address Space<br>SHARC+ Data Access | Normal Word Address Space<br>SHARC+ Data Access | VISA Address Space<br>SHARC+ Instruction Fetch | ISA Address Space<br>SHARC+ Instruction Fetch |
|----------------------------------|------------------------------------------|-------------------------------------------------|------------------------------------------------|-----------------------------------------------|
| SPI2/OSPI0<br>Memory<br>(512 MB) | 0x60000000–0x600FFFFF                    | 0x04000000–0x07FFFFFFF                          | 0x00F80000–0x00FFFFFFF                         | 0x00780000–0x007FFFFFFF                       |
|                                  | 0x60100000–0x602FFFFF                    |                                                 | Not applicable                                 |                                               |
|                                  | 0x60300000–0x6FFFFFFF                    |                                                 | Not applicable                                 | Not applicable                                |
|                                  | 0x70000000–0x7FFFFFFF                    | Not applicable                                  | Not applicable                                 | Not applicable                                |

<sup>1</sup> The SHARC+ VISA/ISA address space for instruction fetch and the normal word address space for data access do not cover the entire byte address space.

**Table 6. DMC Memory Map<sup>1</sup>**

|             | Byte Address Space<br>SHARC+ Data Access | Normal Word Address Space<br>SHARC+ Data Access | VISA Address Space<br>SHARC+ Instruction Fetch | ISA Address Space<br>SHARC+ Instruction Fetch |
|-------------|------------------------------------------|-------------------------------------------------|------------------------------------------------|-----------------------------------------------|
| DMC0 (1 GB) | 0x80000000–0x805FFFFF                    | 0x10000000–0x17FFFFFFF                          | Not applicable                                 | 0x00400000–0x004FFFFFFF                       |
|             | 0x80600000–0x809FFFFF                    |                                                 | Not applicable                                 | Not applicable                                |
|             | 0x80A00000–0x80FFFFFFF                   |                                                 | 0x00800000–0x00AFFFFFFF                        | Not applicable                                |
|             | 0x81000000–0x9FFFFFFF                    |                                                 | Not applicable                                 | Not applicable                                |
|             | 0xA0000000–0xBFFFFFFF                    | Not applicable                                  | Not applicable                                 | Not applicable                                |

<sup>1</sup> The SHARC+ VISA/ISA address space for instruction fetch and the normal word address space for data access do not cover the entire byte address space.

## System Crossbars (SCBs)

The system crossbars (SCBs) are the fundamental building blocks of a switch fabric style for on-chip system bus interconnection. The SCBs connect system bus requesters to system bus completers, providing concurrent data transfer between multiple bus requesters and multiple bus completers. A hierarchical model—built from multiple SCBs—provides a power and area efficient system interconnection.

The SCBs provide the following features:

- Highly efficient, pipelined bus transfer protocol for sustained throughput
- Full-duplex bus operation for flexibility and reduced latency
- Concurrent bus transfer support to allow multiple bus requesters to access bus completers simultaneously
- Protection model (secure) support for selective bus interconnect protection

## Direct Memory Access (DMA)

The processors use direct memory access (DMA) to transfer data within memory spaces or between a memory space and a peripheral. The processors can specify data transfer operations and return to normal processing while the fully integrated DMA controller carries out the data transfers independent of processor activity.

DMA transfers can occur between memory and a peripheral or between one memory and another memory. Each memory to memory DMA stream uses two channels: the source channel and the destination channel.

All DMA channels can transport data to and from all on-chip and off-chip memories. Programs can use two types of DMA transfers: descriptor-based or register-based. Register-based DMA allows the processors to program DMA control registers directly to initiate a DMA transfer. On completion, the DMA control registers automatically update with original setup values for continuous transfer. Descriptor-based DMA transfers require a set of parameters stored within memory to initiate a DMA sequence. Descriptor-based DMA transfers allow multiple DMA sequences to be chained together. Program a DMA channel to set up and start another DMA transfer automatically after the current sequence completes.

The DMA engine supports the following DMA operations:

- A single linear buffer that stops on completion
- A linear buffer with negative, positive, or zero stride length
- A circular autorefreshing buffer that interrupts when each buffer becomes full
- A similar circular buffer that interrupts on fractional buffers, such as at the halfway point
- The 1D DMA uses a set of identical ping pong buffers defined by a linked ring of two-word descriptor sets, each containing a link pointer and an address

- The 1D DMA uses a linked list of four-word descriptor sets containing a link pointer, an address, a length, and a configuration
- The 2D DMA uses an array of one-word descriptor sets, specifying only the base DMA address
- The 2D DMA uses a linked list of multiword descriptor sets, specifying all configurable parameters

## Memory Direct Memory Access (MDMA)

The processor supports various memory direct memory access (MDMA) operations, including,

- Enhanced bandwidth MDMA channels with cyclic redundancy check (CRC) protection (32-bit bus width, run on SYSCLK)
- Enhanced bandwidth MDMA channel (32-bit bus width, runs on SYSCLK)
- Maximum bandwidth MDMA channel (64-bit bus width, runs on SYSCLK)

## Extended Memory DMA

Extended memory DMA supports various operating modes, such as delay line (which allows processor reads and writes to external delay line buffers and to the external memory), with limited core interaction and scatter/gather DMA (writes to and from noncontiguous memory blocks).

## Cyclic Redundancy Check (CRC) Protection

The cyclic redundancy check (CRC) protection modules allow system software to calculate the signature of code, data, or both in memory, the content of memory-mapped registers, or periodic communication message objects. Dedicated hardware circuitry compares the signature with precalculated values and triggers appropriate fault events.

For example, the system software initiates the signature calculation of the entire memory contents every 100 ms and compares this with expected, precalculated values. If a mismatch occurs, a fault condition is generated through the processor core or the trigger routing unit.

The CRC is a hardware module based on a CRC32 engine that computes the CRC value of the 32-bit data-words presented to it. The source channel of the memory to memory DMA (in memory scan mode) provides data. The data can be optionally forwarded to the destination channel (memory transfer mode). The main features of the CRC peripheral are as follows:

- Memory scan mode
- Memory transfer mode
- Data verify mode
- Data fill mode
- User-programmable CRC32 polynomial
- Bit and byte mirroring option (endianness)
- Fault and error interrupt mechanisms

- 1D and 2D fill block to initialize an array with constants
- 32-bit CRC signature of a block of memory or an MMR block

## Event Handling

The processors provide event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing a higher priority event takes precedence over servicing a lower priority event.

The processors provide support for four different types of events:

- An emulation event causes the processors to enter emulation mode, allowing command and control of the processors through the JTAG interface.
- A reset event resets the processors.
- An exception event occurs synchronously to program flow (in other words, the exception is taken before the instruction is allowed to complete). Conditions triggered by the SHARC+ core, such as data alignment (SIMD or long word) or compute violations (fixed or floating point) and illegal instructions, cause core exceptions. Conditions triggered by the SEC, such as error correcting code (ECC), parity, watchdog, or system clock, cause system exceptions.
- An interrupt event occurs asynchronously to program flow. Interrupts are caused by input signals, timers, and other peripherals, as well as by an explicit software instruction.

## System Event Controller (SEC)

The SHARC+ core event controller receives interrupt requests from the system event controller (SEC). The SEC features include the following:

- Comprehensive system event source management, including interrupt enable, fault enable, priority, and source grouping
- A distributed programming model where each system event source control and all status fields are independent of each other
- Determinism where all system events have the same propagation delay and provide unique identification of a specific system event source
- A completer control port that provides access to all SEC registers for configuration, status, and interrupt and fault services
- Global locking that supports a register level protection model to prevent writes to locked registers
- Fault management including fault action configuration, time out, external indication, and system reset

## Trigger Routing Unit (TRU)

The trigger routing unit (TRU) provides system-level sequence control without core intervention. The TRU maps trigger generators to trigger receivers. Trigger receivers can be configured to respond to triggers in various ways. Common applications enabled by the TRU include,

- Automatically triggering the start of a DMA sequence after a sequence from another DMA channel completes
- Software triggering
- Synchronization of concurrent activities

## SECURITY FEATURES

The following sections describe the security features of the ADSP-2156x processors.

### Cryptographic Hardware Accelerators

The ADSP-2156x processors support standards-based hardware accelerated encryption, decryption, authentication, and true random number generation.

Support for the hardware accelerated cryptographic ciphers includes the following:

- AES in ECB, CBC, ICM, and CTR modes with 128-bit, 192-bit, and 256-bit keys
- DES in ECB and CBC mode with 56-bit key
- 3DES in ECB and CBC mode with 3x 56-bit key
- ARC4 in stateful, stateless mode, up to 128-bit key

Support for the hardware accelerated hash functions includes the following:

- SHA-1
- SHA-2 with 224-bit and 256-bit digests
- HMAC transforms for SHA-1 and SHA-2
- MD5

Public key accelerator (PKA) is available to offload computation intensive public key cryptography operations.

Both a hardware-based nondeterministic random number generator and pseudorandom number generator are available.

Secure boot is also available with 224-bit and 256-bit elliptic curve digital signatures ensuring integrity and authenticity of the boot stream. Optionally, ensuring confidentiality through AES-128 encryption is available.

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Employ secure debug to allow only trusted users to access the system with debug tools.



## CAUTION

This product includes security features that can be used to protect embedded nonvolatile memory contents and prevent execution of unauthorized code. When security is enabled on this device (either by the ordering party or the subsequent receiving parties), the ability of Analog Devices to conduct failure analysis on returned devices is limited. Contact Analog Devices for details on the failure analysis limitations for this device.

## System Protection Unit (SPU)

The system protection unit (SPU) guards against accidental or unwanted access to an MMR space of the peripheral by providing a write protection mechanism. The user can choose and configure the protected peripherals as well as configure which of the three system MMR requesters (SHARC+ core, memory DMA, and Arm® CoreSight™ debug) the peripherals are guarded against.

The SPU is also part of the security infrastructure. Along with providing write protection functionality, the SPU is employed to define which resources in the system are secure or nonsecure as well as block access to secure resources from nonsecure requesters.

## System Memory Protection Unit (SMPU)

The system memory protection unit (SMPU) provides memory protection against read and/or write transactions to defined regions of memory. There are SMPU units in the ADSP-2156x processors for each memory space, except for SHARC L1 memory.

The SMPU is also part of the security infrastructure. It allows the user to protect against arbitrary read and/or write transactions and allows regions of memory to be defined as secure and prevent nonsecure requesters from accessing those memory regions.

## SECURITY FEATURES DISCLAIMER

Analog Devices does not guarantee that the Security Features described herein provide absolute security. ACCORDINGLY, ANALOG DEVICES HEREBY DISCLAIMS ANY AND ALL EXPRESS AND IMPLIED WARRANTIES THAT THE SECURITY FEATURES CANNOT BE BREACHED, COMPROMISED, OR OTHERWISE CIRCUMVENTED AND IN NO EVENT SHALL ANALOG DEVICES BE LIABLE FOR ANY LOSS, DAMAGE, DESTRUCTION, OR RELEASE OF DATA, INFORMATION, PHYSICAL PROPERTY, OR INTELLECTUAL PROPERTY.

## SAFETY FEATURES

The ADSP-2156x processors are designed to support functional safety applications. Whereas the level of safety is mainly dominated by the system concept, the following primitives are provided by the processors to build a robust safety concept.

### Multiparity Bit Protected SHARC+ Core L1 Memories

In the SHARC+ core L1 memory space, whether SRAM or cache, multiple parity bits protect each word to detect the single event upsets that occur in all RAMs. Parity also protects the cache tags and BTB.

### Error Correcting Code (ECC) Protected L2 Memories

Error correcting code (ECC) corrects single event upsets. A single error correct/double error detect (SEC/DED) code protects the L2 memory. By default, ECC is enabled, but it can be disabled on a per bank basis. Single-bit errors correct transparently. If enabled, dual-bit errors can issue a system event or fault. ECC protection is fully transparent to the user, even if L2 memory is read or written by 8-bit or 16-bit entities.

### Parity Protected Peripheral Memories

Parity protection is added to the following peripheral memories:

- ASRC
- IIR
- FIR
- CRYPTO
- MLB
- TRACE

### Cyclic Redundancy Check (CRC) Protected Memories

Whereas parity bit and ECC protection mainly protect against random soft errors in L1 and L2 memory cells, the CRC engines can protect against systematic errors (pointer errors) and static content (instruction code) of L1, L2, and even L3 memories (DDR3, DDR3L). The processors feature two CRC engines that are embedded in the memory to memory DMA controllers.

CRC checksums can be calculated or compared automatically during memory transfers. Alternatively, single or multiple memory regions can be continuously scrubbed by a single DMA work unit as per DMA descriptor chain instructions. The CRC engine also protects data loaded during the boot process.

### Signal Watchdogs

The 10 general-purpose timers feature modes to monitor off-chip signals. The watchdog period mode monitors whether external signals toggle with a period within an expected range. The watchdog width mode monitors whether the pulse widths of external signals are within an expected range. Both modes help detect undesired toggling or lack of toggling of system level signals.

## System Event Controller (SEC)

Besides system events, the system event controller (SEC) further supports fault management, including fault action configuration as timeout, internal indication by system interrupt, or external indication through the `SYS_FAULT` pin and system reset.

## Memory Error Controller (MEC)

The memory error controller (MEC) manages memory parity/ECC errors and warnings from the cores and peripherals and sends out interrupts and triggers.

## PROCESSOR PERIPHERALS

The following sections describe the peripherals of the ADSP-2156x processors.

### Dynamic Memory Controller (DMC)

The 16-bit dynamic memory controller (DMC) interfaces to

- DDR3 (JESD79-3), 512 Mb to 8 Gb
- DDR3L (JESD79-3-1A), 512 Mb to 8 Gb

See [Table 6](#) for the DMC memory map.

### Digital Audio Interface (DAI)

The processors support two digital audio interface (DAI) units. The DAI can connect various peripherals to any of the DAI pins.

The application code makes these connections using the signal routing unit (SRU), shown in [Figure 1](#).

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to interconnect under software control. This functionality allows easy use of the DAI associated peripherals for a wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI includes the peripherals described in the following sections (SPORTs, ASRC, S/PDIF, and PCG). DAI Pin Buffer 20 and DAI Pin Buffer 19 can change the polarity of the input signals. Most signals of the peripherals belonging to different DAIs cannot be interconnected, with few exceptions.

The DAI\_PINx pin buffers may also be used as GPIO pins. DAI input signals allow the triggering of interrupts on the rising edge, falling edge, or both.

See the [ADSP-21562/3/5/6/7/9 SHARC+ Processor Hardware Reference](#) manual for complete information on the use of the DAIs and SRUs.

### Serial Port (SPORT)

The processors feature eight synchronous serial ports (SPORTs), providing an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. These devices include Analog Devices AD19xx and ADAU19xx families of audio codecs, analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). Two data lines, a clock, and a

frame sync comprise a SPORT half. The data lines can be programmed to either transmit or receive data, and each SPORT half has a dedicated DMA channel.

An individual SPORT module consists of two independently configurable SPORT halves with identical functionality. Two bidirectional data lines—primary (0) and secondary (1)—are available per SPORT half and are configurable as either transmitters or receivers. Therefore, each SPORT half permits two unidirectional streams into or out of the same SPORT. This bidirectional functionality provides greater flexibility for serial communications. For full-duplex configuration, one half SPORT provides two transmit data signals, and the other half SPORT provides two receive data signals. The frame sync and clock are shared.

Serial ports operate in the following six modes:

- Standard DSP serial mode
- Multichannel time division multiplexing (TDM) mode
- I<sup>2</sup>S mode
- Packed I<sup>2</sup>S mode
- Left justified mode
- Right justified mode

### Asynchronous Sample Rate Converter (ASRC)

The asynchronous sample rate converter (ASRC) contains eight ASRC blocks. The ASRC provides up to 140 dB signal-to-noise ratio (SNR). The ASRC block performs synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The ASRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the ASRC can clean up audio data from jittery clock sources such as the S/PDIF receiver.

### S/PDIF-Compatible Digital Audio Receiver/Transmitter

The Sony/Philips Digital Interface Format (S/PDIF) is a standard audio data transfer format that allows the transfer of digital audio signals from one device to another. There are two S/PDIF transmit/receive blocks on the processor. The digital audio interface carries three types of information: audio data, nonaudio data (compressed data), and timing information.

The S/PDIF interface supports one stereo channel or compressed audio streams. The S/PDIF transmitter and receiver are AES3 compatible and support the sample rate from 24 kHz to 192 kHz. The S/PDIF receiver supports professional jitter standards.

The S/PDIF receiver/transmitter has no separate DMA channels. The S/PDIF transmitter receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the transmitter can be formatted as left justified, I<sup>2</sup>S, or right justified with word widths of 16, 18, 20, or 24 bits. The S/PDIF receiver converts a biphase encoded signal into I<sup>2</sup>S serial format. The serial data, clock, and frame sync outputs/inputs from/to the S/PDIF receiver/transmitter are routed through the

SRU. They can be connected to various peripherals, such as the SPORTs, external pins, and the precision clock generators (PCGs), and are controlled by the SRU control registers.

## **Precision Clock Generators (PCG)**

The precision clock generators (PCG) consist of four units: Unit A and Unit B located in the DAI0 block, and Unit C and Unit D located in the DAI1 block. The PCG can generate a pair of signals (clock and frame sync) derived from a clock input signal (SCLK0, SYS\_CLKIN0, or DAI pin buffer). Each unit can also output to the pin buffers of the opposite DAI unit. All units are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

## **Universal Asynchronous Receiver/Transmitter (UART) Ports**

The processors provide full-duplex universal asynchronous receiver/transmitter (UART) ports, fully compatible with PC standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits as well as no parity, even parity, or odd parity.

Optionally, an additional address bit can be transferred to interrupt only addressed nodes in multidrop bus (MDB) systems. A frame is terminated by a configurable number of stop bits.

The UART ports support automatic hardware flow control through the clear to send (CTS) input and request to send (RTS) output with programmable assertion first in, first out (FIFO) levels.

To help support the Local Interconnect Network (LIN) protocols, a special command causes the transmitter to queue a break command of programmable bit length into the transmit buffer. Similarly, the number of stop bits can be extended by a programmable interframe space.

## **Serial Peripheral Interface (SPI) Ports**

The processors have four industry-standard SPI-compatible ports that allow the processors to communicate with multiple SPI-compatible devices.

The baseline SPI peripheral is a synchronous, 4-wire interface consisting of two data pins, one device select pin, and a gated clock pin. The two data pins allow full-duplex operation to other SPI-compatible devices. An extra two (optional) data pins are provided to support quad-SPI operation. Enhanced modes of operation, such as flow control, fast mode, and dual-I/O mode (DIOM), are also supported. DMA mode allows for transferring several words with minimal central processing unit (CPU) interaction.

With a range of configurable options, the SPI ports provide a glueless hardware interface with other SPI-compatible devices in master mode, slave mode, and multimaster environments. The SPI peripheral includes programmable baud rates, clock phase, and clock polarity. The peripheral can operate in a multimaster environment by interfacing with several other

devices, acting as either a master device or a slave device. In a multimaster environment, the SPI peripheral uses open-drain outputs to avoid data bus contention. The flow control features enable slow slave devices to interface with fast master devices by providing an SPI ready pin (SPI\_RDY), which flexibly controls the transfers.

The baud rate and clock phase and polarities of the SPI port are programmable. The port has integrated DMA channels for both transmit and receive data streams.

## **Octal Serial Peripheral Interface (OSPI) Port**

The octal serial peripheral interface (OSPI) port provides an increased external memory data bus width (up to eight bits in parallel). The OSPI port supports DDR modes of operation, which enable the transfer of up to 16 bits of data each clock cycle. The OSPI port provides overall data throughput and performance improvement, including faster boot time.

Features of the OSPI port include:

- Support for single-, dual-, quad-, or octal-I/O transfers
- Multiple modes of operation including direct and software triggered instruction generator (STIG)
- Support for execute in place (XIP): continuous mode
- Programmable page and block sizes
- Programmable write protected regions
- Programmable memory timing
- Support for DDR commands

## **Link Port (LP)**

Two 8-bit wide link ports (LP) for the BGA package can connect to the link ports of other DSPs or peripherals. Link ports are bidirectional and have eight data lines, an acknowledge line, and a clock line.

## **Timers**

The processors include several timers that are described in the following sections.

### **General-Purpose (GP) Timers (TIMER)**

There is one general-purpose (GP) timer unit, providing 10 general-purpose programmable timers. Each timer has an external pin that can be configured as PWM or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input on the TM\_TMR[n] pins, an external TM\_CLK input pin, or to the internal SCLK0.

These timer units can be used in conjunction with the UARTs to measure the width of the pulses in the data stream to provide a software autobaud detect function for the respective serial channels.

The GP timers can generate interrupts to the processor core, providing periodic events for synchronization to either the system clock or to external signals. Timer events can also trigger

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other peripherals via the TRU (for instance, to signal a fault). Each timer can also be started and stopped by any trigger generator without core intervention.

## Watchdog Timer (WDT)

Two on-chip software watchdog timers (WDT) can be used by the SHARC+ core. A software watchdog can improve system availability by forcing the processors to a known state, via a general-purpose interrupt, or a fault, if the timer expires before being reset by software.

The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts down to zero from the programmed value, protecting the system from remaining in an unknown state where software that normally resets the timer stops running due to an external noise condition or software error.

## General-Purpose Counters (CNT)

A 32-bit general-purpose counter (CNT) is provided that can operate in general-purpose up/down count modes and can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumbwheels. Count direction is controlled by a level-sensitive input pin or by two edge detectors.

A third counter input can provide flexible zero marker support and can input the push button signal of thumbwheel devices. All three CNT0 pins have a programmable debouncing circuit.

Internal signals forwarded to a GP timer enable the timer to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmed count values are exceeded.

## Housekeeping Analog-to-Digital Converter (HADC)

The housekeeping analog-to-digital converter (HADC) provides a general-purpose, multichannel successive approximation ADC. It supports the following set of features:

- 12-bit ADC core with built in sample and hold.
- Four single-ended input channels for the BGA package; two single-ended input channels for the LQFP package.
- Throughput rates up to 1 MSPS.
- Single external reference with analog inputs between 0 V and 1.8 V.
- Selectable ADC clock frequency including the ability to program a prescaler.
- Adaptable conversion type; allows single or continuous conversion with option of autoscan.
- Autosequencing capability with up to four autoconversions in a single session. Each conversion can be programmed to select one to four input channels.
- Four data registers for the BGA package and two data registers for the LQFP package (all individually addressable) to store conversion values.

Figure 5 shows the channel multiplex diagram for the HADC input pins for the BGA package (ADSP-21566, ADSP-21567, and ADSP-21569).

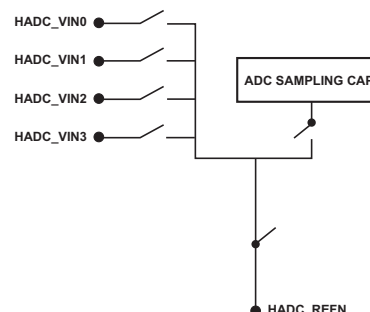


Figure 5. Channel Multiplex of HADC Input Pins for BGA Package

Figure 6 shows the channel multiplex diagram for the HADC input pins for the LQFP package (ADSP-21562, ADSP-21563, and ADSP-21565).

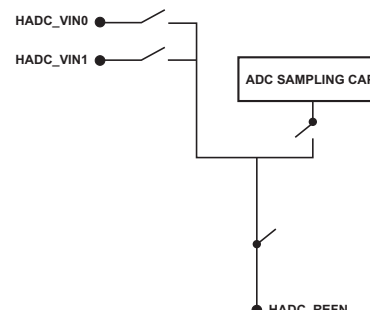


Figure 6. Channel Multiplex of HADC Input Pins for LQFP Package

Figure 7 shows the input impedance of the HADC, represented with internal resistance and capacitance. The VIN signal represents the HADC input pins (HADC\_VINx).

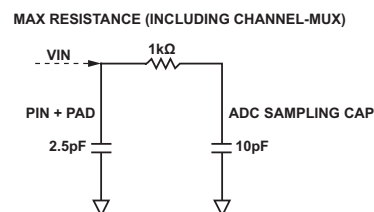


Figure 7. HADC Internal Circuit Schematic

## Media Local Bus (MediaLB)

The automotive model has a Microchip MediaLB (MLB) device interface that allows the processors to function as a media local bus device. It includes support for 3-pin media local bus

protocols. The MLB 3-pin configuration supports speeds up to  $1024 \times \text{FS}$ . The MLB also supports up to 64 logical channels with up to 468 bytes of data per MLB frame.

The MLB interface supports MOST25, MOST50, and MOST150 data rates and operates in device mode only.

## 2-Wire Controller Interface (TWI)

The processors include 2-wire interface (TWI) modules that provide a simple exchange method of control data between multiple devices. The TWI module is compatible with the widely used I<sup>2</sup>C bus standard. The TWI module offers the capabilities of simultaneous controller and target operation and support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (TWI\_SCL) and data (TWI\_SDA) and supports the protocol at speeds up to 400 kbps. The TWI interface pins are compatible with 3.3 V logic levels.

Additionally, the TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

## General-Purpose I/O (GPIO)

Each general-purpose port pin can be individually controlled by manipulating the port control, status, and interrupt registers:

- The GPIO direction control register specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers have a write-one-to-modify mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins.
- GPIO interrupt mask registers allow each individual GPIO pin to function as an interrupt to the processors. GPIO pins defined as inputs can be configured to generate hardware interrupts, whereas output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers specify whether individual pins are level or edge sensitive and specify, if edge sensitive, whether the rising edge or both the rising and falling edges of the signal are significant.

## Pin Interrupts

Every port pin on the processors can request interrupts in either an edge sensitive or a level sensitive manner with programmable polarity. Interrupt functionality is decoupled from GPIO operation. Three system-level interrupt channels (PINT0–PINT2) are reserved for this purpose. Each of these interrupt channels can manage up to 32 interrupt pins. The assignment from pin to interrupt is not performed on a pin by pin basis. Rather, groups of eight pins (half ports) are flexibly assigned to interrupt channels.

Every pin interrupt channel features a special set of 32-bit memory-mapped registers that enable half port assignment and interrupt management. This functionality includes masking, identification, and clearing of requests. These registers also enable access to the respective pin states and use of the interrupt

latches, regardless of whether the interrupt is masked. Most control registers feature multiple MMR address entries to write-one-to-set or write-one-to-clear them individually.

## Core Flags I/O Pins

The processor features four flag I/O pins, which allow for external control and monitoring of the SHARC+ core FLAGS register. User code can write to bits in this register to be driven to pins configured as outputs, and code execution can be made conditional based on the settings of the pins configured as inputs.

## SYSTEM ACCELERATION

The following sections describe the system acceleration blocks of the ADSP-2156x processors.

### Finite Impulse Response (FIR) Accelerator

The finite impulse response (FIR) accelerator consists of a 1024 word coefficient memory, a 1024 word deep delay line for the data, and four multiplier-accumulator (MAC) units. A controller manages the accelerator. The FIR accelerator runs at the core clock frequency. The FIR accelerator can access all memory spaces and can run concurrently with the IIR accelerator on the processor.

### Infinite Impulse Response (IIR) Accelerator

The infinite impulse response (IIR) accelerator consists of a 1440 word coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data, and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the core clock frequency. The IIR accelerator can access all memory spaces and run concurrently with the other accelerators on the processor.

In addition to operating at core clock, the FIR/IIR accelerators support various enhanced features, including the ability to halt the accelerator for dynamic queuing of unlimited FIR/IIR channels, selective interrupt generation for each channel, and trigger requester/completer support.

## SYSTEM DESIGN

The following sections provide an introduction to system design features and power supply issues.

### Clock Management

The processors provide three operating modes, each with a different performance and power profile. Control of clocking to each of the processor peripherals reduces power consumption. The processors do not support any low power operation modes. Control of clocking to each of the processor peripherals can reduce the power consumption.

### Reset Control Unit (RCU)

Reset is the initial state of the whole processor, or the core, and is the result of a hardware or software triggered event. In this state, all control registers are set to default values and functional units are idle. Exiting a full system reset begins with the core ready to boot.

The reset control unit (RCU) controls how all the functional units enter and exit reset. Differences in functional requirements and clocking constraints define how reset signals are generated. Programs must guarantee that none of the reset functions put the system into an undefined state or cause resources to stall. This requirement is particularly important when the core resets (programs must ensure that there is no pending system activity involving the core when it is reset).

From a system perspective, reset is defined by both the reset target and the reset source.

The reset target is defined as the following:

- System reset—all functional units except the RCU are set to default states.
- Hardware reset—all functional units are set to default states without exception. History is lost.
- Core only reset—affects the core only. When in reset state, the core is not accessed by any bus requester.

The reset source is defined as the following:

- System reset—can be triggered by software (writing to the RCU\_CTL register) or by another functional unit, such as the dynamic power management (DPM) unit or any of the SEC, TRU, or emulator inputs.
- Hardware reset—the `SYS_HWRST` input signal asserts active (pulled down).
- Core only reset—can be triggered by software (writing to the RCU\_CTL register).
- Trigger request (peripheral).

## Clock Generation Unit (CGU)

The ADSP-2156x processors support two independent PLLs. Each PLL is part of a clock generation unit (CGU). Each CGU is driven externally by the same clock source, thus providing flexibility in determining the internal clocking frequencies for each clock domain.

Frequencies generated by each CGU are derived from a common multiplier with different divider values available for each output.

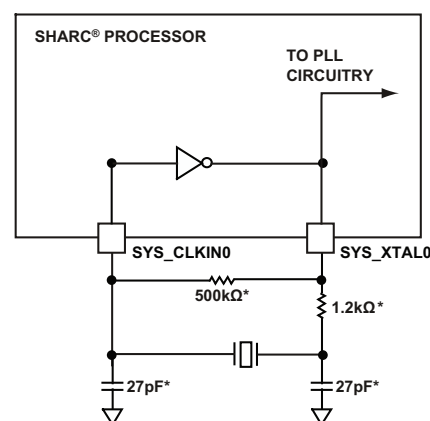
The CGU generates all on-chip clocks and synchronization signals. Multiplication factors are programmed to define the PLLCLK frequency.

Programmable values divide the PLLCLK frequency to generate the core clock (CCLK), the system clocks, the DDR3/DDR3L clock (DCLK), and the output clock (OCLK). For more information on clocking, see the [ADSP-21562/3/5/6/7/9 SHARC+ Processor Hardware Reference manual](#).

Writing to the CGU control registers does not affect the behavior of the PLL immediately. Registers are first programmed with a new value and the PLL logic executes the changes to ensure a smooth transition from the current conditions to the new conditions.

## System Crystal Oscillator

The processor can be clocked by an external crystal (see [Figure 8](#)), a sine wave input, or a buffered, shaped clock derived from an external clock oscillator. If using an external clock, it must be compatible with the  $V_{IHCLKIN}$  and  $V_{ILCLKIN}$  specifications and must not be halted, changed, or operated below the specified frequency during normal operation (see the [Operating Conditions](#) section). When using an external clock, the clock signal is connected to the `SYS_CLKIN0` pin of the processor and the `SYS_XTAL0` pin must be left unconnected. Alternatively, because the processor includes an on-chip oscillator circuit, an external crystal can be used.



NOTE: VALUES MARKED WITH \* MUST BE CUSTOMIZED, DEPENDING ON THE CRYSTAL AND LAYOUT. ANALYZE CAREFULLY. VALID FREQUENCY RANGE IS 20 MHz TO 30 MHz FOR `SYS_CLKIN0`.

Figure 8. External Crystal Connection

For fundamental frequency operation, use the circuit shown in [Figure 8](#). A parallel resonant, fundamental frequency, micro-processor grade crystal is connected across the `SYS_CLKIN0` pin and the `SYS_XTAL0` pin.

The two capacitors and the series resistor, shown in [Figure 8](#), fine tune phase and amplitude of the sine frequency. The capacitor and resistor values shown in [Figure 8](#) are typical values only. The capacitor values are dependent upon the load capacitance recommendations of the crystal manufacturer and the physical layout of the printed circuit board (PCB). The resistor value depends on the drive level specified by the crystal manufacturer. The user must verify the customized values based on careful investigations on multiple devices over the required temperature range.

## Clock Distribution Unit (CDU)

The two clock generation units each provide outputs that feed a clock distribution unit (CDU). The clock outputs `CLKO0`–`CLKO1` and the clock generation unit outputs are connected to various targets. For more information, refer to the [ADSP-21562/3/5/6/7/9 SHARC+ Processor Hardware Reference manual](#).

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## Clock Out/External Clock

The SYS\_CLKOUT output pin has programmable options to output divided down versions of the on-chip clocks. By default, the SYS\_CLKOUT pin drives a buffered version of the SYS\_CLKIN0 input. Refer to the [ADSP-21562/3/5/6/7/9 SHARC+ Processor Hardware Reference](#) manual to change the default mapping of clocks.

## Booting

The processors have several mechanisms for automatically loading internal and external memory after a reset. The boot mode is defined by the SYS\_BMODE[n] input pins. There are two categories of boot modes. In flash boot modes, the processors actively load data from serial memories. In external host boot modes, the processors receive data over a serial interface from an external host device.

The boot modes are shown in [Table 7](#). These modes are implemented by the SYS\_BMODE[n] bits of the reset configuration register and are sampled during power-on resets and software initiated resets.

Table 7. Boot Modes

| SYS_BMODE[n] Setting <sup>1</sup> | Boot Mode           |
|-----------------------------------|---------------------|
| 000                               | No boot             |
| 001                               | SPI2 flash          |
| 010                               | External SPI2 host  |
| 011                               | External UART0 host |
| 100                               | External LP0 host   |
| 101 <sup>2</sup>                  | Octal SPI flash     |
| 110                               | Reserved            |
| 111                               | Reserved            |

<sup>1</sup> SYS\_BMODE2 pin is applicable only for the BGA package.

<sup>2</sup> Though octal SPI flash boot is not supported on the LQFP package, it is available through the ROM API.

In the ADSP-2156x processors, the SHARC+ core controls the boot process, including loading all internal and external memory. The option for secure boot is available on all models.

## Thermal Monitoring Unit (TMU)

The thermal monitoring unit (TMU) provides on-chip temperature measurement for applications that require substantial power consumption. The TMU is integrated into the processor die and digital infrastructure using an MMR-based system access to measure the die temperature variations in real-time.

TMU features include the following:

- On-chip temperature sensing
- Programmable over temperature and under temperature limits
- Programmable conversion rate
- Averaging feature available

## Power Supplies

The processors have separate power supply connections for

- Internal (VDD\_INT)
- External I/O (VDD\_EXT)
- External I/O Reference (VDD\_REF)
- HADC/TMU (VDD\_ANA)
- DMC (VDD\_DMC)

## Power Management

As shown in [Table 8](#), the processors support five different power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions.

The power dissipated by a processor is largely a function of the clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation.

Table 8. Power Domains

| Power Domain                                                         | V <sub>DD</sub> Range            |
|----------------------------------------------------------------------|----------------------------------|
| All Internal Logic                                                   | V <sub>DD_INT</sub>              |
| DDR3/DDR3L                                                           | V <sub>DD_DMC</sub>              |
| HADC/TMU                                                             | V <sub>DD_ANA</sub>              |
| All Other I/O (Includes SYS, JTAG, and Ports Pins Except SYS_CLKIN0) | V <sub>DD_EXT</sub>              |
| SYS_CLKIN0                                                           | V <sub>DD_REF</sub> <sup>1</sup> |

<sup>1</sup> V<sub>DD\_REF</sub> requires a minimum of 10 nF and 100 nF decoupling capacitance to meet source/sink requirements.

## Power-Up and Power-Down Sequencing

At all times (including during power-up/power-down sequencing), the VDD\_REF, VDD\_ANA, and VDD\_EXT supplies must stay within the V<sub>DELTA\_EXT\_REF</sub> specification listed in the [Operating Conditions](#) table. SYS\_XTAL0 oscillations (SYS\_CLKIN0) start when power is applied to the VDD\_REF pins. The rising edge of  $\overline{\text{SYS\_HWRST}}$  initiates the PLL locking sequence. The rising edge of  $\overline{\text{SYS\_HWRST}}$  must occur after all voltage supplies and SYS\_CLKIN0 oscillations are valid. For further details and information, see the [Power-Up Reset Timing](#) section.

## Target Board JTAG Emulator Connector

The Analog Devices DSP tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the processors to monitor and control the target board processor during emulation. The Analog Devices DSP tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor JTAG interface ensures the emulator does not affect target system loading or timing.

For information on JTAG emulator operation, see the appropriate emulator hardware user's guide at [SHARC Processors Software and Tools](#).

## SYSTEM DEBUG

The processors include various features that allow easy system debug. These are described in the following sections.

### System Watchpoint Unit (SWU)

The system watchpoint unit (SWU) is a single module that connects to a single system bus and provides transaction monitoring. One SWU is attached to the bus going to each system completer. The SWU provides ports for all system bus address channel signals. Each SWU contains four match groups of registers with associated hardware. These four SWU match groups operate independently but share common event (for example, interrupt and trigger) outputs.

### Debug Access Port (DAP)

The debug access port (DAP) provides IEEE 1149.1 JTAG interface support through the JTAG debug. The DAP provides an optional instrumentation trace for both the core and system. It provides a trace stream that conforms to *MIPI System Trace Protocol version 2 (STPv2)*.

## DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including an integrated development environment, evaluation products, emulators, and a variety of software add-ins.

### Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers the CrossCore® Embedded Studio (CCES) integrated development environment (IDE).

CCES is based on the Eclipse framework. Supporting most Analog Devices processor families, CCES is the IDE of choice for processors, including multicore devices.

CCES seamlessly integrates available software add-ins to support real-time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages (BSPs). For more information, visit [www.analog.com/cces](http://www.analog.com/cces).

### EZ-KIT Evaluation System

For processor evaluation, Analog Devices provides an EZ-KIT® evaluation system (EV-21569-EZKIT), which is a bundle comprised of a System on Module (SOM) board (EV-21569-SOM) and an EZ-KIT SOM carrier board (EV-SOMCRR-EZKIT).

SOM boards are small and low cost. The EV-21569-SOM board has the ADSP-21569 processor, SDRAM and QSPI flash memories, JTAG debug connection, FTDI USB-to-UART, and USB power. SOM boards can be used alone or in combination with a SOM carrier board. SOM carrier boards have high speed connectors for the SOM, a comprehensive set of peripherals, and an on-board emulator. Each SOM carrier board also comes with a power supply.

The USB controller on the SOM carrier board connects to the USB port of the user's PC, enabling CCES to emulate the on-board processor in circuit. This permits users to download,

execute, and debug programs. It also supports in-circuit programming of the on-board flash memory device to store user-specific boot code, enabling standalone operation.

Each EZ-KIT purchased includes an evaluation license for CCES. The CCES evaluation license type restricts CCES features to specific evaluation systems. With the full CCES license type (sold separately), engineers can develop software for any of the CCES-supported evaluation boards (including the SOM when used standalone or when connected to a different carrier board) or any custom system designed around supported Analog Devices processors. The full CCES license type also enables use of ICE-2000 or ICE-1000 emulators for higher performance debugging via JTAG.

When a SOM board is mounted to a SOM carrier board, embedded system evaluation can be performed. The EZ-KIT SOM carrier board provides an evaluation platform for various system peripherals including audio, S/PDIF, CAN, MLB, USB, 10/100/1000 Ethernet, and A<sup>2</sup>B, as well as an OSPI flash memory. The EZ-KIT SOM carrier board also features the USB Debug Agent, which allows for debug and evaluation of the full system (including the processor/memory on the SOM module) without an emulator.

For further information, see:

- [www.analog.com/cces](http://www.analog.com/cces)
- [www.analog.com/EV-21569-SOM](http://www.analog.com/EV-21569-SOM)
- [www.analog.com/EV-SOMCRR-EZKIT](http://www.analog.com/EV-SOMCRR-EZKIT)

### Software Add-Ins for CCES

Analog Devices offers software add-ins which seamlessly integrate with CCES to extend the capabilities and reduce development time. Add-ins include BSPs for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CCES IDE upon add-in installation.

### Board Support Packages (BSPs) for Evaluation Hardware

Software support for the EZ-KIT evaluation systems is provided by software add-ins called board support packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated SOM product.

### Middleware Packages

Analog Devices offers middleware add-ins such as real-time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information, see the [Operating Systems and Middleware](#) page.

### Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with CCES. For more information, visit the [Design Center](#).

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## ***Designing an Emulator-Compatible DSP Board (Target)***

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG test access port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the internal features of the processor via the TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers.

The processor must be halted to send data and commands, but after an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the JTAG port of the DSP to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see [Analog Devices JTAG Emulation Technical Reference \(EE-68\)](#).

## **ADDITIONAL INFORMATION**

This data sheet provides a general overview of the ADSP-2156x architecture and functionality. For detailed information on the core architecture and instruction set, refer to the [SHARC+ Core Programming Reference](#).

## **RELATED SIGNAL CHAINS**

A signal chain is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together. A tool for viewing relationships between specific applications and related components is available at [www.analog.com/circuits](http://www.analog.com/circuits).

The application signal chains page in the Circuits from the Lab<sup>®</sup> site ([www.analog.com/circuits](http://www.analog.com/circuits)) provides the following:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

## ADSP-2156x DETAILED SIGNAL DESCRIPTIONS

Table 9 provides a detailed description of each pin.

**Table 9. ADSP-2156x Detailed Signal Descriptions**

| Signal Name   | Direction | Description                                                                                                                                                                                                                                                                   |
|---------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C0_FLG[n]     | InOut     | <b>Core 0 FLAGS I/O n.</b> External pins associated with the core FLAGS register on SHARC+ core 0.                                                                                                                                                                            |
| CNT_DG        | Input     | <b>Count Down and Gate.</b> Depending on the mode of operation, this input acts either as a count down signal or a gate signal.<br>Count down—this input causes the GP counter to decrement.<br>Gate—stops the GP counter from incrementing or decrementing.                  |
| CNT_UD        | Input     | <b>Count Up and Direction.</b> Depending on the mode of operation, this input acts either as a count up signal or a direction signal.<br>Count up—this input causes the GP counter to increment.<br>Direction—selects whether the GP counter is incrementing or decrementing. |
| CNT_ZM        | Input     | <b>Count Zero Marker.</b> Input that connects to the zero marker output of a rotary device or detects the pressing of a pushbutton.                                                                                                                                           |
| DAI_PIN[nn]   | InOut     | <b>Pin n.</b> The digital applications interface (DAI0) connects various peripherals to any of the DAI0_PINxx pins. Programs make these connections using the signal routing unit (SRU).                                                                                      |
| DMC_A[nn]     | Output    | <b>Address n.</b> Address bus.                                                                                                                                                                                                                                                |
| DMC_BA[n]     | Output    | <b>Bank Address n.</b> Defines which internal bank an activate, read, write, or precharge command is applied to on the dynamic memory. Bank Address n also defines which mode registers (MR, EMR, EMR2, and/or EMR3) load during the load mode register command.              |
| DMC_CAS       | Output    | <b>Column Address Strobe.</b> Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the CAS input of dynamic memory.                                                                                         |
| DMC_CK        | Output    | <b>Clock.</b> Outputs DCLK to external dynamic memory.                                                                                                                                                                                                                        |
| DMC_CK        | Output    | <b>Clock (Complement).</b> Complement of DMC_CK.                                                                                                                                                                                                                              |
| DMC_CKE       | Output    | <b>Clock Enable.</b> Active high clock enable. Connects to the CKE input of the dynamic memory.                                                                                                                                                                               |
| DMC_CS[n]     | Output    | <b>Chip Select n.</b> Commands are recognized by the memory only when this signal is asserted.                                                                                                                                                                                |
| DMC_DQ[nn]    | InOut     | <b>Data n.</b> Bidirectional data bus.                                                                                                                                                                                                                                        |
| DMC_LDM       | Output    | <b>Data Mask for Lower Byte.</b> Mask for DMC_DQ07:DMC_DQ00 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.                                                                                                                      |
| DMC_LDQS      | InOut     | <b>Data Strobe for Lower Byte.</b> DMC_DQ07:DMC_DQ00 data strobe. Output with write data. Input with read data. Can be single-ended or differential depending on register settings.                                                                                           |
| DMC_LDQS      | InOut     | <b>Data Strobe for Lower Byte (Complement).</b> Complement of DMC_LDQS.                                                                                                                                                                                                       |
| DMC_ODT       | Output    | <b>On Die Termination.</b> Enables dynamic memory termination resistances when driven high (assuming the memory is properly configured). ODT is enabled or disabled regardless of read or write commands.                                                                     |
| DMC_RAS       | Output    | <b>Row Address Strobe.</b> Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the RAS input of dynamic memory.                                                                                            |
| DMC_RESET     | Output    | <b>Reset.</b>                                                                                                                                                                                                                                                                 |
| DMC_RZQ       | InOut     | <b>External Calibration Resistor Connection.</b>                                                                                                                                                                                                                              |
| DMC_UDM       | Output    | <b>Data Mask for Upper Byte.</b> Mask for DMC_DQ15:DMC_DQ08 write data when driven high. Sampled on both edges of the data strobe by the dynamic memory.                                                                                                                      |
| DMC_UDQS      | InOut     | <b>Data Strobe for Upper Byte.</b> DMC_DQ15:DMC_DQ08 data strobe. Output with write data. Input with read data. Can be single-ended or differential depending on register settings.                                                                                           |
| DMC_UDQS      | InOut     | <b>Data Strobe for Upper Byte (Complement).</b> Complement of DMC_UDQS.                                                                                                                                                                                                       |
| DMC_VREF      | Input     | <b>Voltage Reference.</b> Connects to half of the VDD_DMC voltage. Applies to the DMC0_VREF pins.                                                                                                                                                                             |
| DMC_WE        | Output    | <b>Write Enable.</b> Defines the operation for external dynamic memory to perform in conjunction with other DMC command signals. Connect to the WE input of dynamic memory.                                                                                                   |
| HADC_EOC_DOUT | Output    | <b>End of Conversion/Serial Data Out.</b> Transitions high for one cycle of the HADC internal clock at the end of every conversion. Alternatively, HADC serial data out can be seen by setting the appropriate bit in HADC_CTL.                                               |

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Table 9. ADSP-2156x Detailed Signal Descriptions (Continued)

| Signal Name | Direction | Description                                                                                                                                                                           |
|-------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HADC_VIN[n] | Input     | <b>Analog Input at Channel n.</b> Analog voltage inputs for digital conversion.                                                                                                       |
| HADC_VREFN  | Input     | <b>Ground Reference for ADC.</b> Connect to an external voltage reference that meets data sheet specifications.                                                                       |
| HADC_VREFP  | Input     | <b>External Reference for ADC.</b> Connect to an external voltage reference that meets data sheet specifications.                                                                     |
| JTG_TCK     | Input     | <b>JTAG Clock.</b> JTAG test access port clock.                                                                                                                                       |
| JTG_TDI     | Input     | <b>JTAG Serial Data In.</b> JTAG test access port data input.                                                                                                                         |
| JTG_TDO     | Output    | <b>JTAG Serial Data Out.</b> JTAG test access port data output.                                                                                                                       |
| JTG_TMS     | Input     | <b>JTAG Mode Select.</b> JTAG test access port mode select.                                                                                                                           |
| JTG_TRST    | Input     | <b>JTAG Reset.</b> JTAG test access port reset.                                                                                                                                       |
| LP_ACK      | InOut     | <b>Acknowledge.</b> Provides handshaking. When the link port is configured as a receiver, LP_ACK is an output. When the link port is configured as a transmitter, LP_ACK is an input. |
| LP_CLK      | InOut     | <b>Clock.</b> When the link port is configured as a receiver, LP_CLK is an input. When the link port is configured as a transmitter, LP_CLK is an output.                             |
| LP_D[n]     | InOut     | <b>Data n.</b> Data bus. Input when receiving, output when transmitting.                                                                                                              |
| MLB_CLK     | InOut     | <b>Single-Ended Clock.</b>                                                                                                                                                            |
| MLB_DAT     | InOut     | <b>Single-Ended Data.</b>                                                                                                                                                             |
| MLB_SIG     | InOut     | <b>Single-Ended Signal.</b>                                                                                                                                                           |
| OSPI_CLK    | Output    | <b>SPI Master Clock Output.</b> SPI master clock output.                                                                                                                              |
| OSPI_D2     | InOut     | <b>Data 2.</b> Transfers serial data in quad and octal modes.                                                                                                                         |
| OSPI_D3     | InOut     | <b>Data 3.</b> Transfers serial data in quad and octal modes.                                                                                                                         |
| OSPI_D4     | InOut     | <b>Data 4.</b> Transfers serial data in octal mode.                                                                                                                                   |
| OSPI_D5     | InOut     | <b>Data 5.</b> Transfers serial data in octal mode.                                                                                                                                   |
| OSPI_D6     | InOut     | <b>Data 6.</b> Transfers serial data in octal mode.                                                                                                                                   |
| OSPI_D7     | InOut     | <b>Data 7.</b> Transfers serial data in octal mode.                                                                                                                                   |
| OSPI_MISO   | InOut     | <b>Master In, Slave Out.</b> Transfers serial data. Operates in the same direction as SPI_MOSI in dual and quad modes.                                                                |
| OSPI_MOSI   | InOut     | <b>Master Out, Slave In.</b> Transfers serial data. Operates in the same direction as SPI_MISO in dual and quad modes.                                                                |
| OSPI_SEL[n] | Output    | <b>Slave Select Output n.</b> Used in master mode to enable the desired slave.                                                                                                        |
| P_[nn]      | InOut     | <b>Position n.</b> General-purpose input/output. See the <a href="#">ADSP-21562/3/5/6/7/9 SHARC+ Processor Hardware Reference</a> manual for programming information.                 |
| SPI_CLK     | Output    | <b>SPI Master Clock Output.</b> SPI master clock output.                                                                                                                              |
| SPI_D2      | InOut     | <b>Data 2.</b> Transfers serial data in quad modes.                                                                                                                                   |
| SPI_D3      | InOut     | <b>Data 3.</b> Transfers serial data in quad modes. Open-drain when ODM mode is enabled.                                                                                              |
| SPI_MISO    | InOut     | <b>Master In, Slave Out.</b> Transfers serial data. Operates in the same direction as SPI_MOSI in dual and quad modes. Open-drain when ODM mode is enabled.                           |
| SPI_MOSI    | InOut     | <b>Master Out, Slave In.</b> Transfers serial data. Operates in the same direction as SPI_MISO in dual and quad modes. Open-drain when ODM mode is enabled.                           |
| SPI_RDY     | InOut     | <b>Ready.</b> Optional flow signal. Output in slave mode, input in master mode.                                                                                                       |
| SPI_SEL[n]  | Output    | <b>Slave Select Output n.</b> Used in master mode to enable the desired slave.                                                                                                        |
| SPI_SS      | Input     | <b>Slave Select Input.</b><br>Slave mode—acts as the slave select input.<br>Master mode—optionally serves as an error detection input for the SPI when there are multiple masters.    |
| SPT_ACLK    | InOut     | <b>Channel A Clock.</b> Data and frame sync are driven or sampled with respect to this clock. This signal can be either internally or externally generated.                           |
| SPT_AD0     | InOut     | <b>Channel A Data 0.</b> Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.                    |

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Table 9. ADSP-2156x Detailed Signal Descriptions (Continued)

| Signal Name                     | Direction | Description                                                                                                                                                                                   |
|---------------------------------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SPT_AD1                         | InOut     | <b>Channel A Data 1.</b> Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.                          |
| SPT_AFS                         | InOut     | <b>Channel A Frame Sync.</b> The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.                                                |
| SPT_ATDV                        | Output    | <b>Channel A Transmit Data Valid.</b> This signal is optional and only active when SPORT is configured in multichannel transmit mode. It is asserted during enabled slots.                    |
| SPT_BCLK                        | InOut     | <b>Channel B Clock.</b> Data and frame sync are driven or sampled with respect to this clock. This signal can be either internally or externally generated.                                   |
| SPT_BD0                         | InOut     | <b>Channel B Data 0.</b> Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.                            |
| SPT_BD1                         | InOut     | <b>Channel B Data 1.</b> Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.                          |
| SPT_BFS                         | InOut     | <b>Channel B Frame Sync.</b> The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.                                                |
| SPT_BTDTV                       | Output    | <b>Channel B Transmit Data Valid.</b> This signal is optional and only active when SPORT is configured in multichannel transmit mode. It is asserted during enabled slots.                    |
| SYS_BMODE[n]                    | Input     | <b>Boot Mode Control n.</b> Selects the boot mode of the processor.                                                                                                                           |
| SYS_CLKINO                      | Input     | <b>Clock/Crystal Input.</b>                                                                                                                                                                   |
| SYS_CLKOUT                      | Output    | <b>Processor Clock Output.</b> Outputs internal clocks. Clocks may be divided down. See the <a href="#">ADSP-21562/3/5/6/7/9 SHARC+ Processor Hardware Reference</a> manual for more details. |
| SYS_FAULT                       | InOut     | <b>Active, High, Fault Output.</b> Indicates internal faults or senses external faults depending on the operating mode.                                                                       |
| $\overline{\text{SYS\_FAULT}}$  | InOut     | <b>Active, Low, Fault Output.</b> Indicates internal faults or senses external faults depending on the operating mode.                                                                        |
| $\overline{\text{SYS\_HWRST}}$  | Input     | <b>Processor Hardware Reset Control.</b> Resets the device when asserted.                                                                                                                     |
| $\overline{\text{SYS\_RESOUT}}$ | Output    | <b>Reset Output.</b> Indicates the device is in the reset state.                                                                                                                              |
| SYS_XTALO                       | Output    | <b>Crystal Output.</b>                                                                                                                                                                        |
| TM_ACI[n]                       | Input     | <b>Alternate Capture Input n.</b> Provides an additional input for WIDCAP, WATCHDOG, and PININT modes.                                                                                        |
| TM_ACLK[n]                      | Input     | <b>Alternate Clock n.</b> Provides an additional time base for an individual timer.                                                                                                           |
| TM_CLK                          | Input     | <b>Clock.</b> Provides an additional global time base for all GP timers.                                                                                                                      |
| TM_TMR[n]                       | InOut     | <b>Timer n.</b> The main input/output signal for each timer.                                                                                                                                  |
| TRACE_CLK                       | Output    | <b>Trace Clock.</b> Clock output.                                                                                                                                                             |
| TRACE_D[nn]                     | Output    | <b>Trace Data n.</b> Unidirectional data bus.                                                                                                                                                 |
| TWI_SCL                         | InOut     | <b>Serial Clock.</b> Clock output when controller, clock input when target.                                                                                                                   |
| TWI_SDA                         | InOut     | <b>Serial Data.</b> Receives or transmits data.                                                                                                                                               |
| $\overline{\text{UART\_CTS}}$   | Input     | <b>Clear to Send.</b> Flow control signal.                                                                                                                                                    |
| $\overline{\text{UART\_RTS}}$   | Output    | <b>Request to Send.</b> Flow control signal.                                                                                                                                                  |
| $\overline{\text{UART\_RX}}$    | Input     | <b>Receive.</b> Receives input. Typically connects to a transceiver that meets the electrical requirements of the device with which it is communicating.                                      |
| $\overline{\text{UART\_TX}}$    | Output    | <b>Transmit.</b> Transmits output. Typically connects to a transceiver that meets the electrical requirements of the device with which it is communicating.                                   |

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## 400-BALL CSP\_BGA SIGNAL DESCRIPTIONS

The processor pin definitions are shown in [Table 10](#) for the 400-ball CSP\_BGA package. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The description column provides a descriptive name for each signal.
- The port column shows whether a signal is multiplexed with other signals on a general-purpose I/O port pin.

- The pin name column identifies the name of the package pin (at power-on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).
- The DAI pins and their associated signal routing units (SRUs) connect inputs and outputs of the DAI peripherals (SPORT, ASRC, S/PDIF, and PCG). See the [ADSP-21562/3/5/6/7/9 SHARC+ Processor Hardware Reference](#) manual for complete information on the use of the DAI and SRUs.

**Table 10. ADSP-2156x 400-Ball CSP\_BGA Signal Descriptions**

| Signal Name | Description                 | Port      | Pin Name   |
|-------------|-----------------------------|-----------|------------|
| C0_FLG0     | SHARC+ Core 0 FLAGS I/O 0   | A         | PA_12      |
| C0_FLG1     | SHARC+ Core 0 FLAGS I/O 1   | A         | PA_13      |
| C0_FLG2     | SHARC+ Core 0 FLAGS I/O 2   | B         | PB_03      |
| C0_FLG3     | SHARC+ Core 0 FLAGS I/O 3   | B         | PB_02      |
| CNT0_DG     | CNT0 Count Down and Gate    | B         | PB_05      |
| CNT0_UD     | CNT0 Count Up and Direction | B         | PB_03      |
| CNT0_ZM     | CNT0 Count Zero Marker      | B         | PB_04      |
| DAI0_PIN01  | DAI0 Pin 1                  | Not Muxed | DAI0_PIN01 |
| DAI0_PIN02  | DAI0 Pin 2                  | Not Muxed | DAI0_PIN02 |
| DAI0_PIN03  | DAI0 Pin 3                  | Not Muxed | DAI0_PIN03 |
| DAI0_PIN04  | DAI0 Pin 4                  | Not Muxed | DAI0_PIN04 |
| DAI0_PIN05  | DAI0 Pin 5                  | Not Muxed | DAI0_PIN05 |
| DAI0_PIN06  | DAI0 Pin 6                  | Not Muxed | DAI0_PIN06 |
| DAI0_PIN07  | DAI0 Pin 7                  | Not Muxed | DAI0_PIN07 |
| DAI0_PIN08  | DAI0 Pin 8                  | Not Muxed | DAI0_PIN08 |
| DAI0_PIN09  | DAI0 Pin 9                  | Not Muxed | DAI0_PIN09 |
| DAI0_PIN10  | DAI0 Pin 10                 | Not Muxed | DAI0_PIN10 |
| DAI0_PIN11  | DAI0 Pin 11                 | Not Muxed | DAI0_PIN11 |
| DAI0_PIN12  | DAI0 Pin 12                 | Not Muxed | DAI0_PIN12 |
| DAI0_PIN19  | DAI0 Pin 19                 | Not Muxed | DAI0_PIN19 |
| DAI0_PIN20  | DAI0 Pin 20                 | Not Muxed | DAI0_PIN20 |
| DAI1_PIN01  | DAI1 Pin 1                  | Not Muxed | DAI1_PIN01 |
| DAI1_PIN02  | DAI1 Pin 2                  | Not Muxed | DAI1_PIN02 |
| DAI1_PIN03  | DAI1 Pin 3                  | Not Muxed | DAI1_PIN03 |
| DAI1_PIN04  | DAI1 Pin 4                  | Not Muxed | DAI1_PIN04 |
| DAI1_PIN05  | DAI1 Pin 5                  | Not Muxed | DAI1_PIN05 |
| DAI1_PIN06  | DAI1 Pin 6                  | Not Muxed | DAI1_PIN06 |
| DAI1_PIN07  | DAI1 Pin 7                  | Not Muxed | DAI1_PIN07 |
| DAI1_PIN08  | DAI1 Pin 8                  | Not Muxed | DAI1_PIN08 |
| DAI1_PIN09  | DAI1 Pin 9                  | Not Muxed | DAI1_PIN09 |
| DAI1_PIN10  | DAI1 Pin 10                 | Not Muxed | DAI1_PIN10 |
| DAI1_PIN11  | DAI1 Pin 11                 | Not Muxed | DAI1_PIN11 |
| DAI1_PIN12  | DAI1 Pin 12                 | Not Muxed | DAI1_PIN12 |
| DAI1_PIN19  | DAI1 Pin 19                 | Not Muxed | DAI1_PIN19 |
| DAI1_PIN20  | DAI1 Pin 20                 | Not Muxed | DAI1_PIN20 |

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Table 10. ADSP-2156x 400-Ball CSP\_BGA Signal Descriptions (Continued)

| Signal Name                     | Description                                   | Port      | Pin Name                        |
|---------------------------------|-----------------------------------------------|-----------|---------------------------------|
| DMC0_A00                        | DMC0 Address 0                                | Not Muxed | DMC0_A00                        |
| DMC0_A01                        | DMC0 Address 1                                | Not Muxed | DMC0_A01                        |
| DMC0_A02                        | DMC0 Address 2                                | Not Muxed | DMC0_A02                        |
| DMC0_A03                        | DMC0 Address 3                                | Not Muxed | DMC0_A03                        |
| DMC0_A04                        | DMC0 Address 4                                | Not Muxed | DMC0_A04                        |
| DMC0_A05                        | DMC0 Address 5                                | Not Muxed | DMC0_A05                        |
| DMC0_A06                        | DMC0 Address 6                                | Not Muxed | DMC0_A06                        |
| DMC0_A07                        | DMC0 Address 7                                | Not Muxed | DMC0_A07                        |
| DMC0_A08                        | DMC0 Address 8                                | Not Muxed | DMC0_A08                        |
| DMC0_A09                        | DMC0 Address 9                                | Not Muxed | DMC0_A09                        |
| DMC0_A10                        | DMC0 Address 10                               | Not Muxed | DMC0_A10                        |
| DMC0_A11                        | DMC0 Address 11                               | Not Muxed | DMC0_A11                        |
| DMC0_A12                        | DMC0 Address 12                               | Not Muxed | DMC0_A12                        |
| DMC0_A13                        | DMC0 Address 13                               | Not Muxed | DMC0_A13                        |
| DMC0_A14                        | DMC0 Address 14                               | Not Muxed | DMC0_A14                        |
| DMC0_A15                        | DMC0 Address 15                               | Not Muxed | DMC0_A15                        |
| DMC0_BA0                        | DMC0 Bank Address Input 0                     | Not Muxed | DMC0_BA0                        |
| DMC0_BA1                        | DMC0 Bank Address Input 1                     | Not Muxed | DMC0_BA1                        |
| DMC0_BA2                        | DMC0 Bank Address Input 2                     | Not Muxed | DMC0_BA2                        |
| $\overline{\text{DMC0\_CAS}}$   | DMC0 Column Address Strobe                    | Not Muxed | $\overline{\text{DMC0\_CAS}}$   |
| DMC0_CK                         | DMC0 Clock                                    | Not Muxed | DMC0_CK                         |
| $\overline{\text{DMC0\_CK}}$    | DMC0 Clock (Complement)                       | Not Muxed | $\overline{\text{DMC0\_CK}}$    |
| DMC0_CKE                        | DMC0 Clock Enable                             | Not Muxed | DMC0_CKE                        |
| $\overline{\text{DMC0\_CS0}}$   | DMC0 Chip Select 0                            | Not Muxed | $\overline{\text{DMC0\_CS0}}$   |
| DMC0_DQ00                       | DMC0 Data 0                                   | Not Muxed | DMC0_DQ00                       |
| DMC0_DQ01                       | DMC0 Data 1                                   | Not Muxed | DMC0_DQ01                       |
| DMC0_DQ02                       | DMC0 Data 2                                   | Not Muxed | DMC0_DQ02                       |
| DMC0_DQ03                       | DMC0 Data 3                                   | Not Muxed | DMC0_DQ03                       |
| DMC0_DQ04                       | DMC0 Data 4                                   | Not Muxed | DMC0_DQ04                       |
| DMC0_DQ05                       | DMC0 Data 5                                   | Not Muxed | DMC0_DQ05                       |
| DMC0_DQ06                       | DMC0 Data 6                                   | Not Muxed | DMC0_DQ06                       |
| DMC0_DQ07                       | DMC0 Data 7                                   | Not Muxed | DMC0_DQ07                       |
| DMC0_DQ08                       | DMC0 Data 8                                   | Not Muxed | DMC0_DQ08                       |
| DMC0_DQ09                       | DMC0 Data 9                                   | Not Muxed | DMC0_DQ09                       |
| DMC0_DQ10                       | DMC0 Data 10                                  | Not Muxed | DMC0_DQ10                       |
| DMC0_DQ11                       | DMC0 Data 11                                  | Not Muxed | DMC0_DQ11                       |
| DMC0_DQ12                       | DMC0 Data 12                                  | Not Muxed | DMC0_DQ12                       |
| DMC0_DQ13                       | DMC0 Data 13                                  | Not Muxed | DMC0_DQ13                       |
| DMC0_DQ14                       | DMC0 Data 14                                  | Not Muxed | DMC0_DQ14                       |
| DMC0_DQ15                       | DMC0 Data 15                                  | Not Muxed | DMC0_DQ15                       |
| DMC0_LDM                        | DMC0 Data Mask for Lower Byte                 | Not Muxed | DMC0_LDM                        |
| DMC0_LDQS                       | DMC0 Data Strobe for Lower Byte               | Not Muxed | DMC0_LDQS                       |
| $\overline{\text{DMC0\_LDQS}}$  | DMC0 Data Strobe for Lower Byte (Complement)  | Not Muxed | $\overline{\text{DMC0\_LDQS}}$  |
| DMC0_ODT                        | DMC0 On-die Termination                       | Not Muxed | DMC0_ODT                        |
| $\overline{\text{DMC0\_RAS}}$   | DMC0 Row Address Strobe                       | Not Muxed | $\overline{\text{DMC0\_RAS}}$   |
| $\overline{\text{DMC0\_RESET}}$ | DMC0 Reset (DDR3 Only)                        | Not Muxed | $\overline{\text{DMC0\_RESET}}$ |
| DMC0_RZQ                        | DMC0 External Calibration Resistor Connection | Not Muxed | DMC0_RZQ                        |
| DMC0_UDM                        | DMC0 Data Mask for Upper Byte                 | Not Muxed | DMC0_UDM                        |

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Table 10. ADSP-2156x 400-Ball CSP\_BGA Signal Descriptions (Continued)

| Signal Name                    | Description                                  | Port      | Pin Name                       |
|--------------------------------|----------------------------------------------|-----------|--------------------------------|
| DMC0_UDQS                      | DMC0 Data Strobe for Upper Byte              | Not Muxed | DMC0_UDQS                      |
| $\overline{\text{DMC0\_UDQS}}$ | DMC0 Data Strobe for Upper Byte (Complement) | Not Muxed | $\overline{\text{DMC0\_UDQS}}$ |
| DMC0_VREF                      | DMC0 Voltage Reference                       | Not Muxed | DMC0_VREF0, DMC0_VREF1         |
| $\overline{\text{DMC0\_WE}}$   | DMC0 Write Enable                            | Not Muxed | $\overline{\text{DMC0\_WE}}$   |
| HADC0_EOC_DOUT                 | HADC0 End of Conversion / Serial Data Out    | A         | PA_11                          |
| HADC0_VIN0                     | HADC0 Analog Input at channel 0              | Not Muxed | HADC0_VIN0                     |
| HADC0_VIN1                     | HADC0 Analog Input at channel 1              | Not Muxed | HADC0_VIN1                     |
| HADC0_VIN2                     | HADC0 Analog Input at channel 2              | Not Muxed | HADC0_VIN2                     |
| HADC0_VIN3                     | HADC0 Analog Input at channel 3              | Not Muxed | HADC0_VIN3                     |
| HADC0_VREFN                    | HADC0 Ground Reference for ADC               | Not Muxed | HADC0_VREFN                    |
| HADC0_VREFP                    | HADC0 External Reference for ADC             | Not Muxed | HADC0_VREFP                    |
| JTG_TCK                        | JTAG Clock                                   | Not Muxed | JTG_TCK                        |
| JTG_TDI                        | JTAG Serial Data In                          | Not Muxed | JTG_TDI                        |
| JTG_TDO                        | JTAG Serial Data Out                         | Not Muxed | JTG_TDO                        |
| JTG_TMS                        | JTAG Mode Select                             | Not Muxed | JTG_TMS                        |
| $\overline{\text{JTG\_TRST}}$  | JTAG Reset                                   | Not Muxed | $\overline{\text{JTG\_TRST}}$  |
| LP0_ACK                        | LP0 Acknowledge                              | B         | PB_04                          |
| LP0_CLK                        | LP0 Clock                                    | B         | PB_06                          |
| LP0_D0                         | LP0 Data 0                                   | B         | PB_07                          |
| LP0_D1                         | LP0 Data 1                                   | B         | PB_08                          |
| LP0_D2                         | LP0 Data 2                                   | B         | PB_09                          |
| LP0_D3                         | LP0 Data 3                                   | B         | PB_10                          |
| LP0_D4                         | LP0 Data 4                                   | B         | PB_11                          |
| LP0_D5                         | LP0 Data 5                                   | B         | PB_12                          |
| LP0_D6                         | LP0 Data 6                                   | B         | PB_13                          |
| LP0_D7                         | LP0 Data 7                                   | B         | PB_14                          |
| LP1_ACK                        | LP1 Acknowledge                              | B         | PB_02                          |
| LP1_CLK                        | LP1 Clock                                    | C         | PC_07                          |
| LP1_D0                         | LP1 Data 0                                   | B         | PB_15                          |
| LP1_D1                         | LP1 Data 1                                   | C         | PC_00                          |
| LP1_D2                         | LP1 Data 2                                   | C         | PC_01                          |
| LP1_D3                         | LP1 Data 3                                   | C         | PC_02                          |
| LP1_D4                         | LP1 Data 4                                   | C         | PC_03                          |
| LP1_D5                         | LP1 Data 5                                   | C         | PC_04                          |
| LP1_D6                         | LP1 Data 6                                   | C         | PC_05                          |
| LP1_D7                         | LP1 Data 7                                   | C         | PC_06                          |
| MLB0_CLK                       | MLB0 Single-Ended Clock                      | B         | PB_02                          |
| MLB0_DAT                       | MLB0 Single-Ended Data                       | B         | PB_00                          |
| MLB0_SIG                       | MLB0 Single-Ended Signal                     | B         | PB_01                          |
| OSPI0_CLK                      | OSPI0 Clock                                  | A         | PA_04                          |
| OSPI0_D2                       | OSPI0 Data 2                                 | A         | PA_02                          |
| OSPI0_D3                       | OSPI0 Data 3                                 | A         | PA_03                          |
| OSPI0_D4                       | OSPI0 Data 4                                 | A         | PA_06                          |
| OSPI0_D5                       | OSPI0 Data 5                                 | A         | PA_07                          |
| OSPI0_D6                       | OSPI0 Data 6                                 | A         | PA_08                          |
| OSPI0_D7                       | OSPI0 Data 7                                 | A         | PA_09                          |
| OSPI0_MISO/D1                  | OSPI0 Master In, Slave Out                   | A         | PA_00                          |
| OSPI0_MOSI/D0                  | OSPI0 Master Out, Slave In                   | A         | PA_01                          |

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**Table 10. ADSP-2156x 400-Ball CSP\_BGA Signal Descriptions (Continued)**

| Signal Name                     | Description                      | Port      | Pin Name                       |
|---------------------------------|----------------------------------|-----------|--------------------------------|
| $\overline{\text{OSPI0\_SEL1}}$ | OSPI0 Slave Select Output 1      | A         | PA_05                          |
| $\overline{\text{OSPI0\_SEL2}}$ | OSPI0 Slave Select Output 2      | C         | PC_04                          |
| $\overline{\text{OSPI0\_SEL3}}$ | OSPI0 Slave Select Output 3      | C         | PC_05                          |
| SPI0_CLK                        | SPI0 Clock                       | A         | PA_06                          |
| SPI0_MISO                       | SPI0 Master In, Slave Out        | A         | PA_07                          |
| SPI0_MOSI                       | SPI0 Master Out, Slave In        | A         | PA_08                          |
| SPI0_RDY                        | SPI0 Ready                       | B         | PB_11                          |
| $\overline{\text{SPI0\_SEL1}}$  | SPI0 Slave Select Output 1       | A         | PA_09                          |
| $\overline{\text{SPI0\_SEL2}}$  | SPI0 Slave Select Output 2       | B         | PB_05                          |
| $\overline{\text{SPI0\_SEL3}}$  | SPI0 Slave Select Output 3       | B         | PB_14                          |
| $\overline{\text{SPI0\_SEL4}}$  | SPI0 Slave Select Output 4       | B         | PB_15                          |
| $\overline{\text{SPI0\_SS}}$    | SPI0 Slave Select Input          | A         | PA_09                          |
| SPI1_CLK                        | SPI1 Clock                       | A         | PA_10                          |
| SPI1_D2                         | SPI1 Data 2                      | A         | PA_14                          |
| SPI1_D3                         | SPI1 Data 3                      | A         | PA_15                          |
| SPI1_MISO                       | SPI1 Master In, Slave Out        | A         | PA_11                          |
| SPI1_MOSI                       | SPI1 Master Out, Slave In        | A         | PA_12                          |
| SPI1_RDY                        | SPI1 Ready                       | C         | PC_06                          |
| $\overline{\text{SPI1\_SEL1}}$  | SPI1 Slave Select Output 1       | A         | PA_13                          |
| $\overline{\text{SPI1\_SEL2}}$  | SPI1 Slave Select Output 2       | B         | PB_10                          |
| $\overline{\text{SPI1\_SEL3}}$  | SPI1 Slave Select Output 3       | B         | PB_13                          |
| $\overline{\text{SPI1\_SEL4}}$  | SPI1 Slave Select Output 4       | C         | PC_00                          |
| $\overline{\text{SPI1\_SEL5}}$  | SPI1 Slave Select Output 5       | B         | PB_06                          |
| $\overline{\text{SPI1\_SEL6}}$  | SPI1 Slave Select Output 6       | C         | PC_02                          |
| $\overline{\text{SPI1\_SEL7}}$  | SPI1 Slave Select Output 7       | B         | PB_08                          |
| $\overline{\text{SPI1\_SS}}$    | SPI1 Slave Select Input          | A         | PA_13                          |
| SPI2_CLK                        | SPI2 Clock                       | A         | PA_04                          |
| SPI2_D2                         | SPI2 Data 2                      | A         | PA_02                          |
| SPI2_D3                         | SPI2 Data 3                      | A         | PA_03                          |
| SPI2_MISO                       | SPI2 Master In, Slave Out        | A         | PA_00                          |
| SPI2_MOSI                       | SPI2 Master Out, Slave In        | A         | PA_01                          |
| SPI2_RDY                        | SPI2 Ready                       | B         | PB_05                          |
| $\overline{\text{SPI2\_SEL1}}$  | SPI2 Slave Select Output 1       | A         | PA_05                          |
| $\overline{\text{SPI2\_SEL2}}$  | SPI2 Slave Select Output 2       | B         | PB_03                          |
| $\overline{\text{SPI2\_SEL3}}$  | SPI2 Slave Select Output 3       | B         | PB_12                          |
| $\overline{\text{SPI2\_SEL4}}$  | SPI2 Slave Select Output 4       | C         | PC_01                          |
| $\overline{\text{SPI2\_SEL5}}$  | SPI2 Slave Select Output 5       | B         | PB_07                          |
| $\overline{\text{SPI2\_SEL6}}$  | SPI2 Slave Select Output 6       | C         | PC_03                          |
| $\overline{\text{SPI2\_SEL7}}$  | SPI2 Slave Select Output 7       | B         | PB_09                          |
| $\overline{\text{SPI2\_SS}}$    | SPI2 Slave Select Input          | A         | PA_05                          |
| SYS_BMODE0                      | Boot Mode Control Pin 0          | Not Muxed | SYS_BMODE0                     |
| SYS_BMODE1                      | Boot Mode Control Pin 1          | Not Muxed | SYS_BMODE1                     |
| SYS_BMODE2                      | Boot Mode Control Pin 2          | Not Muxed | SYS_BMODE2                     |
| SYS_CLKIN0                      | Clock/Crystal Input              | Not Muxed | SYS_CLKIN0                     |
| SYS_CLKOUT                      | Processor Clock Output           | Not Muxed | SYS_CLKOUT                     |
| SYS_FAULT                       | Active, High, Fault Output       | C         | PC_07                          |
| $\overline{\text{SYS\_FAULT}}$  | Active, Low, Fault Output        | Not Muxed | $\overline{\text{SYS\_FAULT}}$ |
| $\overline{\text{SYS\_HWRST}}$  | Processor Hardware Reset Control | Not Muxed | $\overline{\text{SYS\_HWRST}}$ |

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Table 10. ADSP-2156x 400-Ball CSP\_BGA Signal Descriptions (Continued)

| Signal Name | Description                      | Port      | Pin Name   |
|-------------|----------------------------------|-----------|------------|
| SYS_RESOUT  | Reset Output                     | Not Muxed | SYS_RESOUT |
| SYS_XTAL0   | Crystal Output                   | Not Muxed | SYS_XTAL0  |
| TM0_ACIO    | TIMER0 Alternate Capture Input 0 | A         | PA_07      |
| TM0_ACIO1   | TIMER0 Alternate Capture Input 1 | A         | PA_14      |
| TM0_ACIO2   | TIMER0 Alternate Capture Input 2 | B         | PB_11      |
| TM0_ACIO3   | TIMER0 Alternate Capture Input 3 | B         | PB_00      |
| TM0_ACIO4   | TIMER0 Alternate Capture Input 4 | A         | PA_11      |
| TM0_ACLK1   | TIMER0 Alternate Clock 1         | A         | PA_06      |
| TM0_ACLK2   | TIMER0 Alternate Clock 2         | A         | PA_08      |
| TM0_ACLK3   | TIMER0 Alternate Clock 3         | A         | PA_02      |
| TM0_ACLK4   | TIMER0 Alternate Clock 4         | B         | PB_02      |
| TM0_CLK     | TIMER0 Clock                     | B         | PB_01      |
| TM0_TMR0    | TIMER0 Timer 0                   | A         | PA_10      |
| TM0_TMR1    | TIMER0 Timer 1                   | A         | PA_12      |
| TM0_TMR2    | TIMER0 Timer 2                   | A         | PA_13      |
| TM0_TMR3    | TIMER0 Timer 3                   | B         | PB_03      |
| TM0_TMR4    | TIMER0 Timer 4                   | B         | PB_04      |
| TM0_TMR5    | TIMER0 Timer 5                   | B         | PB_05      |
| TM0_TMR6    | TIMER0 Timer 6                   | B         | PB_08      |
| TM0_TMR7    | TIMER0 Timer 7                   | B         | PB_09      |
| TM0_TMR8    | TIMER0 Timer 8                   | C         | PC_05      |
| TM0_TMR9    | TIMER0 Timer 9                   | C         | PC_07      |
| TRACE0_CLK  | TRACE0 Trace Clock               | B         | PB_06      |
| TRACE0_D00  | TRACE0 Trace Data 0              | B         | PB_07      |
| TRACE0_D01  | TRACE0 Trace Data1               | B         | PB_08      |
| TRACE0_D02  | TRACE0 Trace Data2               | B         | PB_09      |
| TRACE0_D03  | TRACE0 Trace Data 3              | B         | PB_10      |
| TRACE0_D04  | TRACE0 Trace Data4               | C         | PC_00      |
| TRACE0_D05  | TRACE0 Trace Data5               | C         | PC_01      |
| TRACE0_D06  | TRACE0 Trace Data6               | C         | PC_02      |
| TRACE0_D07  | TRACE0 Trace Data 7              | C         | PC_03      |
| TWI0_SCL    | TWI0 Serial Clock                | A         | PA_10      |
| TWI0_SDA    | TWI0 Serial Data                 | A         | PA_11      |
| TWI1_SCL    | TWI1 Serial Clock                | B         | PB_00      |
| TWI1_SDA    | TWI1 Serial Data                 | B         | PB_01      |
| TWI2_SCL    | TWI2 Serial Clock                | A         | PA_14      |
| TWI2_SDA    | TWI2 Serial Data                 | A         | PA_15      |
| TWI3_SCL    | TWI3 Serial Clock                | A         | PA_02      |
| TWI3_SDA    | TWI3 Serial Data                 | A         | PA_03      |
| TWI4_SCL    | TWI4 Serial Clock                | C         | PC_00      |
| TWI4_SDA    | TWI4 Serial Data                 | C         | PC_01      |
| TWI5_SCL    | TWI5 Serial Clock                | C         | PC_02      |
| TWI5_SDA    | TWI5 Serial Data                 | C         | PC_03      |
| UART0_CTS   | UART0 Clear to Send              | A         | PA_09      |
| UART0_RTS   | UART0 Request to Send            | A         | PA_08      |
| UART0_RX    | UART0 Receive                    | A         | PA_07      |
| UART0_TX    | UART0 Transmit                   | A         | PA_06      |
| UART1_CTS   | UART1 Clear to Send              | B         | PB_01      |

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Table 10. ADSP-2156x 400-Ball CSP\_BGA Signal Descriptions (Continued)

| Signal Name             | Description           | Port | Pin Name |
|-------------------------|-----------------------|------|----------|
| UART1_RT $\overline{S}$ | UART1 Request to Send | B    | PB_00    |
| UART1_RX                | UART1 Receive         | A    | PA_14    |
| UART1_TX                | UART1 Transmit        | A    | PA_15    |
| UART2_CT $\overline{S}$ | UART2 Clear to Send   | B    | PB_14    |
| UART2_RT $\overline{S}$ | UART2 Request to Send | B    | PB_13    |
| UART2_RX                | UART2 Receive         | B    | PB_11    |
| UART2_TX                | UART2 Transmit        | B    | PB_12    |

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## GPIO MULTIPLEXING FOR 400-BALL CSP\_BGA PACKAGE

Table 11 through Table 13 identify the pin functions that are multiplexed on the general-purpose I/O pins of the 400-ball CSP\_BGA package.

**Table 11. Signal Multiplexing for Port A**

| Signal Name | Multiplexed Function 0 | Multiplexed Function 1 | Multiplexed Function 2 | Multiplexed Function 3 | Multiplexed Function Input Tap |
|-------------|------------------------|------------------------|------------------------|------------------------|--------------------------------|
| PA_00       | SPI2_MISO              | OSPI0_MISO/D1          |                        |                        |                                |
| PA_01       | SPI2_MOSI              | OSPI0_MOSI/D0          |                        |                        |                                |
| PA_02       | SPI2_D2                | OSPI0_D2               | TWI3_SCL               |                        | TM0_ACLK3                      |
| PA_03       | SPI2_D3                | OSPI0_D3               | TWI3_SDA               |                        |                                |
| PA_04       | SPI2_CLK               | OSPI0_CLK              |                        |                        |                                |
| PA_05       | SPI2_SEL1              | OSPI0_SEL1             |                        |                        | SPI2_SS                        |
| PA_06       | SPI0_CLK               | UART0_TX               | OSPI0_D4               |                        | TM0_ACLK1                      |
| PA_07       | SPI0_MISO              | UART0_RX               | OSPI0_D5               |                        | TM0_ACIO                       |
| PA_08       | SPI0_MOSI              | UART0_RTS              | OSPI0_D6               |                        | TM0_ACLK2                      |
| PA_09       | SPI0_SEL1              | UART0_CTS              | OSPI0_D7               |                        | SPI0_SS                        |
| PA_10       | TWI0_SCL               | SPI1_CLK               | TM0_TMR0               |                        |                                |
| PA_11       | TWI0_SDA               | SPI1_MISO              | HADC0_EOC_DOUT         |                        | TM0_AC14                       |
| PA_12       | C0_FLG0                | SPI1_MOSI              | TM0_TMR1               |                        |                                |
| PA_13       | C0_FLG1                | SPI1_SEL1              | TM0_TMR2               |                        | SPI1_SS                        |
| PA_14       | TWI2_SCL               | SPI1_D2                | UART1_RX               |                        | TM0_AC11                       |
| PA_15       | TWI2_SDA               | SPI1_D3                | UART1_TX               |                        |                                |

**Table 12. Signal Multiplexing for Port B**

| Signal Name | Multiplexed Function 0 | Multiplexed Function 1 | Multiplexed Function 2 | Multiplexed Function 3 | Multiplexed Function Input Tap |
|-------------|------------------------|------------------------|------------------------|------------------------|--------------------------------|
| PB_00       | MLB0_DAT               | TWI1_SCL               | UART1_RTS              |                        | TM0_AC13                       |
| PB_01       | MLB0_SIG               | TWI1_SDA               | UART1_CTS              |                        | TM0_CLK                        |
| PB_02       | MLB0_CLK               | C0_FLG3                | LP1_ACK                |                        | TM0_ACLK4                      |
| PB_03       | TM0_TMR3               | C0_FLG2                | SPI2_SEL2              |                        | CNT0_UD                        |
| PB_04       | TM0_TMR4               | SPI1_RDY               | LP0_ACK                |                        | CNT0_ZM                        |
| PB_05       | TM0_TMR5               | SPI2_RDY               | SPI0_SEL2              |                        | CNT0_DG                        |
| PB_06       | LP0_CLK                | SPI1_SEL5              |                        | TRACE0_CLK             |                                |
| PB_07       | LP0_D0                 | SPI2_SEL5              |                        | TRACE0_D00             |                                |
| PB_08       | LP0_D1                 | SPI1_SEL7              | TM0_TMR6               | TRACE0_D01             |                                |
| PB_09       | LP0_D2                 | SPI2_SEL7              | TM0_TMR7               | TRACE0_D02             |                                |
| PB_10       | LP0_D3                 | SPI1_SEL2              |                        | TRACE0_D03             |                                |
| PB_11       | LP0_D4                 | SPI0_RDY               |                        | UART2_RX               | TM0_AC12                       |
| PB_12       | LP0_D5                 | SPI2_SEL3              |                        | UART2_TX               |                                |
| PB_13       | LP0_D6                 | SPI1_SEL3              |                        | UART2_RTS              |                                |
| PB_14       | LP0_D7                 | SPI0_SEL3              |                        | UART2_CTS              |                                |
| PB_15       | LP1_D0                 | SPI0_SEL4              |                        |                        |                                |

**Table 13. Signal Multiplexing for Port C**

| Signal Name | Multiplexed Function 0 | Multiplexed Function 1 | Multiplexed Function 2 | Multiplexed Function 3 | Multiplexed Function Input Tap |
|-------------|------------------------|------------------------|------------------------|------------------------|--------------------------------|
| PC_00       | LP1_D1                 | TWI4_SCL               | TRACE0_D04             | SPI1_SEL4              |                                |
| PC_01       | LP1_D2                 | TWI4_SDA               | TRACE0_D05             | SPI2_SEL4              |                                |
| PC_02       | LP1_D3                 | TWI5_SCL               | TRACE0_D06             | SPI1_SEL6              |                                |
| PC_03       | LP1_D4                 | TWI5_SDA               | TRACE0_D07             | SPI2_SEL6              |                                |
| PC_04       | LP1_D5                 | OSPI0_SEL2             |                        |                        |                                |
| PC_05       | LP1_D6                 | OSPI0_SEL3             | TM0_TMR8               |                        |                                |
| PC_06       | LP1_D7                 | SPI1_RDY               |                        |                        |                                |
| PC_07       | LP1_CLK                |                        | TM0_TMR9               | SYS_FAULT <sup>1</sup> |                                |

<sup>1</sup>The default PC\_07 pin function is SYS\_FAULT until the PORTC\_FER and PORTC\_MUX registers are explicitly programmed to change it.

Table 14 shows the internal timer signal routing. This table applies to both the 400-ball CSP\_BGA and 120-lead LQFP packages.

**Table 14. Internal Timer Signal Routing**

| Timer Input Signal | Internal Source |
|--------------------|-----------------|
| TM0_ACLK0          | SYS_CLKIN0      |
| TM0_ACi5           | DAI0_PB04_O     |
| TM0_ACLK5          | DAI0_PB03_O     |
| TM0_ACi6           | DAI1_PB04_O     |
| TM0_ACLK6          | DAI1_PB03_O     |
| TM0_ACi7           | CNT0_TO signal  |
| TM0_ACLK7          | SYS_CLKIN0      |
| TM0_ACi8           | DAI0_PB06_O     |
| TM0_ACLK8          | DAI0_PB05_O     |
| TM0_ACi9           | DAI1_PB06_O     |
| TM0_ACLK9          | DAI1_PB05_O     |

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## 120-LEAD LQFP SIGNAL DESCRIPTIONS

The processor pin definitions are shown [Table 15](#) for the 120-lead LQFP package. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The description column provides a descriptive name for each signal.
- The port column shows whether or not a signal is multiplexed with other signals on a general-purpose I/O port pin.

- The pin name column identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).
- The DAI pins and their associated signal routing units (SRUs) connect inputs and outputs of the DAI peripherals (SPORT, ASRC, S/PDIF, and PCG). See the Digital Audio Interface (DAI) chapter of the [ADSP-21562/3/5/6/7/9 SHARC+ Processor Hardware Reference](#) manual for complete information on the use of the DAIs and SRUs.

**Table 15. ADSP-2156x 120-Lead LQFP Signal Descriptions**

| Signal Name    | Description                               | Port      | Pin Name    |
|----------------|-------------------------------------------|-----------|-------------|
| C0_FLG0        | SHARC+ Core 0 FLAGS I/O 0                 | A         | PA_12       |
| C0_FLG1        | SHARC+ Core 0 FLAGS I/O 1                 | A         | PA_13       |
| C0_FLG2        | SHARC+ Core 0 FLAGS I/O 2                 | B         | PB_03       |
| C0_FLG3        | SHARC+ Core 0 FLAGS I/O 3                 | B         | PB_02       |
| CNT0_DG        | CNT0 Count Down and Gate                  | B         | PB_05       |
| CNT0_UD        | CNT0 Count Up and Direction               | B         | PB_03       |
| CNT0_ZM        | CNT0 Count Zero Marker                    | B         | PB_04       |
| DAI0_PIN01     | DAI0 Pin 1                                | Not Muxed | DAI0_PIN01  |
| DAI0_PIN02     | DAI0 Pin 2                                | Not Muxed | DAI0_PIN02  |
| DAI0_PIN03     | DAI0 Pin 3                                | Not Muxed | DAI0_PIN03  |
| DAI0_PIN04     | DAI0 Pin 4                                | Not Muxed | DAI0_PIN04  |
| DAI0_PIN05     | DAI0 Pin 5                                | Not Muxed | DAI0_PIN05  |
| DAI0_PIN06     | DAI0 Pin 6                                | Not Muxed | DAI0_PIN06  |
| DAI0_PIN07     | DAI0 Pin 7                                | Not Muxed | DAI0_PIN07  |
| DAI0_PIN08     | DAI0 Pin 8                                | Not Muxed | DAI0_PIN08  |
| DAI0_PIN09     | DAI0 Pin 9                                | Not Muxed | DAI0_PIN09  |
| DAI0_PIN10     | DAI0 Pin 10                               | Not Muxed | DAI0_PIN10  |
| DAI0_PIN19     | DAI0 Pin 19                               | Not Muxed | DAI0_PIN19  |
| DAI0_PIN20     | DAI0 Pin 20                               | Not Muxed | DAI0_PIN20  |
| DAI1_PIN01     | DAI1 Pin 1                                | Not Muxed | DAI1_PIN01  |
| DAI1_PIN02     | DAI1 Pin 2                                | Not Muxed | DAI1_PIN02  |
| DAI1_PIN03     | DAI1 Pin 3                                | Not Muxed | DAI1_PIN03  |
| DAI1_PIN04     | DAI1 Pin 4                                | Not Muxed | DAI1_PIN04  |
| DAI1_PIN05     | DAI1 Pin 5                                | Not Muxed | DAI1_PIN05  |
| DAI1_PIN06     | DAI1 Pin 6                                | Not Muxed | DAI1_PIN06  |
| DAI1_PIN07     | DAI1 Pin 7                                | Not Muxed | DAI1_PIN07  |
| DAI1_PIN08     | DAI1 Pin 8                                | Not Muxed | DAI1_PIN08  |
| DAI1_PIN09     | DAI1 Pin 9                                | Not Muxed | DAI1_PIN09  |
| DAI1_PIN10     | DAI1 Pin 10                               | Not Muxed | DAI1_PIN10  |
| DAI1_PIN19     | DAI1 Pin 19                               | Not Muxed | DAI1_PIN19  |
| DAI1_PIN20     | DAI1 Pin 20                               | Not Muxed | DAI1_PIN20  |
| HADC0_EOC_DOUT | HADC0 End of Conversion / Serial Data Out | A         | PA_11       |
| HADC0_VIN0     | HADC0 Analog Input at channel 0           | Not Muxed | HADC0_VIN0  |
| HADC0_VIN1     | HADC0 Analog Input at channel 1           | Not Muxed | HADC0_VIN1  |
| HADC0_VREFN    | HADC0 Ground Reference for ADC            | Not Muxed | HADC0_VREFN |

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Table 15. ADSP-2156x 120-Lead LQFP Signal Descriptions (Continued)

| Signal Name   | Description                      | Port      | Pin Name    |
|---------------|----------------------------------|-----------|-------------|
| HADC0_VREFP   | HADC0 External Reference for ADC | Not Muxed | HADC0_VREFP |
| JTG_TCK       | JTAG Clock                       | Not Muxed | JTG_TCK     |
| JTG_TDI       | JTAG Serial Data In              | Not Muxed | JTG_TDI     |
| JTG_TDO       | JTAG Serial Data Out             | Not Muxed | JTG_TDO     |
| JTG_TMS       | JTAG Mode Select                 | Not Muxed | JTG_TMS     |
| JTG_TRST      | JTAG Reset                       | Not Muxed | JTG_TRST    |
| MLB0_CLK      | MLB0 Single-Ended Clock          | B         | PB_02       |
| MLB0_DAT      | MLB0 Single-Ended Data           | B         | PB_00       |
| MLB0_SIG      | MLB0 Single-Ended Signal         | B         | PB_01       |
| OSPI0_CLK     | OSPI0 Clock                      | A         | PA_04       |
| OSPI0_D2      | OSPI0 Data 2                     | A         | PA_02       |
| OSPI0_D3      | OSPI0 Data 3                     | A         | PA_03       |
| OSPI0_D4      | OSPI0 Data 4                     | A         | PA_06       |
| OSPI0_D5      | OSPI0 Data 5                     | A         | PA_07       |
| OSPI0_D6      | OSPI0 Data 6                     | A         | PA_08       |
| OSPI0_D7      | OSPI0 Data 7                     | A         | PA_09       |
| OSPI0_MISO/D1 | OSPI0 Master In, Slave Out       | A         | PA_00       |
| OSPI0_MOSI/D0 | OSPI0 Master Out, Slave In       | A         | PA_01       |
| OSPI0_SEL1    | OSPI0 Slave Select Output 1      | A         | PA_05       |
| SPI0_CLK      | SPI0 Clock                       | A         | PA_06       |
| SPI0_MISO     | SPI0 Master In, Slave Out        | A         | PA_07       |
| SPI0_MOSI     | SPI0 Master Out, Slave In        | A         | PA_08       |
| SPI0_SEL1     | SPI0 Slave Select Output 1       | A         | PA_09       |
| SPI0_SEL2     | SPI0 Slave Select Output 2       | B         | PB_05       |
| SPI0_SS       | SPI0 Slave Select Input          | A         | PA_09       |
| SPI1_CLK      | SPI1 Clock                       | A         | PA_10       |
| SPI1_D2       | SPI1 Data 2                      | A         | PA_14       |
| SPI1_D3       | SPI1 Data 3                      | A         | PA_15       |
| SPI1_MISO     | SPI1 Master In, Slave Out        | A         | PA_11       |
| SPI1_MOSI     | SPI1 Master Out, Slave In        | A         | PA_12       |
| SPI1_RDY      | SPI1 Ready                       | B         | PB_04       |
| SPI1_SEL1     | SPI1 Slave Select Output 1       | A         | PA_13       |
| SPI1_SS       | SPI1 Slave Select Input          | A         | PA_13       |
| SPI2_CLK      | SPI2 Clock                       | A         | PA_04       |
| SPI2_D2       | SPI2 Data 2                      | A         | PA_02       |
| SPI2_D3       | SPI2 Data 3                      | A         | PA_03       |
| SPI2_MISO     | SPI2 Master In, Slave Out        | A         | PA_00       |
| SPI2_MOSI     | SPI2 Master Out, Slave In        | A         | PA_01       |
| SPI2_RDY      | SPI2 Ready                       | B         | PB_05       |
| SPI2_SEL1     | SPI2 Slave Select Output 1       | A         | PA_05       |
| SPI2_SEL2     | SPI2 Slave Select Output 2       | B         | PB_03       |
| SPI2_SS       | SPI2 Slave Select Input          | A         | PA_05       |
| SYS_BMODE0    | Boot Mode Control                | Not Muxed | SYS_BMODE0  |
| SYS_BMODE1    | Boot Mode Control                | Not Muxed | SYS_BMODE1  |
| SYS_CLKIN0    | Clock/Crystal Input              | Not Muxed | SYS_CLKIN0  |
| SYS_CLKOUT    | Processor Clock Output           | Not Muxed | SYS_CLKOUT  |
| SYS_FAULT     | Active-Low Fault Output          | Not Muxed | SYS_FAULT   |
| SYS_HWRST     | Processor Hardware Reset Control | Not Muxed | SYS_HWRST   |

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Table 15. ADSP-2156x 120-Lead LQFP Signal Descriptions (Continued)

| Signal Name       | Description                      | Port      | Pin Name          |
|-------------------|----------------------------------|-----------|-------------------|
| <u>SYS_RESOUT</u> | Reset Output                     | Not Muxed | <u>SYS_RESOUT</u> |
| SYS_XTAL0         | Crystal Output                   | Not Muxed | SYS_XTAL0         |
| TM0_ACIO          | TIMER0 Alternate Capture Input 0 | A         | PA_07             |
| TM0_AC11          | TIMER0 Alternate Capture Input 1 | A         | PA_14             |
| TM0_AC13          | TIMER0 Alternate Capture Input 3 | B         | PB_00             |
| TM0_AC14          | TIMER0 Alternate Capture Input 4 | A         | PA_11             |
| TM0_ACLK1         | TIMER0 Alternate Clock 1         | A         | PA_06             |
| TM0_ACLK2         | TIMER0 Alternate Clock 2         | A         | PA_08             |
| TM0_ACLK3         | TIMER0 Alternate Clock 3         | A         | PA_02             |
| TM0_ACLK4         | TIMER0 Alternate Clock 4         | B         | PB_02             |
| TM0_CLK           | TIMER0 Clock                     | B         | PB_01             |
| TM0_TMR0          | TIMER0 Timer 0                   | A         | PA_10             |
| TM0_TMR1          | TIMER0 Timer 1                   | A         | PA_12             |
| TM0_TMR2          | TIMER0 Timer 2                   | A         | PA_13             |
| TM0_TMR3          | TIMER0 Timer 3                   | B         | PB_03             |
| TM0_TMR4          | TIMER0 Timer 4                   | B         | PB_04             |
| TM0_TMR5          | TIMER0 Timer 5                   | B         | PB_05             |
| TWI0_SCL          | TWI0 Serial Clock                | A         | PA_10             |
| TWI0_SDA          | TWI0 Serial Data                 | A         | PA_11             |
| TWI1_SCL          | TWI1 Serial Clock                | B         | PB_00             |
| TWI1_SDA          | TWI1 Serial Data                 | B         | PB_01             |
| TWI2_SCL          | TWI2 Serial Clock                | A         | PA_14             |
| TWI2_SDA          | TWI2 Serial Data                 | A         | PA_15             |
| TWI3_SCL          | TWI3 Serial Clock                | A         | PA_02             |
| TWI3_SDA          | TWI3 Serial Data                 | A         | PA_03             |
| <u>UART0_CTS</u>  | UART0 Clear to Send              | A         | PA_09             |
| <u>UART0_RTS</u>  | UART0 Request to Send            | A         | PA_08             |
| <u>UART0_RX</u>   | UART0 Receive                    | A         | PA_07             |
| <u>UART0_TX</u>   | UART0 Transmit                   | A         | PA_06             |
| <u>UART1_CTS</u>  | UART1 Clear to Send              | B         | PB_01             |
| <u>UART1_RTS</u>  | UART1 Request to Send            | B         | PB_00             |
| <u>UART1_RX</u>   | UART1 Receive                    | A         | PA_14             |
| <u>UART1_TX</u>   | UART1 Transmit                   | A         | PA_15             |

## GPIO MULTIPLEXING FOR 120-LEAD LQFP PACKAGE

Table 16 and Table 17 identify the pin functions that are multiplexed on the general-purpose I/O pins of the 120-lead LQFP package.

**Table 16. Signal Multiplexing for Port A**

| Signal Name | Multiplexed Function 0 | Multiplexed Function 1 | Multiplexed Function 2 | Multiplexed Function Input Tap |
|-------------|------------------------|------------------------|------------------------|--------------------------------|
| PA_00       | SPI2_MISO              | OSPI0_MISO/D1          |                        |                                |
| PA_01       | SPI2_MOSI              | OSPI0_MOSI/D0          |                        |                                |
| PA_02       | SPI2_D2                | OSPI0_D2               | TWI3_SCL               | TM0_ACLK3                      |
| PA_03       | SPI2_D3                | OSPI0_D3               | TWI3_SDA               |                                |
| PA_04       | SPI2_CLK               | OSPI0_CLK              |                        |                                |
| PA_05       | SPI2_SEL1              | OSPI0_SEL1             |                        | SPI2_SS                        |
| PA_06       | SPI0_CLK               | UART0_TX               | OSPI0_D4               | TM0_ACLK1                      |
| PA_07       | SPI0_MISO              | UART0_RX               | OSPI0_D5               | TM0_ACIO                       |
| PA_08       | SPI0_MOSI              | UART0_RTS              | OSPI0_D6               | TM0_ACLK2                      |
| PA_09       | SPI0_SEL1              | UART0_CTS              | OSPI0_D7               | SPI0_SS                        |
| PA_10       | TWI0_SCL               | SPI1_CLK               | TM0_TMR0               |                                |
| PA_11       | TWI0_SDA               | SPI1_MISO              | HADC0_EOC_DOUT         | TM0_ACIO                       |
| PA_12       | C0_FLG0                | SPI1_MOSI              | TM0_TMR1               |                                |
| PA_13       | C0_FLG1                | SPI1_SEL1              | TM0_TMR2               | SPI1_SS                        |
| PA_14       | TWI2_SCL               | SPI1_D2                | UART1_RX               | TM0_ACIO                       |
| PA_15       | TWI2_SDA               | SPI1_D3                | UART1_TX               |                                |

**Table 17. Signal Multiplexing for Port B**

| Signal Name | Multiplexed Function 0 | Multiplexed Function 1 | Multiplexed Function 2 | Multiplexed Function Input Tap |
|-------------|------------------------|------------------------|------------------------|--------------------------------|
| PB_00       | MLB0_DAT               | TWI1_SCL               | UART1_RTS              | TM0_ACIO                       |
| PB_01       | MLB0_SIG               | TWI1_SDA               | UART1_CTS              | TM0_CLK                        |
| PB_02       | MLB0_CLK               | C0_FLG3                |                        | TM0_ACLK4                      |
| PB_03       | TM0_TMR3               | C0_FLG2                | SPI2_SEL2              | CNT0_UD                        |
| PB_04       | TM0_TMR4               | SPI1_RDY               |                        | CNT0_ZM                        |
| PB_05       | TM0_TMR5               | SPI2_RDY               | SPI0_SEL2              | CNT0_DG                        |

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## ADSP-2156x DESIGNER QUICK REFERENCE

Table 18 provides a quick reference summary of pin related information for circuit board design. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The type column identifies the I/O type or supply type of the pin. The abbreviations used in this column are analog (a), supply (s), ground (g) and Input, Output, and InOut.
- The driver type column identifies the driver type used by the corresponding pin. The driver types are defined in the [Output Drive Currents](#) section of this data sheet.
- The internal termination column specifies the termination present after the processor is powered up (both during reset and after reset).
- The reset termination column specifies the termination present when the processor is in the reset state.
- The reset drive column specifies the active drive on the signal when the processor is in the reset state.
- The power domain column specifies the power supply domain in which the signal resides.
- The description and notes column identifies any special requirements or characteristics for a signal. These recommendations apply whether or not the hardware block associated with the signal is featured on the product. If no special requirements are listed, the signal can be left unconnected if it is not used. For multiplexed GPIO pins, this column identifies the functions available on the pin.

Table 18. ADSP-2156x Designer Quick Reference

| Signal Name | Type  | Driver Type | Internal Termination                        | Reset Termination | Reset Drive | Power Domain | Description and Notes                             |
|-------------|-------|-------------|---------------------------------------------|-------------------|-------------|--------------|---------------------------------------------------|
| DAI0_PIN01  | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI0 Pin 1<br>Notes: See note <sup>2</sup>  |
| DAI0_PIN02  | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI0 Pin 2<br>Notes: See note <sup>2</sup>  |
| DAI0_PIN03  | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI0 Pin 3<br>Notes: See note <sup>2</sup>  |
| DAI0_PIN04  | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI0 Pin 4<br>Notes: See note <sup>2</sup>  |
| DAI0_PIN05  | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI0 Pin 5<br>Notes: See note <sup>2</sup>  |
| DAI0_PIN06  | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI0 Pin 6<br>Notes: See note <sup>2</sup>  |
| DAI0_PIN07  | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI0 Pin 7<br>Notes: See note <sup>2</sup>  |
| DAI0_PIN08  | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI0 Pin 8<br>Notes: See note <sup>2</sup>  |
| DAI0_PIN09  | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI0 Pin 9<br>Notes: See note <sup>2</sup>  |
| DAI0_PIN10  | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI0 Pin 10<br>Notes: See note <sup>2</sup> |
| DAI0_PIN11  | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI0 Pin 11<br>Notes: See note <sup>2</sup> |
| DAI0_PIN12  | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI0 Pin 12<br>Notes: See note <sup>2</sup> |
| DAI0_PIN19  | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI0 Pin 19<br>Notes: See note <sup>2</sup> |
| DAI0_PIN20  | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI0 Pin 20<br>Notes: See note <sup>2</sup> |
| DAI1_PIN01  | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI1 Pin 1<br>Notes: See note <sup>2</sup>  |

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**Table 18. ADSP-2156x Designer Quick Reference (Continued)**

| Signal Name | Type   | Driver Type | Internal Termination                        | Reset Termination | Reset Drive | Power Domain | Description and Notes                             |
|-------------|--------|-------------|---------------------------------------------|-------------------|-------------|--------------|---------------------------------------------------|
| DAI1_PIN02  | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI1 Pin 2<br>Notes: See note <sup>2</sup>  |
| DAI1_PIN03  | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI1 Pin 3<br>Notes: See note <sup>2</sup>  |
| DAI1_PIN04  | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI1 Pin 4<br>Notes: See note <sup>2</sup>  |
| DAI1_PIN05  | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI1 Pin 5<br>Notes: See note <sup>2</sup>  |
| DAI1_PIN06  | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI1 Pin 6<br>Notes: See note <sup>2</sup>  |
| DAI1_PIN07  | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI1 Pin 7<br>Notes: See note <sup>2</sup>  |
| DAI1_PIN08  | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI1 Pin 8<br>Notes: See note <sup>2</sup>  |
| DAI1_PIN09  | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI1 Pin 9<br>Notes: See note <sup>2</sup>  |
| DAI1_PIN10  | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI1 Pin 10<br>Notes: See note <sup>2</sup> |
| DAI1_PIN11  | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI1 Pin 11<br>Notes: See note <sup>2</sup> |
| DAI1_PIN12  | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI1 Pin 12<br>Notes: See note <sup>2</sup> |
| DAI1_PIN19  | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI1 Pin 19<br>Notes: See note <sup>2</sup> |
| DAI1_PIN20  | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: DAI1 Pin 20<br>Notes: See note <sup>2</sup> |
| DMC0_A00    | Output | B           | None                                        | None              | L           | VDD_DMC      | Desc: DMC0 Address 0<br>Notes: No notes           |
| DMC0_A01    | Output | B           | None                                        | None              | L           | VDD_DMC      | Desc: DMC0 Address 1<br>Notes: No notes           |
| DMC0_A02    | Output | B           | None                                        | None              | L           | VDD_DMC      | Desc: DMC0 Address 2<br>Notes: No notes           |
| DMC0_A03    | Output | B           | None                                        | None              | L           | VDD_DMC      | Desc: DMC0 Address 3<br>Notes: No notes           |
| DMC0_A04    | Output | B           | None                                        | None              | L           | VDD_DMC      | Desc: DMC0 Address 4<br>Notes: No notes           |
| DMC0_A05    | Output | B           | None                                        | None              | L           | VDD_DMC      | Desc: DMC0 Address 5<br>Notes: No notes           |
| DMC0_A06    | Output | B           | None                                        | None              | L           | VDD_DMC      | Desc: DMC0 Address 6<br>Notes: No notes           |
| DMC0_A07    | Output | B           | None                                        | None              | L           | VDD_DMC      | Desc: DMC0 Address 7<br>Notes: No notes           |
| DMC0_A08    | Output | B           | None                                        | None              | L           | VDD_DMC      | Desc: DMC0 Address 8<br>Notes: No notes           |
| DMC0_A09    | Output | B           | None                                        | None              | L           | VDD_DMC      | Desc: DMC0 Address 9<br>Notes: No notes           |
| DMC0_A10    | Output | B           | None                                        | None              | L           | VDD_DMC      | Desc: DMC0 Address 10<br>Notes: No notes          |

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Table 18. ADSP-2156x Designer Quick Reference (Continued)

| Signal Name                   | Type   | Driver Type | Internal Termination                                    | Reset Termination | Reset Drive | Power Domain | Description and Notes                               |
|-------------------------------|--------|-------------|---------------------------------------------------------|-------------------|-------------|--------------|-----------------------------------------------------|
| DMC0_A11                      | Output | B           | None                                                    | None              | L           | VDD_DMC      | Desc: DMC0 Address 11<br>Notes: No notes            |
| DMC0_A12                      | Output | B           | None                                                    | None              | L           | VDD_DMC      | Desc: DMC0 Address 12<br>Notes: No notes            |
| DMC0_A13                      | Output | B           | None                                                    | None              | L           | VDD_DMC      | Desc: DMC0 Address 13<br>Notes: No notes            |
| DMC0_A14                      | Output | B           | None                                                    | None              | L           | VDD_DMC      | Desc: DMC0 Address 14<br>Notes: No notes            |
| DMC0_A15                      | Output | B           | None                                                    | None              | L           | VDD_DMC      | Desc: DMC0 Address 15<br>Notes: No notes            |
| DMC0_BA0                      | Output | B           | None                                                    | None              | L           | VDD_DMC      | Desc: DMC0 Bank Address Input 0<br>Notes: No notes  |
| DMC0_BA1                      | Output | B           | None                                                    | None              | L           | VDD_DMC      | Desc: DMC0 Bank Address Input 1<br>Notes: No notes  |
| DMC0_BA2                      | Output | B           | None                                                    | None              | L           | VDD_DMC      | Desc: DMC0 Bank Address Input 2<br>Notes: No notes  |
| $\overline{\text{DMC0\_CAS}}$ | Output | B           | None                                                    | None              | L           | VDD_DMC      | Desc: DMC0 column address strobe<br>Notes: No notes |
| DMC0_CK                       | Output | C           | None                                                    | None              | L           | VDD_DMC      | Desc: DMC0 clock<br>Notes: No notes                 |
| $\overline{\text{DMC0\_CK}}$  | Output | C           | None                                                    | None              | H           | VDD_DMC      | Desc: DMC0 clock (complement)<br>Notes: No notes    |
| DMC0_CKE                      | Output | B           | None                                                    | None              | L           | VDD_DMC      | Desc: DMC0 clock enable<br>Notes: No notes          |
| $\overline{\text{DMC0\_CS0}}$ | Output | B           | None                                                    | None              | L           | VDD_DMC      | Desc: DMC0 Chip Select 0<br>Notes: No notes         |
| DMC0_DQ00                     | InOut  | B           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 Data 0<br>Notes: No notes                |
| DMC0_DQ01                     | InOut  | B           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 Data 1<br>Notes: No notes                |
| DMC0_DQ02                     | InOut  | B           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 Data 2<br>Notes: No notes                |
| DMC0_DQ03                     | InOut  | B           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 Data 3<br>Notes: No notes                |
| DMC0_DQ04                     | InOut  | B           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 Data 4<br>Notes: No notes                |
| DMC0_DQ05                     | InOut  | B           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 Data 5<br>Notes: No notes                |
| DMC0_DQ06                     | InOut  | B           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 Data 6<br>Notes: No notes                |

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Table 18. ADSP-2156x Designer Quick Reference (Continued)

| Signal Name                     | Type   | Driver Type | Internal Termination                                    | Reset Termination | Reset Drive | Power Domain | Description and Notes                                                                                      |
|---------------------------------|--------|-------------|---------------------------------------------------------|-------------------|-------------|--------------|------------------------------------------------------------------------------------------------------------|
| DMC0_DQ07                       | InOut  | B           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 Data 7<br>Notes: No notes                                                                       |
| DMC0_DQ08                       | InOut  | B           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 Data 8<br>Notes: No notes                                                                       |
| DMC0_DQ09                       | InOut  | B           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 Data 9<br>Notes: No notes                                                                       |
| DMC0_DQ10                       | InOut  | B           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 Data 10<br>Notes: No notes                                                                      |
| DMC0_DQ11                       | InOut  | B           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 Data 11<br>Notes: No notes                                                                      |
| DMC0_DQ12                       | InOut  | B           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 Data 12<br>Notes: No notes                                                                      |
| DMC0_DQ13                       | InOut  | B           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 Data 13<br>Notes: No notes                                                                      |
| DMC0_DQ14                       | InOut  | B           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 Data 14<br>Notes: No notes                                                                      |
| DMC0_DQ15                       | InOut  | B           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 Data 15<br>Notes: No notes                                                                      |
| DMC0_LDM                        | Output | B           | None                                                    | None              | L           | VDD_DMC      | Desc: DMC0 data mask for lower byte<br>Notes: No notes                                                     |
| DMC0_LDQS                       | InOut  | C           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 data strobe for lower byte<br>Notes: No notes                                                   |
| $\overline{\text{DMC0\_LDQS}}$  | InOut  | C           | Internal logic ensures that input signal does not float | None              | None        | VDD_DMC      | Desc: DMC0 data strobe for lower byte (complement)<br>Notes: No notes                                      |
| DMC0_ODT                        | Output | B           | None                                                    | None              | L           | VDD_DMC      | Desc: DMC0 on-die termination<br>Notes: No notes                                                           |
| $\overline{\text{DMC0\_RAS}}$   | Output | B           | None                                                    | None              | L           | VDD_DMC      | Desc: DMC0 row address strobe<br>Notes: No notes                                                           |
| $\overline{\text{DMC0\_RESET}}$ | Output | B           | None                                                    | None              | L           | VDD_DMC      | Desc: DMC0 reset (DDR3 only)<br>Notes: No notes                                                            |
| DMC0_RZQ                        | a      | B           | None                                                    | None              | None        | VDD_DMC      | Desc: DMC0 external calibration resistor connection<br>Notes: 34 $\Omega$ external pull-down must be added |
| DMC0_UDM                        | Output | B           | None                                                    | None              | L           | VDD_DMC      | Desc: DMC0 data mask for upper byte<br>Notes: No notes                                                     |

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Table 18. ADSP-2156x Designer Quick Reference (Continued)

| Signal Name                    | Type   | Driver Type | Internal Termination                                    | Reset Termination | Reset Drive                                                                                      | Power Domain | Description and Notes                                                                        |
|--------------------------------|--------|-------------|---------------------------------------------------------|-------------------|--------------------------------------------------------------------------------------------------|--------------|----------------------------------------------------------------------------------------------|
| DMC0_UDQS                      | InOut  | C           | Internal logic ensures that input signal does not float | None              | None                                                                                             | VDD_DMC      | Desc: DMC0 data strobe for upper byte<br>Notes: No notes                                     |
| $\overline{\text{DMC0\_UDQS}}$ | InOut  | C           | Internal logic ensures that input signal does not float | None              | None                                                                                             | VDD_DMC      | Desc: DMC0 data strobe for upper byte (complement)<br>Notes: No notes                        |
| DMC0_VREF                      | a      |             | None                                                    | None              | None                                                                                             | VDD_DMC      | Desc: DMC0 voltage reference<br>Notes: No notes                                              |
| $\overline{\text{DMC0\_WE}}$   | Output | B           | None                                                    | None              | L                                                                                                | VDD_DMC      | Desc: DMC0 write enable<br>Notes: No notes                                                   |
| GND                            | g      |             | None                                                    | None              | None                                                                                             |              | Desc: Ground<br>Notes: No notes                                                              |
| HADC0_VIN0                     | a      | NA          | none                                                    | none              | none                                                                                             | VDD_ANA      | Desc: HADC0 Analog Input at channel 0<br>Notes: Connect to GND if not used <sup>3</sup> .    |
| HADC0_VIN1                     | a      | NA          | none                                                    | none              | none                                                                                             | VDD_ANA      | Desc: HADC0 Analog Input at channel 1<br>Notes: Connect to GND if not used <sup>3</sup>      |
| HADC0_VIN2                     | a      | NA          | none                                                    | none              | none                                                                                             | VDD_ANA      | Desc: HADC0 Analog Input at channel 2<br>Notes: Connect to GND if not used <sup>3</sup>      |
| HADC0_VIN3                     | a      | NA          | none                                                    | none              | none                                                                                             | VDD_ANA      | Desc: HADC0 Analog Input at channel 3<br>Notes: Connect to GND if not used <sup>3</sup>      |
| HADC0_VREFN                    | s      | NA          | none                                                    | none              | none                                                                                             | VDD_ANA      | Desc: HADC0 Ground Reference for ADC<br>Notes: Connect to GND if not used <sup>3</sup>       |
| HADC0_VREFP                    | s      | NA          | none                                                    | none              | none                                                                                             | VDD_ANA      | Desc: HADC0 External Reference for ADC<br>Notes: Connect to VDD_REF if HADC/TMU is not used. |
| JTG_TCK                        | Input  |             | Pull-up                                                 | Pull-up           | None                                                                                             | VDD_EXT      | Desc: JTAG clock<br>Notes: See note <sup>2</sup>                                             |
| JTG_TDI                        | Input  |             | Pull-up                                                 | Pull-up           | None                                                                                             | VDD_EXT      | Desc: JTAG serial data in<br>Notes: See note <sup>2</sup>                                    |
| JTG_TDO                        | Output | A           | None                                                    | None              | High-Z when $\overline{\text{JTG\_TRST}}$ is low, not affected by $\overline{\text{SYS\_HWRST}}$ | VDD_EXT      | Desc: JTAG serial data out<br>Notes: No notes                                                |
| JTG_TMS                        | InOut  | A           | Pull-up                                                 | Pull-up           | None                                                                                             | VDD_EXT      | Desc: JTAG mode select<br>Notes: See note <sup>2</sup>                                       |
| $\overline{\text{JTG\_TRST}}$  | Input  |             | Pull-down                                               | Pull-down         | None                                                                                             | VDD_EXT      | Desc: JTAG reset<br>Notes: See note <sup>2</sup>                                             |
| PA_00                          | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup>             | None              | None                                                                                             | VDD_EXT      | Desc: Port A Position 0<br>Notes: See note <sup>2</sup>                                      |
| PA_01                          | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup>             | None              | None                                                                                             | VDD_EXT      | Desc: Port A Position 1<br>Notes: See note <sup>2</sup>                                      |

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Table 18. ADSP-2156x Designer Quick Reference (Continued)

| Signal Name | Type  | Driver Type | Internal Termination                        | Reset Termination | Reset Drive | Power Domain | Description and Notes                                    |
|-------------|-------|-------------|---------------------------------------------|-------------------|-------------|--------------|----------------------------------------------------------|
| PA_02       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port A Position 2<br>Notes: See note <sup>2</sup>  |
| PA_03       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port A Position 3<br>Notes: See note <sup>2</sup>  |
| PA_04       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port A Position 4<br>Notes: See note <sup>2</sup>  |
| PA_05       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port A Position 5<br>Notes: See note <sup>2</sup>  |
| PA_06       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port A Position 6<br>Notes: See note <sup>2</sup>  |
| PA_07       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port A Position 7<br>Notes: See note <sup>2</sup>  |
| PA_08       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port A Position 8<br>Notes: See note <sup>2</sup>  |
| PA_09       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port A Position 9<br>Notes: See note <sup>2</sup>  |
| PA_10       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port A Position 10<br>Notes: See note <sup>2</sup> |
| PA_11       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port A Position 11<br>Notes: See note <sup>2</sup> |
| PA_12       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port A Position 12<br>Notes: See note <sup>2</sup> |
| PA_13       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port A Position 13<br>Notes: See note <sup>2</sup> |
| PA_14       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port A Position 14<br>Notes: See note <sup>2</sup> |
| PA_15       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port A Position 15<br>Notes: See note <sup>2</sup> |
| PB_00       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port B Position 0<br>Notes: See note <sup>2</sup>  |
| PB_01       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port B Position 1<br>Notes: See note <sup>2</sup>  |
| PB_02       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port B Position 2<br>Notes: See note <sup>2</sup>  |
| PB_03       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port B Position 3<br>Notes: See note <sup>2</sup>  |
| PB_04       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port B Position 4<br>Notes: See note <sup>2</sup>  |
| PB_05       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port B Position 5<br>Notes: See note <sup>2</sup>  |
| PB_06       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port B Position 6<br>Notes: See note <sup>2</sup>  |
| PB_07       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port B Position 7<br>Notes: See note <sup>2</sup>  |
| PB_08       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port B Position 8<br>Notes: See note <sup>2</sup>  |
| PB_09       | InOut | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port B Position 9<br>Notes: See note <sup>2</sup>  |

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Table 18. ADSP-2156x Designer Quick Reference (Continued)

| Signal Name                     | Type   | Driver Type | Internal Termination                        | Reset Termination | Reset Drive | Power Domain | Description and Notes                                                                                                   |
|---------------------------------|--------|-------------|---------------------------------------------|-------------------|-------------|--------------|-------------------------------------------------------------------------------------------------------------------------|
| PB_10                           | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port B Position 10<br>Notes: See note <sup>2</sup>                                                                |
| PB_11                           | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port B Position 11<br>Notes: See note <sup>2</sup>                                                                |
| PB_12                           | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port B Position 12<br>Notes: See note <sup>2</sup>                                                                |
| PB_13                           | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port B Position 13<br>Notes: See note <sup>2</sup>                                                                |
| PB_14                           | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port B Position 14<br>Notes: See note <sup>2</sup>                                                                |
| PB_15                           | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port B Position 15<br>Notes: See note <sup>2</sup>                                                                |
| PC_00                           | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port C Position 0<br>Notes: See note <sup>2</sup>                                                                 |
| PC_01                           | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port C Position 1<br>Notes: See note <sup>2</sup>                                                                 |
| PC_02                           | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port C Position 2<br>Notes: See note <sup>2</sup>                                                                 |
| PC_03                           | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port C Position 3<br>Notes: See note <sup>2</sup>                                                                 |
| PC_04                           | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port C Position 4<br>Notes: See note <sup>2</sup>                                                                 |
| PC_05                           | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port C Position 5<br>Notes: See note <sup>2</sup>                                                                 |
| PC_06                           | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port C Position 6<br>Notes: See note <sup>2</sup>                                                                 |
| PC_07                           | InOut  | A           | Programmable pull-up/pull-down <sup>1</sup> | None              | None        | VDD_EXT      | Desc: Port C Position 7 (default is SYS_FAULT)<br>Notes: External pull-down required to keep signal in deasserted state |
| SYS_BMODE0                      | Input  | NA          | None                                        | None              | None        | VDD_EXT      | Desc: Boot Mode Control 0<br>Notes: Cannot be left unconnected                                                          |
| SYS_BMODE1                      | Input  | NA          | None                                        | None              | None        | VDD_EXT      | Desc: Boot Mode Control 1<br>Notes: Cannot be left unconnected                                                          |
| SYS_BMODE2                      | Input  | NA          | None                                        | None              | None        | VDD_EXT      | Desc: Boot Mode Control 2<br>Notes: Cannot be left unconnected                                                          |
| SYS_CLKIN0                      | a      | NA          | None                                        | None              | None        | VDD_REF      | Desc: Clock/crystal input<br>Notes: Cannot be left unconnected                                                          |
| SYS_CLKOUT                      | a      | A           | None                                        | None              | None        | VDD_EXT      | Desc: Processor clock output<br>Notes: No notes                                                                         |
| $\overline{\text{SYS\_FAULT}}$  | InOut  | A           | None                                        | None              | None        | VDD_EXT      | Desc: Active low fault output<br>Notes: External pull-up required to keep signal in deasserted state                    |
| $\overline{\text{SYS\_HWRST}}$  | Input  | NA          | None                                        | None              | None        | VDD_EXT      | Desc: Processor hardware reset control<br>Notes: Cannot be left unconnected                                             |
| $\overline{\text{SYS\_RESOUT}}$ | Output | A           | None                                        | None              | L           | VDD_EXT      | Desc: Reset output<br>Notes: No notes                                                                                   |

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Table 18. ADSP-2156x Designer Quick Reference (Continued)

| Signal Name | Type | Driver Type | Internal Termination | Reset Termination | Reset Drive | Power Domain | Description and Notes                                                                                               |
|-------------|------|-------------|----------------------|-------------------|-------------|--------------|---------------------------------------------------------------------------------------------------------------------|
| SYS_XTALO   | a    | NA          | None                 | None              | None        | VDD_REF      | Desc: Crystal output<br>Notes: Leave unconnected if an oscillator provides SYS_CLKIN0                               |
| VDD_ANA     | s    |             | none                 | none              | none        |              | Desc: Analog VDD<br>Notes: VDD_REF can be used to source the VDD_ANA power supply for HADC and TMU.                 |
| VDD_DMC     | s    |             | None                 | None              | None        |              | Desc: DMC voltage domain<br>Notes: No notes                                                                         |
| VDD_EXT     | s    |             | None                 | None              | None        |              | Desc: External voltage domain<br>Notes: No notes                                                                    |
| VDD_INT     | s    |             | None                 | None              | None        |              | Desc: Internal voltage domain<br>Notes: No notes                                                                    |
| VDD_REF     | s    |             | None                 | None              | None        |              | Desc: External voltage reference<br>Notes: VDD_REF can be used to source the VDD_ANA power supply for HADC and TMU. |

<sup>1</sup> Disable by default.

<sup>2</sup> When present, the internal pull-up/pull-down design holds the internal path from the pins at the expected logic levels. To pull up or pull down the external pads to the expected logic levels, use external resistors.

<sup>3</sup> All HADC0\_VINx pins and the HADC0\_VREFN pin can be connected directly to GND if HADC and TMU are not used.

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## SPECIFICATIONS

Specifications are subject to change without notice. For information about product specifications, contact your Analog Devices, Inc., representative.

### OPERATING CONDITIONS

All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.

| Parameter                               |                                                                                               | Conditions                    | Min                           | Nominal                       | Max                           | Unit |
|-----------------------------------------|-----------------------------------------------------------------------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|------|
| V <sub>DD_INT</sub>                     | Internal (Core) Supply Voltage                                                                | 400 MHz ≤ CCLK ≤ 1 GHz        | 0.95                          | 1.00                          | 1.05                          | V    |
| V <sub>DD_EXT</sub>                     | External (I/O) Supply Voltage                                                                 |                               | 3.13                          | 3.30                          | 3.47                          | V    |
| V <sub>DD_ANA</sub>                     | Analog Power Supply Voltage                                                                   |                               | 1.71                          | 1.80                          | 1.89                          | V    |
| V <sub>DD_DMC</sub> <sup>1</sup>        | DDR3L Controller Supply Voltage                                                               |                               | 1.283                         | 1.350                         | 1.418                         | V    |
|                                         | DDR3 Controller Supply Voltage                                                                |                               | 1.425                         | 1.500                         | 1.575                         | V    |
| V <sub>DD_REF</sub> <sup>2</sup>        | External (I/O) Reference Supply Voltage                                                       |                               | 1.71                          | 1.80                          | 1.89                          | V    |
| V <sub>DDR_VREF</sub> <sup>3</sup>      | DDR3 Reference Voltage                                                                        |                               | 0.49 × V <sub>DD_DMC</sub>    | 0.50 × V <sub>DD_DMC</sub>    | 0.51 × V <sub>DD_DMC</sub>    | V    |
| V <sub>DELTA_EXT_REF</sub> <sup>4</sup> | (V <sub>DD_EXT</sub> – V <sub>DD_REF</sub> ) and (V <sub>DD_EXT</sub> – V <sub>DD_ANA</sub> ) |                               | –1.89                         |                               | +1.89                         | V    |
| V <sub>HADC_REF</sub> <sup>5</sup>      | HADC Reference Voltage                                                                        |                               | 1.71                          | 1.80                          | V <sub>DD_ANA</sub>           | V    |
| V <sub>HADC0_VINx</sub>                 | HADC Input Voltage                                                                            |                               | 0                             |                               | V <sub>HADC_REF</sub> + 0.09  | V    |
| V <sub>IH</sub> <sup>6</sup>            | High Level Input Voltage                                                                      |                               | V <sub>DD_EXT</sub> = 3.47 V  | 2.0                           |                               | V    |
| V <sub>IHCLKIN</sub> <sup>2</sup>       | High Level Clock Input Voltage                                                                |                               | V <sub>DD_REF</sub> = 1.89 V  | 0.65 × V <sub>DD_REF</sub>    | V <sub>DD_REF</sub>           | V    |
| V <sub>IL</sub> <sup>6</sup>            | Low Level Input Voltage                                                                       |                               | V <sub>DD_EXT</sub> = 3.13 V  |                               | 0.8                           | V    |
| V <sub>ILCLKIN</sub> <sup>2</sup>       | Low Level Clock Input Voltage                                                                 |                               | V <sub>DD_REF</sub> = 1.71 V  | –0.30                         | +0.35 × V <sub>DD_REF</sub>   | V    |
| V <sub>IL_DDR3L</sub> <sup>7</sup>      | Low Level Input Voltage                                                                       |                               | V <sub>DD_DMC</sub> = 1.283 V |                               | V <sub>DDR_VREF</sub> – 0.175 | V    |
| V <sub>IL_DDR3</sub> <sup>7</sup>       | Low Level Input Voltage                                                                       | V <sub>DD_DMC</sub> = 1.425 V |                               | V <sub>DDR_VREF</sub> – 0.175 | V                             |      |
| V <sub>IH_DDR3L</sub> <sup>7</sup>      | High Level Input Voltage                                                                      | V <sub>DD_DMC</sub> = 1.418 V | V <sub>DDR_VREF</sub> + 0.175 |                               | V                             |      |
| V <sub>IH_DDR3</sub> <sup>7</sup>       | High Level Input Voltage                                                                      | V <sub>DD_DMC</sub> = 1.575 V | V <sub>DDR_VREF</sub> + 0.175 |                               | V                             |      |
| CONSUMER GRADE                          |                                                                                               |                               |                               |                               |                               |      |
| T <sub>J</sub>                          | Junction Temperature<br>400-Ball CSP_BGA                                                      |                               | 0                             |                               | 110                           | °C   |
| T <sub>J</sub>                          | Junction Temperature<br>120-Lead LQFP_EP                                                      |                               | 0                             |                               | 110                           | °C   |
| INDUSTRIAL GRADE                        |                                                                                               |                               |                               |                               |                               |      |
| T <sub>J</sub>                          | Junction Temperature<br>400-Ball CSP_BGA                                                      |                               | –40                           |                               | +125                          | °C   |
| T <sub>J</sub>                          | Junction Temperature<br>120-Lead LQFP_EP                                                      |                               | –40                           |                               | +125                          | °C   |
| AUTOMOTIVE GRADE <sup>8</sup>           |                                                                                               |                               |                               |                               |                               |      |
| T <sub>J</sub>                          | Junction Temperature<br>400-Ball CSP_BGA                                                      |                               | –40                           |                               | +125                          | °C   |
| T <sub>J</sub>                          | Junction Temperature<br>120-Lead LQFP_EP                                                      |                               | –40                           |                               | +125                          | °C   |

<sup>1</sup> Applies to DDR3L/DDR3 signals.

<sup>2</sup> Applies to SYS\_CLKIN0 pin.

<sup>3</sup> Applies to DMC0\_VREF pins.

<sup>4</sup> See Figure 11.

<sup>5</sup> V<sub>HADC\_VREF</sub> must always be less than V<sub>DD\_ANA</sub>.

<sup>6</sup> Parameter value applies to all input and bidirectional pins except the DMC pins.

<sup>7</sup> This parameter applies to all DMC0 pins.

<sup>8</sup> Automotive application use profile only. Not supported for nonautomotive use. Contact Analog Devices for more information.

## Clock Related Operating Conditions

Table 19 describes the core clock, system clock, and peripheral clock timing requirements. The data presented in the table applies to all speed grades except where noted.

**Table 19. Clock Operating Conditions**

| Parameter                                                                                    | Conditions                                                                                                                                             | Min | Typ | Max   | Unit |
|----------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-------|------|
| f <sub>CCLK</sub> Core Clock (CCLK) Frequency                                                | f <sub>CCLK</sub> = 2 × f <sub>SYSCLK</sub>                                                                                                            | 400 |     | 1000  | MHz  |
| f <sub>SYSCLK</sub> SYSCLK Frequency <sup>1</sup>                                            |                                                                                                                                                        | 200 |     | 500   | MHz  |
| f <sub>SCLK0</sub> SCLK0 Frequency                                                           | f <sub>SYSCLK</sub> = N × f <sub>SCLK0</sub><br>where N = 2 or 4 or 6                                                                                  | 30  |     | 125   | MHz  |
| f <sub>SCLK1</sub> SCLK1 Frequency                                                           | f <sub>SYSCLK</sub> ≥ f <sub>SCLK1</sub>                                                                                                               |     |     | 250   | MHz  |
| f <sub>DCLK</sub> DDR3 Clock (DCLK) Frequency <sup>2</sup>                                   | All combinations are supported except for:<br>[f <sub>CCLK</sub> > 800 MHz and T <sub>j</sub> < 0°C and<br>f <sub>CCLK</sub> :f <sub>DCLK</sub> = 2:1] | 300 |     | 667   | MHz  |
| f <sub>OCLK</sub> Output Clock (OCLK) Frequency <sup>3</sup>                                 |                                                                                                                                                        |     |     | 125   | MHz  |
| f <sub>SYS_CLKOUTJ</sub> SYS_CLKOUT Period Jitter <sup>4, 5</sup>                            |                                                                                                                                                        |     | ±1  |       | %    |
| f <sub>LCLKTPROG</sub> Programmed Link Port Transmit Clock                                   |                                                                                                                                                        |     |     | 125   | MHz  |
| f <sub>LCLKREXT</sub> External Link Port Receive Clock <sup>6, 7</sup>                       | f <sub>LCLKREXT</sub> ≤ f <sub>OCLK_0</sub>                                                                                                            |     |     | 125   | MHz  |
| f <sub>SPTCLKPROG</sub> Programmed SPT Clock When Transmitting Data and Frame Sync           |                                                                                                                                                        |     |     | 62.5  | MHz  |
| f <sub>SPTCLKPROG</sub> Programmed SPT Clock When Receiving Data or Frame Sync               |                                                                                                                                                        |     |     | 31.25 | MHz  |
| f <sub>SPTCLKEXT</sub> External SPT Clock When Receiving Data and Frame Sync <sup>6, 7</sup> | f <sub>SPTCLKEXT</sub> ≤ f <sub>SCLK0</sub>                                                                                                            |     |     | 62.5  | MHz  |
| f <sub>SPTCLKEXT</sub> External SPT Clock Transmitting Data or Frame Sync <sup>6, 7</sup>    | f <sub>SPTCLKEXT</sub> ≤ f <sub>SCLK0</sub>                                                                                                            |     |     | 31.25 | MHz  |
| f <sub>SPICLKPROG</sub> Programmed SPI Clock When Transmitting Data                          | f <sub>SPICLK</sub> :f <sub>SCLK0</sub> ratio = 1:1                                                                                                    |     |     | 75    | MHz  |
| f <sub>SPICLKPROG</sub> Programmed SPI Clock When Receiving Data                             | f <sub>SPICLK</sub> :f <sub>SCLK0</sub> ratio = 1:1                                                                                                    |     |     | 75    | MHz  |
| f <sub>SPICLKPROG</sub> Programmed SPI Clock When Transmitting Data                          | f <sub>SPICLK</sub> :f <sub>SCLK0</sub> ratio = 1:2                                                                                                    |     |     | 62.5  | MHz  |
| f <sub>SPICLKPROG</sub> Programmed SPI Clock When Receiving Data                             | f <sub>SPICLK</sub> :f <sub>SCLK0</sub> ratio = 1:2                                                                                                    |     |     | 62.5  | MHz  |
| f <sub>SPICLKEXT</sub> External SPI Clock When Receiving Data <sup>6, 7</sup>                | f <sub>SPICLKEXT</sub> ≤ f <sub>CDU_CLK00</sub>                                                                                                        |     |     | 62.5  | MHz  |
| f <sub>SPICLKEXT</sub> External SPI Clock When Transmitting Data <sup>6, 7</sup>             | f <sub>SPICLKEXT</sub> ≤ f <sub>CDU_CLK00</sub>                                                                                                        |     |     | 45    | MHz  |
| f <sub>TMRLCKEXT</sub> External Timer Clock (TMx_CLK)                                        | f <sub>TMRLCKEXT</sub> ≤ f <sub>SCLK0</sub> / 4                                                                                                        |     |     | 31.25 | MHz  |

<sup>1</sup>When using MLB, there is a requirement that the f<sub>SYSCLK</sub> value must be a minimum of 100 MHz for 3-pin mode and for all supported speeds.

<sup>2</sup>To ensure proper operation of the DDR3/3L, all the DDR3/3L guidelines must be strictly followed. See [ADSP-2156x Board Design Guidelines for Dynamic Memory Controller \(EE-418\)](#).

<sup>3</sup>f<sub>OCLK</sub> must not exceed f<sub>SCLK0</sub> when selected as SYS\_CLKOUT.

<sup>4</sup>SYS\_CLKOUT jitter is dependent on the application system design including pin switching activity, board layout, and the jitter characteristics of the SYS\_CLKIN source. Due to the dependency on these factors, the measured jitter may be higher or lower than this typical specification for each end application.

<sup>5</sup>The value in the Typ field is the percentage of the SYS\_CLKOUT period.

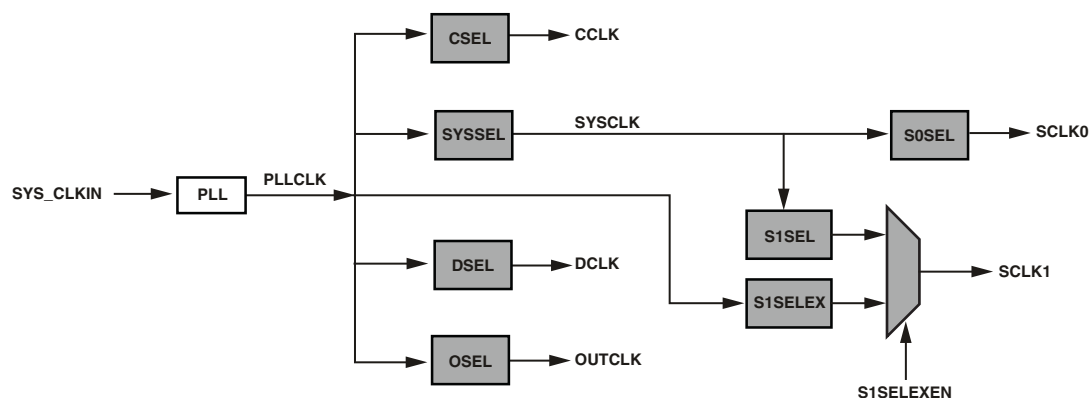
<sup>6</sup>The maximum achievable frequency for any peripheral in external clock mode is dependent on being able to meet the setup and hold times in the ac timing specifications section for that peripheral.

<sup>7</sup>The peripheral external clock frequency must also be less than or equal to the frequency that clocks the peripheral.

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Table 20. Phase-Locked Loop (PLL) Operating Conditions

| Parameter                               | Min  | Max  | Unit |
|-----------------------------------------|------|------|------|
| $f_{\text{PLLCLK}}$ PLL Clock Frequency | 1.20 | 2.00 | GHz  |



REFER TO THE ADSP-2156x SHARC+ PROCESSOR HARDWARE REFERENCE  
FOR INFORMATION ABOUT ALLOWED DIVIDER VALUES AND PROGRAMMING MODELS.

Figure 9. Clock Relationships and Divider Values

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## ELECTRICAL CHARACTERISTICS

All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.

| Parameter                          | Conditions                                                                                                                                                                                                                                                                                                                  | Min   | Typ  | Max  | Unit |
|------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------|------|------|
| V <sub>OH</sub>                    | High Level Output Voltage<br>V <sub>DD_EXT</sub> = minimum,<br>(I <sub>OH</sub> = -2.0 mA, DS1) <sup>1</sup> , (I <sub>OH</sub> = -4.0 mA, DS2) <sup>2</sup>                                                                                                                                                                | 2.4   |      |      | V    |
| V <sub>OL</sub>                    | Low Level Output Voltage<br>V <sub>DD_EXT</sub> = minimum,<br>(I <sub>OL</sub> = 2.0 mA, DS1) <sup>1</sup> , (I <sub>OL</sub> = 4.0 mA, DS2) <sup>2</sup>                                                                                                                                                                   |       |      | 0.4  | V    |
| V <sub>OH_XTAL</sub> <sup>3</sup>  | High Level Output Voltage<br>V <sub>DD_REF</sub> = minimum, I <sub>OH</sub> = -1.0 mA                                                                                                                                                                                                                                       | 1.26  |      |      | V    |
| V <sub>OL_XTAL</sub> <sup>3</sup>  | Low Level Output Voltage<br>V <sub>DD_REF</sub> = minimum, I <sub>OL</sub> = 1.0 mA                                                                                                                                                                                                                                         |       |      | 0.45 | V    |
| V <sub>OH_DDR3L</sub> <sup>4</sup> | High Level Output Voltage for<br>DDR3L Drive Strength = 100 Ω<br>V <sub>DD_DDR</sub> = minimum, I <sub>OH</sub> = -1.0 mA                                                                                                                                                                                                   | 0.963 |      |      | V    |
| V <sub>OL_DDR3L</sub> <sup>4</sup> | Low Level Output Voltage for<br>DDR3L Drive Strength = 100 Ω<br>V <sub>DD_DDR</sub> = minimum, I <sub>OL</sub> = 1.0 mA                                                                                                                                                                                                     |       |      | 0.32 | V    |
| V <sub>OH_DDR3</sub> <sup>5</sup>  | High Level Output Voltage for<br>DDR3 Drive Strength = 100 Ω<br>V <sub>DD_DDR</sub> = minimum, I <sub>OH</sub> = -1.0 mA                                                                                                                                                                                                    | 1.105 |      |      | V    |
| V <sub>OL_DDR3</sub> <sup>5</sup>  | Low Level Output Voltage for<br>DDR3 Drive Strength = 100 Ω<br>V <sub>DD_DDR</sub> = minimum, I <sub>OL</sub> = 1.0 mA                                                                                                                                                                                                      |       |      | 0.32 | V    |
| I <sub>IH</sub> <sup>6</sup>       | High Level Input Current<br>V <sub>DD_EXT</sub> = maximum, V <sub>IN</sub> = V <sub>DD_EXT</sub> maximum                                                                                                                                                                                                                    |       |      | 10   | μA   |
| I <sub>IL</sub> <sup>6</sup>       | Low Level Input Current<br>V <sub>DD_EXT</sub> = maximum, V <sub>IN</sub> = 0 V                                                                                                                                                                                                                                             |       |      | 10   | μA   |
| I <sub>IL_PU</sub> <sup>7</sup>    | Low Level Input Current<br>Pull-Up<br>V <sub>DD_EXT</sub> = maximum, V <sub>IN</sub> = 0 V                                                                                                                                                                                                                                  |       |      | 200  | μA   |
| I <sub>IH_PD</sub> <sup>8</sup>    | High Level Input Current<br>Pull-Down<br>V <sub>DD_EXT</sub> = maximum, V <sub>IN</sub> = V <sub>DD_EXT</sub> maximum                                                                                                                                                                                                       |       |      | 200  | μA   |
| I <sub>OZH</sub> <sup>9</sup>      | Three-State Leakage Current<br>V <sub>DD_EXT</sub> /V <sub>DD_DDR</sub> = maximum,<br>V <sub>IN</sub> = V <sub>DD_EXT</sub> /V <sub>DD_DDR</sub> maximum                                                                                                                                                                    |       |      | 10   | μA   |
| I <sub>OZL</sub> <sup>9</sup>      | Three-State Leakage Current<br>V <sub>DD_EXT</sub> /V <sub>DD_DDR</sub> = maximum, V <sub>IN</sub> = 0 V                                                                                                                                                                                                                    |       |      | 10   | μA   |
| C <sub>IN</sub> <sup>10</sup>      | Input Capacitance<br>T <sub>J</sub> = 25°C                                                                                                                                                                                                                                                                                  |       |      | 5    | pF   |
| I <sub>DD_IDLE</sub>               | V <sub>DD_INT</sub> Current in Idle<br>f <sub>CCLK</sub> = 1000 MHz<br>ASF <sub>SHARC</sub> = 0.35<br>f <sub>SYSCLK</sub> = 500 MHz<br>f <sub>SCLK0</sub> = 125 MHz<br>f <sub>SCLK1</sub> = 250 MHz<br>(Other clocks are disabled)<br>No peripheral or DMA activity<br>T <sub>J</sub> = 25°C<br>V <sub>DD_INT</sub> = 1.0 V |       | 654  |      | mA   |
| I <sub>DD_TYP</sub>                | V <sub>DD_INT</sub> Current<br>f <sub>CCLK</sub> = 1000 MHz<br>ASF <sub>SHARC</sub> = 1.0<br>f <sub>SYSCLK</sub> = 500 MHz<br>f <sub>SCLK0</sub> = 125 MHz<br>f <sub>SCLK1</sub> = 250 MHz<br>(Other clocks are disabled)<br>DMA data rate = 456 MB/s<br>T <sub>J</sub> = 25°C<br>V <sub>DD_INT</sub> = 1.0 V               |       | 1157 |      | mA   |

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| Parameter            |                                     | Conditions                                                                                                                                                                                                                                                                           | Min | Typ | Max | Unit |
|----------------------|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| I <sub>DD_IDLE</sub> | V <sub>DD_INT</sub> Current in Idle | f <sub>CCLK</sub> = 800 MHz<br>ASF <sub>SHARC</sub> = 0.35<br>f <sub>SYCLK</sub> = 400 MHz<br>f <sub>SCLK0</sub> = 100 MHz<br>f <sub>SCLK1</sub> = 228.6 MHz<br>(Other clocks are disabled)<br>No peripheral or DMA activity<br>T <sub>J</sub> = 25°C<br>V <sub>DD_INT</sub> = 1.0 V |     | 535 |     | mA   |
| I <sub>DD_TYP</sub>  | V <sub>DD_INT</sub> Current         | f <sub>CCLK</sub> = 800 MHz<br>ASF <sub>SHARC</sub> = 1.0<br>f <sub>SYCLK</sub> = 400 MHz<br>f <sub>SCLK0</sub> = 100 MHz<br>f <sub>SCLK1</sub> = 228.6 MHz<br>(Other clocks are disabled)<br>DMA data rate = 456 MB/s<br>T <sub>J</sub> = 25°C<br>V <sub>DD_INT</sub> = 1.0 V       |     | 946 |     | mA   |
| I <sub>DD_IDLE</sub> | V <sub>DD_INT</sub> Current in Idle | f <sub>CCLK</sub> = 600 MHz<br>ASF <sub>SHARC</sub> = 0.35<br>f <sub>SYCLK</sub> = 300 MHz<br>f <sub>SCLK0</sub> = 75 MHz<br>f <sub>SCLK1</sub> = 240 MHz<br>(Other clocks are disabled)<br>No peripheral or DMA activity<br>T <sub>J</sub> = 25°C<br>V <sub>DD_INT</sub> = 1.0 V    |     | 417 |     | mA   |
| I <sub>DD_TYP</sub>  | V <sub>DD_INT</sub> Current         | f <sub>CCLK</sub> = 600 MHz<br>ASF <sub>SHARC</sub> = 1.0<br>f <sub>SYCLK</sub> = 300 MHz<br>f <sub>SCLK0</sub> = 75 MHz<br>f <sub>SCLK1</sub> = 240 MHz<br>(Other clocks are disabled)<br>DMA data rate = 456 MB/s<br>T <sub>J</sub> = 25°C<br>V <sub>DD_INT</sub> = 1.0 V          |     | 735 |     | mA   |

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| Parameter                                    | Conditions                                                                                                                                                                                                                               | Min | Typ | Max                                                                                                 | Unit |
|----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----------------------------------------------------------------------------------------------------|------|
| $I_{DD\_IDLE}$ $V_{DD\_INT}$ Current in Idle | $f_{CCLK} = 400$ MHz<br>$ASF_{SHARC} = 0.35$<br>$f_{SYSCLK} = 200$ MHz<br>$f_{SCLK0} = 100$ MHz<br>$f_{SCLK1} = 250$ MHz<br>(Other clocks are disabled)<br>No peripheral or DMA activity<br>$T_J = 25^{\circ}C$<br>$V_{DD\_INT} = 1.0$ V |     | 311 |                                                                                                     | mA   |
| $I_{DD\_TYP}$ $V_{DD\_INT}$ Current          | $f_{CCLK} = 400$ MHz<br>$ASF_{SHARC} = 1.0$<br>$f_{SYSCLK} = 200$ MHz<br>$f_{SCLK0} = 100$ MHz<br>$f_{SCLK1} = 250$ MHz<br>(Other clocks are disabled)<br>DMA data rate = 456 MB/s<br>$T_J = 25^{\circ}C$<br>$V_{DD\_INT} = 1.0$ V       |     | 536 |                                                                                                     | mA   |
| $I_{DD\_INT}^{11}$ $V_{DD\_INT}$ Current     | $f_{CCLK} > 0$ MHz<br>$f_{SCLK0/1} \geq 0$ MHz                                                                                                                                                                                           |     |     | $I_{DD\_INT\_TOT}$<br>See equation in the <a href="#">Total Internal Power Dissipation</a> section. | mA   |

<sup>1</sup> Applies to all output and bidirectional pins operating at less than or equal to 62.5 MHz, except DMC and SYS\_XTAL0.

<sup>2</sup> Applies to all output and bidirectional pins operating above 62.5 MHz and less than or equal to 125 MHz, except DMC.

<sup>3</sup> Applies to SYS\_XTAL0 pin.

<sup>4</sup> Applies to all DMC output and bidirectional signals in DDR3L mode.

<sup>5</sup> Applies to all DMC output and bidirectional signals in DDR3 mode.

<sup>6</sup> Applies to input pins: SYS\_BMODE2-0, SYS\_CLKIN, and  $\overline{SYS\_HWRST}$ .

<sup>7</sup> Applies to input pins with internal pull-ups: JTG\_TDI, JTG\_TMS, and JTG\_TCK.

<sup>8</sup> Applies to JTAG\_TRST signal.

<sup>9</sup> Applies to signals: PA15 to PA0, PB15 to PB0, PC7 to PC0, DAI0\_PINx, DAI1\_PINx, DMC0\_DQx, DMC0\_LDQS, DMC0\_UDQS,  $\overline{DMC0\_LDQS}$ ,  $\overline{DMC0\_UDQS}$ , SYS\_FAULT, and JTG\_TDO.

<sup>10</sup> Applies to all signal pins.

<sup>11</sup> See [Estimating Power for ADSP-2156x SHARC+ Processors \(EE-414\)](#) for further information.

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## Total Internal Power Dissipation

Total power dissipation has two components:

- Static, including leakage current
- Dynamic, due to transistor switching characteristics for each clock domain

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. The following equation describes the internal current consumption.

$$I_{DD\_INT\_TOT} = I_{DD\_INT\_STATIC} + I_{DD\_INT\_CCLK\_SHARC\_DYN} + I_{DD\_INT\_DCLK\_DYN} + I_{DD\_INT\_SYSCLK\_DYN} + I_{DD\_INT\_SCLK0\_DYN} + I_{DD\_INT\_SCLK1\_DYN} + I_{DD\_INT\_OCLK\_DYN} + I_{DD\_INT\_ACCL\_DYN} + I_{DD\_INT\_DMA\_DR\_DYN}$$

where  $I_{DD\_INT\_STATIC}$  is the sole contributor to the static power dissipation component and is specified as a function of voltage ( $V_{DD\_INT}$ ) and junction temperature ( $T_J$ ) in Table 21.

**Table 21. Static Current— $I_{DD\_INT\_STATIC}$  (mA)**

| $T_J$ (°C) | Voltage ( $V_{DD\_INT}$ ) |        |        |
|------------|---------------------------|--------|--------|
|            | 0.95 V                    | 1.00 V | 1.05 V |
| –45        | 12                        | 15     | 18     |
| –40        | 13                        | 15     | 19     |
| –20        | 17                        | 21     | 27     |
| –10        | 21                        | 26     | 32     |
| 0          | 26                        | 32     | 39     |
| +10        | 33                        | 40     | 49     |
| +25        | 48                        | 58     | 70     |
| +40        | 71                        | 84     | 102    |
| +55        | 105                       | 124    | 148    |
| +70        | 157                       | 184    | 217    |
| +85        | 235                       | 272    | 318    |
| +100       | 347                       | 401    | 465    |
| +105       | 397                       | 457    | 530    |
| +115       | 515                       | 591    | 683    |
| +125       | 665                       | 762    | 880    |

The other eight addends in the  $I_{DD\_INT\_TOT}$  equation comprise the dynamic power dissipation component and fall into four broad categories: application dependent currents, clock currents, currents from high speed peripheral operation, and data transmission currents.

## Application Dependent Current

The application dependent currents include the dynamic current in the core clock domain of the SHARC+ core, as well as the dynamic current in the accelerator block.

Dynamic current consumed by the core is subject to an activity scaling factor (ASF) that represents application code running on the processor core (see Table 22). The ASF is combined with the CCLK frequency and  $V_{DD\_INT}$  dependent dynamic current data in Table 23 to calculate this portion of the total dynamic power dissipation component.

$$I_{DD\_INT\_CCLK\_SHARC\_DYN} = \text{Table 23} \times ASF_{SHARC}$$

**Table 22. Activity Scaling Factors for the SHARC+® Core ( $ASF_{SHARC}$ )**

| $I_{DD\_INT}$ Power Vector | ASF  |
|----------------------------|------|
| $I_{DD\_LS}$               | 0.21 |
| $I_{DD\_IDLE}$             | 0.35 |
| $I_{DD\_NOP}$              | 0.68 |
| $I_{DD\_TYP\_3070}$        | 0.81 |
| $I_{DD\_TYP\_5050}$        | 0.92 |
| $I_{DD\_TYP\_7030}$        | 1.00 |
| $I_{DD\_PEAK\_100}$        | 1.09 |

**Table 23. Dynamic Current for SHARC+® Core (mA, with  $ASF = 1.00$ )**

| $f_{CCLK}$ (MHz) | Voltage ( $V_{DD\_INT}$ ) |        |        |
|------------------|---------------------------|--------|--------|
|                  | 0.95 V                    | 1.00 V | 1.05 V |
| 400              | 271                       | 285    | 299    |
| 450              | 305                       | 321    | 337    |
| 500              | 339                       | 357    | 374    |
| 550              | 373                       | 392    | 412    |
| 600              | 406                       | 428    | 449    |
| 650              | 440                       | 463    | 487    |
| 700              | 474                       | 499    | 524    |
| 750              | 508                       | 535    | 561    |
| 800              | 542                       | 570    | 599    |
| 850              | 576                       | 606    | 636    |
| 900              | 610                       | 642    | 674    |
| 950              | 643                       | 677    | 711    |
| 1000             | 677                       | 713    | 749    |

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## Clock Current

The dynamic clock currents provide the total power dissipated by all transistors switching in the clock paths. The power dissipated by each clock domain is dependent on voltage ( $V_{DD\_INT}$ ), operating frequency, and a unique scaling factor.

$$I_{DD\_INT\_SYSCLK\_DYN} \text{ (mA)} = 0.626 \times f_{SYSCLK} \text{ (MHz)} \times V_{DD\_INT} \text{ (V)}$$

$$I_{DD\_INT\_SCLK0\_DYN} \text{ (mA)} = 0.23 \times f_{SCLK0} \text{ (MHz)} \times V_{DD\_INT} \text{ (V)}$$

$$I_{DD\_INT\_SCLK1\_DYN} \text{ (mA)} = 0.018 \times f_{SCLK1} \text{ (MHz)} \times V_{DD\_INT} \text{ (V)}$$

$$I_{DD\_INT\_DCLK\_DYN} \text{ (mA)} = 0.125 \times f_{DCLK} \text{ (MHz)} \times V_{DD\_INT} \text{ (V)}$$

$$I_{DD\_INT\_OCLK\_DYN} \text{ (mA)} = 0.048 \times f_{OCLK} \text{ (MHz)} \times V_{DD\_INT} \text{ (V)}$$

## Data Transmission Current

The data transmission current represents the power dissipated when moving data throughout the system via DMA. This current is proportional to the data rate. Refer to the power calculator available with [Estimating Power for ADSP-2156x SHARC+ Processors \(EE-414\)](#) to estimate  $I_{DD\_INT\_DMA\_DR\_DYN}$  based on the bandwidth of the data transfer.

## HADC

### HADC Electrical Characteristics

Table 24. HADC Electrical Characteristics

| Parameter                 | Conditions                                                                            | Typ | Unit    |
|---------------------------|---------------------------------------------------------------------------------------|-----|---------|
| $I_{DD\_HADC\_IDLE}$      | Current consumption on $V_{DD\_HADC}$<br>HADC is powered on, but not converting       | 2.0 | mA      |
| $I_{DD\_HADC\_ACTIVE}$    | Current consumption on $V_{DD\_HADC}$ during a conversion                             | 2.5 | mA      |
| $I_{DD\_HADC\_POWERDOWN}$ | Current consumption on $V_{DD\_HADC}$<br>Analog circuitry of the HADC is powered down | 40  | $\mu$ A |

## HADC DC Accuracy

Table 25. HADC DC Accuracy<sup>1</sup>

| Parameter                       | Typ     | Unit <sup>2</sup> |
|---------------------------------|---------|-------------------|
| Resolution                      | 10      | Bits              |
| No Missing Codes (NMC)          | 10      | Bits              |
| Integral Nonlinearity (INL)     | $\pm 2$ | LSB               |
| Differential Nonlinearity (DNL) | $\pm 1$ | LSB               |
| Offset Error                    | $\pm 5$ | LSB               |
| Offset Error Matching           | $\pm 5$ | LSB               |
| Gain Error                      | $\pm 3$ | LSB               |
| Gain Error Matching             | $\pm 3$ | LSB               |

<sup>1</sup> See the [Operating Conditions](#) section for the HADC0\_VINx specification.

<sup>2</sup> LSB = HADC0\_VREFP  $\div$  1024.

## HADC Timing Specifications

Table 26. HADC Timing Specifications

| Parameter                    | Typ                    | Max | Unit    |
|------------------------------|------------------------|-----|---------|
| Conversion Time <sup>1</sup> | $20 \times T_{SAMPLE}$ |     | $\mu$ s |
| Throughput Range             |                        | 1   | MSPS    |
| $T_{WAKEUP}$                 |                        | 100 | $\mu$ s |

<sup>1</sup> Refer to the [ADSP-21562/3/5/6/7/9 SHARC+ Processor Hardware Reference](#) for additional information about  $T_{SAMPLE}$ .

## TMU

### TMU Characteristics

Table 27. TMU Characteristics

| Parameter  | Typ     | Unit         |
|------------|---------|--------------|
| Resolution | 1       | $^{\circ}$ C |
| Accuracy   | $\pm 6$ | $^{\circ}$ C |

Table 28. TMU Gain and Offset

| Junction Temperature Range         | TMU_GAIN                     | TMU_OFFSET |
|------------------------------------|------------------------------|------------|
| $-40^{\circ}$ C to $+40^{\circ}$ C | Contact Analog Devices, Inc. |            |
| $40^{\circ}$ C to $85^{\circ}$ C   | Contact Analog Devices, Inc. |            |
| $85^{\circ}$ C to $125^{\circ}$ C  | Contact Analog Devices, Inc. |            |

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## ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 29 may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 29. Absolute Maximum Ratings

| Parameter                                                                                     | Rating                           |
|-----------------------------------------------------------------------------------------------|----------------------------------|
| Internal (Core) Supply Voltage ( $V_{DD\_INT}$ )                                              | -0.3 V to +1.05 V                |
| External (I/O) Supply Voltage ( $V_{DD\_EXT}$ )                                               | -0.3 V to +3.47 V                |
| External (I/O) Reference Supply Voltage ( $V_{DD\_REF}$ )                                     | -0.3 V to +1.89 V                |
| ( $V_{DD\_EXT} - V_{DD\_REF}$ ) and ( $V_{DD\_EXT} - V_{DD\_ANA}$ ) ( $V_{DELTA\_EXT\_REF}$ ) | -1.89 V to +1.89 V               |
| DDR3 Controller Supply Voltage ( $V_{DD\_DMC}$ )                                              | -0.3 V to +1.60 V                |
| Analog Supply Voltage ( $V_{DD\_ANA}$ )                                                       | -0.3 V to +1.89 V                |
| HADC Reference Voltage ( $V_{HADC\_REF}$ )                                                    | -0.3 V to +1.89 V                |
| DDR3 Input Voltage <sup>1</sup>                                                               | -0.3 V to +1.60 V                |
| Digital Input Voltage <sup>1, 2</sup>                                                         | -0.3 V to +3.47 V                |
| TWI Input Voltage <sup>1, 3</sup>                                                             | -0.3 V to +3.47 V                |
| Output Voltage Swing                                                                          | -0.3 V to $V_{DD\_EXT} + 0.5$ V  |
| Analog Input Voltage <sup>4</sup>                                                             | -0.2 V to $V_{DD\_ANA} + 0.09$ V |
| $I_{OH}/I_{OL}$ Current per Signal <sup>2</sup>                                               | 6 mA (maximum)                   |
| Storage Temperature Range                                                                     | -65°C to +150°C                  |
| Junction Temperature While Biased                                                             | 125°C                            |

<sup>1</sup> Applies only when the related power supply ( $V_{DD\_DMC}$  or  $V_{DD\_EXT}$ ) is within specification. When the power supply is below specification, the range is the voltage being applied to that power domain  $\pm 0.2$  V.

<sup>2</sup> Applies to 100% transient duty cycle.

<sup>3</sup> Applies to TWI\_SCL and TWI\_SDA.

<sup>4</sup> Applies only when  $V_{DD\_ANA}$  is within specifications and  $\leq 1.8$  V. When  $V_{DD\_ANA}$  is within specifications and  $> 1.8$  V, the maximum rating is 1.89 V. When  $V_{DD\_ANA}$  is below specifications, the range is  $V_{DD\_ANA} \pm 0.09$  V.

Table 30. Maximum Duty Cycle for Input Transient Voltage for  $V_{DD\_INT}$  and  $V_{DD\_EXT}$

| $V_{DD\_INT}$ (V) <sup>1</sup> | $V_{DD\_EXT}$ (V) <sup>1</sup> | Maximum Duty Cycle <sup>2</sup> |
|--------------------------------|--------------------------------|---------------------------------|
| 1.120                          |                                | 5%                              |
| 1.103                          |                                | 10%                             |
| 1.086                          |                                | 20%                             |
| 1.077                          |                                | 30%                             |
| 1.065                          |                                | 50%                             |
| 1.056                          |                                | 75%                             |
| 1.050                          | 3.470                          | 100%                            |

<sup>1</sup> The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.

<sup>2</sup> Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

Table 31. Maximum Duty Cycle for Input Transient Voltage

| 3.3 V $V_{IN}$ Max (V) <sup>1</sup> | 1.8 V $V_{IN}$ Max (V) <sup>1</sup> | Maximum Duty Cycle <sup>2</sup> |
|-------------------------------------|-------------------------------------|---------------------------------|
| 3.47                                | 1.89                                | 100%                            |

<sup>1</sup> The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.

<sup>2</sup> Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## TIMING SPECIFICATIONS

All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.

### Power-Up Reset Timing

Table 32 and Figure 10 show the relationship between power supply startup and processor reset timing, as relating to the clock generation unit (CGU) and the reset control unit (RCU).

In Figure 10, the  $V_{DD\_SUPPLIES}$  are  $V_{DD\_INT}$ ,  $V_{DD\_EXT}$ ,  $V_{DD\_DMC}$ ,  $V_{DD\_REF}$ , and  $V_{DD\_ANA}$ . There are some considerations that system design must take into account:

1. The  $V_{\Delta\_EXT\_REF}$  specification must be met at all times, including during power-up reset and when powering down the device (Figure 11).
2. Any I/O pin operating in the  $V_{DD\_EXT}$  power domain, such as  $\overline{SYS\_HWRST}$ ,  $\overline{SYS\_RESOUT}$ , and so on, may actually momentarily drive until the  $V_{DD\_SUPPLIES}$  rail is powered up. Systems sharing these signals on the board must determine if there are any issues that need to be addressed based on this behavior.

Table 32. Power-Up Reset Timing

| Parameter                  |                                                                                                                                                                                                     | Min                  | Max | Unit    |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-----|---------|
| <i>Timing Requirements</i> |                                                                                                                                                                                                     |                      |     |         |
| $t_{RST\_IN\_PWR}$         | $\overline{SYS\_HWRST}$ Deasserted after $V_{DD\_SUPPLIES}$ ( $V_{DD\_INT}$ , $V_{DD\_EXT}$ , $V_{DD\_DMC}$ , $V_{DD\_REF}$ , $V_{DD\_ANA}$ ) and $SYS\_CLKIN0$ are Stable and Within Specification | $11 \times t_{CKIN}$ |     | ns      |
| $t_{PWR\_UP}$              | $V_{DD\_SUPPLIES}$ Power Ramp Up                                                                                                                                                                    | 100                  |     | $\mu s$ |
| $t_{PWR\_DOWN}$            | $V_{DD\_SUPPLIES}$ Power Ramp Down                                                                                                                                                                  | 100                  |     | $\mu s$ |

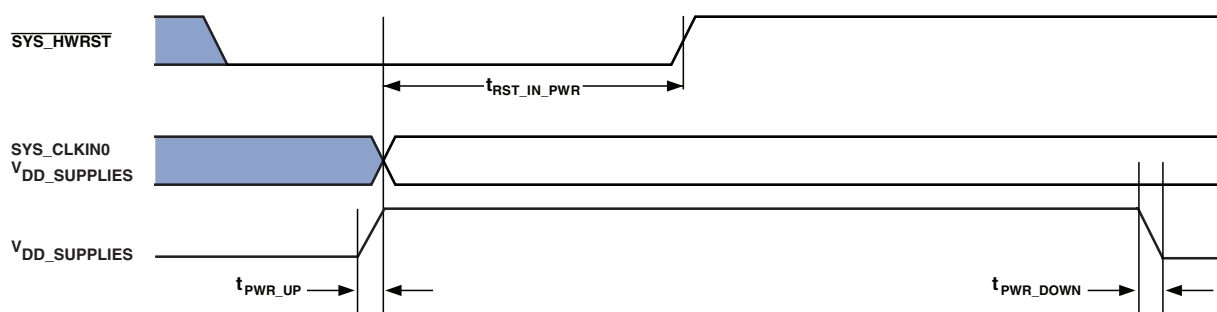


Figure 10. Power-Up Reset Timing

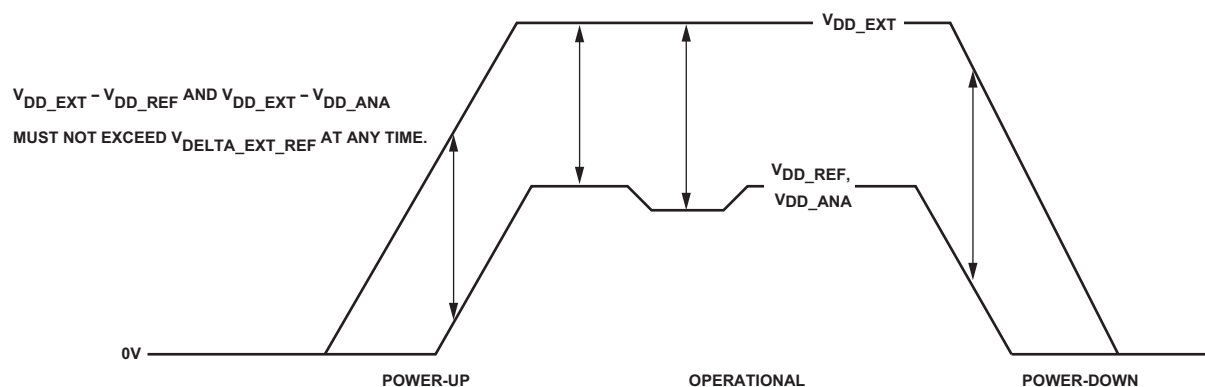


Figure 11. Power-Up and Power-Down Voltage Delta Requirement

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## Clock and Reset Timing

Table 33 and Figure 12 describe clock and reset operations related to the CGU and RCU. Per the CCLK, SYSCLK, SCLKx, DCLK, and OCLK timing specifications in Table 19 (Clock Operating Conditions), combinations of SYS\_CLKIN0 and clock multipliers must not select clock rates in excess of the maximum instruction rate of the processor.

Table 33. Clock and Reset Timing

| Parameter                  |                                                            | Min                  | Max | Unit |
|----------------------------|------------------------------------------------------------|----------------------|-----|------|
| <i>Timing Requirements</i> |                                                            |                      |     |      |
| $f_{CKIN}$                 | SYS_CLKIN0 Frequency (Crystal) <sup>1, 2</sup>             | 20                   | 30  | MHz  |
|                            | SYS_CLKIN0 Frequency (External SYS_CLKIN0) <sup>1, 2</sup> | 20                   | 30  | MHz  |
| $t_{CKINL}$                | SYS_CLKIN0 Low Pulse <sup>1</sup>                          | 16.67                |     | ns   |
| $t_{CKINH}$                | SYS_CLKIN0 High Pulse <sup>1</sup>                         | 16.67                |     | ns   |
| $t_{WRST}$                 | $\overline{RESET}$ Asserted Pulse Width Low <sup>3</sup>   | $11 \times t_{CKIN}$ |     | ns   |

<sup>1</sup> Applies to PLL bypass mode and PLL nonbypass mode.

<sup>2</sup> The  $t_{CKIN}$  period (see Figure 12) equals  $1/f_{CKIN}$ .

<sup>3</sup> Applies after power-up sequence is complete. See Table 32 and Figure 10 for power-up reset timing.

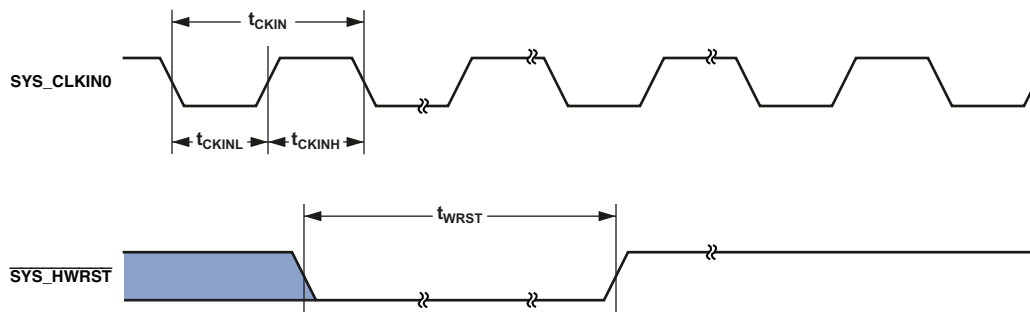


Figure 12. Clock and Reset Timing

## Dynamic Memory Controller (DMC)—Clock, Control, Write and Read Cycle Timing

The DMC clock, control, write and read timings comply with the JEDEC standards. To ensure proper operation of the DDR3/3L, all DDR3/3L guidelines must be strictly followed. See [ADSP-2156x Board Design Guidelines for Dynamic Memory Controller \(EE-418\)](#).

## Link Ports (LPs)

In LP receive mode, the LP clock is supplied externally and is called  $f_{LCLKREXT}$ , therefore the period can be represented by

$$t_{LCLKREXT} = \frac{1}{f_{LCLKREXT}}$$

In LP transmit mode, the programmed LP clock ( $f_{LCLKTPROG}$ ) frequency in megahertz is set by the following equation where VALUE is a field in the LP\_DIV register that can be set from 1 to 255:

$$f_{LCLKTPROG} = \frac{f_{OCLK_0}}{(VALUE \times 2)}$$

In the case where VALUE = 0,  $f_{LCLKTPROG} = f_{OCLK_0}$ . For all settings of VALUE, the following equation is true:

$$t_{LCLKTPROG} = \frac{1}{f_{LCLKTPROG}}$$

Calculation of the link receiver data setup and hold relative to the link clock is required to determine the maximum allowable skew that can be introduced in the transmission path length difference between LPx\_Dx and LPx\_CLK. Setup skew is the maximum delay that can be introduced in LPx\_Dx relative to LPx\_CLK (setup skew =  $t_{LCLKTWH}$  minimum –  $t_{DLDC}$  –  $t_{SLDCL}$ ). Hold skew is the maximum delay that can be introduced in LPx\_CLK relative to LPx\_Dx (hold skew =  $t_{LCLKTWL}$  minimum –  $t_{HLDCH}$  –  $t_{HLDCL}$ ). See [Table 35](#) for LP transmit timing.

**Table 34. LPs—Receive<sup>1</sup>**

| Parameter                                                    | Min                         | Max                          | Unit |
|--------------------------------------------------------------|-----------------------------|------------------------------|------|
| <i>Timing Requirements</i>                                   |                             |                              |      |
| $f_{LCLKREXT}$ LPx_CLK Frequency                             |                             | 125                          | MHz  |
| $t_{SLDCL}$ Data Setup Before LPx_CLK Low                    | 1.5                         |                              | ns   |
| $t_{HLDCL}$ Data Hold After LPx_CLK Low                      | 1.4                         |                              | ns   |
| $t_{LCLKW}$ LPx_CLK Period <sup>2</sup>                      | $t_{LCLKREXT} - 1$          |                              | ns   |
| $t_{LCLKRWL}$ LPx_CLK Width Low <sup>2</sup>                 | $0.5 \times t_{LCLKREXT}$   |                              | ns   |
| $t_{LCLKRWH}$ LPx_CLK Width High <sup>2</sup>                | $0.5 \times t_{LCLKREXT}$   |                              | ns   |
| <i>Switching Characteristic</i>                              |                             |                              |      |
| $t_{DLALC}$ LPx_ACK Low Delay After LPx_CLK Low <sup>3</sup> | $1.5 \times t_{OCLK_0} + 4$ | $2.5 \times t_{OCLK_0} + 12$ | ns   |

<sup>1</sup>Specifications apply to LP0 and LP1.

<sup>2</sup>This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external LPx\_CLK. For the external LPx\_CLK ideal maximum frequency, see the  $f_{LCLKREXT}$  specification in [Table 19](#). For LPx\_CLK generated by ADSP-215xx link ports transmit and connected to link ports receive, the width or period requirement can be taken from [Table 35](#), LPs—Transmit.

<sup>3</sup>LPx\_ACK goes low with  $t_{DLALC}$  relative to fall of LPx\_CLK after first byte, but does not go low if the link buffer of the receiver is not about to fill.

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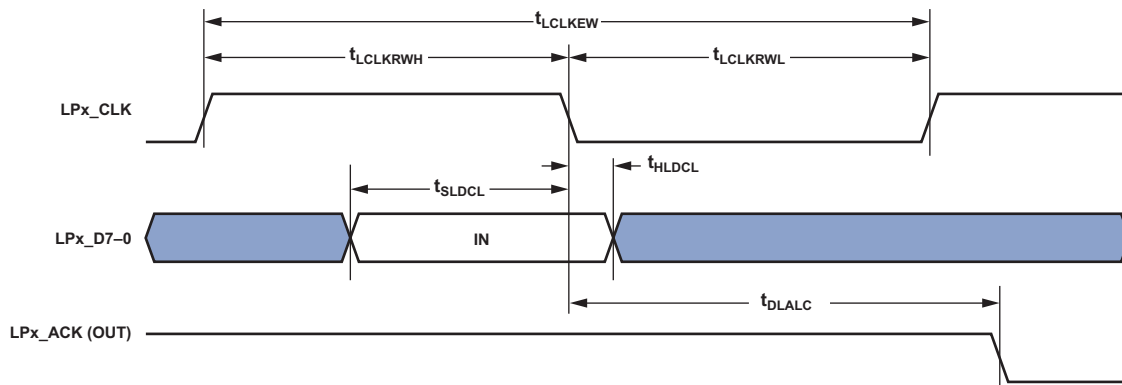


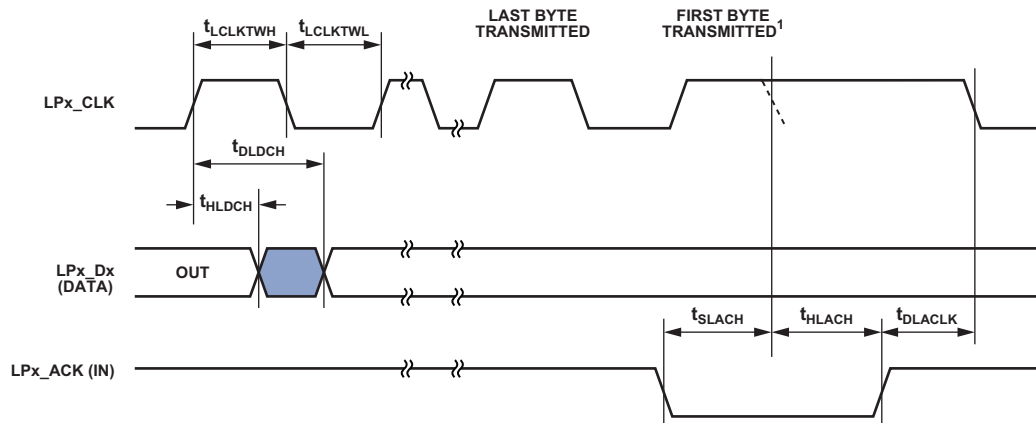
Figure 13. LPs—Receive

Table 35. LPs—Transmit<sup>1</sup>

| Parameter                                               | Min                            | Max                                              | Unit |
|---------------------------------------------------------|--------------------------------|--------------------------------------------------|------|
| <i>Timing Requirements</i>                              |                                |                                                  |      |
| t <sub>SLACH</sub> LPx_ACK Setup Before LPx_CLK Low     | $2 \times t_{OCLK\_0} + 13.5$  |                                                  | ns   |
| t <sub>HLACH</sub> LPx_ACK Hold After LPx_CLK Low       | -2.5                           |                                                  | ns   |
| <i>Switching Characteristics</i>                        |                                |                                                  |      |
| t <sub>DLDC</sub> Data Delay After LPx_CLK High         |                                | 2.23                                             | ns   |
| t <sub>HLDC</sub> Data Hold After LPx_CLK High          | -1.04                          |                                                  | ns   |
| t <sub>LCLKTWL</sub> <sup>2</sup> LPx_CLK Width Low     | $0.4 \times t_{LCLKTPROG}$     | $0.6 \times t_{LCLKTPROG}$                       | ns   |
| t <sub>LCLKTWH</sub> <sup>2</sup> LPx_CLK Width High    | $0.4 \times t_{LCLKTPROG}$     | $0.6 \times t_{LCLKTPROG}$                       | ns   |
| t <sub>LCLKTW</sub> <sup>2</sup> LPx_CLK Period         | $N \times t_{LCLKTPROG} - 0.7$ |                                                  | ns   |
| t <sub>DLACK</sub> LPx_CLK Low Delay After LPx_ACK High | $t_{OCLK\_0} + 4$              | $2 \times t_{OCLK\_0} + 1 \times t_{LPCLK} + 10$ | ns   |

<sup>1</sup>Specifications apply to LP0 and LP1.

<sup>2</sup>See Table 19 for details on the minimum period that can be programmed for t<sub>LCLKTPROG</sub>.



## NOTES

The t<sub>SLACH</sub> and t<sub>HLACH</sub> specifications apply only to the LPx\_CLK falling edge. If these specifications are met, LPx\_CLK extends and the dotted LPx\_CLK falling edge does not occur as shown. The position of the dotted falling edge can be calculated using the t<sub>LCLKTWH</sub> specification. t<sub>LCLKTWH</sub> Min must be used for t<sub>SLACH</sub> and t<sub>LCLKTWH</sub> Max for t<sub>HLACH</sub>.

Figure 14. LPs—Transmit

## Serial Ports (SPORTs)

To determine whether a device is compatible with the SPORT at clock speed  $n$ , the following specifications must be confirmed: frame sync delay and frame sync setup and hold; data delay and data setup and hold; and serial clock (SPTx\_CLK) width. In [Figure 15](#), either the rising edge or the falling edge of SPTx\_A/BCLK (external or internal) can be used as the active sampling edge.

When externally generated, the SPORT clock is called  $f_{\text{SPTCLKEXT}}$ :

$$t_{\text{SPTCLKEXT}} = \frac{1}{f_{\text{SPTCLKEXT}}}$$

When internally generated, the programmed SPORT clock ( $f_{\text{SPTCLKPROG}}$ ) frequency in megahertz is set by the following equation:

$$f_{\text{SPTCLKPROG}} = \frac{f_{\text{SCLK0}}}{(\text{CLKDIV} + 1)}$$

$$t_{\text{SPTCLKPROG}} = \frac{1}{f_{\text{SPTCLKPROG}}}$$

where  $\text{CLKDIV}$  is a field in the SPORT\_DIV register that can be set from 0 to 65,535.

**Table 36. SPORTs—External Clock<sup>1</sup>**

| Parameter                 |                                                                                                                       | Min                                | Max | Unit |
|---------------------------|-----------------------------------------------------------------------------------------------------------------------|------------------------------------|-----|------|
| Timing Requirements       |                                                                                                                       |                                    |     |      |
| t <sub>SFSE</sub>         | Frame Sync Setup Before SPTx_CLK<br>(Externally Generated Frame Sync in Either Transmit or Receive Mode) <sup>2</sup> | 2                                  |     | ns   |
| t <sub>HFSE</sub>         | Frame Sync Hold After SPTx_CLK<br>(Externally Generated Frame Sync in Either Transmit or Receive Mode) <sup>2</sup>   | 3                                  |     | ns   |
| t <sub>SDRE</sub>         | Receive Data Setup Before Receive SPTx_CLK <sup>2</sup>                                                               | 2                                  |     | ns   |
| t <sub>HDRE</sub>         | Receive Data Hold After SPTx_CLK <sup>2</sup>                                                                         | 3                                  |     | ns   |
| t <sub>SPTCLKW</sub>      | SPTx_CLK Width <sup>3</sup>                                                                                           | 0.5 × t <sub>SPTCLKEXT</sub> – 1.5 |     | ns   |
| t <sub>SPTCLK</sub>       | SPTx_CLK Period <sup>3</sup>                                                                                          | t <sub>SPTCLKEXT</sub> – 1.5       |     | ns   |
| Switching Characteristics |                                                                                                                       |                                    |     |      |
| t <sub>DFSE</sub>         | Frame Sync Delay After SPTx_CLK<br>(Internally Generated Frame Sync in Either Transmit or Receive Mode) <sup>4</sup>  |                                    | 11  | ns   |
| t <sub>HOFSE</sub>        | Frame Sync Hold After SPTx_CLK<br>(Internally Generated Frame Sync in Either Transmit or Receive Mode) <sup>4</sup>   | 2                                  |     | ns   |
| t <sub>DDTE</sub>         | Transmit Data Delay After Transmit SPTx_CLK <sup>4</sup>                                                              |                                    | 11  | ns   |
| t <sub>HDTE</sub>         | Transmit Data Hold After Transmit SPTx_CLK <sup>4</sup>                                                               | 2                                  |     | ns   |

<sup>1</sup>Specifications apply to all four SPORTs.

<sup>2</sup>Referenced to sample edge.

<sup>3</sup>This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the ideal maximum external SPTx\_CLK. For the external SPTx\_CLK ideal maximum frequency, see the  $f_{\text{SPTCLKEXT}}$  specification in [Table 19](#).

<sup>4</sup>Referenced to drive edge.

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**Table 37. SPORTs—Internal Clock<sup>1</sup>**

| Parameter                        |                                                                                                                       | Min                                    | Max | Unit |
|----------------------------------|-----------------------------------------------------------------------------------------------------------------------|----------------------------------------|-----|------|
| <i>Timing Requirements</i>       |                                                                                                                       |                                        |     |      |
| t <sub>SFSI</sub>                | Frame Sync Setup Before SPTx_CLK<br>(Externally Generated Frame Sync in Either Transmit or Receive Mode) <sup>2</sup> | 12                                     |     | ns   |
| t <sub>HFSI</sub>                | Frame Sync Hold After SPTx_CLK<br>(Externally Generated Frame Sync in Either Transmit or Receive Mode) <sup>2</sup>   | –0.5                                   |     | ns   |
| t <sub>SDRI</sub>                | Receive Data Setup Before SPTx_CLK <sup>2</sup>                                                                       | 3.4                                    |     | ns   |
| t <sub>HDRI</sub>                | Receive Data Hold After SPTx_CLK <sup>2</sup>                                                                         | 2                                      |     | ns   |
| <i>Switching Characteristics</i> |                                                                                                                       |                                        |     |      |
| t <sub>DFSI</sub>                | Frame Sync Delay After SPTx_CLK (Internally Generated Frame Sync in Transmit or Receive Mode) <sup>3</sup>            |                                        | 3.5 | ns   |
| t <sub>HOFI</sub>                | Frame Sync Hold After SPTx_CLK (Internally Generated Frame Sync in Transmit or Receive Mode) <sup>3</sup>             | –3                                     |     | ns   |
| t <sub>DDTI</sub>                | Transmit Data Delay After SPTx_CLK <sup>3</sup>                                                                       |                                        | 3.5 | ns   |
| t <sub>HDTI</sub>                | Transmit Data Hold After SPTx_CLK <sup>3</sup>                                                                        | –3                                     |     | ns   |
| t <sub>SPTCLKIW</sub>            | SPTx_CLK Width <sup>4</sup>                                                                                           | $0.5 \times t_{\text{SPTCLKPROG}} - 2$ |     | ns   |
| t <sub>SPTCLKWI</sub>            | SPTx_CLK Period <sup>4</sup>                                                                                          | $t_{\text{SPTCLKPROG}} - 1.5$          |     | ns   |

<sup>1</sup>Specifications apply to all four SPORTs.

<sup>2</sup>Referenced to the sample edge.

<sup>3</sup>Referenced to drive edge.

<sup>4</sup>See [Table 19](#) for details on the minimum period that can be programmed for  $f_{\text{SPTCLKPROG}}$ .

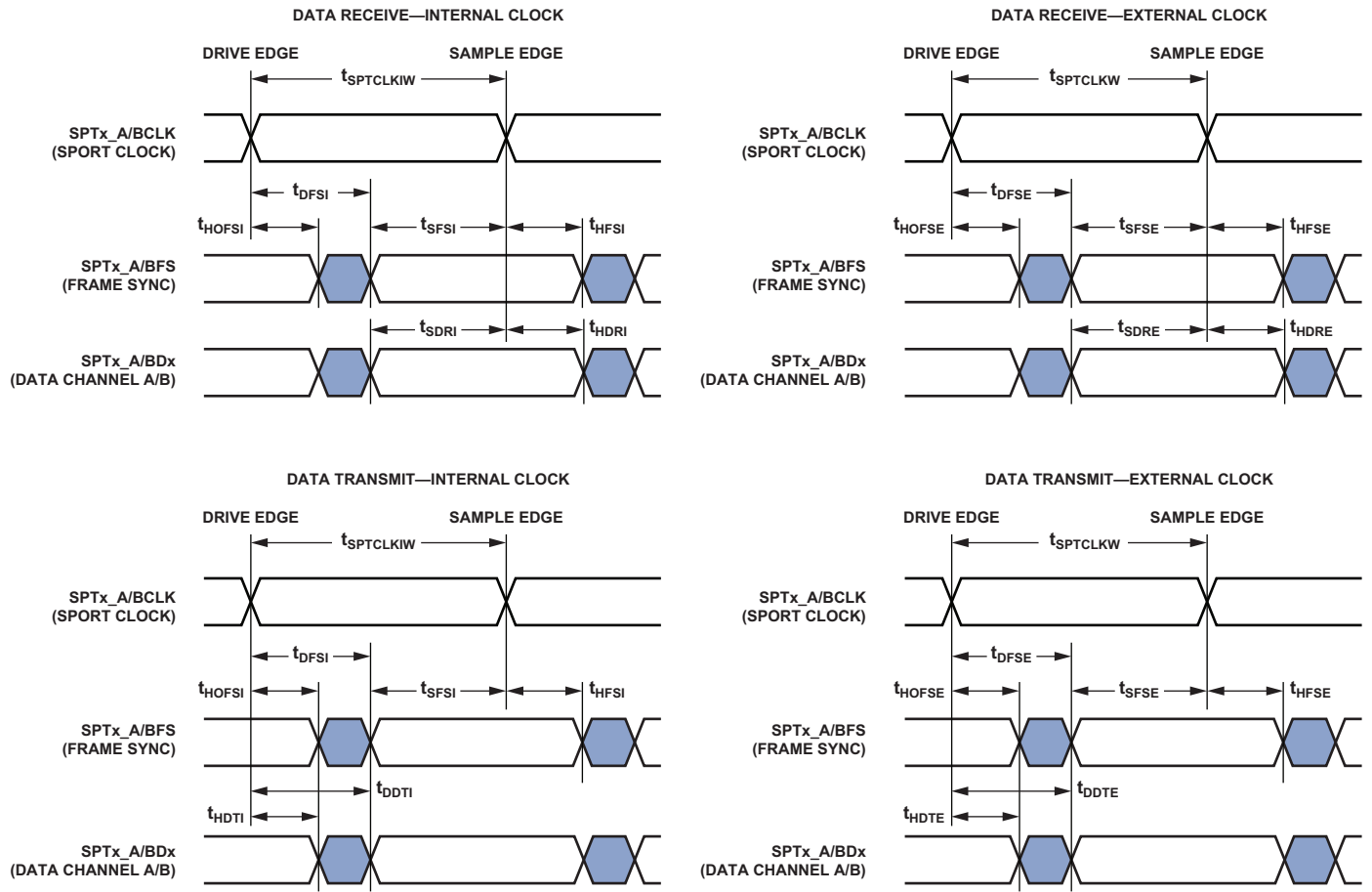


Figure 15. SPORTs

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**Table 38. SPORTs—Enable and Three-State<sup>1</sup>**

| Parameter                        |                                                           | Min  | Max | Unit |
|----------------------------------|-----------------------------------------------------------|------|-----|------|
| <i>Switching Characteristics</i> |                                                           |      |     |      |
| $t_{DDTEN}$                      | Data Enable From External Transmit SPTx_CLK <sup>2</sup>  | 1    |     | ns   |
| $t_{DDTTE}$                      | Data Disable From External Transmit SPTx_CLK <sup>2</sup> |      | 14  | ns   |
| $t_{DDTIN}$                      | Data Enable From Internal Transmit SPTx_CLK <sup>2</sup>  | -2.5 |     | ns   |
| $t_{DDTTI}$                      | Data Disable From Internal Transmit SPTx_CLK <sup>2</sup> |      | 2.8 | ns   |

<sup>1</sup>Specifications apply to all four SPORTs.

<sup>2</sup>Referenced to drive edge.

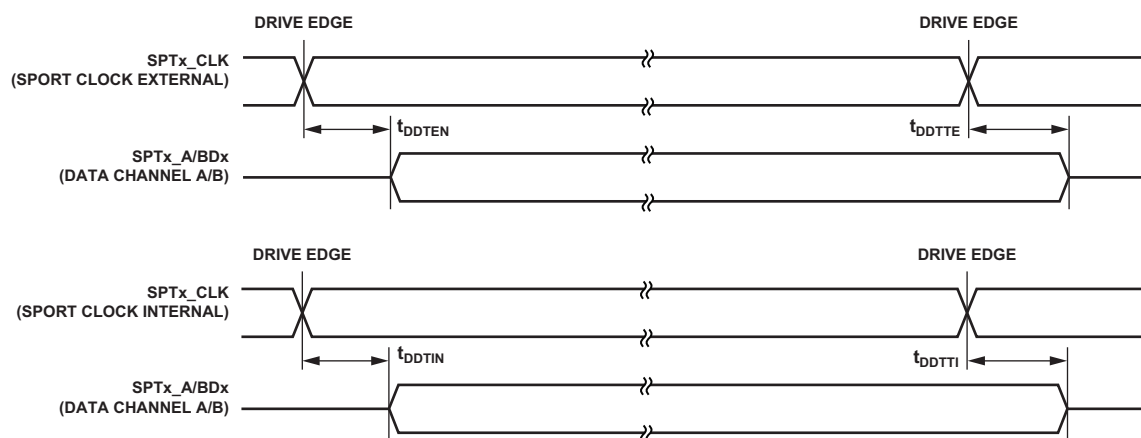


Figure 16. SPORTs—Enable and Three-State

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The SPTx\_TDV output signal becomes active in SPORT multichannel mode. During transmit slots (enabled with active channel selection registers) the SPTx\_TDV is asserted for communication with external devices.

**Table 39. SPORTs—Transmit Data Valid (TDV)<sup>1</sup>**

| Parameter                        |                                                                         | Min  | Max | Unit |
|----------------------------------|-------------------------------------------------------------------------|------|-----|------|
| <i>Switching Characteristics</i> |                                                                         |      |     |      |
| $t_{DRDVEN}$                     | Data Valid Enable Delay From Drive Edge of External Clock <sup>2</sup>  | 2    |     | ns   |
| $t_{DFDVEN}$                     | Data Valid Disable Delay From Drive Edge of External Clock <sup>2</sup> |      | 14  | ns   |
| $t_{DRDVIN}$                     | Data Valid Enable Delay From Drive Edge of Internal Clock <sup>2</sup>  | -2.5 |     | ns   |
| $t_{DFDVIN}$                     | Data Valid Disable Delay From Drive Edge of Internal Clock <sup>2</sup> |      | 3.5 | ns   |

<sup>1</sup> Specifications apply to all four SPORTs.

<sup>2</sup> Referenced to drive edge.

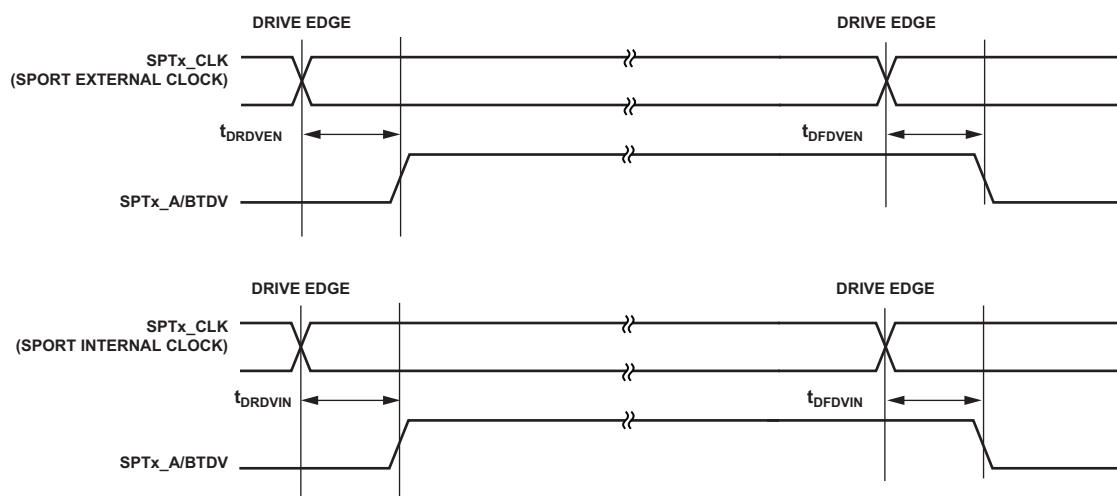


Figure 17. SPORTs—Transmit Data Valid Internal and External Clock

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**Table 40. SPORTs—External Late Frame Sync<sup>1</sup>**

| Parameter                        |                                                                                                                                         | Min | Max | Unit |
|----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------|
| <i>Switching Characteristics</i> |                                                                                                                                         |     |     |      |
| $t_{DDLTFSE}$                    | Data Delay From Late External Transmit Frame Sync or External Receive Frame Sync with SPORT_MCTL_A/B bits MCE = 1, MFD = 0 <sup>2</sup> |     | 14  | ns   |
| $t_{DDTENFS}$                    | Data Enable for SPORT_MCTL_A/B bits MCE = 1, MFD = 0 <sup>2</sup>                                                                       | 0.5 |     | ns   |

<sup>1</sup>Specifications apply to all four SPORTs.

<sup>2</sup>The  $t_{DDLTFSE}$  and  $t_{DDTENFS}$  parameters apply to left justified as well as standard serial mode and MCE = 1, MFD = 0.

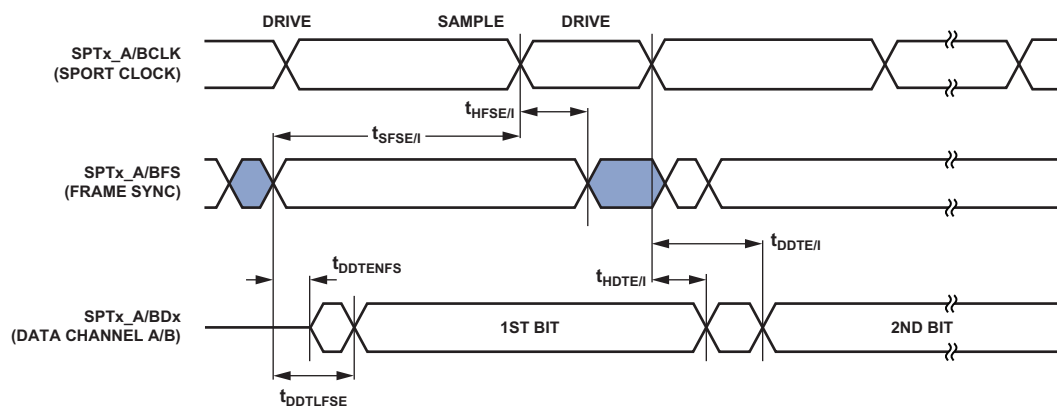


Figure 18. External Late Frame Sync

## Asynchronous Sample Rate Converter (ASRC)—Serial Input Port

The ASRC input signals are routed from the DAI0\_PINx pins using the SRU. Therefore, the timing specifications provided in [Table 41](#) are valid at the DAI0\_PINx pins.

**Table 41. ASRC, Serial Input Port**

| Parameter                                                       | Min                  | Max | Unit |
|-----------------------------------------------------------------|----------------------|-----|------|
| <i>Timing Requirements</i>                                      |                      |     |      |
| $t_{SRCSFS}^1$ Frame Sync Setup Before Serial Clock Rising Edge | 4                    |     | ns   |
| $t_{SRCHFS}^1$ Frame Sync Hold After Serial Clock Rising Edge   | 5.5                  |     | ns   |
| $t_{SRCSD}^1$ Data Setup Before Serial Clock Rising Edge        | 4                    |     | ns   |
| $t_{SRCHD}^1$ Data Hold After Serial Clock Rising Edge          | 5.5                  |     | ns   |
| $t_{SRCLKW}$ Clock Width                                        | $t_{SCLK0} - 1$      |     | ns   |
| $t_{SRCLK}$ Clock Period                                        | $2 \times t_{SCLK0}$ |     | ns   |

<sup>1</sup> The serial clock, data, and frame sync signals can originate from any of the DAI pins. The serial clock and frame sync signals can also originate via PCG or SPORTs. The input of the PCG can be either CLKIN or any of the DAI pins.

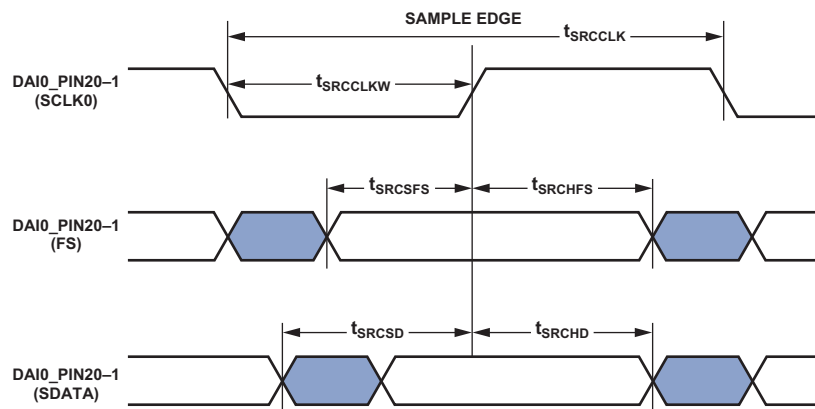


Figure 19. ASRC Serial Input Port Timing

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## Asynchronous Sample Rate Converter (ASRC)—Serial Output Port

For the serial output port, the frame sync is an input and it must meet setup and hold times with regard to SCLK0 on the output port. The serial data output has a hold time and delay specification with regard to the serial clock. The serial clock rising edge is the sampling edge, and the falling edge is the drive edge.

**Table 42. ASRC, Serial Output Port**

| Parameter                        |                                                     | Min                  | Max | Unit |
|----------------------------------|-----------------------------------------------------|----------------------|-----|------|
| <i>Timing Requirements</i>       |                                                     |                      |     |      |
| $t_{SRCSFS}^1$                   | Frame Sync Setup Before Serial Clock Rising Edge    | 4                    |     | ns   |
| $t_{SRCHFS}^1$                   | Frame Sync Hold After Serial Clock Rising Edge      | 5.5                  |     | ns   |
| $t_{SRCLKW}$                     | Clock Width                                         | $t_{SCLK0} - 1$      |     | ns   |
| $t_{SRCCLK}$                     | Clock Period                                        | $2 \times t_{SCLK0}$ |     | ns   |
| <i>Switching Characteristics</i> |                                                     |                      |     |      |
| $t_{SRCTDD}^1$                   | Transmit Data Delay After Serial Clock Falling Edge |                      | 13  | ns   |
| $t_{SRCTDH}^1$                   | Transmit Data Hold After Serial Clock Falling Edge  | 1                    |     | ns   |

<sup>1</sup>The serial clock, data, and frame sync signals can originate from any of the DAI pins. The serial clock and frame sync signals can also originate via PCG or SPORTs. The input of the PCG can be either CLKIN, SCLK0, or any of the DAI pins.

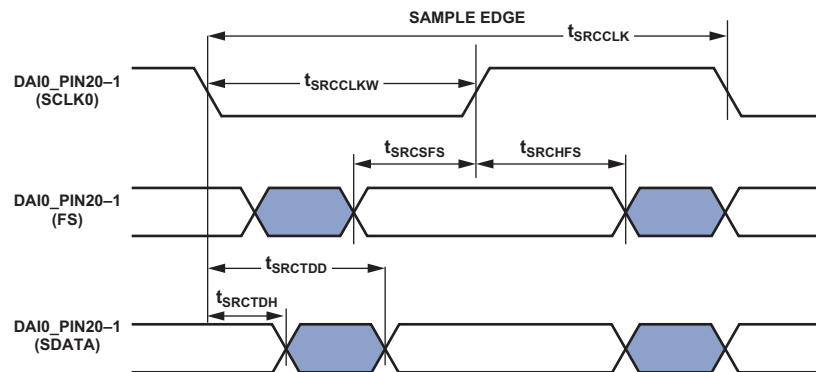


Figure 20. ASRC Serial Output Port Timing

## SPI Port—Master Timing

### SPI0, SPI1, and SPI2

Table 43 and Figure 21 describe the SPI port master operations.

When internally generated, the programmed SPI clock ( $f_{\text{SPICLKPROG}}$ ) frequency in megahertz is set by the following equation:

$$f_{\text{SPICLKPROG}} = \frac{f_{\text{CDU_CLK00}}}{(\text{BAUD} + 1)}$$

$$t_{\text{SPICLKPROG}} = \frac{1}{f_{\text{SPICLKPROG}}}$$

where *BAUD* is a field in the SPIx\_CLK register that can be set from 0 to 65,535.

Note that

- In dual-mode data transmit, the SPIx\_MISO signal is also an output.
- In quad-mode data transmit, the SPIx\_MISO, SPIx\_D2, and SPIx\_D3 signals are also outputs.
- In dual-mode data receive, the SPIx\_MOSI signal is also an input.
- In quad-mode data receive, the SPIx\_MOSI, SPIx\_D2, and SPIx\_D3 signals are also inputs.
- Quad mode is supported by SPI1 and SPI2.
- CPHA is a configuration bit in the SPI\_CTL register.

**Table 43. SPI Port—Master Timing<sup>1</sup>**

| Parameter                        |                                                                                    | Min                                      | Max | Unit |
|----------------------------------|------------------------------------------------------------------------------------|------------------------------------------|-----|------|
| <i>Timing Requirements</i>       |                                                                                    |                                          |     |      |
| $t_{\text{SSPDM}}$               | Data Input Valid to SPIx_CLK Edge (Data Input Setup)                               | 3.5                                      |     | ns   |
| $t_{\text{HSPDM}}$               | SPIx_CLK Sampling Edge to Data Input Invalid                                       | 2                                        |     | ns   |
| <i>Switching Characteristics</i> |                                                                                    |                                          |     |      |
| $t_{\text{SDSCIM}}$              | $\overline{\text{SPIx\_SEL}}$ Low to First SPI_CLK Edge for CPHA = 1 <sup>2</sup>  | $t_{\text{SPICLKPROG}} - 5$              |     | ns   |
|                                  | $\overline{\text{SPIx\_SEL}}$ Low to First SPI_CLK Edge for CPHA = 0 <sup>2</sup>  | $1.5 \times t_{\text{SPICLKPROG}} - 5$   |     | ns   |
| $t_{\text{SPICHM}}$              | SPIx_CLK High Period <sup>3</sup>                                                  | $0.5 \times t_{\text{SPICLKPROG}} - 1.5$ |     | ns   |
| $t_{\text{SPICLM}}$              | SPIx_CLK Low Period <sup>3</sup>                                                   | $0.5 \times t_{\text{SPICLKPROG}} - 1.5$ |     | ns   |
| $t_{\text{SPICLK}}$              | SPIx_CLK Period <sup>3</sup>                                                       | $t_{\text{SPICLKPROG}} - 1.5$            |     | ns   |
| $t_{\text{HDSM}}$                | Last SPIx_CLK Edge to $\overline{\text{SPIx\_SEL}}$ High for CPHA = 1 <sup>2</sup> | $1.5 \times t_{\text{SPICLKPROG}} - 5$   |     | ns   |
|                                  | Last SPIx_CLK Edge to $\overline{\text{SPIx\_SEL}}$ High for CPHA = 0 <sup>2</sup> | $t_{\text{SPICLKPROG}} - 5$              |     | ns   |
| $t_{\text{SPITDM}}$              | Sequential Transfer Delay <sup>2, 4</sup>                                          | $t_{\text{SPICLKPROG}} - 1.5$            |     | ns   |
| $t_{\text{DDSPDM}}$              | SPIx_CLK Edge to Data Out Valid (Data Out Delay)                                   |                                          | 2.7 | ns   |
| $t_{\text{HDSPIDM}}$             | SPIx_CLK Edge to Data Out Invalid (Data Out Hold)                                  | -3.75                                    |     | ns   |

<sup>1</sup> All specifications apply to SPI0, SPI1, and SPI2.

<sup>2</sup> Specification assumes the LEADX and LAGX bits in the SPI\_DLY register are 1.

<sup>3</sup> See Table 19 for details on the minimum period that can be programmed for  $t_{\text{SPICLKPROG}}$ .

<sup>4</sup> Applies to sequential mode with STOP ≥ 1.

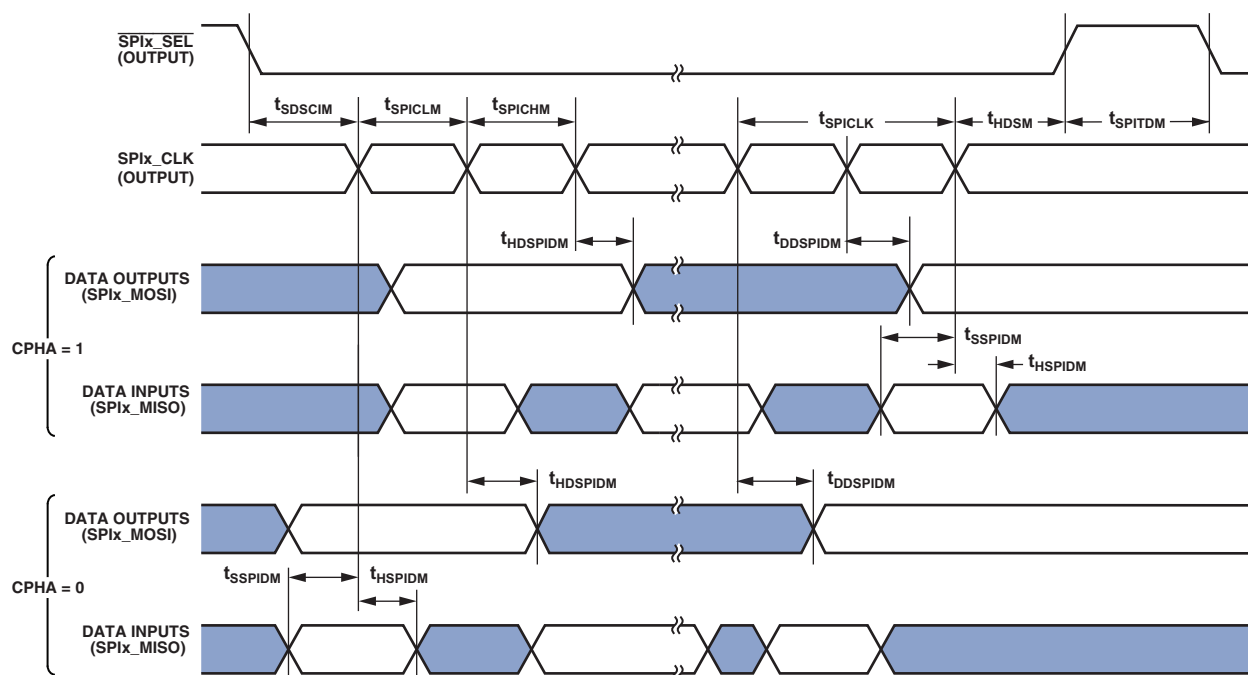


Figure 21. SPI Port—Master Timing

## SPI Port—Slave Timing

### SPI0, SPI1, and SPI2

Table 44 and Figure 22 describe SPI port slave operations. Note that

- In dual-mode data transmit, the SPIx\_MOSI signal is also an output.
- In quad-mode data transmit, the SPIx\_MOSI, SPIx\_D2, and SPIx\_D3 signals are also outputs.
- In dual-mode data receive, the SPIx\_MISO signal is also an input.
- In quad-mode data receive, the SPIx\_MISO, SPIx\_D2, and SPIx\_D3 signals are also inputs.
- In SPI slave mode, the SPI clock is supplied externally and is called  $f_{\text{SPICLKEXT}}$ :

$$t_{\text{SPICLKEXT}} = \frac{1}{f_{\text{SPICLKEXT}}}$$

- Quad mode is supported by SPI1 and SPI2.
- CPHA is a configuration bit in the SPI\_CTL register.

**Table 44. SPI Port—Slave Timing<sup>1</sup>**

| Parameter                                                                     | Min                    | Max   | Unit |
|-------------------------------------------------------------------------------|------------------------|-------|------|
| Timing Requirements                                                           |                        |       |      |
| tSPICHS      SPIx_CLK High Period <sup>2</sup>                                | 0.5 × tSPICLKEXT – 1.5 |       | ns   |
| tSPICLS      SPIx_CLK Low Period <sup>2</sup>                                 | 0.5 × tSPICLKEXT – 1.5 |       | ns   |
| tSPICLK      SPIx_CLK Period <sup>2</sup>                                     | tSPICLKEXT – 1.5       |       | ns   |
| tHDS          Last SPIx_CLK Edge to $\overline{\text{SPIx\_SS}}$ Not Asserted | 5                      |       | ns   |
| tSPITDS      Sequential Transfer Delay                                        | tSPICLKEXT – 1.5       |       | ns   |
| tSDSCI $\overline{\text{SPIx\_SS}}$ Assertion to First SPIx_CLK Edge          | 11.7                   |       | ns   |
| tSSPID       Data Input Valid to SPIx_CLK Edge (Data Input Setup)             | 2                      |       | ns   |
| tHSPID       SPIx_CLK Sampling Edge to Data Input Invalid                     | 1.6                    |       | ns   |
| Switching Characteristics                                                     |                        |       |      |
| tDSOE $\overline{\text{SPIx\_SS}}$ Assertion to Data Out Active               | 0                      | 14.12 | ns   |
| tDSDHI $\overline{\text{SPIx\_SS}}$ Deassertion to Data High Impedance        | 0                      | 12.6  | ns   |
| tDDSPID     SPIx_CLK Edge to Data Out Valid (Data Out Delay)                  | 14.16                  |       | ns   |
| tHDSPID     SPIx_CLK Edge to Data Out Invalid (Data Out Hold)                 | 1.5                    |       | ns   |

<sup>1</sup> All specifications apply to SPI0, SPI1, and SPI2.

<sup>2</sup> This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPIx\_CLK. For the external SPIx\_CLK ideal maximum frequency, see the  $f_{\text{SPICLKEXT}}$  specification in Table 19.

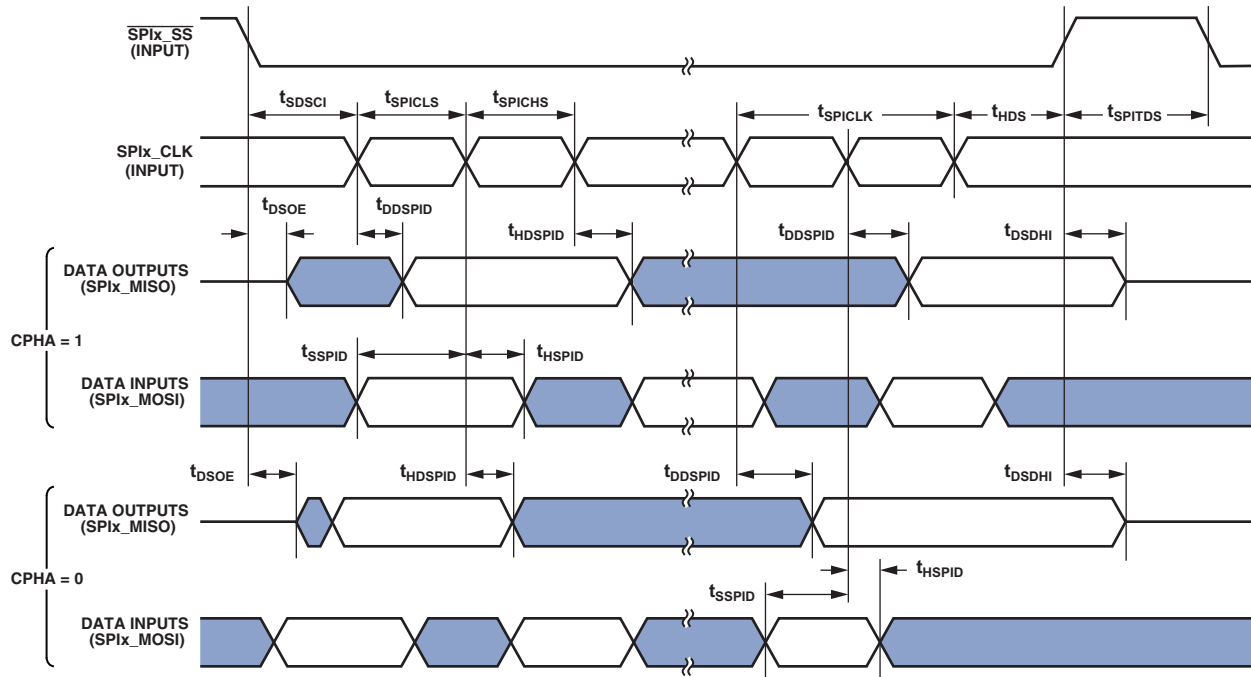


Figure 22. SPI Port—Slave Timing

SPI Port—SPIx\_RDY Slave Timing

SPIx\_RDY provides flow control. CPOL, CPHA, and FCCH are configuration bits in the SPIx\_CTL register.

Table 45. SPI Port—SPIx\_RDY Slave Timing<sup>1</sup>

| Parameter                                                             | Conditions | Min            | Max                 | Unit |
|-----------------------------------------------------------------------|------------|----------------|---------------------|------|
| <i>Switching Characteristic</i>                                       |            |                |                     |      |
| tDSPISCKRDYS SPIx_RDY Deassertion From Last Valid Input SPIx_CLK Edge | FCCH = 0   | 3 × tCDU_CLK00 | 4 × tCDU_CLK00 + 10 | ns   |
|                                                                       | FCCH = 1   | 4 × tCDU_CLK00 | 5 × tCDU_CLK00 + 10 | ns   |

<sup>1</sup> All specifications apply to all three SPIs.

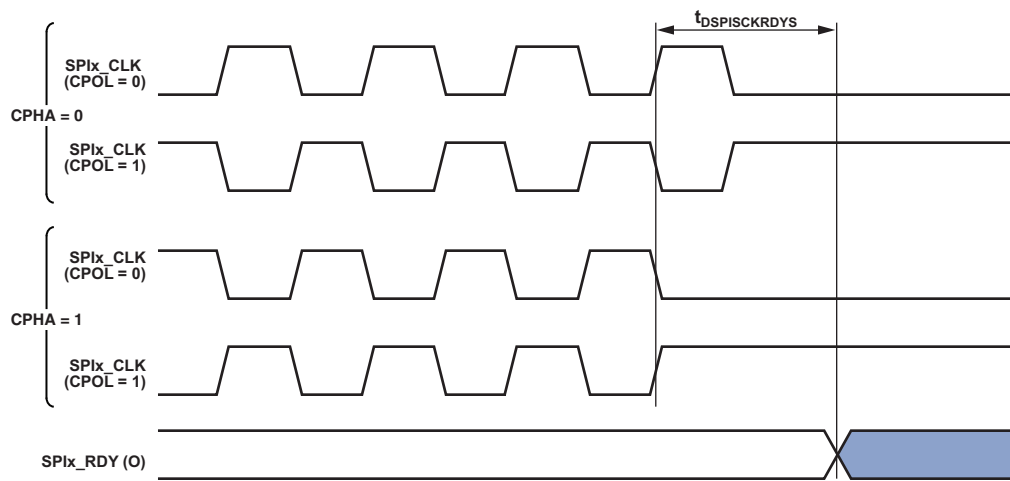


Figure 23. SPIx\_RDY Deassertion from Valid Input SPIx\_CLK Edge in Slave Mode

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## SPI Port—Open Drain Mode (ODM) Timing

In Figure 24 and Figure 25, the outputs can be SPIx\_MOSI, SPIx\_MISO, SPIx\_D2, and/or SPIx\_D3, depending on the mode of operation. CPOL and CPHA are configuration bits in the SPI\_CTL register.

Table 46. SPI Port—ODM Master Mode Timing<sup>1</sup>

| Parameter                                                                  | Min  | Max | Unit |
|----------------------------------------------------------------------------|------|-----|------|
| <i>Switching Characteristics</i>                                           |      |     |      |
| $t_{\text{HDSPIODMM}}$ SPIx_CLK Edge to High Impedance From Data Out Valid | -1.5 |     | ns   |
| $t_{\text{DSDPIODMM}}$ SPIx_CLK Edge to Data Out Valid From High Impedance |      | 6   | ns   |

<sup>1</sup> All specifications apply to all three SPIs.

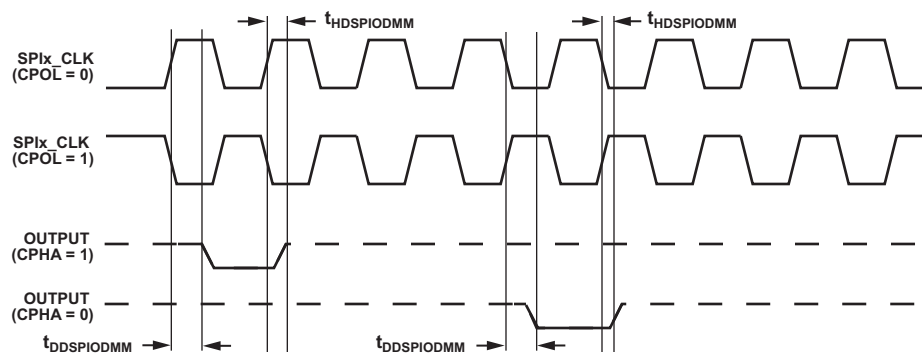


Figure 24. ODM Master Mode

Table 47. SPI Port—ODM Slave Mode<sup>1</sup>

| Parameter                                                                  | Min | Max | Unit |
|----------------------------------------------------------------------------|-----|-----|------|
| <i>Timing Requirements</i>                                                 |     |     |      |
| $t_{\text{HDSPIODMS}}$ SPIx_CLK Edge to High Impedance From Data Out Valid | 0   |     | ns   |
| $t_{\text{DSDPIODMS}}$ SPIx_CLK Edge to Data Out Valid From High Impedance |     | 11  | ns   |

<sup>1</sup> All specifications apply to all three SPIs.

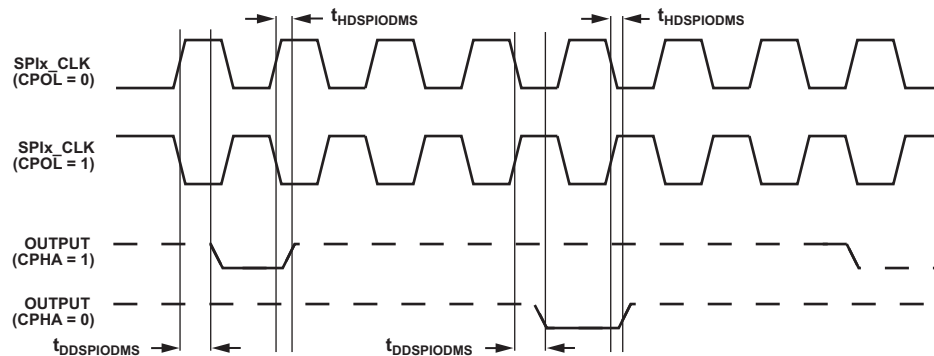


Figure 25. ODM Slave Mode

## SPI Port—SPIx\_RDY Master Timing

SPIx\_RDY is used to provide flow control. CPOL and CPHA are configuration bits in the SPIx\_CTL register, whereas LEADX, LAGX, and STOP are configuration bits in the SPIx\_DLY register.

**Table 48. SPI Port—SPIx\_RDY Master Timing<sup>1</sup>**

| Parameter                                                                               | Conditions         | Min                                                       | Max                                                         | Unit |
|-----------------------------------------------------------------------------------------|--------------------|-----------------------------------------------------------|-------------------------------------------------------------|------|
| <i>Timing Requirement</i>                                                               |                    |                                                           |                                                             |      |
| $t_{SRDYSCKM}$ Setup Time for SPIx_RDY Deassertion Before Last Valid Data SPIx_CLK Edge |                    | $(2 + 2 \times \text{BAUD}^2) \times t_{CDU\_CLK00} + 11$ |                                                             | ns   |
| <i>Switching Characteristic</i>                                                         |                    |                                                           |                                                             |      |
| $t_{DRDYSCKM}^3$ Assertion of SPIx_RDY to First SPIx_CLK Edge of Next Transfer          | BAUD = 0, CPHA = 0 | $4.5 \times t_{CDU\_CLK00}$                               | $5.5 \times t_{CDU\_CLK00} + 11$                            | ns   |
|                                                                                         | BAUD = 0, CPHA = 1 | $4 \times t_{CDU\_CLK00}$                                 | $5 \times t_{CDU\_CLK00} + 11$                              | ns   |
|                                                                                         | BAUD > 0, CPHA = 0 | $(1 + 1.5 \times \text{BAUD}^2) \times t_{CDU\_CLK00}$    | $(2 + 2.5 \times \text{BAUD}^2) \times t_{CDU\_CLK00} + 11$ | ns   |
|                                                                                         | BAUD > 0, CPHA = 1 | $(1 + 1 \times \text{BAUD}^2) \times t_{CDU\_CLK00}$      | $(2 + 2 \times \text{BAUD}^2) \times t_{CDU\_CLK00} + 11$   | ns   |

<sup>1</sup> All specifications apply to all three SPIs.

<sup>2</sup> BAUD value is set using the SPIx\_CLK.BAUD bits. BAUD value = SPIx\_CLK.BAUD bits + 1.

<sup>3</sup> Specification assumes the LEADX, LAGX, and STOP bits in the SPI\_DLY register are zero.

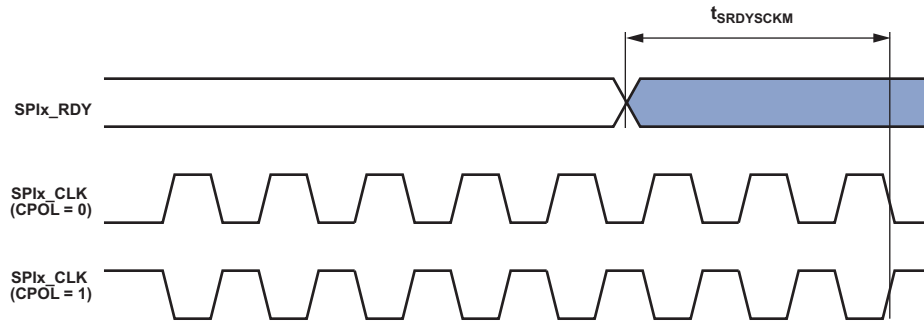


Figure 26. SPIx\_RDY Setup Before SPIx\_CLK

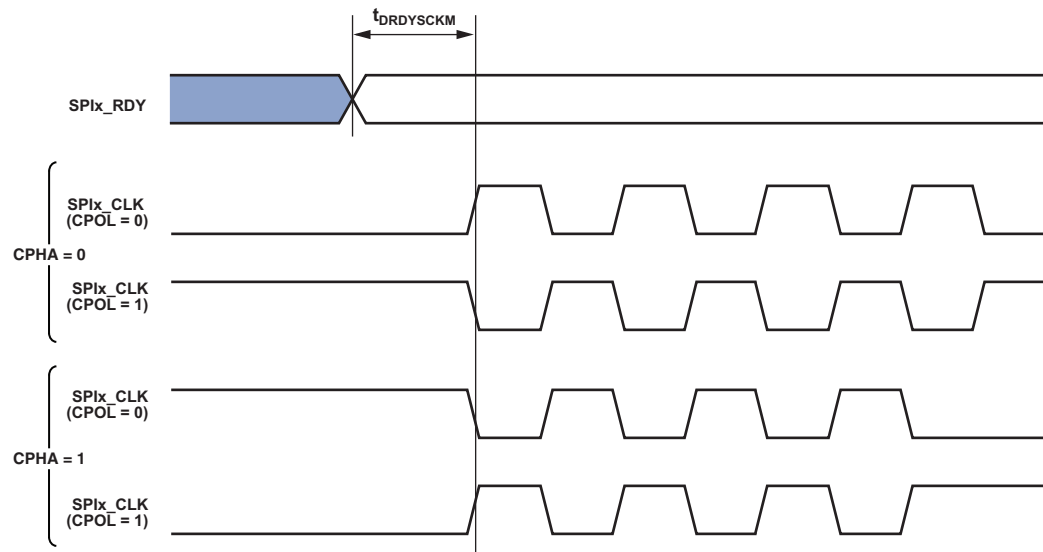


Figure 27. SPIx\_CLK Switching Diagram after SPIx\_RDY Assertion

## OSPI Port—Master Timing

### OSPI0

Table 49 and Figure 28 describe the OSPI port master operations. Slave mode is not supported for OSPI.

When internally generated, the programmed SPI clock ( $f_{SPICLKPROG}$ ) frequency in megahertz is set by the following equation:

$$f_{SPICLKPROG} = \frac{f_{SYSCLK}}{PRG\_MBD}$$

$$t_{SPICLKPROG} = \frac{1}{f_{SPICLKPROG}}$$

where  $PRG\_MBD$  is the master mode baud rate divisor.

Note that

- In dual-mode data transmit, the OSPI0\_MISO signal is also an output.
- In quad-mode data transmit, the OSPI0\_MISO, OSPI0\_D2, and OSPI0\_D3 signals are also outputs.
- In octal-mode data transmit, the OSPI0\_MISO, OSPI0\_D2, OSPI0\_D3, OSPI0\_D4, OSPI0\_D5, OSPI0\_D6, and OSPI0\_D7 signals are also outputs.
- In dual-mode data receive, the OSPI0\_MOSI signal is also an input.
- In quad-mode data receive, the OSPI0\_MOSI, OSPI0\_D2, and OSPI0\_D3 signals are also inputs.
- In octal-mode data receive, the OSPI0\_MISO, OSPI0\_D2, OSPI0\_D3, OSPI0\_D4, OSPI0\_D5, OSPI0\_D6, and OSPI0\_D7 signals are also outputs.
- CPHA is a configuration bit in the OSPI0\_CTL register.

**Table 49. OSPI0 Port—Master Timing<sup>1</sup>**

| Parameter                                                                                     | Min                                                              | Max                                        | Unit |
|-----------------------------------------------------------------------------------------------|------------------------------------------------------------------|--------------------------------------------|------|
| <i>Timing Requirements</i>                                                                    |                                                                  |                                            |      |
| $t_{SSPIDM}$ Data Input Valid to OSPI0_CLK Sampling Edge (Data Input Setup) <sup>2</sup>      | $t_{SYSCLK} + 2$                                                 |                                            | ns   |
| $t_{HSPIDM}$ OSPI0_CLK Sampling Edge to Data Input Invalid (Data Input Hold) <sup>2</sup>     | 1                                                                |                                            | ns   |
| <i>Switching Characteristics</i>                                                              |                                                                  |                                            |      |
| $t_{SDSCIM}$ $\overline{OSPI0\_SEL}$ Low to First OSPI0_CLK Edge <sup>3</sup>                 | $0.5 \times t_{SPICLKPROG} + PRG\_CSSOT \times t_{SYSCLK} - 1.5$ |                                            | ns   |
| $t_{SPICHM}$ OSPI0_CLK High Period <sup>4</sup>                                               | $0.5 \times t_{SPICLKPROG} - 1.5$                                |                                            | ns   |
| $t_{SPICLM}$ OSPI0_CLK Low Period <sup>4</sup>                                                | $0.5 \times t_{SPICLKPROG} - 1.5$                                |                                            | ns   |
| $t_{SPICLK}$ OSPI0_CLK Period <sup>4</sup>                                                    | $t_{SPICLKPROG} - 1.5$                                           |                                            | ns   |
| $t_{HDSM}$ Last OSPI0_CLK Edge to $\overline{OSPI0\_SEL}$ High for Mode = 0 <sup>5</sup>      | $PRG\_CSEOT \times t_{SYSCLK} - 1$                               |                                            | ns   |
|                                                                                               | $PRG\_CSEOT \times t_{SYSCLK} + 0.5 \times t_{SPICLKPROG} - 1$   |                                            | ns   |
| $t_{DDSPIDM}$ OSPI0_CLK Edge to Data Out Valid to Driving Edge (Data Out Delay) <sup>7</sup>  |                                                                  | $(PRG\_WRHLD + 1) \times t_{SYSCLK} + 2.5$ | ns   |
| $t_{HDSPIDM}$ OSPI0_CLK Edge to Data Out Invalid to Driving Edge (Data Out Hold) <sup>7</sup> | $PRG\_WRHLD \times t_{SYSCLK} - 1$                               |                                            | ns   |
| $t_{PD}$ OSPI0_CLK Internal to OSPI0_CLK Output Delay (Propagation Delay)                     | 2.2                                                              | 5.5                                        | ns   |

<sup>1</sup> All specifications apply to OSPI0 only.

<sup>2</sup>  $t_{SSPIDM}$  and  $t_{HSPIDM}$  specifications are characterized for OSPI0\_RDC settings of 2 for DDR mode and 4 for SDR mode.

<sup>3</sup>  $PRG\_CSSOT$  = chip select start of transfer (defined in OSPI0\_DLY[7:0]).

<sup>4</sup> See Table 19 for details on the minimum period that can be programmed for  $t_{SPICLKPROG}$ .

<sup>5</sup>  $PRG\_CSEOT$  = chip select end of transfer (defined in OSPI0\_DLY[15:8]).

<sup>6</sup> Mode = clock phase and clock polarity bits (defined in OSPI0\_CTL[2:1]).

<sup>7</sup>  $PRG\_WRHLD$  = transmit delay to improve output hold (defined in OSPI0\_RDC[19:16]).

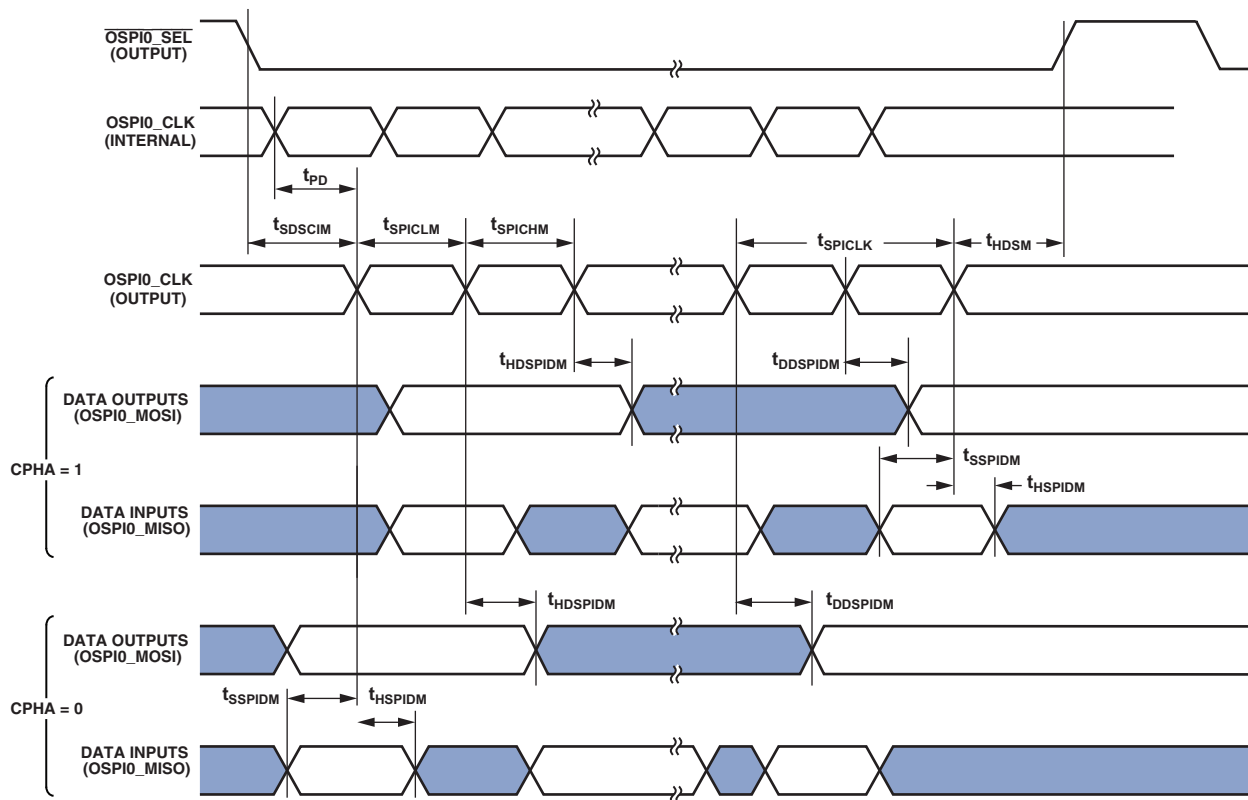


Figure 28. OSPI Port—Master Timing

## Precision Clock Generator (PCG) (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes inputs directly from the DAI pins (via pin buffers) and sends outputs directly to the DAI pins. For the other cases, where the PCG inputs and outputs are not directly routed to/from DAI pins (via pin buffers), there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI0\_PINx).

**Table 50. PCG (Direct Pin Routing)**

| Parameter                                                                            | Min                                       | Max                                        | Unit |
|--------------------------------------------------------------------------------------|-------------------------------------------|--------------------------------------------|------|
| <i>Timing Requirements</i>                                                           |                                           |                                            |      |
| $t_{PCGIP}$ Input Clock Period                                                       | $t_{SCLK0} \times 2$                      |                                            | ns   |
| $t_{STRIG}$ PCG Trigger Setup Before Falling Edge of PCG Input Clock                 | 4.5                                       |                                            | ns   |
| $t_{HTRIG}$ PCG Trigger Hold After Falling Edge of PCG Input Clock                   | 3                                         |                                            | ns   |
| <i>Switching Characteristics</i>                                                     |                                           |                                            |      |
| $t_{DPCGIO}$ PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock | 2                                         | 10                                         | ns   |
| $t_{DTRIGCLK}$ PCG Output Clock Delay After PCG Trigger                              | $2 + (2.5 \times t_{PCGIP})$              | $13.5 + (2.5 \times t_{PCGIP})$            | ns   |
| $t_{DTRIGFS}^1$ PCG Frame Sync Delay After PCG Trigger                               | $2.5 + ((2.5 + D - PH) \times t_{PCGIP})$ | $13.5 + ((2.5 + D - PH) \times t_{PCGIP})$ | ns   |
| $t_{PCGOW}^2$ Output Clock Period                                                    | $2 \times t_{PCGIP} - 1$                  |                                            | ns   |

<sup>1</sup>D = FSxDIV, PH = FSxPHASE. For more information, see the [ADSP-21562/3/5/6/7/9 SHARC+ Processor Hardware Reference](#).

<sup>2</sup>Normal mode of operation.

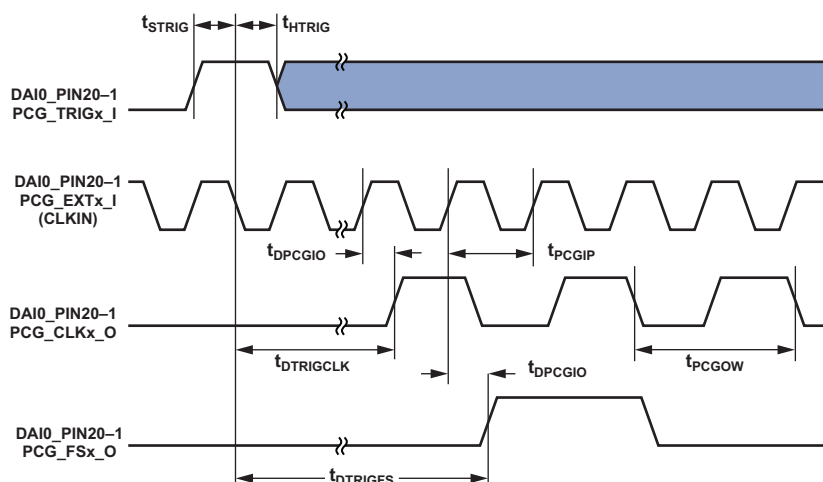


Figure 29. PCG (Direct Pin Routing)

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## General-Purpose IO Port Timing

Table 51 and Figure 30 describe I/O timing, related to the general-purpose ports (PORT).

**Table 51. General-Purpose Port Timing**

| Parameter                                            | Min                        | Max | Unit |
|------------------------------------------------------|----------------------------|-----|------|
| <i>Timing Requirement</i>                            |                            |     |      |
| $t_{WFI}$ General-Purpose Port Pin Input Pulse Width | $2 \times t_{SCLK0} - 1.5$ |     | ns   |

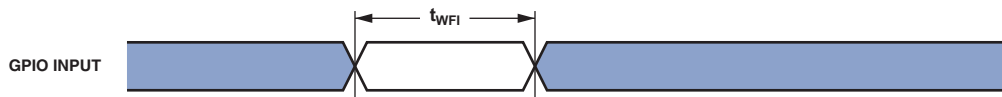


Figure 30. General-Purpose Port Timing

## General-Purpose I/O Timer Cycle Timing

Table 52, Table 53, and Figure 31 describe timer expired operations related to the general-purpose timer (TIMER0). The width value is the timer period assigned in the TMx\_TMRn\_WIDTH register and can range from 1 to  $2^{32} - 1$ . When externally generated, the TMx\_CLK clock is called  $f_{TMRLCKEXT}$ :

$$t_{TMRLCKEXT} = \frac{1}{f_{TMRLCKEXT}}$$

**Table 52. Timer Cycle Timing—Internal Mode**

| Parameter                                                                     | Min                            | Max                            | Unit |
|-------------------------------------------------------------------------------|--------------------------------|--------------------------------|------|
| <i>Timing Requirements</i>                                                    |                                |                                |      |
| $t_{WL}$ Timer Pulse Width Input Low (Measured In SCLK0 Cycles) <sup>1</sup>  | $2 \times t_{SCLK0}$           |                                | ns   |
| $t_{WH}$ Timer Pulse Width Input High (Measured In SCLK0 Cycles) <sup>1</sup> | $2 \times t_{SCLK0}$           |                                | ns   |
| <i>Switching Characteristic</i>                                               |                                |                                |      |
| $t_{HTO}$ Timer Pulse Width Output (Measured In SCLK0 Cycles) <sup>2</sup>    | $t_{SCLK0} \times WIDTH - 1.7$ | $t_{SCLK0} \times WIDTH + 1.5$ | ns   |

<sup>1</sup>The minimum pulse width applies for timer signals in width capture and external clock modes.

<sup>2</sup>WIDTH refers to the value in the TMRx\_WIDTH register (it can vary from 2 to  $2^{32} - 1$ ).

**Table 53. Timer Cycle Timing—External Mode**

| Parameter                                                                       | Min                               | Max                               | Unit |
|---------------------------------------------------------------------------------|-----------------------------------|-----------------------------------|------|
| <i>Timing Requirements</i>                                                      |                                   |                                   |      |
| $t_{WL}$ Timer Pulse Width Input Low (Measured In EXT_CLK Cycles) <sup>1</sup>  | $2 \times t_{EXT\_CLK}$           |                                   | ns   |
| $t_{WH}$ Timer Pulse Width Input High (Measured In EXT_CLK Cycles) <sup>1</sup> | $2 \times t_{EXT\_CLK}$           |                                   | ns   |
| $t_{EXT\_CLK}$ Timer External Clock Period <sup>2</sup>                         | $t_{TMRLCKEXT}$                   |                                   | ns   |
| <i>Switching Characteristic</i>                                                 |                                   |                                   |      |
| $t_{HTO}$ Timer Pulse Width Output (Measured In EXT_CLK Cycles) <sup>3</sup>    | $t_{EXT\_CLK} \times WIDTH - 1.5$ | $t_{EXT\_CLK} \times WIDTH + 1.5$ | ns   |

<sup>1</sup>The minimum pulse width applies for timer signals in width capture and external clock modes.

<sup>2</sup>This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external TMR\_CLK. For the external TMR\_CLK maximum frequency, see the  $f_{TMRLCKEXT}$  specification in Table 19.

<sup>3</sup>WIDTH refers to the value in the TMRx\_WIDTH register (it can vary from 1 to  $2^{32} - 1$ ).

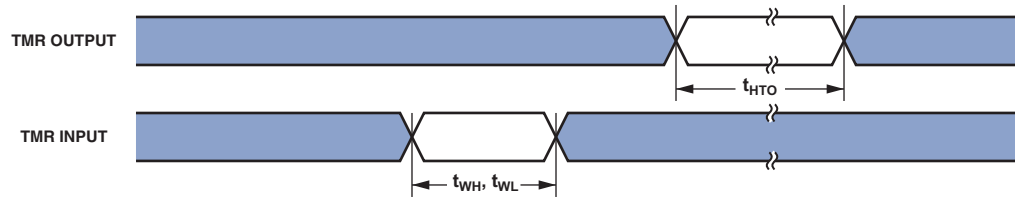


Figure 31. Timer Cycle Timing

## DAIx Pin to DAIx Pin Direct Routing (DAI0 Block and DAI1 Block)

Table 54 and Figure 32 describe I/O timing related to the digital audio interface (DAI) for direct pin connections only (for example, DAIx\_PB01\_I to DAIx\_PB02\_O).

Table 54. DAI Pin to DAI Pin Routing

| Parameter                                                       | Min | Max | Unit |
|-----------------------------------------------------------------|-----|-----|------|
| <i>Switching Characteristic</i>                                 |     |     |      |
| t <sub>DPIO</sub> Delay DAI Pin Input Valid to DAI Output Valid | 1.5 | 12  | ns   |

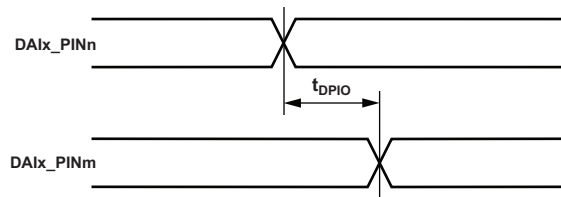


Figure 32. DAI Pin to DAI Pin Direct Routing

## Up/Down Counter/Rotary Encoder Timing

Table 55 and Figure 33 describe timing related to the general-purpose counter (CNT).

Table 55. Up/Down Counter/Rotary Encoder Timing

| Parameter                                                            | Min                    | Max | Unit |
|----------------------------------------------------------------------|------------------------|-----|------|
| <i>Timing Requirement</i>                                            |                        |     |      |
| t <sub>WCOUNT</sub> Up/Down Counter/Rotary Encoder Input Pulse Width | 2 × t <sub>SCLK0</sub> |     | ns   |

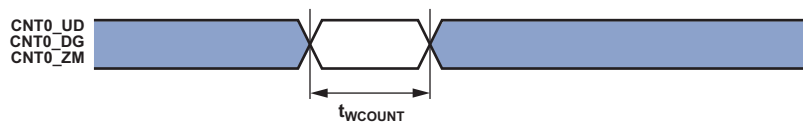


Figure 33. Up/Down Counter/Rotary Encoder Timing

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## Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The UART ports receive and transmit operations are described in the [ADSP-21562/3/5/6/7/9 SHARC+ Processor Hardware Reference](#).

### Sony/Philips Digital Interface (S/PDIF) Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left justified, I<sup>2</sup>S, or right justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

#### S/PDIF Transmitter Serial Input Waveforms

Table 56 and Figure 34 show the right justified mode. Frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of the serial clock. The MSB is delayed the minimum in 24-bit output mode or the maximum in 16-bit output mode from a frame sync transition, so that when there are 64 serial clock periods per frame sync period, the LSB of the data is right justified to the next frame sync transition.

**Table 56. S/PDIF Transmitter Right Justified Mode**

| Parameter                                                 | Conditions       | Nominal | Unit  |
|-----------------------------------------------------------|------------------|---------|-------|
| <i>Timing Requirement</i>                                 |                  |         |       |
| $t_{RJD}$ Frame Sync to MSB Delay in Right Justified Mode | 16-bit word mode | 16      | SCLK0 |
|                                                           | 18-bit word mode | 14      | SCLK0 |
|                                                           | 20-bit word mode | 12      | SCLK0 |
|                                                           | 24-bit word mode | 8       | SCLK0 |

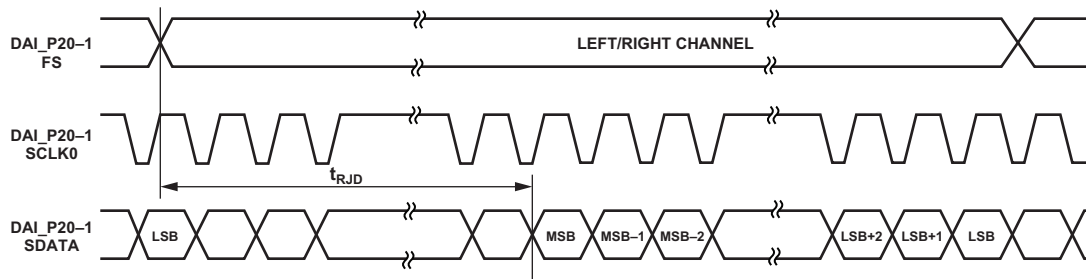


Figure 34. Right Justified Mode

Table 57 and Figure 35 show the default I<sup>2</sup>S justified mode. The frame sync is low for the left channel and high for the right channel. Data is valid on the rising edge of the serial clock. The MSB is left justified to the frame sync transition but with a delay.

**Table 57. S/PDIF Transmitter I<sup>2</sup>S Mode**

| Parameter                                                   | Nominal | Unit  |
|-------------------------------------------------------------|---------|-------|
| Timing Requirement                                          |         |       |
| $t_{I2SD}$ Frame Sync to MSB Delay in I <sup>2</sup> S Mode | 1       | SCLK0 |

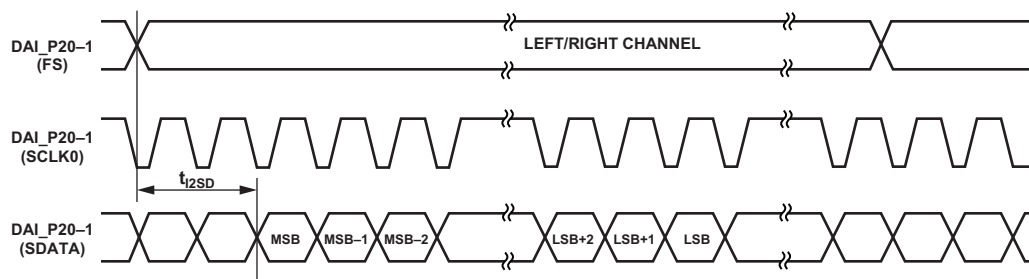


Figure 35. I<sup>2</sup>S Justified Mode

Table 58 and Figure 36 show the left justified mode. The frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of the serial clock. The MSB is left justified to the frame sync transition with no delay.

**Table 58. S/PDIF Transmitter Left Justified Mode**

| Parameter                                                | Nominal | Unit  |
|----------------------------------------------------------|---------|-------|
| Timing Requirement                                       |         |       |
| $t_{LJD}$ Frame Sync to MSB Delay in Left Justified Mode | 0       | SCLK0 |

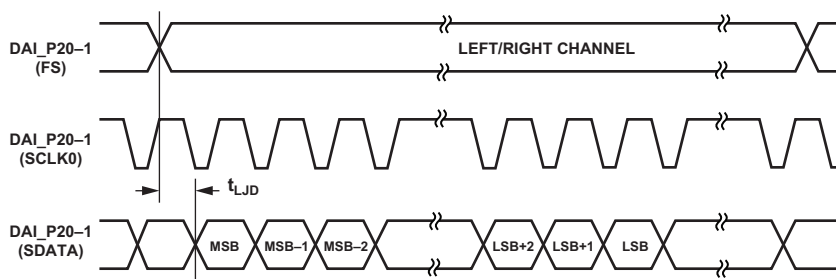


Figure 36. Left Justified Mode

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## S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 59. Input signals are routed to the DAI0\_PINx pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI0\_PINx pins.

**Table 59. S/PDIF Transmitter Input Data Timing**

| Parameter                                                      | Min | Max | Unit |
|----------------------------------------------------------------|-----|-----|------|
| <i>Timing Requirements</i>                                     |     |     |      |
| $t_{SISFS}^1$ Frame Sync Setup Before Serial Clock Rising Edge | 3.4 |     | ns   |
| $t_{SIHFS}^1$ Frame Sync Hold After Serial Clock Rising Edge   | 3   |     | ns   |
| $t_{SISD}^1$ Data Setup Before Serial Clock Rising Edge        | 3   |     | ns   |
| $t_{SIHD}^1$ Data Hold After Serial Clock Rising Edge          | 3   |     | ns   |
| $t_{SITXCLKW}$ Transmit Clock Width                            | 9   |     | ns   |
| $t_{SITXCLK}$ Transmit Clock Period                            | 20  |     | ns   |
| $t_{SISCLKW}$ Clock Width                                      | 36  |     | ns   |
| $t_{SISCLK}$ Clock Period                                      | 80  |     | ns   |

<sup>1</sup>The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The input of the PCG can be either CLKIN or any of the DAI pins.

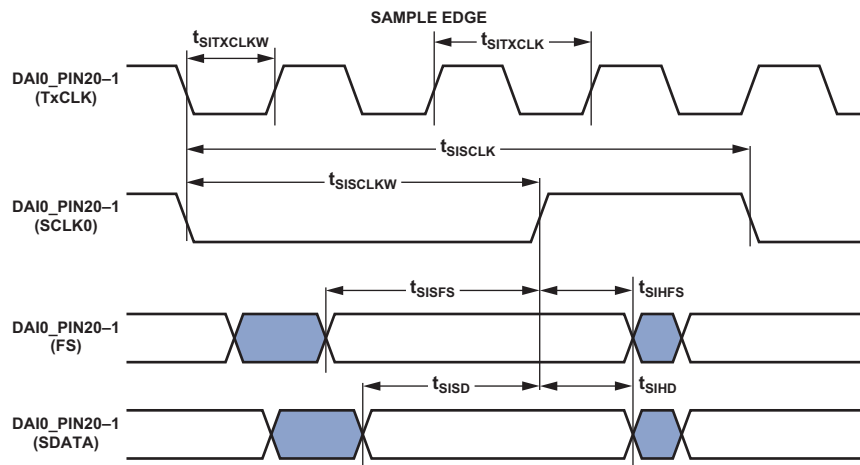


Figure 37. S/PDIF Transmitter Input Timing

## Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter requires an oversampling clock input. This high frequency clock (TxCLK) input is divided down to generate the internal biphase clock.

**Table 60. Oversampling Clock (TxCLK) Switching Characteristics**

| Parameter                                               | Max                                                  | Unit |
|---------------------------------------------------------|------------------------------------------------------|------|
| <i>Switching Characteristics</i>                        |                                                      |      |
| $f_{TXCLK\_384}$ Frequency for TxCLK = 384 × Frame Sync | Oversampling ratio × frame sync $\leq 1/t_{SITXCLK}$ | MHz  |
| $f_{TXCLK\_256}$ Frequency for TxCLK = 256 × Frame Sync | 49.2                                                 | MHz  |
| $f_{FS}$ Frame Rate (FS)                                | 192.0                                                | kHz  |

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital PLL mode, the internal digital PLL generates the  $512 \times \text{FS}$  clock.

Table 61. S/PDIF Receiver Internal Digital PLL Mode Timing

| Parameter                        |                                        | Min | Max | Unit |
|----------------------------------|----------------------------------------|-----|-----|------|
| <i>Switching Characteristics</i> |                                        |     |     |      |
| $t_{\text{DFSI}}$                | Frame Sync Delay After Serial Clock    |     | 5   | ns   |
| $t_{\text{HOFSI}}$               | Frame Sync Hold After Serial Clock     | -2  |     | ns   |
| $t_{\text{DDTI}}$                | Transmit Data Delay After Serial Clock |     | 5   | ns   |
| $t_{\text{HDTI}}$                | Transmit Data Hold After Serial Clock  | -2  |     | ns   |

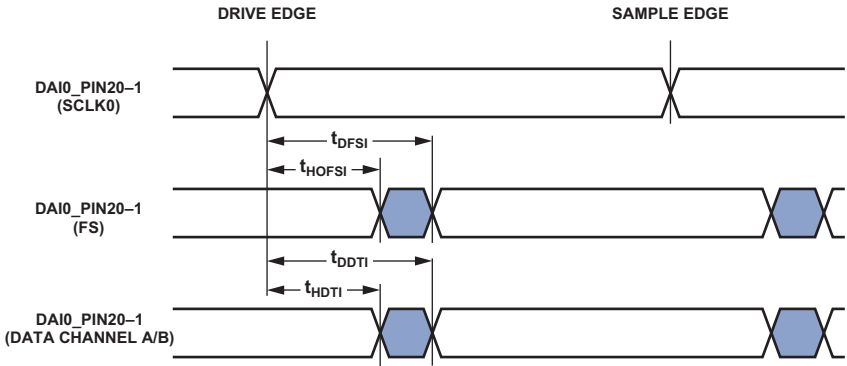


Figure 38. S/PDIF Receiver Internal Digital PLL Mode Timing

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## MediaLB (MLB)

All the numbers shown in [Table 62](#) are applicable for all MLB speed modes (1024 FS, 512 FS, and 256 FS) for the 3-pin protocol, unless otherwise specified. Refer to the *Media Local Bus Specification Version 4.2* for more details.

**Table 62. 3-Pin MLB Interface Specifications**

| Parameter                                                     | Min | Typ  | Max | Unit |
|---------------------------------------------------------------|-----|------|-----|------|
| $t_{MLBCLK}$ MLB Clock Period                                 |     |      |     |      |
| 1024 FS                                                       |     | 20.3 |     | ns   |
| 512 FS                                                        |     | 40   |     | ns   |
| 256 FS                                                        |     | 81   |     | ns   |
| $t_{MCKL}$ MLBCLK Low Time                                    |     |      |     |      |
| 1024 FS                                                       | 6.1 |      |     | ns   |
| 512 FS                                                        | 14  |      |     | ns   |
| 256 FS                                                        | 30  |      |     | ns   |
| $t_{MCKH}$ MLBCLK High Time                                   |     |      |     |      |
| 1024 FS                                                       | 9.3 |      |     | ns   |
| 512 FS                                                        | 14  |      |     | ns   |
| 256 FS                                                        | 30  |      |     | ns   |
| $t_{MCKR}$ MLBCLK Rise Time ( $V_{IL}$ to $V_{IH}$ )          |     |      |     |      |
| 1024 FS                                                       |     |      | 1   | ns   |
| 512 FS/256 FS                                                 |     |      | 3   | ns   |
| $t_{MCKF}$ MLBCLK Fall Time ( $V_{IH}$ to $V_{IL}$ )          |     |      |     |      |
| 1024 FS                                                       |     |      | 1   | ns   |
| 512 FS/256 FS                                                 |     |      | 3   | ns   |
| $t_{MPWV}^1$ MLBCLK Pulse Width Variation                     |     |      |     |      |
| 1024 FS                                                       |     |      | 0.7 | nspp |
| 512 FS/256                                                    |     |      | 2.0 | nspp |
| $t_{DSMCF}$ DAT/SIG Input Setup Time                          | 1   |      |     | ns   |
| $t_{DHMCF}$ DAT/SIG Input Hold Time                           | 2   |      |     | ns   |
| $t_{MCFDZ}$ DAT/SIG Output Time to Three-State                | 0   |      | 15  | ns   |
| $t_{MCDRV}$ DAT/SIG Output Data Delay From MLBCLK Rising Edge |     |      | 8   | ns   |
| $t_{MDZH}^2$ Bus Hold Time                                    |     |      |     |      |
| 1024 FS                                                       | 2   |      |     | ns   |
| 512 FS/256                                                    | 4   |      |     | ns   |
| $C_{MLB}$ DAT/SIG Pin Load                                    |     |      |     |      |
| 1024 FS                                                       |     |      | 40  | pf   |
| 512 FS/256                                                    |     |      | 60  | pf   |

<sup>1</sup> Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in nanoseconds peak-to-peak.

<sup>2</sup> Board designs must ensure the high impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

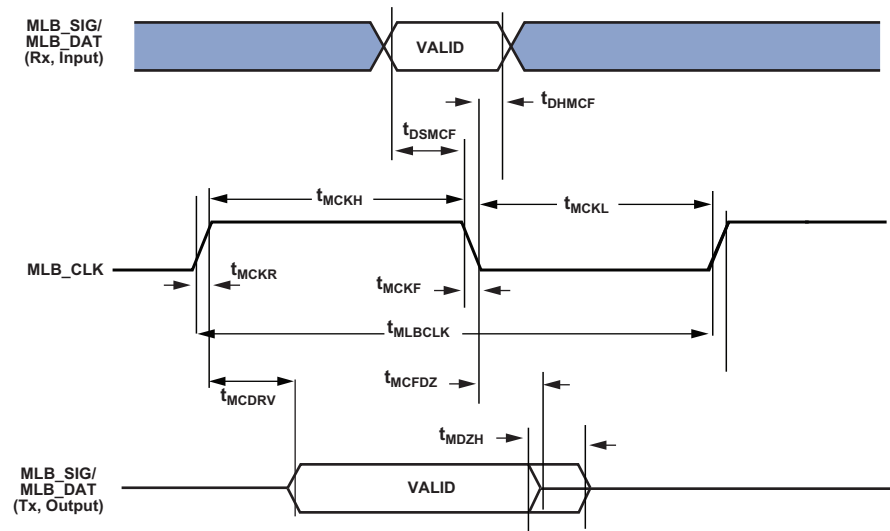


Figure 39. MLB Timing (3-Pin Interface)

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## Program Trace Macrocell (PTM) Timing

Table 63 and Figure 40 provide I/O timing related to the PTM.

Table 63. TRACE0 Timing

| Parameter                        |                                            | Min                        | Max                        | Unit |
|----------------------------------|--------------------------------------------|----------------------------|----------------------------|------|
| <i>Switching Characteristics</i> |                                            |                            |                            |      |
| $t_{DTRD}$                       | TRACE0 Data Delay From Trace Clock Maximum |                            | $0.5 \times t_{SCLK0} + 3$ | ns   |
| $t_{HTRD}$                       | TRACE0 Data Hold From Trace Clock Minimum  | $0.5 \times t_{SCLK0} - 2$ |                            | ns   |
| $t_{PTRCK}$                      | TRACE0 Clock Period Minimum                | $2 \times t_{SCLK0} - 1$   |                            | ns   |

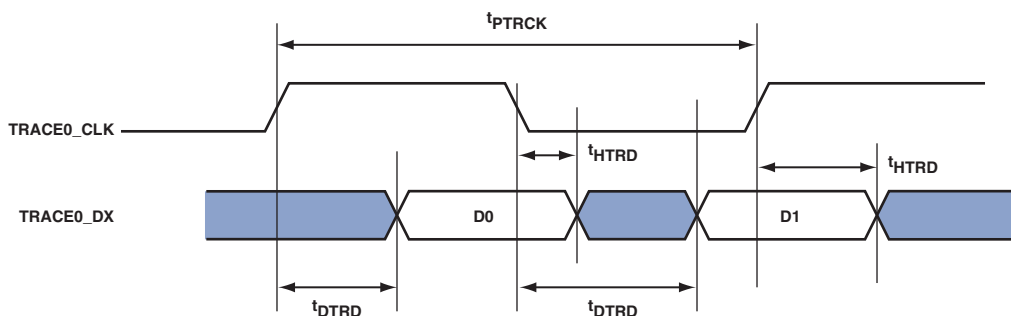


Figure 40. Trace Timing

## Debug Interface (JTAG Emulation Port) Timing

Table 64 and Figure 41 provide I/O timing related to the debug interface (JTAG emulator port).

**Table 64. JTAG Emulation Port Timing**

| Parameter                        |                                                                | Min | Max | Unit     |
|----------------------------------|----------------------------------------------------------------|-----|-----|----------|
| <i>Timing Requirements</i>       |                                                                |     |     |          |
| $t_{TCK}$                        | JTG_TCK Period                                                 | 20  |     | ns       |
| $t_{STAP}$                       | JTG_TDI, JTG_TMS Setup Before JTG_TCK High                     | 4   |     | ns       |
| $t_{HTAP}$                       | JTG_TDI, JTG_TMS Hold After JTG_TCK High                       | 4   |     | ns       |
| $t_{SSYS}$                       | System Inputs Setup Before JTG_TCK High <sup>1</sup>           | 4   |     | ns       |
| $t_{HSYS}$                       | System Inputs Hold After JTG_TCK High <sup>1</sup>             | 4   |     | ns       |
| $t_{TRSTW}$                      | JTG_TRST Pulse Width (Measured in JTG_TCK Cycles) <sup>2</sup> | 4   |     | $T_{CK}$ |
| <i>Switching Characteristics</i> |                                                                |     |     |          |
| $t_{DTDO}$                       | JTG_TDO Delay From JTG_TCK Low                                 |     | 12  | ns       |
| $t_{DSYS}$                       | System Outputs Delay After JTG_TCK Low <sup>3</sup>            |     | 17  | ns       |

<sup>1</sup>System Inputs = DAI0\_PIN20-19, DAI0\_PIN12-1, DAI1\_PIN20-19, DAI1\_PIN12-1, DMC0\_A15-0, DMC0\_DQ15-0,  $\overline{DMC0\_RESET}$ , PA\_15-0, PB\_15-0, PC\_7-0, SYS\_BMODE2-0, SYS\_FAULT.

<sup>2</sup>50 MHz maximum.

<sup>3</sup>System Outputs = DMC0\_A15-0, DMC0\_BA2-0,  $\overline{DMC0\_CAS}$ , DMC0\_CK, DMC0\_CKE,  $\overline{DMC0\_CS0}$ , DMC0\_DQ15-0, DMC0\_LDM, DMC0\_LDQS, DMC0\_ODT,  $\overline{DMC0\_RAS}$ ,  $\overline{DMC0\_RESET}$ , DMC0\_UDM, DMC0\_UDQS,  $\overline{DMC0\_WE}$ , PA\_15-0, PB\_15-0, PC\_7-0, SYS\_CLKOUT, SYS\_FAULT, SYS\_RESOUT.

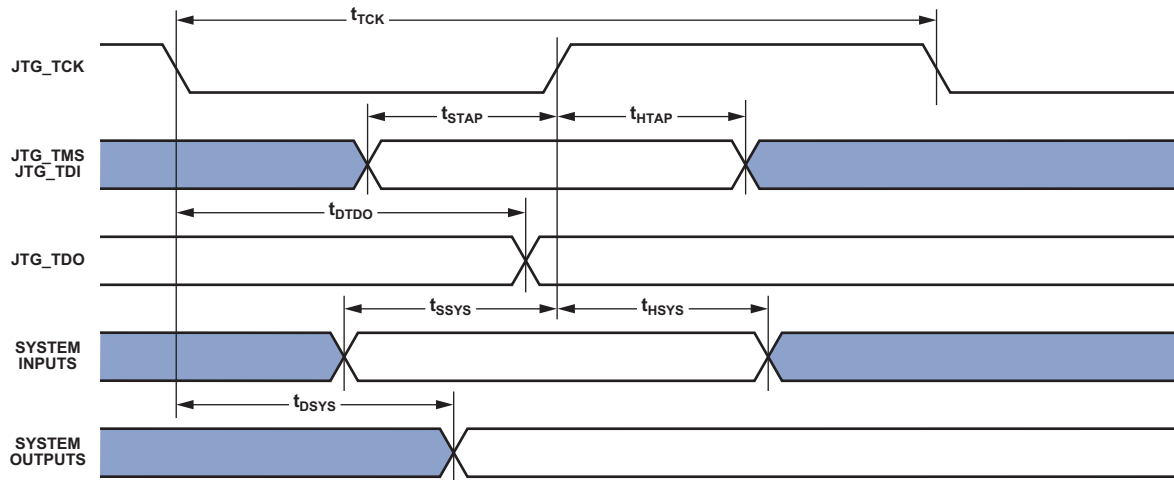


Figure 41. JTAG Port Timing

# ADSP-21562/21563/21565/21566/21567/21569

## OUTPUT DRIVE CURRENTS

Figure 42 through Figure 47 show typical current voltage characteristics for the output drivers of the ADSP-2156x processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

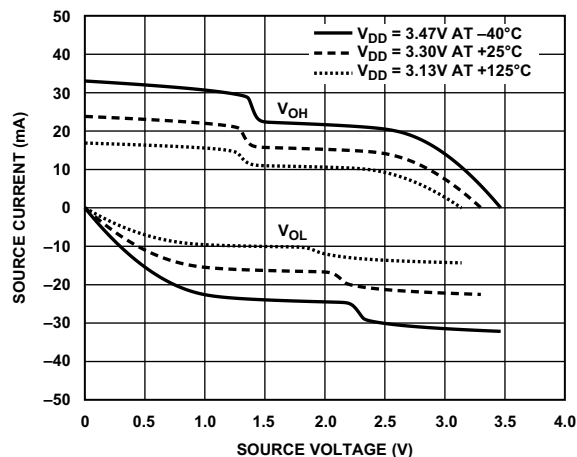


Figure 42. Driver Type A Current for All Pins Operating at Less Than or Equal to 62.5 MHz (3.3 V  $V_{DD\_EXT}$ )

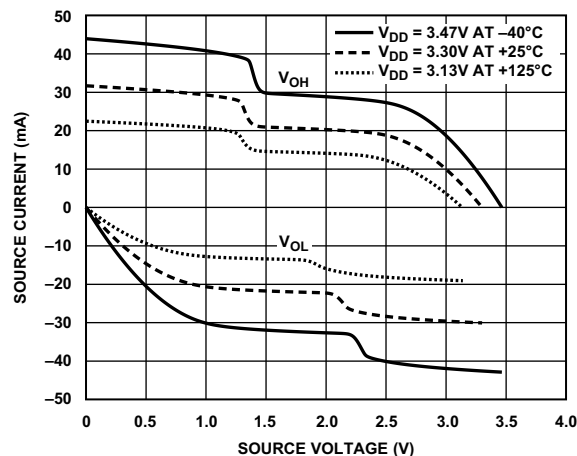


Figure 43. Driver Type A Current for All Pins Operating Above 62.5 MHz and Less Than or Equal to 125 MHz (3.3 V  $V_{DD\_EXT}$ )

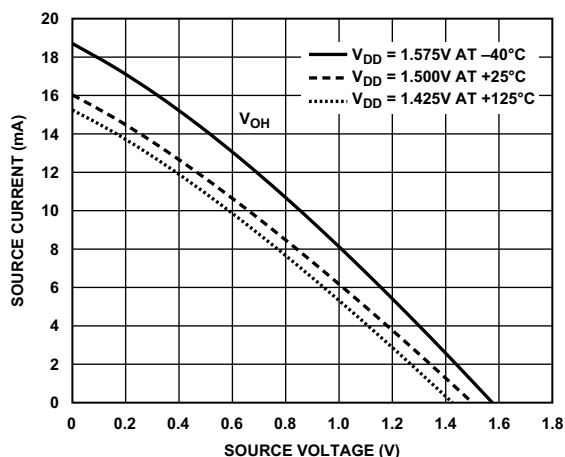


Figure 44. Driver Type B and Driver Type C (DDR3 Drive Strength 100  $\Omega$ )

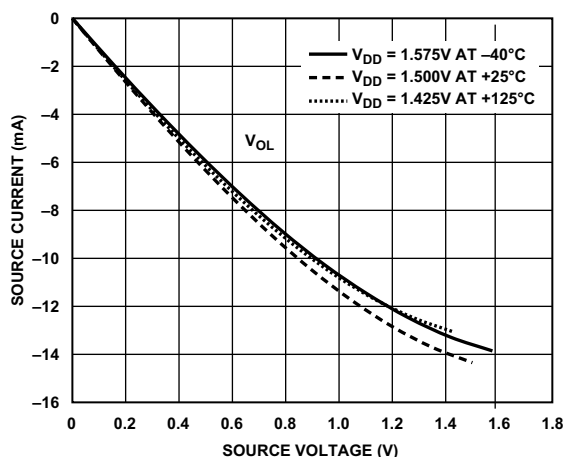


Figure 45. Driver Type B and Driver Type C (DDR3 Drive Strength 100  $\Omega$ )

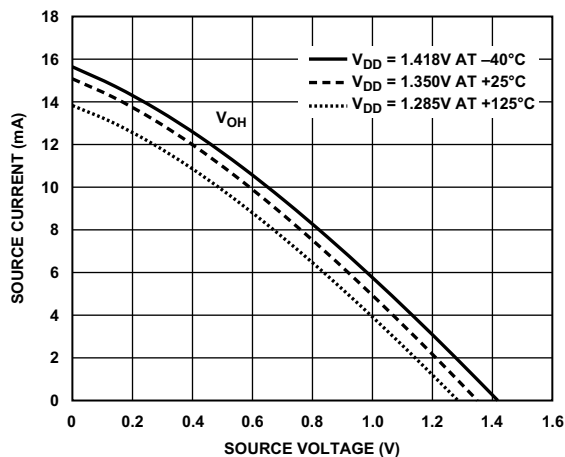


Figure 46. Driver Type B and Driver Type C (DDR3L Drive Strength 100  $\Omega$ )

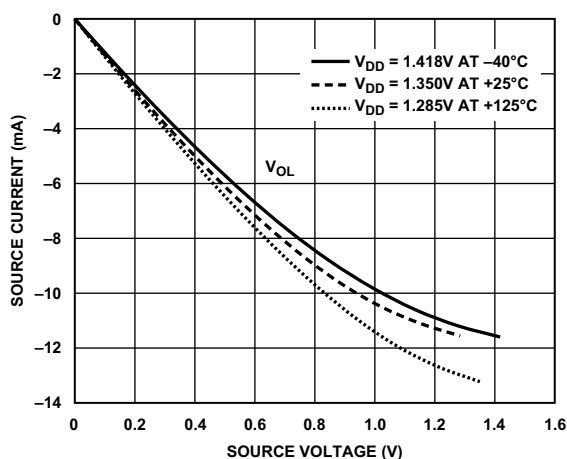


Figure 47. Driver Type B and Driver Type C (DDR3L Drive Strength 100  $\Omega$ )

## TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 48 shows the measurement point for ac measurements (except output enable/disable). The measurement point,  $V_{MEAS}$ , is  $V_{DD\_EXT}/2$  for  $V_{DD\_EXT}$  (nominal) = 3.3 V.

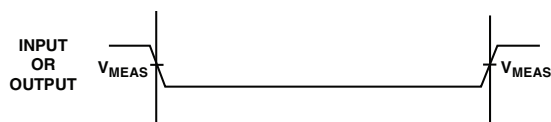


Figure 48. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

## Output Enable Time Measurement

Output pins are considered enabled when they make a transition from a high impedance state to the point when they start driving.

The output enable time,  $t_{ENA}$ , is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving, as shown on the right side of Figure 49. If multiple pins are enabled, the measurement value is that of the first pin to start driving.

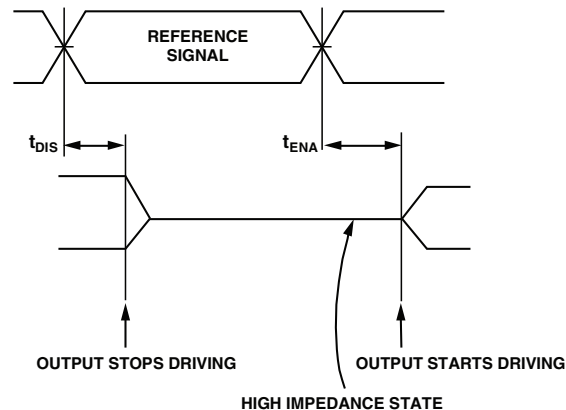


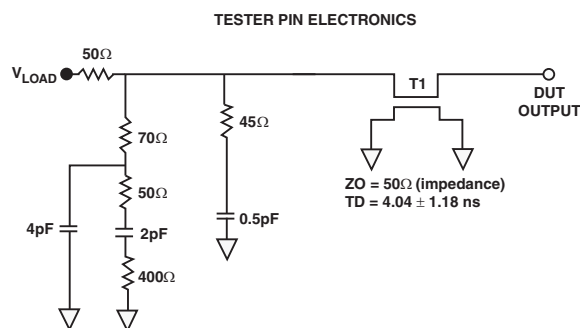
Figure 49. Output Enable/Disable

## Output Disable Time Measurement

Output pins are considered disabled when they stop driving, enter a high impedance state, and start to decay from the output high or low voltage. The output disable time,  $t_{DIS}$ , is the interval from when a reference signal reaches a high or low voltage level to the point when the output stops driving, as shown on the left side of Figure 49).

## Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 50).  $V_{LOAD}$  is equal to  $V_{DD\_EXT}/2$ . Figure 51 through Figure 54 show how output rise time varies with capacitance. The delay and hold specifications given must be derated by a factor derived from these figures. The graphs in Figure 51 through Figure 54 cannot be linear outside the ranges shown.



NOTES:  
THE WORST-CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFLECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, THE SYSTEM CAN INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 50. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

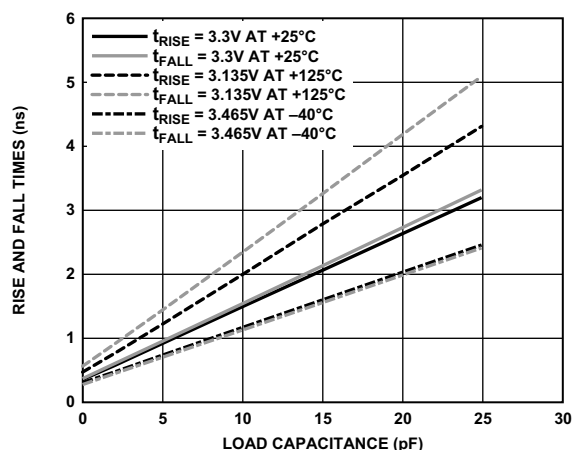


Figure 51. Driver Type A Rise and Fall Times (10% to 90%) vs. Load Capacitance for All Pins Operating Above 62.5 MHz and Less Than or Equal to 125 MHz

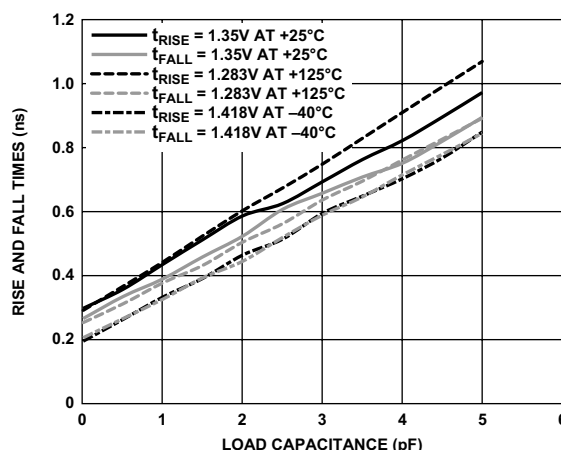


Figure 54. Driver Type B and Driver Type C Rise and Fall Times (10% to 90%) vs. Load Capacitance for DDR3L at 100 Ω

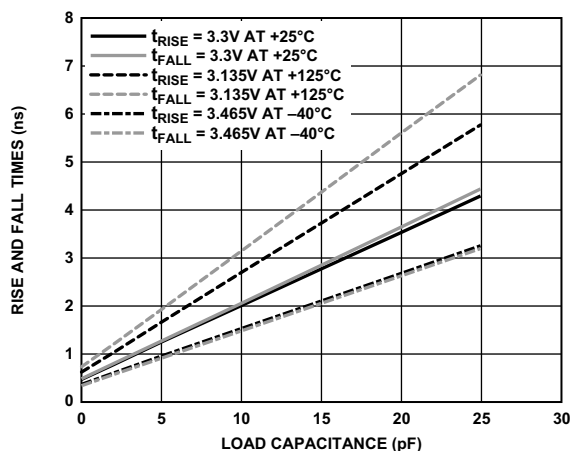


Figure 52. Driver Type A Rise and Fall Times (10% to 90%) vs. Load Capacitance for All Pins Operating at Less Than or Equal to 62.5 MHz

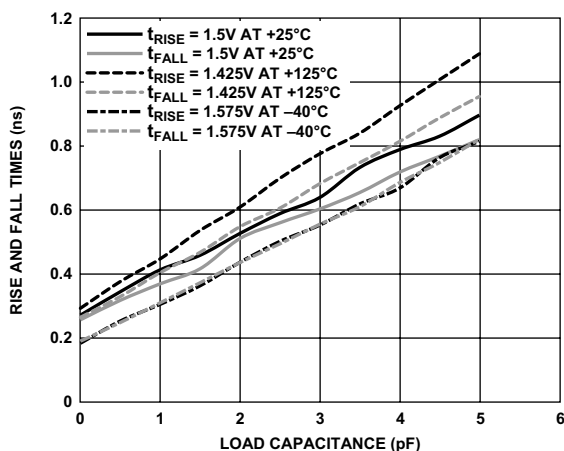


Figure 53. Driver Type B and Driver Type C Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for DDR3 at 100 Ω

## ENVIRONMENTAL CONDITIONS

The ADSP-2156x processors are rated for performance over the temperature range specified in [Operating Conditions](#).

Application system thermal simulation is required for accurate temperature analysis. The thermal simulation must account for all specific 3D system design features, including, but not limited to other heat sources, use of heat sinks, use of thermal interface materials, and the system enclosure details. Thermal models of the package are available from Analog Devices under the [Tools and Simulations](#) tab of the product web page. The thermal model(s) are compatible with all major thermal simulation tools.

The use of JEDEC  $\theta_{JA}$ ,  $\theta_{JC}$ , or  $\Psi_{JT}$  thermal parameters for application system thermal estimates is not recommended as indicated in the JEDEC51 specifications:

“This methodology is not meant to and will not predict the performance of a package in an application-specific environment.”

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## ADSP-2156x 400-BALL BGA BALL ASSIGNMENTS

The ADSP-2156x 400-Ball BGA Ball Assignments (Numerical by Ball Number) table lists the 400-ball BGA package by ball number.

The ADSP-2156x 400-Ball BGA Ball Assignments (Alphabetical by Pin Name) table lists the 400-ball BGA package by pin name.

### ADSP-2156x 400-BALL BGA BALL ASSIGNMENTS (NUMERICAL BY BALL NUMBER)

| Ball No. | Pin Name          | Ball No. | Pin Name          | Ball No. | Pin Name         | Ball No. | Pin Name  |
|----------|-------------------|----------|-------------------|----------|------------------|----------|-----------|
| A01      | GND               | C01      | DMC0_LDM          | E01      | DMC0_DQ05        | G01      | DMC0_DQ04 |
| A02      | DMC0_DQ11         | C02      | DMC0_DQ08         | E02      | DMC0_DQ06        | G02      | DMC0_DQ02 |
| A03      | DMC0_DQ10         | C03      | GND               | E03      | GND              | G03      | GND       |
| A04      | <u>DMC0_UDQ5</u>  | C04      | GND               | E04      | VDD_INT          | G04      | VDD_INT   |
| A05      | DMC0_DQ15         | C05      | GND               | E05      | VDD_INT          | G05      | VDD_INT   |
| A06      | DMC0_UDM          | C06      | GND               | E06      | VDD_INT          | G06      | VDD_DMC   |
| A07      | PB_00             | C07      | PB_03             | E07      | VDD_INT          | G07      | VDD_DMC   |
| A08      | SYS_BMODE2        | C08      | PB_05             | E08      | VDD_INT          | G08      | VDD_DMC   |
| A09      | <u>SYS_HWRST</u>  | C09      | PB_01             | E09      | VDD_INT          | G09      | VDD_DMC   |
| A10      | <u>JTG_TRST</u>   | C10      | <u>SYS_RESOUT</u> | E10      | VDD_INT          | G10      | VDD_REF   |
| A11      | <u>SYS_FAULT</u>  | C11      | JTG_TDO           | E11      | VDD_INT          | G11      | VDD_REF   |
| A12      | <u>DMC0_WE</u>    | C12      | JTG_TMS           | E12      | VDD_INT          | G12      | VDD_DMC   |
| A13      | DMC0_A14          | C13      | JTG_TDI           | E13      | VDD_INT          | G13      | VDD_DMC   |
| A14      | DMC0_A13          | C14      | GND               | E14      | VDD_INT          | G14      | VDD_DMC   |
| A15      | DMC0_A10          | C15      | GND               | E15      | VDD_INT          | G15      | VDD_DMC   |
| A16      | DMC0_A08          | C16      | GND               | E16      | VDD_INT          | G16      | VDD_INT   |
| A17      | DMC0_BA1          | C17      | GND               | E17      | VDD_INT          | G17      | VDD_INT   |
| A18      | DMC0_A07          | C18      | GND               | E18      | GND              | G18      | GND       |
| A19      | DMC0_A04          | C19      | DMC0_A03          | E19      | DMC0_BA2         | G19      | DMC0_RZQ  |
| A20      | GND               | C20      | DMC0_A02          | E20      | <u>DMC0_CAS</u>  | G20      | DMC0_VREF |
| B01      | GND               | D01      | DMC0_DQ07         | F01      | <u>DMC0_LDQS</u> | H01      | DMC0_DQ03 |
| B02      | GND               | D02      | GND               | F02      | DMC0_LDQS        | H02      | GND       |
| B03      | DMC0_DQ12         | D03      | DMC0_DQ09         | F03      | GND              | H03      | GND       |
| B04      | DMC0_UDQ5         | D04      | GND               | F04      | VDD_INT          | H04      | VDD_INT   |
| B05      | DMC0_DQ14         | D05      | GND               | F05      | VDD_INT          | H05      | VDD_INT   |
| B06      | DMC0_DQ13         | D06      | GND               | F06      | VDD_DMC          | H06      | VDD_DMC   |
| B07      | PB_04             | D07      | GND               | F07      | VDD_DMC          | H07      | VDD_DMC   |
| B08      | PB_02             | D08      | VDD_EXT           | F08      | VDD_DMC          | H08      | GND       |
| B09      | SYS_BMODE1        | D09      | VDD_EXT           | F09      | VDD_DMC          | H09      | GND       |
| B10      | SYS_BMODE0        | D10      | VDD_EXT           | F10      | VDD_DMC          | H10      | GND       |
| B11      | JTG_TCK           | D11      | VDD_EXT           | F11      | VDD_DMC          | H11      | GND       |
| B12      | <u>DMC0_RESET</u> | D12      | GND               | F12      | VDD_DMC          | H12      | GND       |
| B13      | DMC0_A15          | D13      | GND               | F13      | VDD_DMC          | H13      | GND       |
| B14      | DMC0_A12          | D14      | GND               | F14      | VDD_DMC          | H14      | VDD_DMC   |
| B15      | DMC0_A11          | D15      | GND               | F15      | VDD_DMC          | H15      | VDD_DMC   |
| B16      | DMC0_A09          | D16      | GND               | F16      | VDD_INT          | H16      | VDD_INT   |
| B17      | DMC0_BA0          | D17      | GND               | F17      | VDD_INT          | H17      | VDD_INT   |
| B18      | DMC0_A06          | D18      | GND               | F18      | GND              | H18      | GND       |
| B19      | GND               | D19      | DMC0_A00          | F19      | <u>DMC0_RAS</u>  | H19      | DMC0_ODT  |
| B20      | DMC0_A05          | D20      | DMC0_A01          | F20      | <u>DMC0_CS0</u>  | H20      | DMC0_CKE  |

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| Ball No. | Pin Name  | Ball No. | Pin Name    | Ball No. | Pin Name   | Ball No. | Pin Name   |
|----------|-----------|----------|-------------|----------|------------|----------|------------|
| J01      | DMC0_DQ01 | L09      | GND         | N17      | GND        | T05      | VDD_EXT    |
| J02      | DMC0_DQ00 | L10      | GND         | N18      | GND        | T06      | VDD_REF    |
| J03      | GND       | L11      | GND         | N19      | HADC0_VIN0 | T07      | VDD_REF    |
| J04      | DMC0_VREF | L12      | GND         | N20      | HADC0_VIN1 | T08      | VDD_REF    |
| J05      | VDD_INT   | L13      | GND         | P01      | GND        | T09      | VDD_REF    |
| J06      | VDD_DMC   | L14      | VDD_INT     | P02      | PA_02      | T10      | VDD_REF    |
| J07      | VDD_DMC   | L15      | VDD_INT     | P03      | PA_01      | T11      | VDD_REF    |
| J08      | GND       | L16      | GND         | P04      | VDD_EXT    | T12      | VDD_REF    |
| J09      | GND       | L17      | GND         | P05      | VDD_REF    | T13      | VDD_REF    |
| J10      | GND       | L18      | HADC0_VREFN | P06      | VDD_INT    | T14      | VDD_REF    |
| J11      | GND       | L19      | VDD_ANA     | P07      | VDD_INT    | T15      | VDD_REF    |
| J12      | GND       | L20      | HADC0_VREFP | P08      | VDD_INT    | T16      | VDD_EXT    |
| J13      | GND       | M01      | GND         | P09      | VDD_INT    | T17      | GND        |
| J14      | VDD_INT   | M02      | GND         | P10      | VDD_INT    | T18      | DAI1_PIN09 |
| J15      | VDD_INT   | M03      | SYS_CLKOUT  | P11      | VDD_INT    | T19      | DAI1_PIN06 |
| J16      | VDD_INT   | M04      | VDD_EXT     | P12      | VDD_INT    | T20      | DAI1_PIN04 |
| J17      | VDD_INT   | M05      | VDD_INT     | P13      | VDD_INT    | U01      | GND        |
| J18      | GND       | M06      | VDD_INT     | P14      | VDD_INT    | U02      | PA_10      |
| J19      | DMC0_CK   | M07      | VDD_INT     | P15      | VDD_REF    | U03      | PA_08      |
| J20      | DMC0_CK   | M08      | GND         | P16      | VDD_EXT    | U04      | GND        |
| K01      | GND       | M09      | GND         | P17      | GND        | U05      | GND        |
| K02      | GND       | M10      | GND         | P18      | DAI1_PIN02 | U06      | VDD_EXT    |
| K03      | GND       | M11      | GND         | P19      | GND        | U07      | VDD_EXT    |
| K04      | VDD_EXT   | M12      | GND         | P20      | GND        | U08      | VDD_EXT    |
| K05      | VDD_INT   | M13      | GND         | R01      | PA_04      | U09      | VDD_EXT    |
| K06      | VDD_INT   | M14      | VDD_INT     | R02      | GND        | U10      | VDD_EXT    |
| K07      | VDD_DMC   | M15      | VDD_REF     | R03      | PA_03      | U11      | VDD_EXT    |
| K08      | GND       | M16      | VDD_EXT     | R04      | VDD_EXT    | U12      | VDD_EXT    |
| K09      | GND       | M17      | GND         | R05      | VDD_REF    | U13      | VDD_EXT    |
| K10      | GND       | M18      | GND         | R06      | VDD_INT    | U14      | VDD_EXT    |
| K11      | GND       | M19      | HADC0_VIN2  | R07      | VDD_INT    | U15      | VDD_EXT    |
| K12      | GND       | M20      | HADC0_VIN3  | R08      | VDD_INT    | U16      | GND        |
| K13      | GND       | N01      | SYS_CLKIN0  | R09      | VDD_INT    | U17      | GND        |
| K14      | VDD_INT   | N02      | GND         | R10      | VDD_INT    | U18      | DAI1_PIN10 |
| K15      | VDD_INT   | N03      | PA_00       | R11      | VDD_INT    | U19      | DAI1_PIN07 |
| K16      | VDD_INT   | N04      | VDD_EXT     | R12      | VDD_INT    | U20      | DAI1_PIN05 |
| K17      | GND       | N05      | VDD_REF     | R13      | VDD_INT    | V01      | PA_07      |
| K18      | GND       | N06      | VDD_INT     | R14      | VDD_INT    | V02      | PA_09      |
| K19      | GND       | N07      | VDD_INT     | R15      | VDD_REF    | V03      | GND        |
| K20      | GND       | N08      | GND         | R16      | VDD_EXT    | V04      | GND        |
| L01      | SYS_XTAL0 | N09      | GND         | R17      | GND        | V05      | PB_06      |
| L02      | GND       | N10      | GND         | R18      | DAI1_PIN03 | V06      | PB_09      |
| L03      | GND       | N11      | GND         | R19      | DAI1_PIN08 | V07      | PB_12      |
| L04      | VDD_EXT   | N12      | GND         | R20      | DAI1_PIN01 | V08      | PA_11      |
| L05      | VDD_INT   | N13      | GND         | T01      | GND        | V09      | DAI0_PIN02 |
| L06      | VDD_INT   | N14      | VDD_INT     | T02      | PA_05      | V10      | DAI0_PIN06 |
| L07      | VDD_INT   | N15      | VDD_REF     | T03      | PA_06      | V11      | DAI0_PIN09 |
| L08      | GND       | N16      | VDD_EXT     | T04      | GND        | V12      | DAI0_PIN20 |

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| Ball No. | Pin Name   |
|----------|------------|
| V13      | PC_00      |
| V14      | PC_05      |
| V15      | GND        |
| V16      | GND        |
| V17      | DAI1_PIN19 |
| V18      | GND        |
| V19      | DAI1_PIN11 |
| V20      | DAI1_PIN12 |
| W01      | GND        |
| W02      | GND        |
| W03      | PB_08      |
| W04      | PB_07      |
| W05      | PB_13      |
| W06      | PA_12      |
| W07      | PA_14      |
| W08      | PA_15      |
| W09      | DAI0_PIN03 |
| W10      | DAI0_PIN05 |
| W11      | DAI0_PIN08 |
| W12      | DAI0_PIN12 |
| W13      | DAI0_PIN19 |
| W14      | PB_15      |
| W15      | PC_01      |
| W16      | PC_03      |
| W17      | PC_06      |
| W18      | DAI1_PIN20 |
| W19      | GND        |
| W20      | GND        |
| Y01      | GND        |
| Y02      | GND        |
| Y03      | PB_10      |
| Y04      | PB_11      |
| Y05      | GND        |
| Y06      | PA_13      |
| Y07      | GND        |
| Y08      | DAI0_PIN01 |
| Y09      | DAI0_PIN04 |
| Y10      | DAI0_PIN07 |
| Y11      | DAI0_PIN10 |
| Y12      | DAI0_PIN11 |
| Y13      | GND        |
| Y14      | PB_14      |
| Y15      | PC_02      |
| Y16      | GND        |
| Y17      | PC_04      |
| Y18      | PC_07      |
| Y19      | GND        |
| Y20      | GND        |

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## ADSP-2156x 400-BALL BGA BALL ASSIGNMENTS (ALPHABETICAL BY PIN NAME)

| Pin Name   | Ball No. | Pin Name   | Ball No. | Pin Name | Ball No. | Pin Name | Ball No. |
|------------|----------|------------|----------|----------|----------|----------|----------|
| DAI0_PIN01 | Y08      | DMC0_BA2   | E19      | GND      | C16      | GND      | K13      |
| DAI0_PIN02 | V09      | DMC0_CAS   | E20      | GND      | C17      | GND      | K17      |
| DAI0_PIN03 | W09      | DMC0_CK    | J19      | GND      | C18      | GND      | K18      |
| DAI0_PIN04 | Y09      | DMC0_CK    | J20      | GND      | D02      | GND      | K19      |
| DAI0_PIN05 | W10      | DMC0_CKE   | H20      | GND      | D04      | GND      | K20      |
| DAI0_PIN06 | V10      | DMC0_CS0   | F20      | GND      | D05      | GND      | L02      |
| DAI0_PIN07 | Y10      | DMC0_DQ00  | J02      | GND      | D06      | GND      | L03      |
| DAI0_PIN08 | W11      | DMC0_DQ01  | J01      | GND      | D07      | GND      | L08      |
| DAI0_PIN09 | V11      | DMC0_DQ02  | G02      | GND      | D12      | GND      | L09      |
| DAI0_PIN10 | Y11      | DMC0_DQ03  | H01      | GND      | D13      | GND      | L10      |
| DAI0_PIN11 | Y12      | DMC0_DQ04  | G01      | GND      | D14      | GND      | L11      |
| DAI0_PIN12 | W12      | DMC0_DQ05  | E01      | GND      | D15      | GND      | L12      |
| DAI0_PIN19 | W13      | DMC0_DQ06  | E02      | GND      | D16      | GND      | L13      |
| DAI0_PIN20 | V12      | DMC0_DQ07  | D01      | GND      | D17      | GND      | L16      |
| DAI1_PIN01 | R20      | DMC0_DQ08  | C02      | GND      | D18      | GND      | L17      |
| DAI1_PIN02 | P18      | DMC0_DQ09  | D03      | GND      | E03      | GND      | M01      |
| DAI1_PIN03 | R18      | DMC0_DQ10  | A03      | GND      | E18      | GND      | M02      |
| DAI1_PIN04 | T20      | DMC0_DQ11  | A02      | GND      | F03      | GND      | M08      |
| DAI1_PIN05 | U20      | DMC0_DQ12  | B03      | GND      | F18      | GND      | M09      |
| DAI1_PIN06 | T19      | DMC0_DQ13  | B06      | GND      | G03      | GND      | M10      |
| DAI1_PIN07 | U19      | DMC0_DQ14  | B05      | GND      | G18      | GND      | M11      |
| DAI1_PIN08 | R19      | DMC0_DQ15  | A05      | GND      | H02      | GND      | M12      |
| DAI1_PIN09 | T18      | DMC0_LDM   | C01      | GND      | H03      | GND      | M13      |
| DAI1_PIN10 | U18      | DMC0_LDQS  | F01      | GND      | H08      | GND      | M17      |
| DAI1_PIN11 | V19      | DMC0_LDQS  | F02      | GND      | H09      | GND      | M18      |
| DAI1_PIN12 | V20      | DMC0_ODT   | H19      | GND      | H10      | GND      | N02      |
| DAI1_PIN19 | V17      | DMC0_RAS   | F19      | GND      | H11      | GND      | N08      |
| DAI1_PIN20 | W18      | DMC0_RESET | B12      | GND      | H12      | GND      | N09      |
| DMC0_A00   | D19      | DMC0_RZQ   | G19      | GND      | H13      | GND      | N10      |
| DMC0_A01   | D20      | DMC0_UDM   | A06      | GND      | H18      | GND      | N11      |
| DMC0_A02   | C20      | DMC0_UDQS  | A04      | GND      | J03      | GND      | N12      |
| DMC0_A03   | C19      | DMC0_UDQS  | B04      | GND      | J08      | GND      | N13      |
| DMC0_A04   | A19      | DMC0_VREF  | G20      | GND      | J09      | GND      | N17      |
| DMC0_A05   | B20      | DMC0_VREF  | J04      | GND      | J10      | GND      | N18      |
| DMC0_A06   | B18      | DMC0_WE    | A12      | GND      | J11      | GND      | P01      |
| DMC0_A07   | A18      | GND        | A01      | GND      | J12      | GND      | P17      |
| DMC0_A08   | A16      | GND        | A20      | GND      | J13      | GND      | P19      |
| DMC0_A09   | B16      | GND        | B01      | GND      | J18      | GND      | P20      |
| DMC0_A10   | A15      | GND        | B02      | GND      | K01      | GND      | R02      |
| DMC0_A11   | B15      | GND        | B19      | GND      | K02      | GND      | R17      |
| DMC0_A12   | B14      | GND        | C03      | GND      | K03      | GND      | T01      |
| DMC0_A13   | A14      | GND        | C04      | GND      | K08      | GND      | T04      |
| DMC0_A14   | A13      | GND        | C05      | GND      | K09      | GND      | T17      |
| DMC0_A15   | B13      | GND        | C06      | GND      | K10      | GND      | U01      |
| DMC0_BA0   | B17      | GND        | C14      | GND      | K11      | GND      | U04      |
| DMC0_BA1   | A17      | GND        | C15      | GND      | K12      | GND      | U05      |

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| Pin Name        | Ball No. | Pin Name          | Ball No. | Pin Name | Ball No. | Pin Name | Ball No. |
|-----------------|----------|-------------------|----------|----------|----------|----------|----------|
| GND             | U16      | PB_02             | B08      | VDD_DMC  | G14      | VDD_INT  | E17      |
| GND             | U17      | PB_03             | C07      | VDD_DMC  | G15      | VDD_INT  | F04      |
| GND             | V03      | PB_04             | B07      | VDD_DMC  | H06      | VDD_INT  | F05      |
| GND             | V04      | PB_05             | C08      | VDD_DMC  | H07      | VDD_INT  | F16      |
| GND             | V15      | PB_06             | V05      | VDD_DMC  | H14      | VDD_INT  | F17      |
| GND             | V16      | PB_07             | W04      | VDD_DMC  | H15      | VDD_INT  | G04      |
| GND             | V18      | PB_08             | W03      | VDD_DMC  | J06      | VDD_INT  | G05      |
| GND             | W01      | PB_09             | V06      | VDD_DMC  | J07      | VDD_INT  | G16      |
| GND             | W02      | PB_10             | Y03      | VDD_DMC  | K07      | VDD_INT  | G17      |
| GND             | W19      | PB_11             | Y04      | VDD_EXT  | D08      | VDD_INT  | H04      |
| GND             | W20      | PB_12             | V07      | VDD_EXT  | D09      | VDD_INT  | H05      |
| GND             | Y01      | PB_13             | W05      | VDD_EXT  | D10      | VDD_INT  | H16      |
| GND             | Y02      | PB_14             | Y14      | VDD_EXT  | D11      | VDD_INT  | H17      |
| GND             | Y05      | PB_15             | W14      | VDD_EXT  | K04      | VDD_INT  | J05      |
| GND             | Y07      | PC_00             | V13      | VDD_EXT  | L04      | VDD_INT  | J14      |
| GND             | Y13      | PC_01             | W15      | VDD_EXT  | M04      | VDD_INT  | J15      |
| GND             | Y16      | PC_02             | Y15      | VDD_EXT  | M16      | VDD_INT  | J16      |
| GND             | Y19      | PC_03             | W16      | VDD_EXT  | N04      | VDD_INT  | J17      |
| GND             | Y20      | PC_04             | Y17      | VDD_EXT  | N16      | VDD_INT  | K05      |
| HADC0_VIN0      | N19      | PC_05             | V14      | VDD_EXT  | P04      | VDD_INT  | K06      |
| HADC0_VIN1      | N20      | PC_06             | W17      | VDD_EXT  | P16      | VDD_INT  | K14      |
| HADC0_VIN2      | M19      | PC_07             | Y18      | VDD_EXT  | R04      | VDD_INT  | K15      |
| HADC0_VIN3      | M20      | SYS_BMODE0        | B10      | VDD_EXT  | R16      | VDD_INT  | K16      |
| HADC0_VREFN     | L18      | SYS_BMODE1        | B09      | VDD_EXT  | T05      | VDD_INT  | L05      |
| HADC0_VREFP     | L20      | SYS_BMODE2        | A08      | VDD_EXT  | T16      | VDD_INT  | L06      |
| JTG_TCK         | B11      | SYS_CLKIN0        | N01      | VDD_EXT  | U06      | VDD_INT  | L07      |
| JTG_TDI         | C13      | SYS_CLKOUT        | M03      | VDD_EXT  | U07      | VDD_INT  | L14      |
| JTG_TDO         | C11      | <u>SYS_FAULT</u>  | A11      | VDD_EXT  | U08      | VDD_INT  | L15      |
| JTG_TMS         | C12      | <u>SYS_HWRST</u>  | A09      | VDD_EXT  | U09      | VDD_INT  | M05      |
| <u>JTG_TRST</u> | A10      | <u>SYS_RESOUT</u> | C10      | VDD_EXT  | U10      | VDD_INT  | M06      |
| PA_00           | N03      | SYS_XTAL0         | L01      | VDD_EXT  | U11      | VDD_INT  | M07      |
| PA_01           | P03      | VDD_ANA           | L19      | VDD_EXT  | U12      | VDD_INT  | M14      |
| PA_02           | P02      | VDD_DMC           | F06      | VDD_EXT  | U13      | VDD_INT  | N06      |
| PA_03           | R03      | VDD_DMC           | F07      | VDD_EXT  | U14      | VDD_INT  | N07      |
| PA_04           | R01      | VDD_DMC           | F08      | VDD_EXT  | U15      | VDD_INT  | N14      |
| PA_05           | T02      | VDD_DMC           | F09      | VDD_INT  | E04      | VDD_INT  | P06      |
| PA_06           | T03      | VDD_DMC           | F10      | VDD_INT  | E05      | VDD_INT  | P07      |
| PA_07           | V01      | VDD_DMC           | F11      | VDD_INT  | E06      | VDD_INT  | P08      |
| PA_08           | U03      | VDD_DMC           | F12      | VDD_INT  | E07      | VDD_INT  | P09      |
| PA_09           | V02      | VDD_DMC           | F13      | VDD_INT  | E08      | VDD_INT  | P10      |
| PA_10           | U02      | VDD_DMC           | F14      | VDD_INT  | E09      | VDD_INT  | P11      |
| PA_11           | V08      | VDD_DMC           | F15      | VDD_INT  | E10      | VDD_INT  | P12      |
| PA_12           | W06      | VDD_DMC           | G06      | VDD_INT  | E11      | VDD_INT  | P13      |
| PA_13           | Y06      | VDD_DMC           | G07      | VDD_INT  | E12      | VDD_INT  | P14      |
| PA_14           | W07      | VDD_DMC           | G08      | VDD_INT  | E13      | VDD_INT  | R06      |
| PA_15           | W08      | VDD_DMC           | G09      | VDD_INT  | E14      | VDD_INT  | R07      |
| PB_00           | A07      | VDD_DMC           | G12      | VDD_INT  | E15      | VDD_INT  | R08      |
| PB_01           | C09      | VDD_DMC           | G13      | VDD_INT  | E16      | VDD_INT  | R09      |

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| Pin Name | Ball No. |
|----------|----------|
| VDD_INT  | R10      |
| VDD_INT  | R11      |
| VDD_INT  | R12      |
| VDD_INT  | R13      |
| VDD_INT  | R14      |
| VDD_REF  | G10      |
| VDD_REF  | G11      |
| VDD_REF  | M15      |
| VDD_REF  | N05      |
| VDD_REF  | N15      |
| VDD_REF  | P05      |
| VDD_REF  | P15      |
| VDD_REF  | R05      |
| VDD_REF  | R15      |
| VDD_REF  | T06      |
| VDD_REF  | T07      |
| VDD_REF  | T08      |
| VDD_REF  | T09      |
| VDD_REF  | T10      |
| VDD_REF  | T11      |
| VDD_REF  | T12      |
| VDD_REF  | T13      |
| VDD_REF  | T14      |
| VDD_REF  | T15      |

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## CONFIGURATION OF THE 400-BALL CSP\_BGA

Figure 55 shows an overview of signal placement on the 400-ball CSP\_BGA.

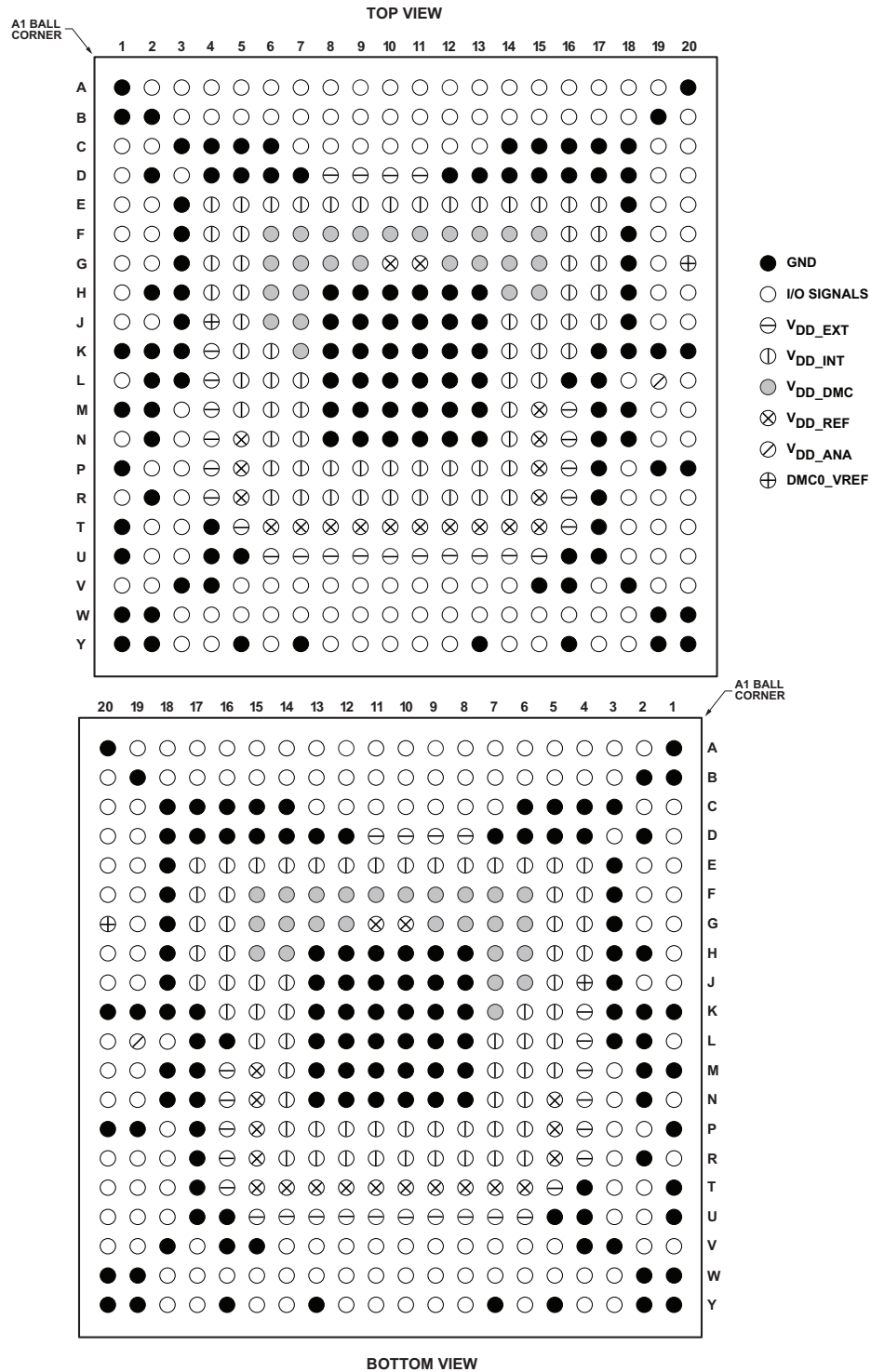


Figure 55. 400-Ball CSP\_BGA Configuration

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## ADSP-2156x 120-LEAD LQFP LEAD ASSIGNMENTS

The ADSP-2156x 120-Lead LQFP Lead Assignments (Numerical by Lead Number) table lists the 120-lead LQFP package by lead number.

The ADSP-2156x 120-Lead LQFP Lead Assignments (Alphabetical by Pin Name) table lists the 120-lead LQFP package by pin name.

### ADSP-2156x 120-LEAD LQFP LEAD ASSIGNMENTS (NUMERICAL BY LEAD NUMBER)

| Lead No. | Pin Name   | Lead No. | Pin Name   | Lead No. | Pin Name          | Lead No.                                                                                                                | Pin Name |
|----------|------------|----------|------------|----------|-------------------|-------------------------------------------------------------------------------------------------------------------------|----------|
| 01       | VDD_INT    | 41       | DAI0_PIN01 | 81       | HADC0_VIN0        | 121 <sup>1</sup>                                                                                                        | GND      |
| 02       | GND        | 42       | DAI0_PIN02 | 82       | HADC0_VIN1        | <sup>1</sup> Pin121 is the GND supply (see <a href="#">Figure 57</a> ) for the processor; this pad must connect to GND. |          |
| 03       | VDD_INT    | 43       | DAI0_PIN03 | 83       | HADC0_VREFP       |                                                                                                                         |          |
| 04       | VDD_INT    | 44       | VDD_INT    | 84       | HADC0_VREFN       |                                                                                                                         |          |
| 05       | SYS_CLKIN0 | 45       | VDD_INT    | 85       | VDD_ANA           |                                                                                                                         |          |
| 06       | SYS_XTAL0  | 46       | DAI0_PIN04 | 86       | GND               |                                                                                                                         |          |
| 07       | VDD_REF    | 47       | DAI0_PIN05 | 87       | VDD_INT           |                                                                                                                         |          |
| 08       | VDD_INT    | 48       | DAI0_PIN06 | 88       | VDD_INT           |                                                                                                                         |          |
| 09       | GND        | 49       | DAI0_PIN07 | 89       | VDD_INT           |                                                                                                                         |          |
| 10       | SYS_CLKOUT | 50       | VDD_EXT    | 90       | GND               |                                                                                                                         |          |
| 11       | VDD_REF    | 51       | VDD_REF    | 91       | VDD_INT           |                                                                                                                         |          |
| 12       | VDD_EXT    | 52       | DAI0_PIN08 | 92       | GND               |                                                                                                                         |          |
| 13       | VDD_INT    | 53       | DAI0_PIN09 | 93       | VDD_INT           |                                                                                                                         |          |
| 14       | PA_00      | 54       | DAI0_PIN10 | 94       | VDD_INT           |                                                                                                                         |          |
| 15       | PA_01      | 55       | DAI0_PIN19 | 95       | VDD_INT           |                                                                                                                         |          |
| 16       | PA_02      | 56       | DAI0_PIN20 | 96       | JTG_TDI           |                                                                                                                         |          |
| 17       | VDD_INT    | 57       | VDD_INT    | 97       | JTG_TCK           |                                                                                                                         |          |
| 18       | PA_03      | 58       | GND        | 98       | JTG_TMS           |                                                                                                                         |          |
| 19       | PA_04      | 59       | VDD_INT    | 99       | JTG_TDO           |                                                                                                                         |          |
| 20       | PA_05      | 60       | VDD_INT    | 100      | VDD_REF           |                                                                                                                         |          |
| 21       | PA_06      | 61       | VDD_INT    | 101      | VDD_EXT           |                                                                                                                         |          |
| 22       | VDD_INT    | 62       | GND        | 102      | <u>SYS_FAULT</u>  |                                                                                                                         |          |
| 23       | VDD_REF    | 63       | DAI1_PIN20 | 103      | <u>JTG_TRST</u>   |                                                                                                                         |          |
| 24       | VDD_EXT    | 64       | DAI1_PIN19 | 104      | <u>SYS_HWRST</u>  |                                                                                                                         |          |
| 25       | PA_07      | 65       | DAI1_PIN10 | 105      | SYS_BMODE0        |                                                                                                                         |          |
| 26       | PA_08      | 66       | DAI1_PIN09 | 106      | SYS_BMODE1        |                                                                                                                         |          |
| 27       | PA_09      | 67       | VDD_REF    | 107      | <u>SYS_RESOUT</u> |                                                                                                                         |          |
| 28       | PA_10      | 68       | VDD_EXT    | 108      | PB_00             |                                                                                                                         |          |
| 29       | VDD_INT    | 69       | VDD_INT    | 109      | PB_01             |                                                                                                                         |          |
| 30       | GND        | 70       | DAI1_PIN08 | 110      | VDD_INT           |                                                                                                                         |          |
| 31       | GND        | 71       | DAI1_PIN07 | 111      | VDD_EXT           |                                                                                                                         |          |
| 32       | VDD_INT    | 72       | DAI1_PIN06 | 112      | VDD_REF           |                                                                                                                         |          |
| 33       | VDD_INT    | 73       | DAI1_PIN05 | 113      | PB_02             |                                                                                                                         |          |
| 34       | PA_11      | 74       | DAI1_PIN04 | 114      | PB_03             |                                                                                                                         |          |
| 35       | PA_12      | 75       | DAI1_PIN03 | 115      | PB_04             |                                                                                                                         |          |
| 36       | PA_13      | 76       | DAI1_PIN02 | 116      | PB_05             |                                                                                                                         |          |
| 37       | PA_14      | 77       | DAI1_PIN01 | 117      | VDD_INT           |                                                                                                                         |          |
| 38       | VDD_EXT    | 78       | VDD_EXT    | 118      | VDD_INT           |                                                                                                                         |          |
| 39       | VDD_REF    | 79       | VDD_REF    | 119      | VDD_INT           |                                                                                                                         |          |
| 40       | PA_15      | 80       | VDD_INT    | 120      | GND               |                                                                                                                         |          |

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## ADSP-2156x 120-LEAD LQFP LEAD ASSIGNMENTS (ALPHABETICAL BY PIN NAME)

| Pin Name    | Lead No.         | Pin Name   | Lead No. | Pin Name                                                                                                                | Lead No. |
|-------------|------------------|------------|----------|-------------------------------------------------------------------------------------------------------------------------|----------|
| DAIO_PIN01  | 41               | PA_03      | 18       | VDD_INT                                                                                                                 | 45       |
| DAIO_PIN02  | 42               | PA_04      | 19       | VDD_INT                                                                                                                 | 57       |
| DAIO_PIN03  | 43               | PA_05      | 20       | VDD_INT                                                                                                                 | 59       |
| DAIO_PIN04  | 46               | PA_06      | 21       | VDD_INT                                                                                                                 | 60       |
| DAIO_PIN05  | 47               | PA_07      | 25       | VDD_INT                                                                                                                 | 61       |
| DAIO_PIN06  | 48               | PA_08      | 26       | VDD_INT                                                                                                                 | 69       |
| DAIO_PIN07  | 49               | PA_09      | 27       | VDD_INT                                                                                                                 | 80       |
| DAIO_PIN08  | 52               | PA_10      | 28       | VDD_INT                                                                                                                 | 87       |
| DAIO_PIN09  | 53               | PA_11      | 34       | VDD_INT                                                                                                                 | 88       |
| DAIO_PIN10  | 54               | PA_12      | 35       | VDD_INT                                                                                                                 | 89       |
| DAIO_PIN19  | 55               | PA_13      | 36       | VDD_INT                                                                                                                 | 91       |
| DAIO_PIN20  | 56               | PA_14      | 37       | VDD_INT                                                                                                                 | 93       |
| DAI1_PIN01  | 77               | PA_15      | 40       | VDD_INT                                                                                                                 | 94       |
| DAI1_PIN02  | 76               | PB_00      | 108      | VDD_INT                                                                                                                 | 95       |
| DAI1_PIN03  | 75               | PB_01      | 109      | VDD_INT                                                                                                                 | 110      |
| DAI1_PIN04  | 74               | PB_02      | 113      | VDD_INT                                                                                                                 | 117      |
| DAI1_PIN05  | 73               | PB_03      | 114      | VDD_INT                                                                                                                 | 118      |
| DAI1_PIN06  | 72               | PB_04      | 115      | VDD_INT                                                                                                                 | 119      |
| DAI1_PIN07  | 71               | PB_05      | 116      | VDD_REF                                                                                                                 | 07       |
| DAI1_PIN08  | 70               | SYS_BMODE0 | 105      | VDD_REF                                                                                                                 | 11       |
| DAI1_PIN09  | 66               | SYS_BMODE1 | 106      | VDD_REF                                                                                                                 | 23       |
| DAI1_PIN10  | 65               | SYS_CLKIN0 | 05       | VDD_REF                                                                                                                 | 39       |
| DAI1_PIN19  | 64               | SYS_CLKOUT | 10       | VDD_REF                                                                                                                 | 51       |
| DAI1_PIN20  | 63               | SYS_FAULT  | 102      | VDD_REF                                                                                                                 | 67       |
| GND         | 02               | SYS_HWRST  | 104      | VDD_REF                                                                                                                 | 79       |
| GND         | 09               | SYS_RESOUT | 107      | VDD_REF                                                                                                                 | 100      |
| GND         | 30               | SYS_XTAL0  | 06       | VDD_REF                                                                                                                 | 112      |
| GND         | 31               | VDD_ANA    | 85       | <sup>1</sup> Pin121 is the GND supply (see <a href="#">Figure 57</a> ) for the processor; this pad must connect to GND. |          |
| GND         | 58               | VDD_EXT    | 12       |                                                                                                                         |          |
| GND         | 62               | VDD_EXT    | 24       |                                                                                                                         |          |
| GND         | 86               | VDD_EXT    | 38       |                                                                                                                         |          |
| GND         | 90               | VDD_EXT    | 50       |                                                                                                                         |          |
| GND         | 92               | VDD_EXT    | 68       |                                                                                                                         |          |
| GND         | 120              | VDD_EXT    | 78       |                                                                                                                         |          |
| GND         | 121 <sup>1</sup> | VDD_EXT    | 101      |                                                                                                                         |          |
| HADC0_VIN0  | 81               | VDD_EXT    | 111      |                                                                                                                         |          |
| HADC0_VIN1  | 82               | VDD_INT    | 01       |                                                                                                                         |          |
| HADC0_VREFN | 84               | VDD_INT    | 03       |                                                                                                                         |          |
| HADC0_VREFP | 83               | VDD_INT    | 04       |                                                                                                                         |          |
| JTG_TCK     | 97               | VDD_INT    | 08       |                                                                                                                         |          |
| JTG_TDI     | 96               | VDD_INT    | 13       |                                                                                                                         |          |
| JTG_TDO     | 99               | VDD_INT    | 17       |                                                                                                                         |          |
| JTG_TMS     | 98               | VDD_INT    | 22       |                                                                                                                         |          |
| JTG_TRST    | 103              | VDD_INT    | 29       |                                                                                                                         |          |
| PA_00       | 14               | VDD_INT    | 32       |                                                                                                                         |          |
| PA_01       | 15               | VDD_INT    | 33       |                                                                                                                         |          |
| PA_02       | 16               | VDD_INT    | 44       |                                                                                                                         |          |

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## CONFIGURATION OF THE 120-LEAD LQFP LEAD CONFIGURATION

Figure 56 shows the top view of the 120-lead LQFP lead configuration and Figure 57 shows the bottom view of the 120-lead LQFP lead configuration.

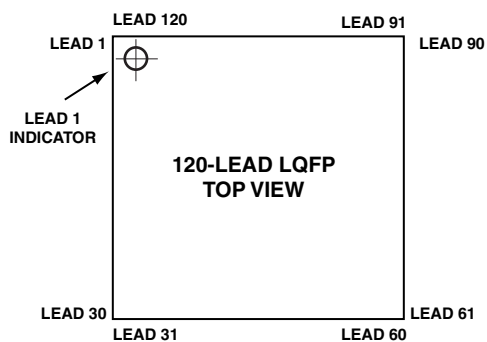


Figure 56. 120-Lead LQFP Lead Configuration (Top View)

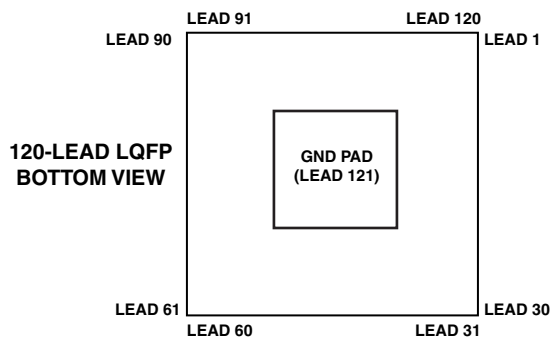


Figure 57. 120-Lead LQFP Lead Configuration (Bottom View)

OUTLINE DIMENSIONS

Dimensions in [Figure 58](#) (for the 400-ball BGA) and [Figure 59](#) (for the 120-lead LQFP) are shown in millimeters.

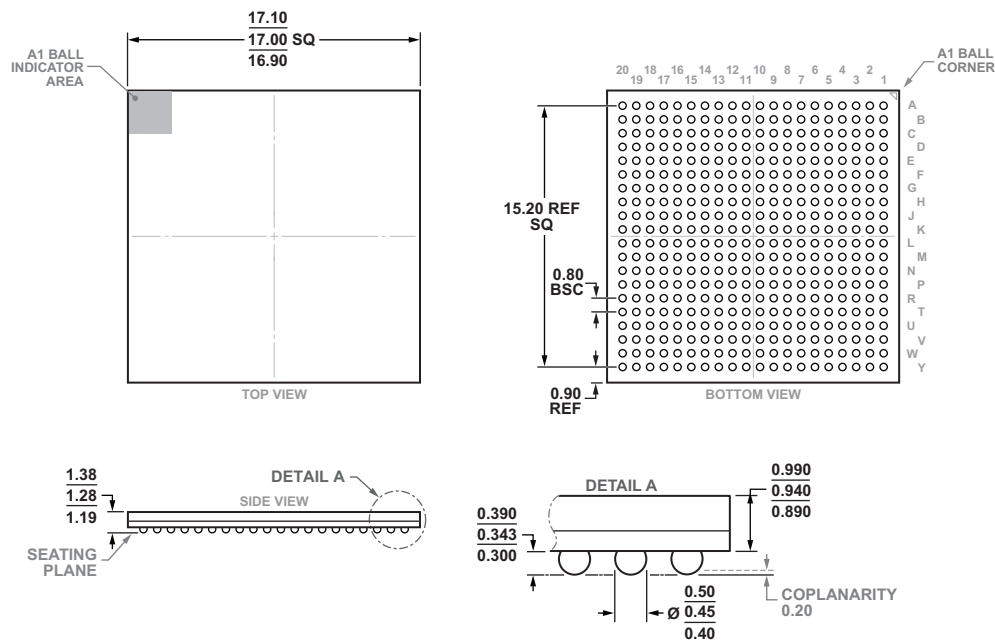
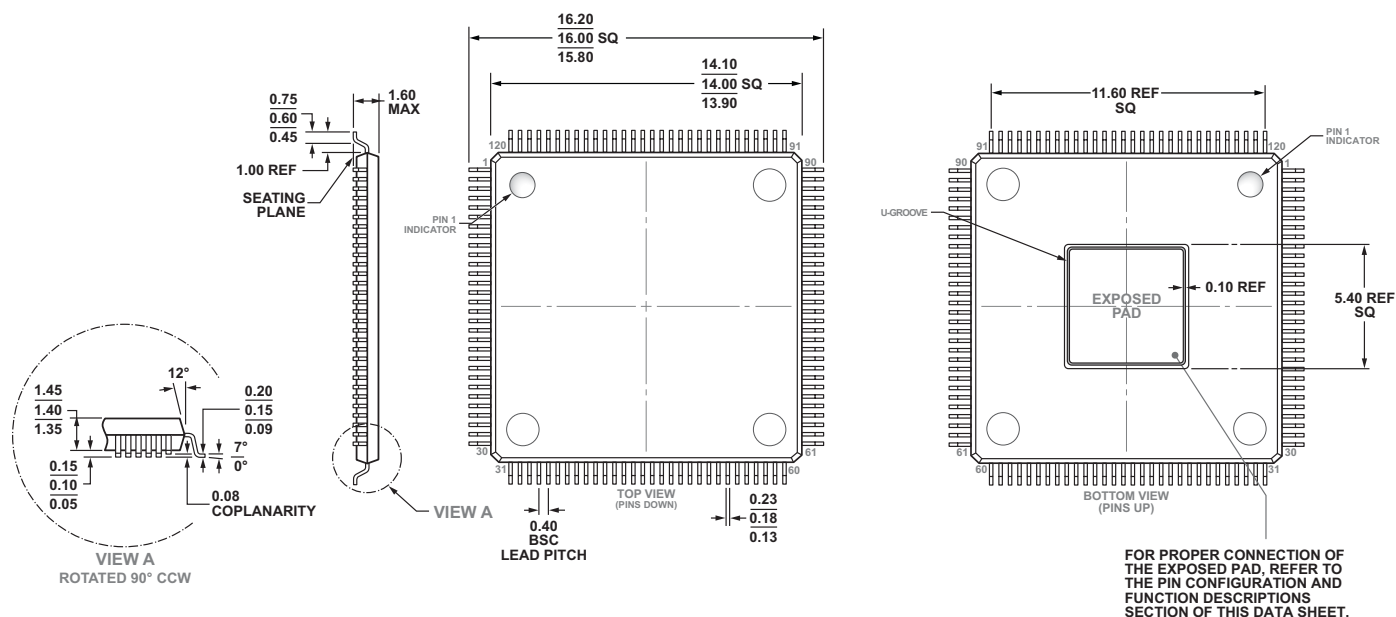


Figure 58. 400-Ball Chip Scale Package Ball Grid Array [CSP\_BGA]  
(BC-400-3)  
Dimensions shown in millimeters

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COMPLIANT TO JEDEC STANDARDS MS-026-BEE-HD

Figure 59. 120-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP]  
(SW-120-4)

Dimensions shown in millimeters

## SURFACE-MOUNT DESIGN

Table 65 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard*.

Table 65. CSP\_BGA Data for Use with Surface-Mount Design

| Package  | Package Ball Attach Type | Package Solder Mask Opening | Package Ball Pad Size |
|----------|--------------------------|-----------------------------|-----------------------|
| BC-400-3 | Solder Mask Defined      | 0.4 mm Diameter             | 0.5 mm Diameter       |

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## AUTOMOTIVE PRODUCTS

The following models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the nonautomotive models; therefore designers should review the [Specifications](#) section of this data sheet carefully. Only the automotive grade products shown in [Table 66](#) are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

**Table 66. Automotive Products**

| Model <sup>1, 2</sup> | Processor Instruction Rate (Max) | Temperature Range <sup>3</sup> | External Memory Port | Package Description           | Package Option |
|-----------------------|----------------------------------|--------------------------------|----------------------|-------------------------------|----------------|
| ADSP-21562WCSWZ4      | 400 MHz                          | –40°C to +125°C                | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP-21562WCSWZ4RL    | 400 MHz                          | –40°C to +125°C                | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP-21563WCSWZ6      | 600 MHz                          | –40°C to +125°C                | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP-21563WCSWZ6RL    | 600 MHz                          | –40°C to +125°C                | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP-21563WCSWZ8      | 800 MHz                          | –40°C to +125°C                | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP-21563WCSWZ8RL    | 800 MHz                          | –40°C to +125°C                | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP-21565WCSWZ8      | 800 MHz                          | –40°C to +125°C                | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP-21565WCSWZ8RL    | 800 MHz                          | –40°C to +125°C                | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP-21565WCSWZ10     | 1000 MHz                         | –40°C to +125°C                | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP21565WCSWZ10RL    | 1000 MHz                         | –40°C to +125°C                | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP-21566WCBCZ4      | 400 MHz                          | –40°C to +125°C                | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP-21566WCBCZ4RL    | 400 MHz                          | –40°C to +125°C                | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP-21567WCBCZ6      | 600 MHz                          | –40°C to +125°C                | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP-21567WCBCZ6RL    | 600 MHz                          | –40°C to +125°C                | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP-21567WCBCZ8      | 800 MHz                          | –40°C to +125°C                | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP-21567WCBCZ8RL    | 800 MHz                          | –40°C to +125°C                | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP-21569WCBCZ8      | 800 MHz                          | –40°C to +125°C                | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP-21569WCBCZ8RL    | 800 MHz                          | –40°C to +125°C                | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP-21569WCBCZ10     | 1000 MHz                         | –40°C to +125°C                | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP21569WCBCZ10RL    | 1000 MHz                         | –40°C to +125°C                | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |

<sup>1</sup> Z = RoHS compliant part.

<sup>2</sup> RL = Supplied on Tape and Reel.

<sup>3</sup> Referenced temperature is junction temperature. See [Operating Conditions](#) for junction temperature (T<sub>J</sub>) specification.

# ADSP-21562/21563/21565/21566/21567/21569

## ORDERING GUIDE

| Model <sup>1</sup> | Processor Instruction Rate (Max) | Temperature Range <sup>2</sup> | External Memory Port | Package Description           | Package Option |
|--------------------|----------------------------------|--------------------------------|----------------------|-------------------------------|----------------|
| ADSP-21562BSWZ4    | 400 MHz                          | –40°C to +125°C                | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP-21562KSWZ4    | 400 MHz                          | 0°C to +110°C                  | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP-21563BSWZ8    | 800 MHz                          | –40°C to +125°C                | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP-21563KSWZ8    | 800 MHz                          | 0°C to +110°C                  | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP-21565BSWZ8    | 800 MHz                          | –40°C to +125°C                | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP-21565BSWZ10   | 1000 MHz                         | –40°C to +125°C                | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP-21565KSWZ8    | 800 MHz                          | 0°C to +110°C                  | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP-21565KSWZ10   | 1000 MHz                         | 0°C to +110°C                  | 0                    | 120-Lead LQFP_EP, Exposed Pad | SW-120-4       |
| ADSP-21566BBCZ4    | 400 MHz                          | –40°C to +125°C                | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP-21566KBCZ4    | 400 MHz                          | 0°C to +110°C                  | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP-21567BBCZ6    | 600 MHz                          | –40°C to +125°C                | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP-21567BBCZ8    | 800 MHz                          | –40°C to +125°C                | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP-21567KBCZ6    | 600 MHz                          | 0°C to +110°C                  | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP-21567KBCZ8    | 800 MHz                          | 0°C to +110°C                  | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP-21569BBCZ8    | 800 MHz                          | –40°C to +125°C                | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP-21569BBCZ10   | 1000 MHz                         | –40°C to +125°C                | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP-21569KBCZ8    | 800 MHz                          | 0°C to +110°C                  | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |
| ADSP-21569KBCZ10   | 1000 MHz                         | 0°C to +110°C                  | 1                    | Pad 400-Ball CSP_BGA          | BC-400-3       |

<sup>1</sup> Z =RoHS compliant part.

<sup>2</sup> Referenced temperature is junction temperature. See [Operating Conditions](#) for junction temperature (T<sub>J</sub>) specification.

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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