THE DATASHEET OF

M02171G-12

M02171

11.3Gbps Dual Loop VCSEL Driver with Integrated Micro Controller

The M02171 is designed to drive vertical cavity surface emitting lasers used in Transmitter optical sub-assemblies and supports data rates up to 11.3 Gbps. The M02171 supports both common anode and common cathode VCSEL configurations. It combines the diagnostic monitoring Interface compliant with SFP, XFP, SFP+ and a driver compatible with VCSEL lasers in a compact 5mm x 5mm QFN package.

The M02171 features dual loop control, which compensates for changes in laser slope efficiency over temperature and life. These features can also reduce or eliminate temperature calibration, thus improving system reliability and reducing overall cost. Integrated safety circuitry provides latched bias and modulation current shutdown if a fault condition is detected and provides either internal V_{CC} switch or ground switch. The device comes with firmware required for diagnostic monitoring, offering a seamless interface for calibration and setup.

Other available solutions: M02170 - 11.3Gbps Dual Loop DML Driver with Integrated Micro Controller
M02172 - 11.3Gbps EML Driver with Integrated Micro Controller

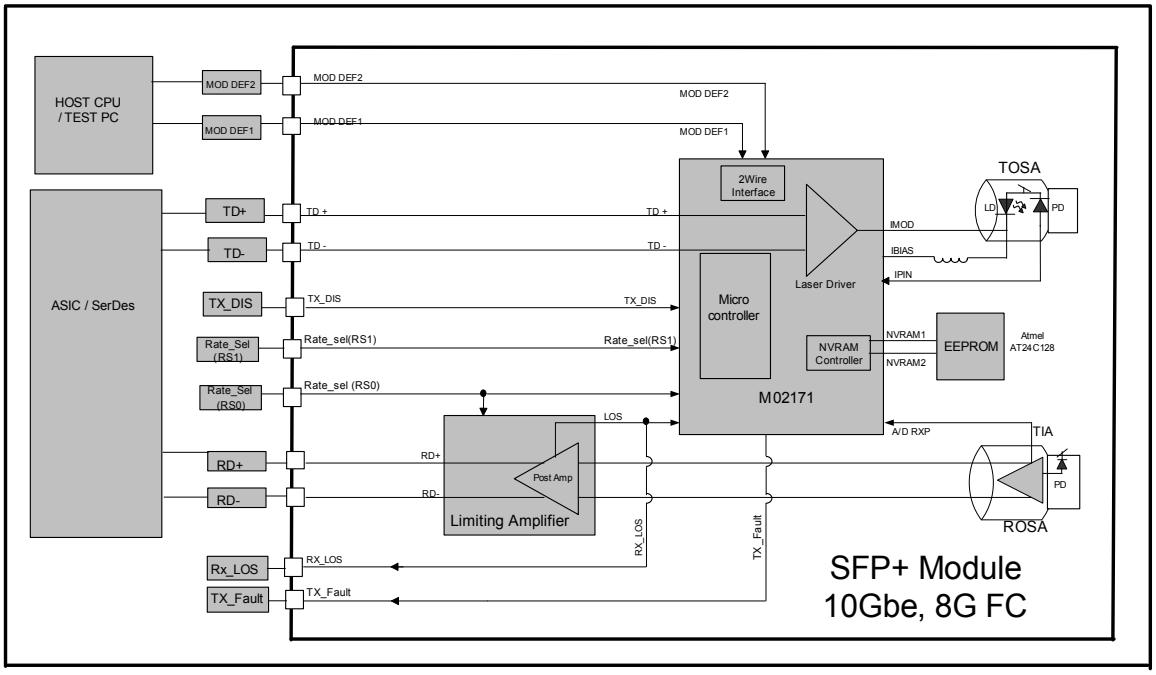
Features

- Data Rates to 11.3 Gbps. Single 3.3V supply
- Dual Loop Control for average optical power and modulation amplitude
- Programmable VCSEL bias current to 15mA
- Programmable VCSEL modulation current to 15mA
- Integrated mode supports SFF-8472/SFP/SFP+ Requirements
- External micro controller mode supports SFF-8472/XFP/SFP/SFP+ requirements
- SFP/XFP compliant safety circuitry
- Provides internal Vcc and ground switch for single point faults
- Input equalization for SFP+ requirements
- 2-wire or SPI serial interface available
- Programmable GPIO, selectable 6 bit or 10 bit DAC via serial interface
- Five user configurable General purpose I/Os
- Two available auxiliary 12 bit ADC inputs
- Provides complete Calibration and Firmware setup
- 54 mA typical supply current
- Operating Temperature: -40 °C to +95 °C
- 5mm x 5mm QFN package

Applications

- IEEE802.3 10GBASE-SR
- SFP/SFP+/XFP MSA Modules
- 8G Fiber Channel Modules
- SONET OC-192 Optical Transmitters
- SDH STM-64 Optical Transmitters

M02171 Interface (Integrated Mode) in SFP+ Module



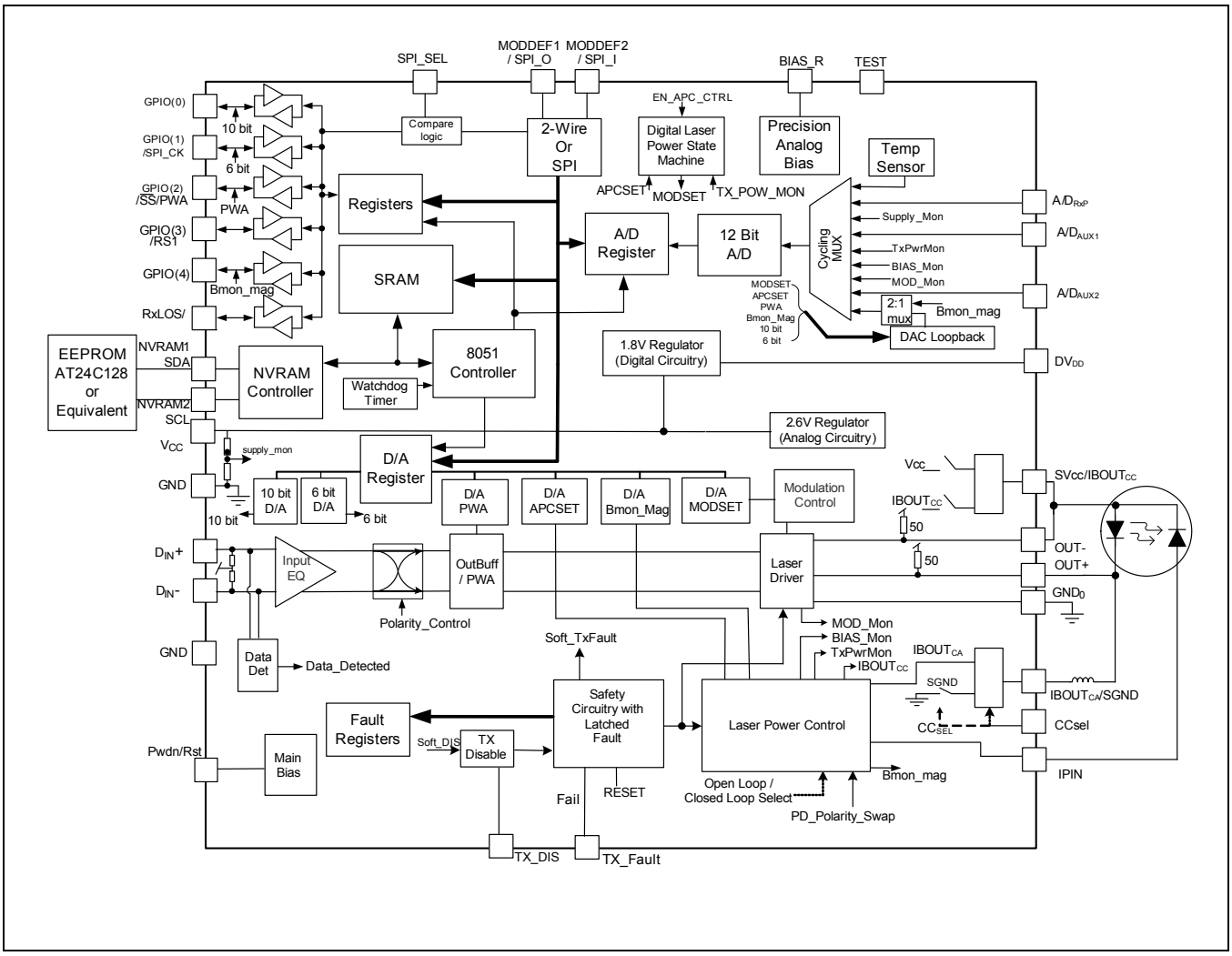
Ordering Information

Part Number	Package	Operating Temperature
M02171G-12*	32 pin, 5mm x 5mm QFN	-40°C to +95°C
*The G in the part number indicates that this is an RoHS compliant package. Refer to www.mindspeed.com for additional information.		

Revision History

Revision	Level	Date	ASIC Revision	Description
E	Release	December 2010	-12	Update Ordering Information. Remove 8k EEPROM download option as it is not required to meet the SFP t_init and t_serial timing requirements. Update package diagram measurements.
D	Release	May 2009	-12	Final characterization results included in specifications. Applications figure added for Emcore and JDSU TOSAs. Minor corrections made to text explanations.
C	Advance	April 2007	-11P	Added SPI, Functional description and Applications information
B	Advance	March 2007	-11P	Change Pins 9,10 and 29, updated drawings to include changes to SFP+
A	Advance	January 2007	-11P	Initial

M02171 Block Diagram



1.0 Product Specification

1.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{CC}	3.3 V power supply voltage	-0.4 to +4.0	V
T_A	Operating Ambient Temperature	-40 to +95	°C
T_{STG}	Storage temperature	-65 to +150	°C
$IBOUT_{CA(MAX)}$	Maximum bias output current at $IBOUT_{CA}$	25	mA
$IBOUT_{CC(MAX)}$	Maximum bias output current at $IBOUT_{CC}$	25	mA
$I_{MOD(MAX)}$	Max. modulation current - common anode or common cathode operation	25	mA_{PP}

1.2 Recommended Operating Conditions

Table 1-2. Recommended Operating Conditions

Parameter	Rating	Units
Power supply (V_{CC}-GND)	3.3 ±5%	V
Operating ambient	-40 to +95	°C

1.3 DC Characteristics

V_{CC} = 3.05 to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C, I_{MOD} = 5mA, I_{BIAS} = 5mA, unless otherwise noted.

Table 1-3. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CC}	V_{CC} operating voltage		3.05	3.3	3.55	V
I_{CC}	I_{CC} supply current (1)	High-rate mode	–	54	84	mA
		Low-rate mode	–	42	–	
		Increase due to enabling Pulse Width Adjust	–	2	–	
I_{CC_DIS}	I_{CC} when part Disabled	Device is in disabled	–	36	48	mA
V_{CCTHL}	3.3 V supply detection (low voltage) threshold	Minimum of either V_{CC} supply low detection voltage or internal Power on Reset voltage	–	2.6	2.85	V
V_{CCTHH}	3.3 V supply detection (high voltage) threshold		3.55	3.8	4.00	V
V_{FAULTL}	Low fault voltage detection threshold ($IBOUT_{CA}$, BIAS_R)	Fault condition occurs when voltage drops below this level	–	400	600	mV
V_{FAULTH}	High fault voltage detection threshold ($IBOUT_{CC}$)	Fault condition occurs when voltage exceeds this level	V_{CC} - 0.6	V_{CC} - 0.4	–	V
I_{BIAS_CA}	Bias current adjust range CA (2)	At $IBOUT_{CA}$, $V(IBOUT_{CA})$ > 0.7 V	3	–	15	mA
I_{BIAS_CC}	Bias current adjust range CC	At $IBOUT_{CC}$., $V(IBOUT_{CC})$ < 2.5 V	1	–	15	mA
$I_{BIAS(OFF)\_CA}$	Bias current with output disabled	TX_DIS = high and/or SOFT DIS = high; $V(IBOUT_{CA})$ = V_{CC} for common anode	–	300	600	µA
$I_{BIAS(OFF)\_CC}$	Bias current with output disabled	TX_DIS = high and/or SOFT DIS = high; $V(IBOUT_{CC})$= 0V for common cathode	–	5	150	µA
$BIAS_{RATIO\ CC}$	Ratio of bias current to $BIAS_{MON}$ current	$V(IBOUT_{CC})$= 2.0 V	13.6	14.8	15.8	A/A
$BIAS_{RATIO\ CA}$	Ratio of bias current to $BIAS_{MON}$ current	$V(IBOUT_{CA})$= 1.5 V	13.6	14.8	15.8	A/A
V_{MD}	Monitor diode reverse bias voltage	Minimum is with maximum I_{PIN} current, maximum is with zero I_{PIN} current	1.5	2.0	V_{CC}	V
I_{MD}	Monitor diode current adjustment range (3)	For stable APC loop operation	10	–	1400	µA
C_{MDMAX}	Maximum monitor photodiode capacitance (3)	For stable APC loop operation in analog closed mode; includes any additional parasitic capacitance	–	–	100	pF
V_{IH_DIS}	TTL/CMOS input high voltage (TX_DIS, Pwdn/Rst, SPI_sel, Test)		2.0	–	V_{CC}	V
V_{IL_DIS}	TTL/CMOS input low voltage (TX_DIS, Pwdn/Rst, SPI_sel, Test)		0	–	0.8	V
V_{IH_SEL}	CC_{SEL} CMOS input high voltage		2.4	–	–	V
V_{IL_SEL}	CC_{SEL} CMOS input low voltage		–	–	1.0	V
V_{IH_IO}	GPIO input high voltage	When configured as a digital input	2.0	–	V_{CC}	V
V_{IL_IO}	GPIO input low voltage		0	–	1.0	V

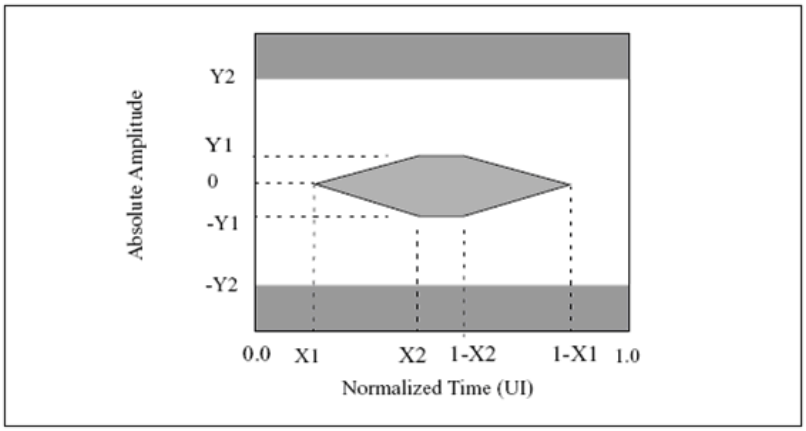
Table 1-3. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$I_{LK\_IO\_04}$	GPIO 0-4 leakage current	When configured as a tristated digital input	-10	0	10	µA
V_{IH_LOS}	LOS input high voltage		2.0	–	V_{CC}	V
V_{IL_LOS}	LOS input low voltage		0	–	0.8	V
V_{OH_FAIL}	Logic output high voltage (FAIL)	With external 10 kΩ pull-up to V_{CC}	V_{CC} - 0.6	–	–	V
V_{OL_FAIL}	Logic output low voltage (FAIL)	I_{OL} = 1.2 mA	–	–	0.4	V
V_{OH_IO}	GPIO output high voltage	When configured as a digital output I_{OH} = -2 mA.	2.4	–	V_{CC}	V
V_{OL_IO}	GPIO output low voltage	When configured as a digital output I_{OL} = 2 mA	0	–	0.4	V
R_{IN}	Differential input resistance		85	100	115	Ω
R_{OUT}	Output resistance		45	55	65	Ω
V_{CMSELF}	Self-biased common mode input voltage		–	V_{CC} - 1.3	–	V
V_{INCM}	Common-mode input compliance voltage (3)	Data inputs	V_{CC} - 1.5	–	V_{CC} -$V_{IN(Diff)}$/4	V
$V_{IN(Diff)}$	Differential input voltage (3)	Peak to Peak, Equalizer off	80	–	1000	mV
		For SFP+ applications. (Refer to the Signal compliance mask in Figure 1-1) Equalizer on				
		X1:SFP+ Eye Mask compliance			0.14	UI
		X2: SFP+ Eye Mask compliance			0.35	UI
		Y1:SFP+ Eye Mask compliance	75			mV
		Y2: SFP+ Eye Mask compliance			400	mV

NOTES:

1. Excludes bias and modulation currents delivered to the laser.
2. To meet $BIAS_{RATIO\_CA}$ specifications. Operation as low as 1 mA is achievable.
3. Guaranteed by design and characterization.

Figure 1-1. Differential Input signal Compliance mask at the input of the M02171



1.4 AC Characteristics

V_{CC} = 3.05 to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C, I_{MOD} = 5mA, I_{BIAS} = 5mA, unless otherwise noted. All values measured with the input equalizer on and using 6 inches (15 cm) of FR4 non-backdrilled stripline trace length.

Table 1-4. AC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
I_{MOD}	Modulation current adjust range	Current delivered to VCSEL assuming a series resistance between 40 - 110 Ω	5	–	15	mA_{PP}
$I_{MOD(OFF)}$	Modulation current with output disabled	TX_DIS = high and/or SOFT_DIS = high	–	15	150	µA
I_{MOD_RATIO}	Ratio of modulation current to MOD_{MON} current	= (I_{OUTP} - I_{OUTN})/I_{MODMON}	–	12.5	–	A/A
PWA	Pulse width adjustment range	50% crossing point at DAC mid range	–	±20	–	ps
t_R / t_F	Modulation output rise / fall times	20% to 80% into 50Ω load. Measured using alternating 1-0 pattern at 2.5 Gbps	– –	21 (1) 30 (2)	29 60	ps ps
OS	Overshoot of modulation output	Into 50Ω load	–	3	–	%
RJ	Random jitter	Measured by 7.5 GHz Bessel filter at output	–	0.4		ps_{RMS}
DJ	Modulation output deterministic jitter (3)	Peak-to-peak into 50Ω load using 2^{15} - 1 PRBS at 10.3 Gbps	–	9	17	ps

NOTES:

1. With RS1=1, For Tx Signalling rates > 4.25Gb/s
2. With RS1=0, For Tx Signalling rates ≤ 4.25Gb/s
3. Includes Duty Cycle Distortion

1.5 Soft Control Timing Management

V_{CC} = 3.05 to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C unless otherwise noted using internal micro controller.

Table 1-5. I/O Timing for Soft Control and Status Functions

Symbol	Parameter	Conditions	Typ	Max	Units
t_off	Tx_DIS assert time	Time from TX_DIS bit set (1) until optical output falls below 10% of nominal	–	100	ms
t_on	TX_DIS deassert time	Time from TX_DIS bit cleared (1) until optical output rises above 90% of nominal	–	100	ms
t_init	Time to initialize, including reset of TX_Fault	Time from power on or negation of TX_FAULT using TX_DISABLE until transmitter output is stable		300	ms
t_fault	TX_Fault assert time	Time from fault to TX_FAULT bit set		100	ms
t_loss_on	RX_LOS assert time	Time from LOS state to RX_LOS bit set		100	ms
t_loss_off	LOS deassert time	Time from non-LOS state to RX_LOS bit cleared		100	ms
t_serial	Serial bus hardware ready	Time from power on until host can read from the serial bus		300	ms

NOTE:

1. Measured from falling clock edge after stop bit of write transaction

1.6 Monitors ADC Specifications

V_{CC} = 3.05 to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C unless otherwise noted.

Table 1-6. A/D Electrical Specifications

Input	Type	Range			Accuracy			Notes
		Minimum	Maximum	Units	Minimum	Maximum	Units	
Tx Power Monitor	(Internal) Current Sinking	10	1400	µA	-10	+10	%	1,2,3
Bias Current Monitor	(Internal) Current Sinking	10	1400	µA	-10	+10	%	1,2,3
Modulation Current Monitor	(Internal) Current Sinking	10	1400	µA	-10	+10	%	1,2,3
Rx Power Monitor	(External) Current Sinking	3	1400	µA	-10	+10	%	1,2,3,4
	Voltage mode	0	2.3	V	-15	+15	mV	2,8,9
Power Supply Monitor	(Internal) Voltage	2.85	3.6	V	-25	+25	mV	2,6
Internal Temperature Monitor	(Internal) Temperature	-40	+105	°C	-3	+3	°C	2,7
AUX1, AUX2	Current Sinking	10	1400	µA	-10	+10	%	1,2,3,4
	Current Sourcing	10	1400	µA	-10	+10	%	1,2,4,5
	Voltage	0	2.3	V	-15	+15	mV	2,8,9
Update Rate	All ADCs	1		kHz	–	–	–	–

NOTES:

1. For definition of sourcing and sinking see Figure 1-2.
2. Module calibration required for valid units.
3. Code 000h means 0 µA, code FFFh means 1600 µA when sinking current. However, the result is only valid in the range specified.
4. Minimum value of monitored current is achieved with internal digital filter (default setting).
5. Code 000h means 0 µA, code FFFh means 1500 µA when sourcing current. However, the result is only valid in the range specified
6. Code 000h means 0 V, code FFFh means 6.55 V. However, the supply monitoring value is only valid in the range specified.
7. ADC output will be offset binary. Code 000h means the lowest temperature the ADC can measure, while FFFh means the highest temperature the ADC can measure.
8. Input impedance of ADC is larger than 100 kΩ.
9. Code 000h means 0 V, code FFFh means 2.3 V. However, the result is only valid in the range specified.

1.7 DAC Specifications

V_{CC} = 3.05 to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C unless otherwise noted.

1.7.1 Bias and Modulation Current DAC Specifications

Table 1-7. Laser Driver Bias and Modulation Current D/A

Parameter	Minimum	Typical	Maximum	Units
Resolution	–	12	–	bits

1.7.2 Internal 6 bit DAC (PWA and BMON_MAG) Specifications

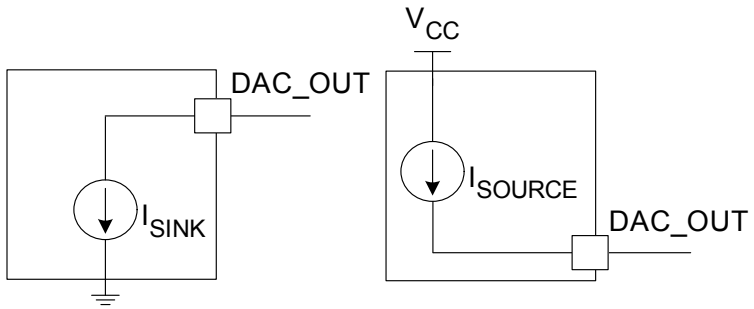
Table 1-8. Internal 6 bit DAC(1)

Parameter	Minimum	Typical	Maximum	Units
Resolution	–	6	–	bits
Full scale output (current sinking)	1.01	–	1.13	mA
Linearity				
DNL	-1	–	+1	LSB
INL	-1	–	+1	LSB
Offset	-5	–	+5	µA
Settling time	–	10	–	µs
Compliance (voltage for sinking current)	1.1	–	2.6	V

NOTE:

1. The pulse width adjust DAC is mapped to GPIO(2) and the BMON_MAG DAC is mapped to GPIO(4).

Figure 1-2. DAC Output Definitions



1.7.3 General Purpose 6 bit DAC Specifications

Table 1-9. General Purpose 6 bit DAC [1]

Parameter	Minimum	Typical	Maximum	Units
Resolution	–	6	–	bits
Full scale output current (current sourcing or sinking)	1.01	1.07	1.13	mA
Linearity				
DNL	-1	–	+1	LSB
INL	-1	–	+1	LSB
Offset				
Current source	–	–	+5	µA
Current sink	-5	-	+5	µA
Settling time	–	10	–	µs
Voltage Compliance				
Current source	0	–	1.1	V
Current sink	1.1	-	2.6	V

NOTE:

1. The General purpose 6 bit DAC is mapped to GPIO(1).

1.7.4 General Purpose 10 bit DAC Specification

Table 1-10. General Purpose10 bit DAC [1,4]

Parameter	Minimum	Typical	Maximum	Units
Resolution	–	10	–	bits
Voltage Mode Operation [2]				
Full scale output voltage	1.37	1.45	+1.53	V
Linearity				
DNL	-1	–	+1	LSB
INL	-4	–	+4	LSB
Offset	–	–	+1.5	mV
Settling time	–	10	–	µs
Output Resistance	0.8	1	1.2	kΩ
Current Mode Operation [2, 3]				
Full scale output current (current sourcing)	1.40	1.48	+1.56	mA
Linearity				
DNL	-1	–	+1	LSB
INL	-4	–	+4	LSB
Offset	–	–	+1.5	µA

Table 1-10. General Purpose10 bit DAC (1,4)

Parameter	Minimum	Typical	Maximum	Units
Settling time	–	10	–	µs
Compliance (voltage for sourcing current)	0	–	1.1	V

NOTES:

1. The General Purpose 10 bit DAC is mapped to GPIO(0).
2. Output may either be a current or a voltage. User selectable.
3. In current mode, DAC output can only source current. See Figure 1-2.

1.8 Inrush Current Specification

V_{CC} = 3.05 to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C unless otherwise noted.

Table 1-11. XFP/SFP+ POR Characteristics

Parameter		Minimum	Typical	Maximum	Units
I_{CC} Peak Inrush ($I_{CC-peak}$)		–	–	50	%
I_{CC} Ramp rate (dI_{CC}/dt) (1)	SFP+			50	mA/µs
	XFP			100	mA/µs

NOTE:

1. Excludes external capacitors. Modules which present a small capacitive load to the host during hotplug are exempt from the inrush current requirements since they limit the total in rush charge.

1.9 Host two-wire Timing Specifications

(MODDEF(1)/SCL and MODDEF(2)/SDA) (Standard Mode or Fast Mode two-wire serial) and NVRAM Controller Timing Specifications (NVRAM1 (SDA) AND NVRAM2 (SCL)) (Fast Mode two-wire serial)

V_{CC} = 3.05 to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C unless otherwise noted.

Table 1-12. Host and NVRAM Controller Timing Specifications (see Figure 1-3)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
f_{SCL_HOST}	Clock Frequency, SCL (1)		–	–	400	kHz
f_{SCL_NVRAM}	Clock Frequency, SCL		530	–	900	kHz
t_{LOW}	Clock Pulse Width Low		1.3	–	–	µs
t_{HIGH}	Clock Pulse Width High		1.0	–	–	µs
t_{AA}	Clock Low to Data Out Valid		0.05	–	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start		1.3	–	–	µs
t_{HDSTA}	Start Hold Time		0.6	–	–	µs

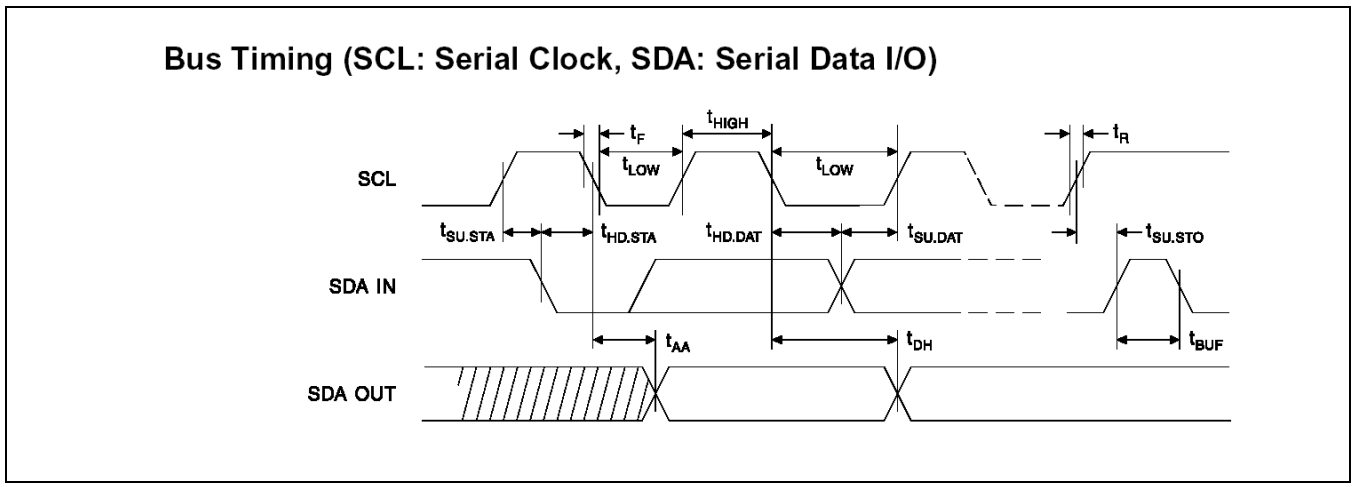
Table 1-12. Host and NVRAM Controller Timing Specifications (see Figure 1-3)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
t_{SUSTA}	Start Set-up Time		0.6	–	–	µs
t_{HDDAT}	Data In Hold Time		3	–	–	ns
t_{SUDAT}	Data In Set-up Time		100	–	–	ns
t_{SUSTO}	Stop Set-up Time		0.6	–	–	µs
t_{f_HOST}	Host Output fall time (2)	20-80%. Capacitive load for each bus line = 10 to 400 pF; $R_{PULL-UP}$ = 4.7 to 10 kΩ	–	–	100	ns
$R_{PULL-UP\_EE}$	Outputs (NVRAM1 and NVRAM2) internal pull-up resistor value (3)		–	8	–	kΩ
t_{f_NVRAM}	NVRAM Controller Output fall time (3)	20-80%. No external pull-up resistor; 13 pf loading	–	–	50	ns
t_{r_NVRAM}	NVRAM Controller Output rise time (3)	20-80%. No external pull-up resistor; 13 pf loading	–	–	300	ns
	Time bus must be free before a new transmission start.	Between STOP and START	20			µs
t_{DH}	Data Out Hold Time		50	–	–	ns

NOTES:

1. The host two wire bus is fully compliant with SFP timing requirements to run at 400 kHz.
2. For the host interface, the output rise time is determined by user selection of $R_{PULL-UP}$ and the total line capacitance.
3. NVRAM two-wire bus only. Since the M02171 NVRAM1/NVRAM2 is a dedicated two-wire serial bus to the external EEPROM, the M02171 internally includes $R_{PULL-UP}$ to eliminate adding these extra external components.

Figure 1-3. Host and NVRAM Controller Timing Diagrams



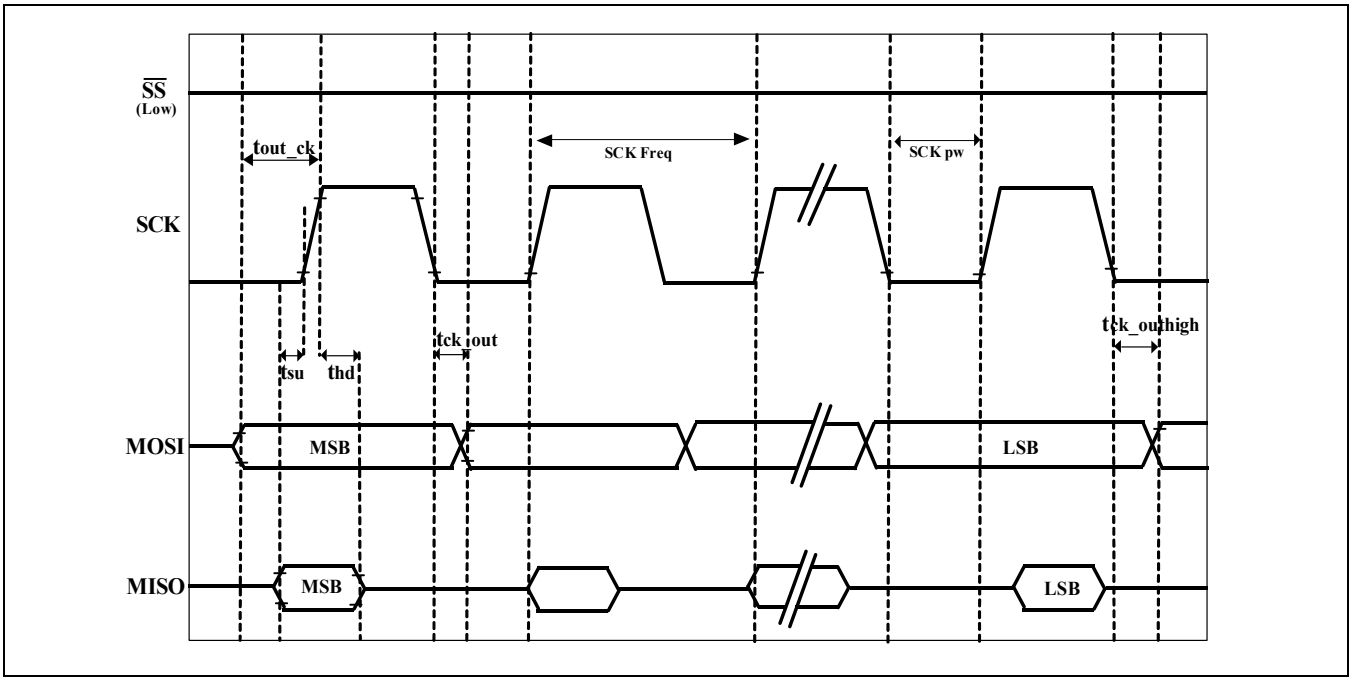
1.10 SPI Electrical Timing Specifications

V_{CC} = 3.05 to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C unless otherwise noted.

Table 1-13. SPI Electrical Timing Specifications

Symbol	Parameter	Min	Typ	Max	Units
	SPI_CK Frequency			10	MHz
	SPI_CK Pulse Width		50% duty cycle		%
	Rise/Fall time		3.6		ns
t_{su}	Setup time		10		ns
t_{hd}	Hold time		10		ns
t_{out_ck}	Out to SPI_CK		0.5 x t_{sck}		ns
t_{ck_out}	SPI_CK to Out		10		ns
$t_{ck\_outhigh}$	SPI_CK to Out high		10		ns

Figure 1-4. SPI Timing Diagram. External controller is Master and M02171 is Slave



1.11 Control and Status I/O Timing

V_{CC} = 3.05 to 3.55V, T_A = -40°C to +95°C, unless otherwise noted. Typical values are V_{CC} = 3.3V, T_A = 25°C unless otherwise. Timing values are for hardware pins.

Table 1-14. Timing Requirements of SFP/XFP/SFP+ Control and Status I/O

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
t_off	TX_DIS assert time	Rising edge of TX_DIS to fall of output signal below 10% of nominal		–	10	µs
t_on	TX_DIS negate time	Falling edge of TX_DIS to rise of output signal above 90% of nominal		–	1	ms
t_init(1)	Time to initialize, including reset of TX_Fault	Time from power on or negation of Tx_Fault using TX_DIS until laser driver output is stable		–	300	ms
t_fault	TX_Fault assert time	From occurrence of fault condition to TX_Fault high		–	100	µs
t_reset	TX_DIS time to start reset	Time TX_DIS must be held high to reset TX_Fault. TX_DIS pulse width required to initialize safety circuitry or reset a latched fault.			10	µs
P-Down/ RST_on	P_Down /RST assert delay	From power down initiation			100	µs
	P_Down reset time	Min length of P_down assert to initiate reset	10			µs

NOTE:

1. From power on or hotplug after supply OK or from falling edge of P_Down/Rst

2.0 Pin Definitions

Table 2-1. Pin Descriptions

QFN Pin Number	Name	Function
1	NVRAM1 (SDA)	SDA interface to external EEPROM (internally pulled up to V_{CC} with 8 kΩ)
2	NVRAM2 (SCL)	SCL interface to external EEPROM (internally pulled up to V_{CC} with 8 kΩ)
3	MODDEF(1)/ SPI_O	For 2-wire: MODDEF1 is the serial clock For SPI: SPI_O is slave output
4	MODDEF(2)/ SPI_I	For 2-wire: MODDEF2 is the serial data For SPI: SPI_I is slave input
5	V_{CC}	3.3V power supply.Connect to 3.3V
6	Pwdn/Rst	Control input. 60 kΩ internal pull up to V_{CC}. When held high, forces the part into a power down standby mode. The negative edge of Pwdn/Rst signal initiates a complete part (POR) reset. Ground for normal operation
7	DINP	Positive Data Input
8	DINN	Negative Data Input
9	SPI_sel	Control input. When held high indicates SPI is selected (internally pulled down with 60KΩ). When low I2C is selected
10	V_{CC}_LD	V_{CC} for the laser driver section. Connect to V_{CC}
11	TX_Fault	Safety circuit fault indicator. Open collector output, external resistor pull up to host_V_{CC} required
12	TX_DIS	Control input for Transmit disable. When high or left floating, shuts off both bias and modulation outputs. Set low for normal operation. 7 kΩ internal resistor pull-up to V_{CC}
13	GND	Ground. Must be connected to ground for proper device operation
14	IPIN	Photodiode current monitor
15	$IBOUT_{CA}$/SGND	Bias current output for common anode operation. Internal ground switch for common cathode operation
16	GND0	Ground for modulation output stage. Must be connected to ground for proper device operation
17	CC_{sel}	When high, common cathode is selected. When low or floating, common anode is selected (internally pulled down with 60 kΩ)
18	OUTP	Positive modulation output
19	OUTN	Negative modulation output
20	GPIO(4)/ BMON DAC	Analog General Purpose I/O. Input or Output or 6bit DAC (current sinking only)
21	SVCC/ $IBOUT_{CC}$	Internal supply switch for common anode operation. Bias current output for common cathode operation
22	A/D_{AUX2}	Auxiliary A/D input
23	BIAS_R	External resistor for precision bias reference
24	A/D_{AUX1}	Auxiliary A/D input

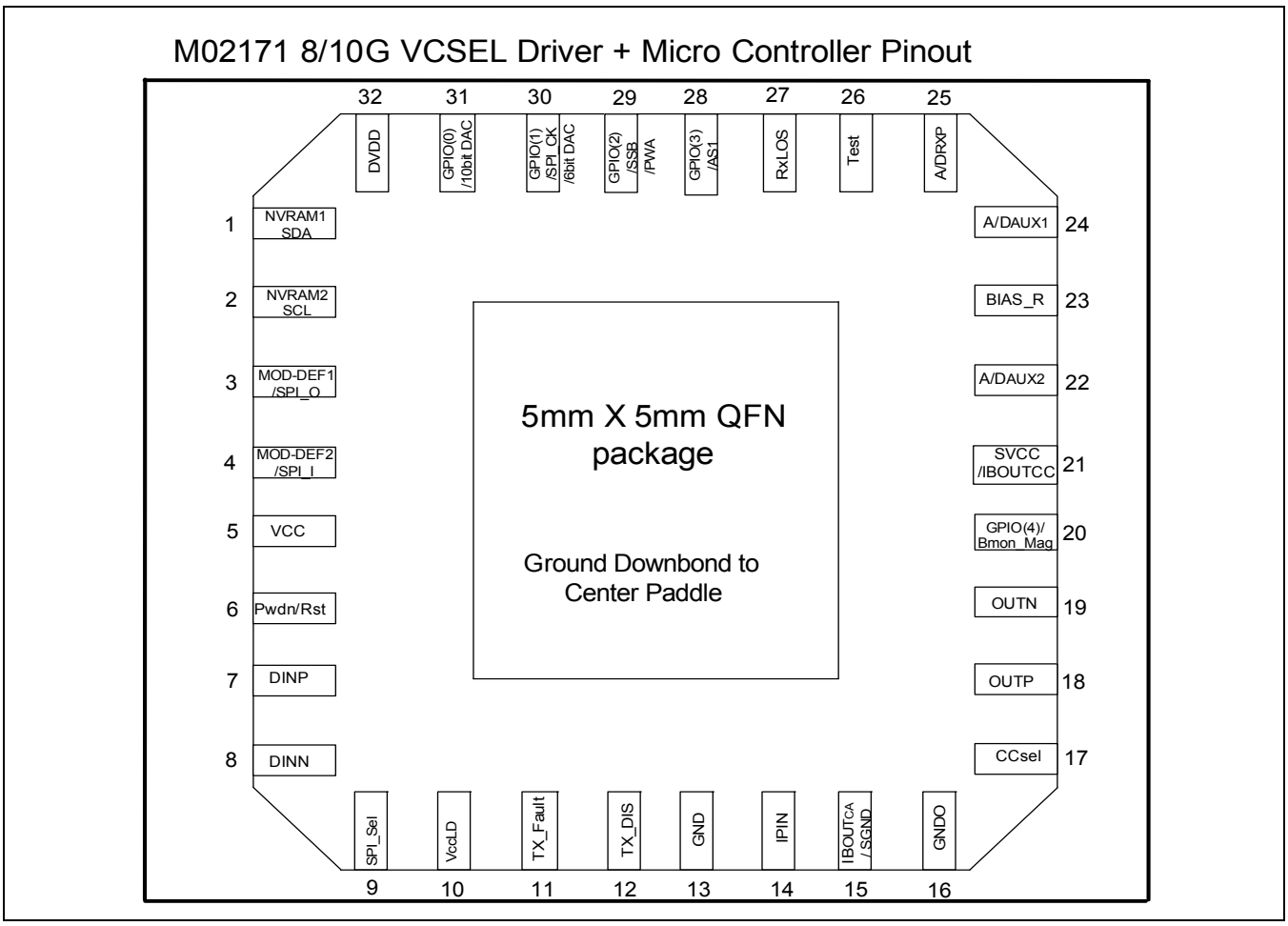
Table 2-1. Pin Descriptions

QFN Pin Number	Name	Function
25	A/D_{RxP}	A/D input for received power monitor
26	TEST	Input for self test. When high, self test is initiated.Connect to ground for normal operation. (internally pulled down with 60 kΩ)
27	RxLOS	Can be selectable Input or Output. If used as input pin, it is Loss of signal from limiting amp (internally pulled down with 60 kΩ). If used as output, it's an ope collector output
28	GPIO(3)/RS1	For SFP+: Can be configured as RS1 rate select (internally pulled down with 60 kΩ using an internal switch) For non SFP+: General purpose I/O
29	GPIO(2)/SS /PWA	For SPI interface: Slave Select is input to M02171 (should be externally terminated with resistor required for application). Must be low before the data transaction and stay low for the duration of the transaction. For non-SPI: General purpose I/O or 6bit DAC. Current sink only
30	GPIO(1)/ SPI_CK/6bit DAC	For SPI interface: SPI_CK is the clock input (10MHz) For non SPI: General purpose I/O or 6 bit DAC (current sourcing or sinking)
31	GPIO(0)/ 10 bit DAC	General purpose I/O or 10 bit DAC. Output can be current or voltage. In current mode, DAC output can only source current
32	DVDD	Internally regulated to 1.8V for Digital circuitry. Typically connect a 10nF capacitor to ground
Paddle	GND	Ground. Must be connected to ground for proper device operation

Table 2-2. GPIO PIN Mapping

QFN Pin Number	Pin Name	Integrated Mode SFP Function	External Micro mode SFP Function	External Micro mode XFP Function
20	GPIO(4)/ BMON_MAG DAC	GPIO or DAC	GPIO or DAC	GPIO or DAC
28	GPIO(3)/ RS1	RS1 or GPIO	RS1 or GPIO	GPIO
29	GPIO(2)/ $\overline{SS}$ /PWA DAC	GPIO or DAC	GPIO or DAC	GPIO or DAC
30	GPIO(1)/ SPI_CK/ 6 bit DAC	GPIO or DAC	GPIO or SPI or DAC	GPIO or SPI or DAC
31	GPIO(0)/ 10 bit DAC	GPIO or DAC	GPIO or DAC	GPIO or DAC

Figure 2-1. Pin Assignments for M02171 Device



NOTE: The package bottom must be adequately grounded to ensure correct thermal and electrical performance. Please reference the Amkor Application Note “Application Notes for Surface Mount Assembly of Amkor’s MicroLeadFrame (MLF) Packages” at www.amkor.com (http://www.amkor.com/products/notes_papers/MLFAppNote.pdf).

3.0 Functional Description

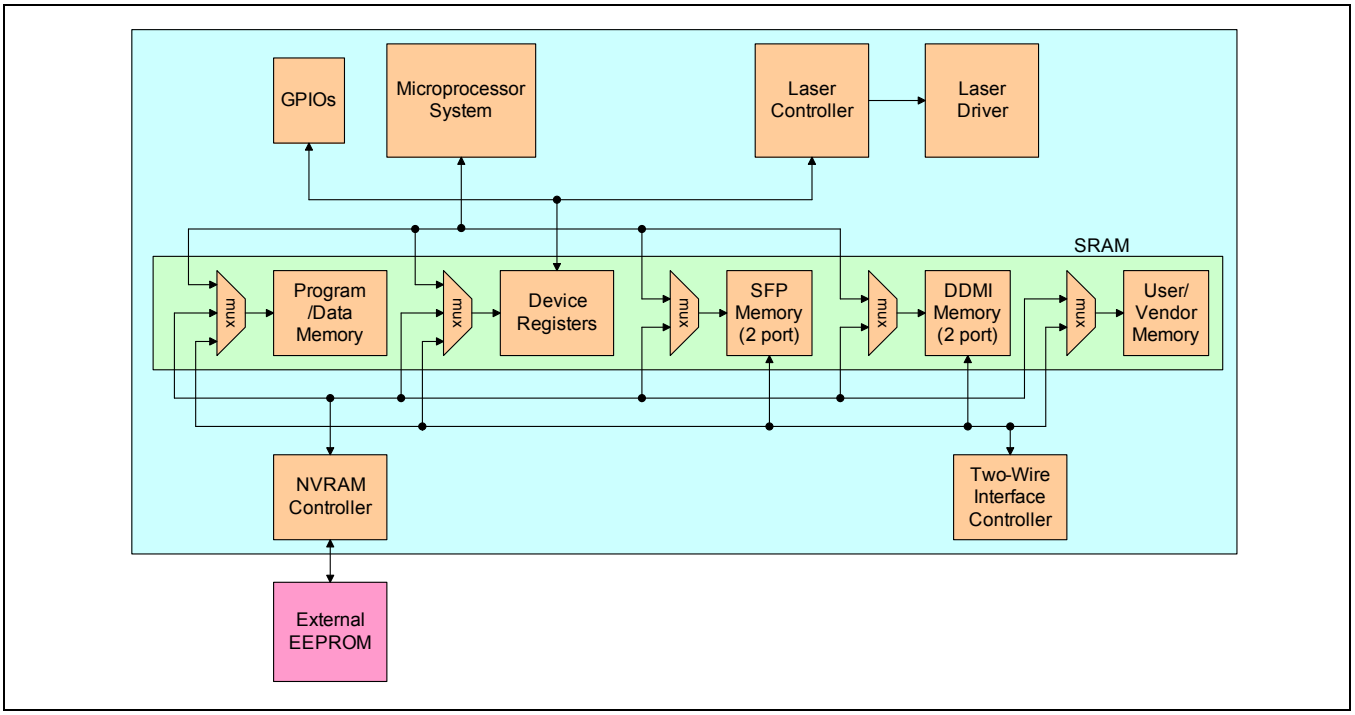
3.1 Overview

The M02171 provides a highly integrated SFF-8472 solution for fiber optic transceivers. It combines the Digital Diagnostic Monitoring Interface for SFF-8472 with a laser driver compatible with VCSELs.

The M02171 monitors temperature, voltage, bias and modulation current, transmit receive power, and other user-defined external parameters. Internal ADCs and comparators allow each parameter to be compared against user-defined threshold levels to provide indication of a fault condition. Integration of the laser driver provides digital control of the laser bias and modulation currents in addition to pulse width control of the modulation current.

Integrated safety circuitry provides latched bias and modulation current shutdown if a fault condition is detected and provides an internal V_{CC} switch for common anode operation and an internal ground switch for common cathode operation.

Figure 3-1. M02171 Architecture



3.2 Features

- Laser Driver with integrated digital diagnostic functions
- 155 Mb/s – 11.3 Gb/s operation
- Integrated power supply switch for redundant shutdown
- Dual closed-loop OMA control, single-closed-loop and open-loop operation with independently programmable bias and modulation currents
- Compliant with SFF-8431, Rev 3.1 “SFP+” standard for 8.5 and 10.3Gbps
- Compliant with SFF-8472, Rev 10.3: Diagnostic Monitoring Interface for Optical Transceivers
  - Temperature
  - Bias current
  - TX Optical Power
  - RX Optical Power
  - Supply voltage
- Software control of Rate Select, Tx Fault, Tx Disable and Rx LOS
- Alarm/Warning flags are implemented for monitored quantities
- Supports Internal test and calibration
- Automatic power control
- SFP/SFP+ compliant safety circuitry with user selectable bypass
- Pulse width adjustment compensates for asymmetrical laser rise and fall times
- Five user configurable General Purpose I/Os
- Up to four user configurable DAC outputs
- Two available auxiliary 12 bit ADC inputs
- SPI or 2-wire interface, compatible with Serial ID, as defined in the SFP MSA
- Internal A/D – D/A loopback for real time diagnostics
- User and OEM password protection
- Power-on meter (journal timer)
- 12 bit ADC resolution results in exceptional monitor accuracies
- Compact: 32 pin QFN, 5mm x 5mm
- Operating Temp: -40 °C to +95 °C

3.3 General Description

3.3.1 Overview

The M02171 integrates the digital diagnostic monitoring requirements of SFF-8472 with a highly integrated laser driver intended for applications to 11.3 Gbps. The level of integration allows easy set up and calibration of laser power and extinction ratio. The timing requirements of SFF-8472 and the SFP/SFP+ MSA are met when using the M02171 including soft control timing and status functions of both standards. In addition, integration allows the modulation current monitor to be available digitally and two auxiliary A/Ds are available for customer use in providing features beyond the standards requirements.

The M02171 provides a turn-key solution for SFF-8472 and SFP/SFP+ compliant modules by including firmware that provides the mandatory features of both and enables the manufacturer to easily implement any optional features of their choosing using a simple GUI interface. The M02171 enables automatic module calibration and test that allows for a significant reduction in test cost and complexity.

Many features are user-adjustable, including the APC loop bias control, modulation current including temperature compensation control of the modulation current and laser pulse width adjustment. The M02171 utilizes control of both the bias and modulation currents which allows for management of the optical extinction ratio by compensating for the effects of temperature and aging of the laser.

Safety circuitry is also included to provide a latched shut-down of laser bias and modulation current if a fault condition occurs. An internal V_{CC} switch provides redundant shutdown when operating the device. Safety logic behavior is user configurable.

3.3.2 Digital Diagnostic Monitoring Interface Features

This section provides detail on how the Digital Diagnostic Monitoring Interface specified in SFF-8472 is supported in the M02171. The DDMI data is stored in an external EEPROM and accessed through the two-wire serial interface. EEPROM memory is also required to store SFP/SFP+ data, microprocessor code and initial device register values. In order to minimize the additional module complexity and expense of multiple external EEPROMs, the M02171 employs internal memory caches to store the SFP and DDMI data on-chip.

There are two serial interfaces. One (pins MODDEF2_SDA and MODDEF1_SCL) provides access by the host to the stored data. The other (pins NVRAM1_SDA and NVRAM2_SCL) is the interface to the single external EEPROM. Upon power-up, when the device comes out of reset, the device register values are downloaded, followed by the SFP and DDMI data and finally, the microprocessor program code is downloaded and the microprocessor enabled. The timing requirements are given in the Product Specifications Section 1.5, “Soft Control Timing Management,” on page 8.

Two time-stamped versions of the DDMI data are stored in the EEPROM (DDMI 0 and DDMI 1, see Figure 4-4) to ensure that at least one valid data set is available in the event that a module failure occurred when the M02171 was in process of writing data from the on-chip cache memory to the external EEPROM. Each data set (DDMI 0 and DDMI 1) has a checksum for the purpose of determining data integrity. The most recent valid data set is copied to the cache. The SFP data and the microprocessor program code each have their own checksum to determine their integrity similar to the DDMI data.

While the module is in an active state, the data in the DDMI cache is updated by the microprocessor at intervals in compliance with the timing requirements of SFF-8472. The host also has access through the serial interface. To comply with the data integrity requirement, the microprocessor first checks to determine if the host is accessing data before updating the memory. In that event, the update is delayed until the activity ceases. Before the update occurs, the microprocessor also disables the acknowledgement signal of the two-wire interface to prevent the host from initiating a memory access while the cache is being updated.

3.3.2.1 DDMI Real-Time Diagnostic Monitoring

Each monitor is independently enabled (to conserve power) by programming the corresponding bit of the ADC_EN register to a 1. The M02171 DDMI memory is updated by the internal M02171 controller with an update interval of < 100 ms (typically 30 ms). The internal M02171 controller must supply the appropriate password before it is allowed to update the DDMI information to prevent corruption of the data if the controller arrives at an unstable state.

The “Ack” of the two-wire interface is disabled during DDMI update. To minimize the duration of the interruption of host access, the internal M02171 controller writes the updated information to shadow registers which is then burst-loaded into the DDMI memory. The interruption of host access will be < 1.2 μs.

The DDMI information is periodically copied back to the external EEPROM for protection against loss due to events such as power outages. The frequency of backup is once every twelve hours (derived from the journal timer). Backup of serial ID, diagnostic and other on-chip memory can be initiated by the host through the two-wire interface.

Having separate on-chip and external nonvolatile storage of the DDMI data is a distinct advantage of the M02171 because it allows rapid update of the DDMI data available to the host without exhausting the write endurance of the EEPROM in a short time period. The two most recent backups of the DDMI data are maintained in the external EEPROM at all times. This ensures that a valid data set remains if there is a module failure during the backup operation. Each version has a checksum and a time stamp which determines the most current version. If the information must be reloaded to the on-chip memory, the most recent version with a valid checksum is copied from the EEPROM. The backup operation is transparent to the host with no access interruption.

3.3.3 Calibration

The M02171 supports both internal and external calibration as defined by SFF-8472. For internal calibration, the calibration is performed by the M02171 internal controller under software control. For external calibration, the controller simply writes the ADC values to the DDMI memory. One of the two calibrations modes must be enabled to achieve the accuracy specifications.

3.3.4 Alarm and Warning Thresholds

The M02171 supports all the alarm and warning indications defined in SFF-8472. Each A/D quantity has a corresponding high alarm, low alarm, high warning and low warning threshold. These values are defined by the module manufacturer during module initialization and/or calibration and allow the module user to determine when a particular value is outside of “normal” limits as determined by the module manufacturer. For these indications to be active the thresholds defined in Table 3.15 of SFF-8472 Rev 10.3 “Alarm and Warning Thresholds (2-Wire Address A2h)” must be set. The nominal response time from an alarm or warning condition to the update of the corresponding status bit is 100 msec.

The M02171 provides very accurate indication of the present conditions of the module. The sampled diagnostic monitoring signals are stored in device registers. The comparison of each to the corresponding stored threshold values is performed under program control of the microprocessor. Using firmware it is possible to compensate the alarm and warning indications for temperature variations.

3.3.5 Optional Status and Control Bits

The M02171 supports all optional status and control bits (byte 110 of 2 Wire address A2h)defined in Table 3.17 of SFF-8472 Rev 10.3.

3.3.6 Data Inputs

The inputs to the internal data buffer are self-biased through resistors to an internal reference voltage V_{TT}. Input signals can be AC coupled to the part by allowing V_{TT} to float, which sets the common mode input voltage to approximately V_{CC} - 1.3V. Both CML and PECL input signals can be AC coupled to the M02171.

3.3.7 Equalization

For SFP+ applications, the input data can be equalized by enabling the equalizer. SFP+ specifies the jitter requirements at the input of the transmitter under various host board transmission line lengths for both microstrip and stripline. Table 3-1 shows common host board configurations with maximum recommended SFP+ host board trace lengths.

Table 3-1. Host board PCB maximum trace lengths

Type	Material	Trace Width (mm)	Loss Tan	Trace Length (mm)
Microstrip	Standard FR4 (4000-6/8)	0.3	0.022	200
	Nelco (4000-13)	0.3	0.016	300
Stripline	Standard FR4 (4000-6/8)	0.125	0.022	150
	Nelco (4000-13)	0.125	0.016	200

3.3.8 Data Polarity / Pulse Width Adjust

After the data passes through the data input buffer, it enters the pulse width adjust buffer. It incorporates a polarity selection as well as a pulse width adjustment control to compensate for laser pulse width distortion. By adjusting the current from the PWA DAC, pulse width can be adjusted from 20% to 80%. Pulse width control can be disabled by setting the PWA_EN bit low, resulting in approximately 50% crossing point at the output and reduces the supply current by 2mA.

3.3.9 Output Buffer

After the data passes through the pulse width adjust buffer, it enters the output buffer. The output buffer reshapes and ground reference the signal in order to drive the output stage with enough speed and correct output levels.

3.3.10 Photodiode polarity

M02171 supports common anode or common cathode photodiode independently from the laser mode.

3.3.11 Rate select function

To comply with the SFP+ rate select requirement, when the device in low rate mode, power is reduced in the signal path and the compensation is switched on at the outputs.

3.3.12 Pwdn/Rst

This is a multifunction input pin for module power down and reset. When held “high”, in order to meet the power dissipation requirements of XFP applications, the laser is forced to low rate mode and the modulation and bias currents are not set by the DAC. They are set by an internal current reference of low value in order to reduce the power dissipation of the module.

3.3.13 Laser Driver Output Stage

The output stage incorporates feedback to maintain performance over the range of laser modulation current. The output stage is nominally configured to be AC coupled to VCSEL’s with resistances from 40 - 100Ω. The M02171 has internal 50Ω terminations between the outputs (OUTP and OUTN) and the internal supply.

The laser driver output stage is separately grounded from the rest of the circuitry (through GNDO) for optimum performance and control of output characteristics.

Two independent high-frequency compensation networks are included to allow additional flexibility with setting the output response characteristics. A binary network and an additional three bits (OC0, OC1, OC2) can be used to

tune two separate internal RC networks at the M02171 output providing control of output stage damping in order to optimize the optical eye diagram.

Laser modulation current is controlled by adjusting the MODSET DAC current. The modulation current can be temperature compensated in the digital state machine by changing the MODSET DAC current by a programmed ratio to the temperature ADC reading. Refer to Section 3.3.16, “Modulation Current Control,” on page 27.

When Pwdn/Rst is high, the MODSET DAC is disconnected and the modulation is set below its lowest value.

3.3.14 GPIO Operation

The M02171 has five GPIOs that can individually be configured as a digital input, a digital input with an interrupt, a digital output, or the output of a DAC. When configured as a digital input the device firmware responds to the signal level on the GPIO. The rate of polling of the GPIO configured as a digital input is defined within the firmware which if implemented, would typically result in polling intervals of 20 ms. The digital input with an interrupt is used in the same way, but as an interrupt the response time to a signal change is typically 3 ms. The interrupt method is completely configurable as one of the four following formats: low level or high level causes the interrupt, or rising or falling edge causes the interrupt. As a digital output, the level can be fixed during device initialization/calibration or can be varied by the device firmware (i.e. as a rate select output to a limit amp responding to the module rate select input). Finally, each GPIO can be the output of one of the internal DACs. The DAC mapping is shown in the block diagram and similar to a digital output, the level can be fixed during device initialization/calibration or can be varied by the device firmware changing the DAC setting in response to a defined event.

3.3.15 Automatic Power Control

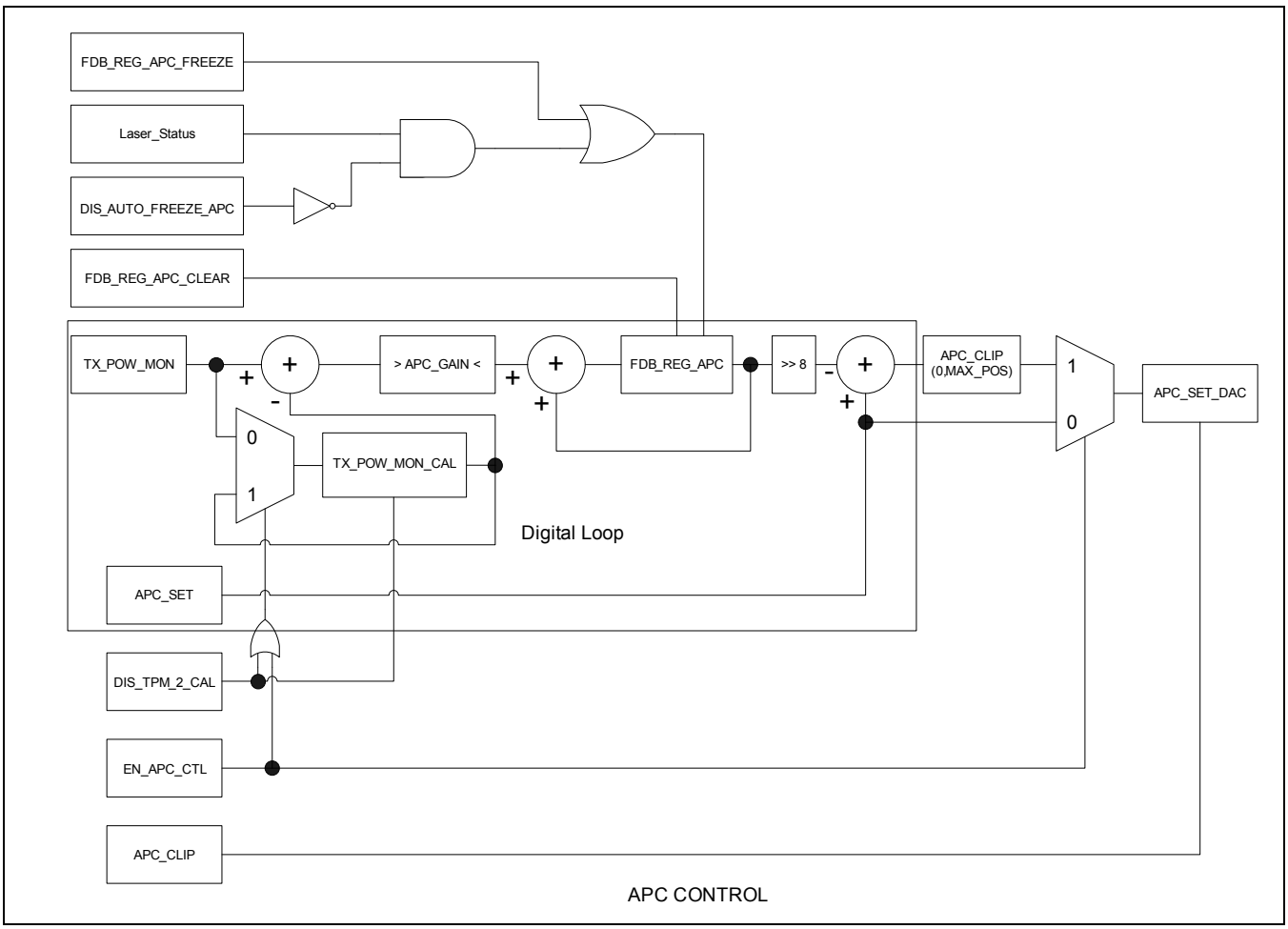
The M02171 incorporates unique and innovative options for controlling the transmitted laser power. Control mechanisms are provided for controlling both the bias current and the modulation current. Each includes multiple techniques which can be independently enabled or disabled. This allows maximum configurability in a wide variety of applications and choice of laser.

3.3.15.1 Bias Current Control

The M02171 allows two methods of controlling the laser bias current: closed loop digital control and open loop control. Each mode is enabled by selections made within the device register settings.

Control of the bias current is illustrated in Figure 3-3. TxPwrMon is an internally mirrored replica of the current flowing into IPIN. The updated TxPwrMon value is written to the TX_POW_MON registers. All modes start with setting the target output power by writing to the APC_SET registers.

Figure 3-2. Bias Current Control



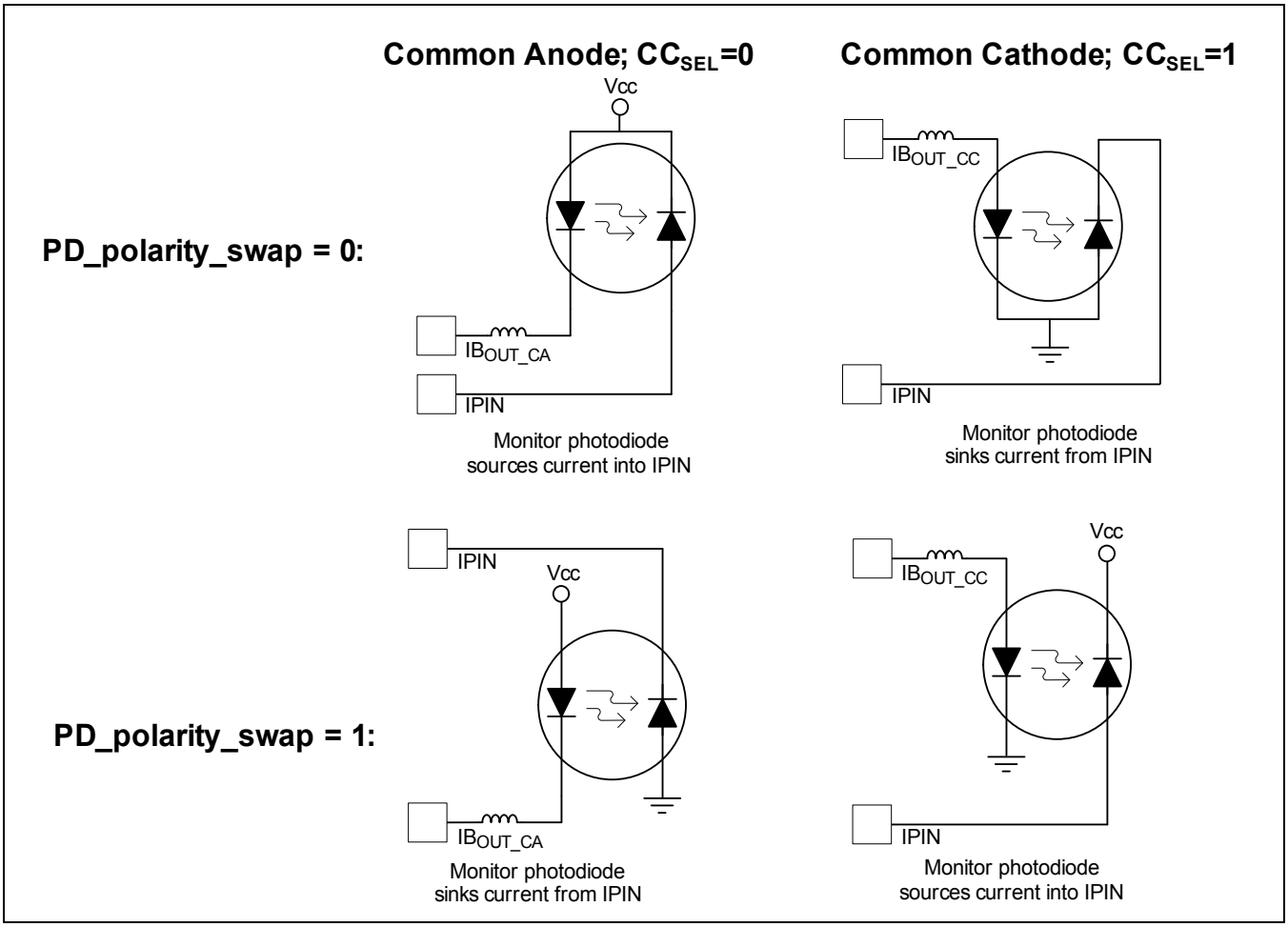
3.3.15.1.1 Closed loop Digital Control

M02171 includes circuitry to automatically maintain laser average output power with use of a monitor photodiode. Figure 3-3 shows various photo diode connection and PD polarity swap configuration examples.

Closed loop digital control is configured by setting EN_APC_CTL high. In closed loop digital control mode the APC_SET registers are the uncalibrated reference level for the average optical power. Closed loop digital control varies the bias current (using the APC_SET_DAC value) to maintain the measured TX_POW_MON equal to the value stored in the TX_POW_MON_CAL registers during module calibration.

Closed loop digital control is a state machine that utilizes the laser monitor photodiode and requires the desired average value of the output optical power to be stored in the TX_POW_MON_CAL registers. An internal current mirror mirrors the monitor photodiode current at IPIN and is labelled TxPwrMON. The most recent value of TxPwrMon is stored in the TX_POW_MON register. The M02171 utilizes a precision integrator (low pass filter) on TX_POW_MON. The output of the integrator is compared to the desired average value of optical power in the TX_POW_MON_CAL registers and the resulting 12 bits adjusts the bias current up or down accordingly through the APC_SET_DAC registers.

Figure 3-3. PD polarity swap configuration examples



3.3.15.1.2 Open loop Control

With open loop control there is no feedback from the laser output to the bias control. A value is simply written that corresponds to the desired value of the output bias current. The bias current maintains this output level regardless of laser performance unless a fault condition occurs whereby the safety loop disables the bias current output.

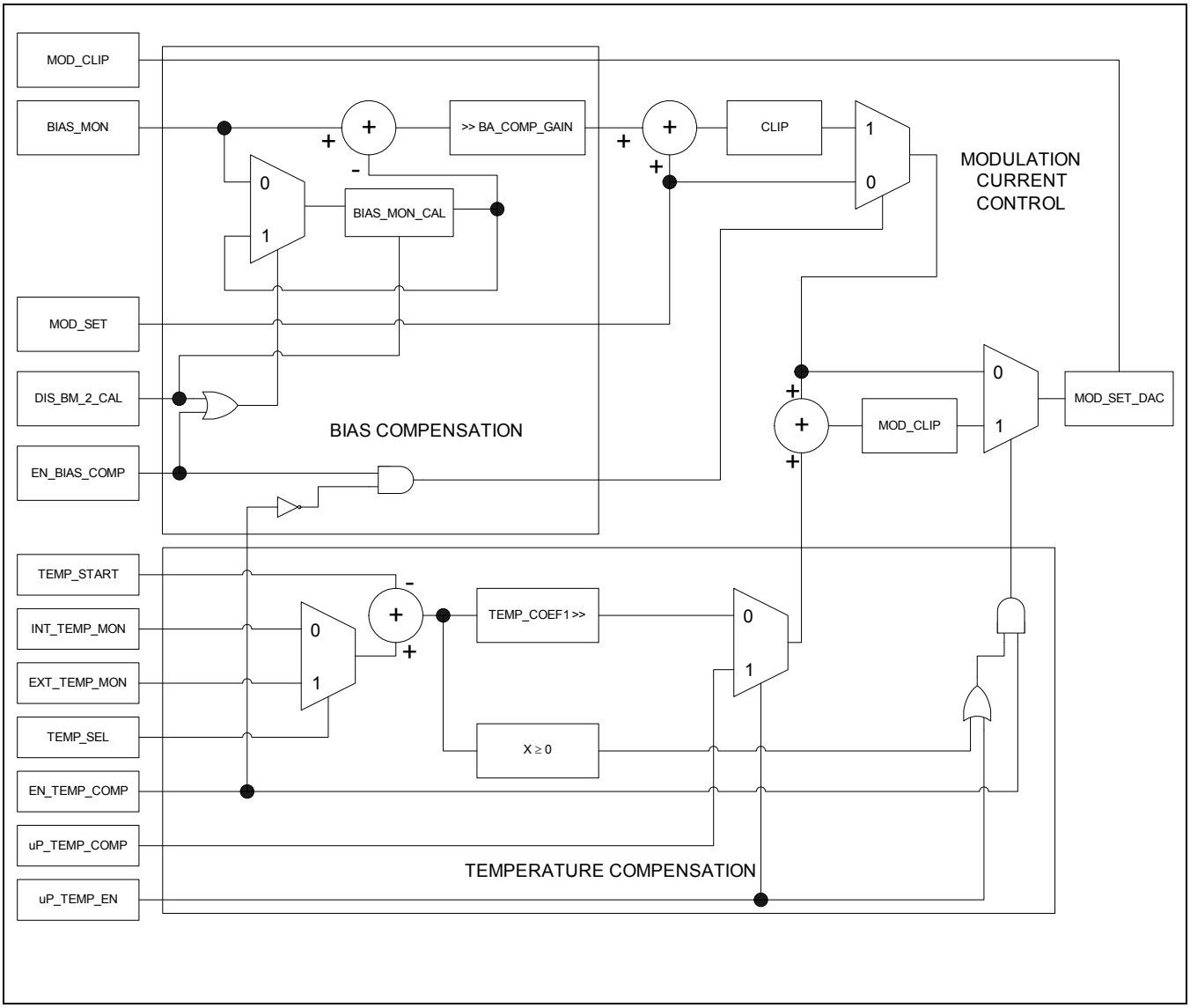
Open loop control of the bias current is achieved by setting EN_APC_CTL low and writing the desired value of the APC_SET DAC input to the APC_SET register.

Even though the bias current is operating open loop, it is possible to implement temperature compensation under firmware control by using either a look-up table or a polynomial to modify the value with temperature.

3.3.16 Modulation Current Control

Control of the modulation current is open loop with programmable compensation for changes in the bias current and for changes in the temperature. This is illustrated in Figure 3-4.

Figure 3-4. Modulation Current Control



The target modulation current is set by writing to the MOD_SET register.

3.3.16.1 BIAS-Adjusted Compensation of Modulation Current

This form of compensation is configured by setting EN_BIAS_COMP high and EN_TEMP_COMP low. The BIAS_MON ADC is periodically sampled. The new MOD_SET_DAC value is computed based on a ratio set in the BA_COMP_GAIN register.

The register BA_COMP_GAIN is equivalent to “percent bias current slope” factor adjustment on the modulation current. If BIAS_MON (the present bias monitor output) is larger than the BIAS_MON_CAL value (established

during module calibration) the modulation current is increased proportionally to their differences (times the programmable constant BA_COMP_GAIN). If the BIAS_MON is smaller than BIAS_MON_CAL then the modulation current is decreased. In this sense, compensation using bias is different from compensation using temperature since BIAS_MON_CAL is a reference current and all modulation current adjustments are made based on any change from this current rather than only by temperature alone.

3.3.16.2 Temperature Compensation of Modulation Current

This form of compensation is configured by setting EN_TEMP_COMP high (default). When enabled, temperature compensation takes precedence over bias-adjusted compensation. The temperature reading can come either from the internal temperature ADC or an external temperature sensor connected to the auxiliary A/D_{AUX2} input, and is selectable by the TEMP_SEL register.

The temperature threshold at which temperature compensation is to start is written into TEMP_START. The first order temperature compensation coefficient TEMP_COEF1 is programmable between -12 to +11. The difference between TEMP_START and the current temperature is multiplied by 2^(TEMP_COEF1). The product is then added to the input MOD_SET and the MOD_SET_DAC value is the result.

The TEMP_START value is in terms of the 12 bit temperature value out of the temperature monitor whether it is based on the internal or an external sensor. The register Temp_Coef1 is the gain applied to the difference between INT_TEMP_MON (or EXT_TEMP_MON) and Temp_Start. The result is the modulation current compensation.

Second order temperature compensation is provided by the internal device controller through the register uP_TEMP_COEF by enabling uP_TEMP_EN. If uP_TEMP_EN is high then temperature compensation will come from the firmware through uP_TEMP_COEF. Through the use of firmware compensation, both look-up tables and higher order compensation are possible and can be used to compensate for modulation current versus temperature.

3.3.17 Current Monitors

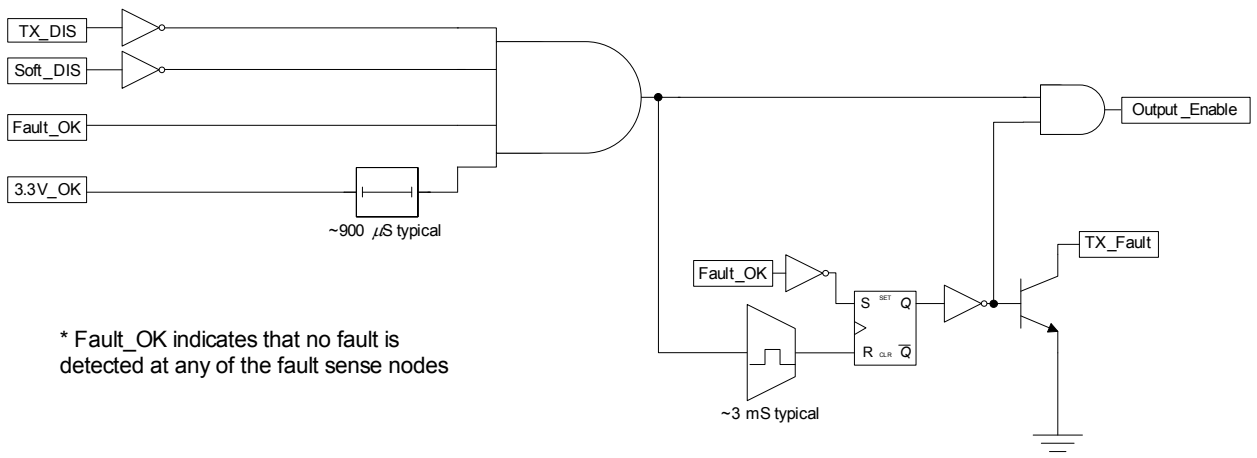
Internal monitors are provided for transmit power ($TxPwr_{MON}$), bias ($BIAS_{MON}$) and modulation current (MOD_{MON}). These are reported through the $TxPwr_{MON}$, $BIAS_{MON}$ and MOD_{MON} A/D registers.

3.3.18 Laser Eye Safety

Using this laser driver in the manner described herein does not ensure that the resulting laser transmitter complies with established standards such as IEC 825. Users must take the necessary precautions to ensure that eye safety and other applicable standards are met. Note that determining and implementing the level of fault tolerance required by the applications that this part is going into is the responsibility of the transmitter designer and manufacturer since the application of this device cannot be controlled by Mindspeed.

3.3.19 Safety Circuitry

Figure 3-5. M02171 Safety Logic (Safety Circuit Bypass Function not Shown)



For information on bypassing the safety logic, see Section 3.3.19.1, “Safety Circuitry Bypass,” on page 29.

Comparators at $V_{CC}LD$, $IBOUT_{CA}$, $IBOUT_{CC}$, IPIN and OUTP will assert the TX_Fault output (and will set the appropriate bit in the Diagnostics 2 area of the DDMI memory map Table 4-1) indicating that a fault condition has occurred. This condition is latched and requires SOFT_DIS or TX_DIS to be toggled or device should be power cycled before device reset occurs. SV_{CC} is opened during a fault or disable condition.

By setting either TX_DIS high or SOFT_DIS high, the bias and modulation output currents are disabled. TX_DIS will disable laser bias and modulation current if left floating. TX_DIS must be forced to a low state to enable the outputs.

Safety Circuitry in the M02171 will disable the modulation and bias current and assert the TX_Fault output immediately upon detecting a fault condition. In addition, the supply voltage that sources the laser current (SV_{CC}) will immediately go open circuit and prevent any current from passing through the laser.

Fault conditions checked by the M02171 include shorts to ground or V_{CC} of all pins which can increase the laser power directly or indirectly (i.e. control circuitry).

For an initialization or power-up sequence to be successful, all the fault detection monitors must signal that the device is “healthy”, unless bypassed (see Section 3.3.19.1).

When TX_DIS goes low, pins are checked for shorts to ground or V_{CC} and a TX_Fault condition is latched if there is a fault.

If the state of the pins is OK, a one-shot at the reset pin begins a countdown which will latch a TX_Fault condition if the bias current has not stabilized to an acceptable level during the one-shot time.

The one-shot width is approximately 3 ms.

3.3.19.1 Safety Circuitry Bypass

The M02171 provides the module vendor the ability to change the behavior of the safety logic. As described above, and shown in Figure 3-5, the default operation is that when a fault is detected, the TX_Fault output is asserted and latched and the laser modulation current is disabled.

There are two registers: Laser Driver Control Register 0 and Laser Driver Control Register 1 that allow the module vendor to determine how the M02171 responds to a fault condition. The soft_scb bit of LD Control Register 0 allows the safety circuitry bypass to be enabled.

When safety circuitry bypass is enabled, a fault condition no longer immediately disables the laser modulation current but will assert the TX_Fault output (and set the appropriate bit in the Diagnostics 2 area of the DDMI memory map Table 4-2) indicating that a fault condition has occurred. This condition is latched and can be cleared by toggling either SOFT_DIS or TX_DIS or power cycling the device. However, the result is that laser modulation is interrupted. An alternative method to reset the TX_Fault latch is available when bypass is enabled, the reset_fail bit of LD Control Register 1 will reset the TX_Fault latch and not interrupt the laser output.

Additionally, there is the provision to disable the latching of the TX_Fault output completely. This is accomplished using Latch_override bit in LD Control Register 1. When enabled, it disables the latching of the TX_Fault output meaning that the TX_Fault output will only remain asserted as long as a fault condition persists. If the fault condition is transient, the TX_Fault output will de-assert when the transient condition causing the fault passes.

3.3.19.2 Fault Conditions

This section describes the M02171 operating modes during fault conditions. Over voltage, under voltage, pins shorted to V_{CC} and pins shorted to ground are included in the fault Table 3-2.

Table 3-2. Circuit Response to Single-Point Fault Conditions

Pin Number	Pin Name	Circuit Response to Over-voltage Condition or Short to Vcc	Circuit Response to Under-Voltage Condition or Short to Ground
1-4	NVRAM1, NVRAM2, MOD-DEF(1) MOD-DEF(2)	Does not affect laser power.	Does not affect laser power.
5	V_{CC}	Outputs are disabled if V_{CC} exceeds the supply detection (high level) threshold.	Outputs are disabled if V_{CC3} voltage is below the supply detection (low level) threshold.
6	Pwdn/Rst	Module stays in power down mode	Does not affect laser power.
7, 8	D_{IN}+, D_{IN}-	The APC loop will attempt to compensate for the change in output power. If the APC loop can not maintain the set average power, a fault state occurs.(1, 2)	The APC loop will attempt to compensate for the change in output power. If the APC loop can not maintain the set average power, a fault state occurs.(1, 2)
9	SPI_sel	Does not affect laser power.	Does not affect laser power.
10	V_{CC}LD	Laser bias current will be shut off, then a fault state occurs.(1)	A fault state occurs.(1)
11	TX_FAULT	Does not affect laser power.	Does not affect laser power.
12	TX_DIS	Bias and modulation outputs are disabled and SVCC is opened when CCSEL is low or floating (or SGND is opened when CCSEL is high).	Does not affect laser power (normal condition for circuit operation).
13	GND	A fault state occurs.(1)	Normal operation.
14	I_{PIN}	A fault state occurs. (1, 3)	A fault state occurs. (1, 3)
15	IB_{OUTCA}/SGND	In either common anode or common cathode configuration, the laser is turned off and a fault state occurs.(1)	Does not affect laser power if output is configured for common cathode. If output is configured for common anode operation, a fault state occurs.(1)
16	GNDO	A fault state occurs.(1)	Normal operation.

Table 3-2. Circuit Response to Single-Point Fault Conditions

Pin Number	Pin Name	Circuit Response to Over-voltage Condition or Short to Vcc	Circuit Response to Under-Voltage Condition or Short to Ground
17	CC_{SEL}	Normal operation for common cathode configuration. If output is configured for common anode operation, a fault state occurs.(1)	Normal operation for common anode configuration. If output is configured for common cathode operation, a fault state occurs.(1)
18	OUTP	Does not affect laser power during common cathode operation. During common anode operation, laser modulation is prevented; the APC loop will increase bias current to compensate for the drop in laser power. If the set output power can not be obtained, a fault state occurs.(1,2)	A fault state occurs.(1)
19	OUTN	Does not affect laser power during common anode operation; does not affect laser power during common cathode operation since output is AC coupled.	Does not affect laser power during common anode operation; does not affect laser power during common cathode operation since output is AC coupled.
20	GPIO(4)	Does not affect laser power.	Does not affect laser power.
21	SSV_{CC}/$IBOUT_{CC}$	Does not affect laser power if output is configured for common anode. If output is configured for common cathode operation, a fault state occurs.(1)	In either common anode or common cathode configuration, the laser is turned off and a fault state occurs.(1)
22	A/D_{AUX2}	Does not affect laser power.	Does not affect laser power.
23	BIAS_R	Turns off internal reference current for laser driver bias and modulation; no laser output.	A fault state occurs.(1)
24	A/D_{AUX1}	Does not affect laser power.	Does not affect laser power.
25	A/D_{RxP}	Does not affect laser power.	Does not affect laser power.
26	TEST	Laser Driver is Disabled	Does not affect laser power.
27-31	RxLOS, GPIO(0-3)	Does not affect laser power.	Does not affect laser power.
32	DV_{DD}	A fault state occurs. (1)	Disables laser driver.

NOTES:

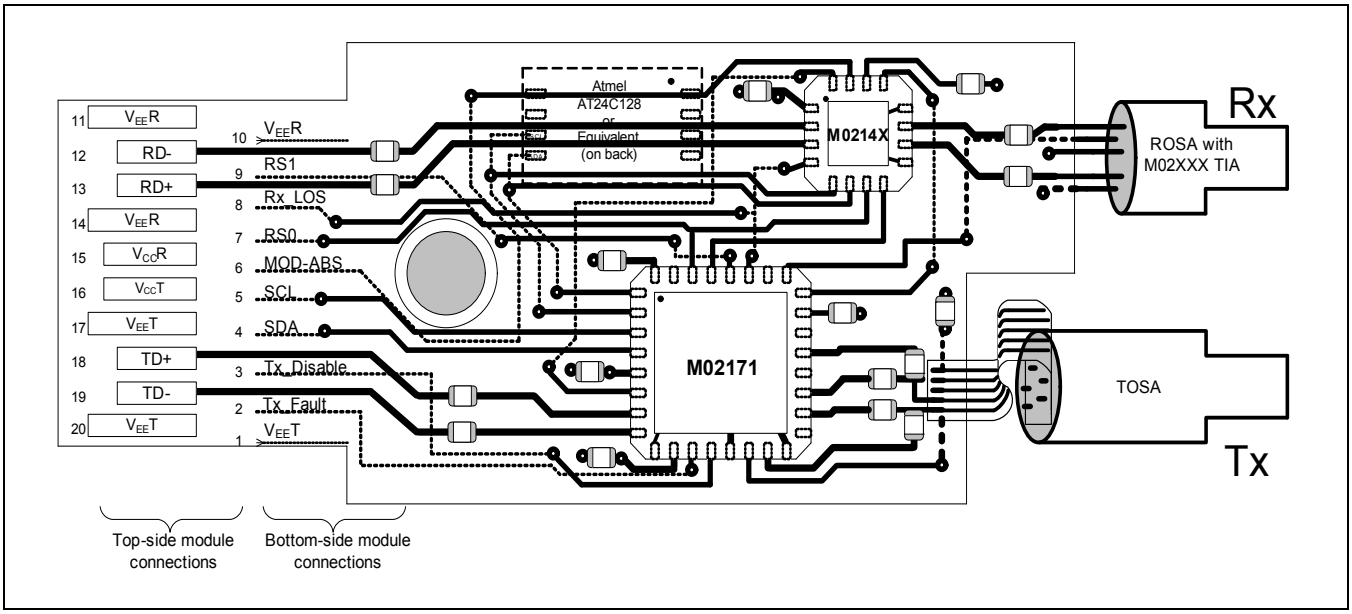
1. Unless the safety circuitry is bypassed, a Fault state will assert the TX_Fault output, disable bias and modulation outputs and open the switch at SV_{CC}.
2. Does not affect laser power when the modulation output is AC coupled to the laser.
3. Does not affect laser power in open loop mode.

4.0 Applications Information

4.1 Applications

- SFP/SFP+ Optical Transceivers
- SONET/SDH Transceivers
- 10 Gigabit Ethernet Modules
- 1G/2G/4/8/10G Fibre Channel Modules

Figure 4-1. M02171 Placement in SFP+ Module



4.2 Configuring the M02171 for Typical Applications

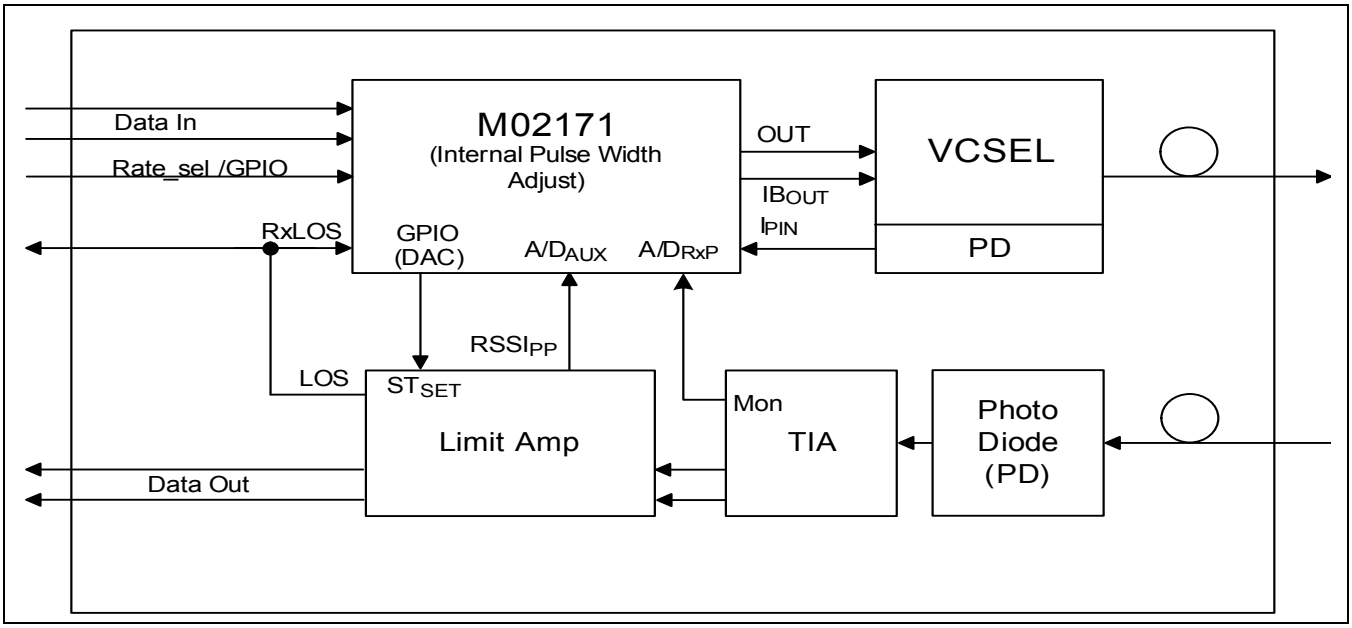
Because of its versatile architecture, the M02171 is easily adapted for a variety of applications. Several typical combinations are presented here, but there is much flexibility for module vendors to create their own variations.

The pulse width adjustment (PWA) DAC, as well as a 10-bit auxiliary DAC and the two 6-bit auxiliary DACs are each connected to one of the four GPIOs to enable their use for external purposes. The received average power (RxP) ADC and the two auxiliary ADCs are external inputs.

4.2.1 Application 1: M02171 with VCSEL

The primary applications for this configuration are 10GFC and other 10G VCSEL-based short reach designs. The block diagram for this application is given in Figure 4-2.

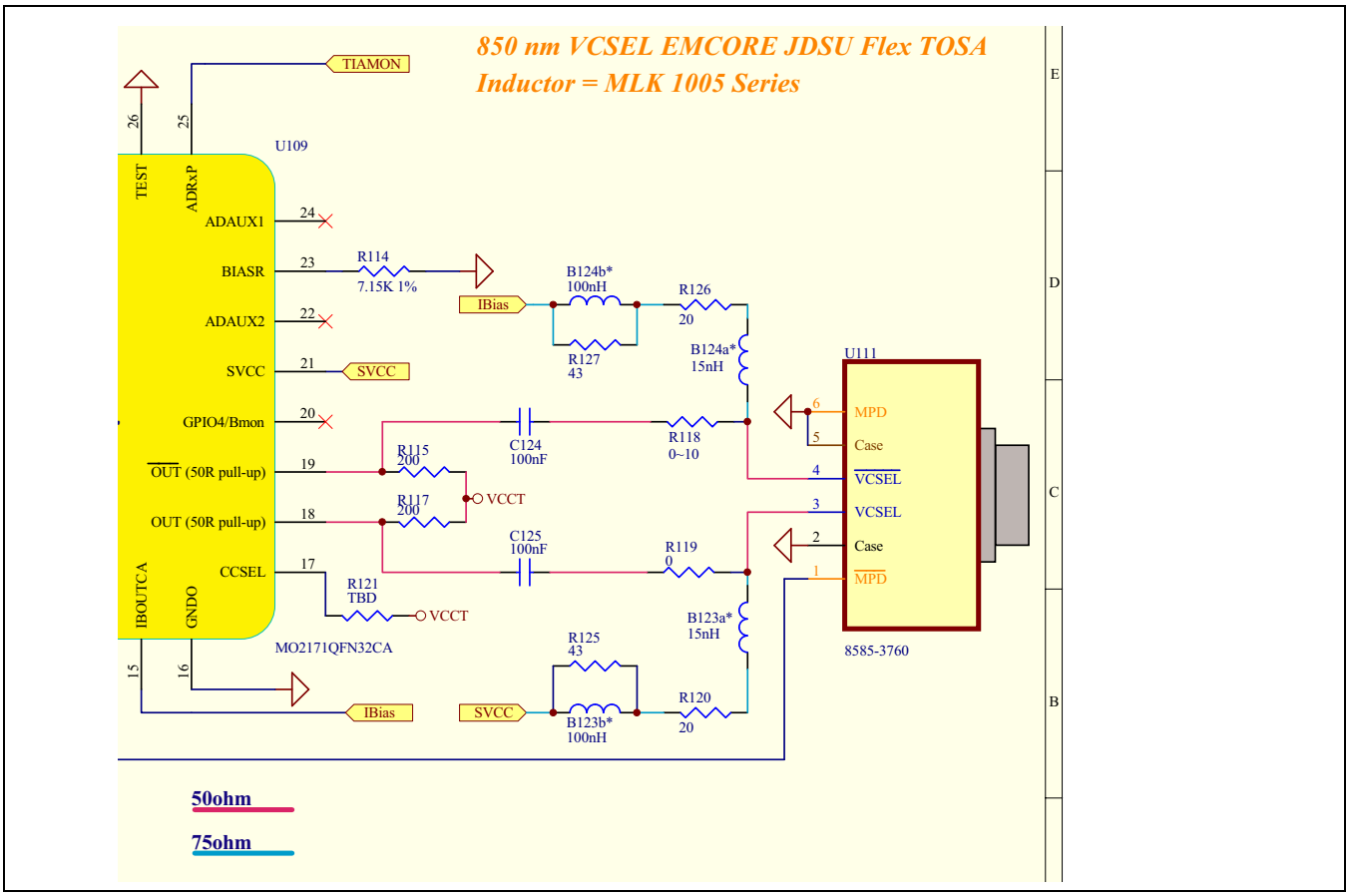
Figure 4-2. M02171 with VCSEL



4.2.1.1 Output Schematic with Emcore or JDSU VCSEL

Below is show the output schematic for the actual SFP+ implemented reference design on an SFP+ form factor PCB using either the JDSU or Emcore VCSEL TOSA. Other reference designs are available. Please contact your local sales representative for information.

Figure 4-3. M02171 with Emcore or JDSU VCSEL



4.3 Device Monitors Calibration

This section describes how the device, using Mindspeed supplied firmware, supports the device monitors calibration requirements of SFF-8472. The standard uses the term calibration to refer to the conversion of the raw monitor ADC values to actual temperature, voltage, power, etc. values. This should not be confused with the module calibration (and configuration) features.

4.3.1 Internal and External Calibration of Monitored Parameters

As specified in SFF8472, the monitored parameters can be calibrated either externally or internally. With internal calibration the measurements are calibrated over the operating temperature and voltage and are interpreted in real world units versus raw A/D values. External calibration stores raw A/D values which must be converted to real world units by the host using calibration constants given in Table 3-16 of SFF-8472, Rev 10.1.

4.3.2 Additional or Reserved Monitors

The M02171 incudes two auxiliary ADCs for monitoring purposes in addition to the modulation current monitor. Provisions exist in SFF-8472 for two more internally calibrated monitor values with associated alarm and warning levels. However, note that an insufficient number of bytes have been reserved by SFF-8472 to support external calibration for these additional monitored values. Therefore the additional Aux_ADC monitors and/or the modulation current monitor can only be mapped to the reserved locations for internally calibrated monitors and warning levels. If these monitors are not mapped to the reserved locations, the values and alarm/warning levels are still stored in PDRAM.

4.3.3 Real Time Module Diagnostic Miscellaneous Status Bits

The device firmware also monitors the status of the module and updates the miscellaneous status bits stored in (A2h, 110). The status bits include:

- Tx Disable
- Soft Tx Disable
- Rx Rate Select
- Soft Rx Select
- Tx Fault
- Rx LOS
- Data_Ready_Bar

4.4 Two-wire Host Memory Access Model

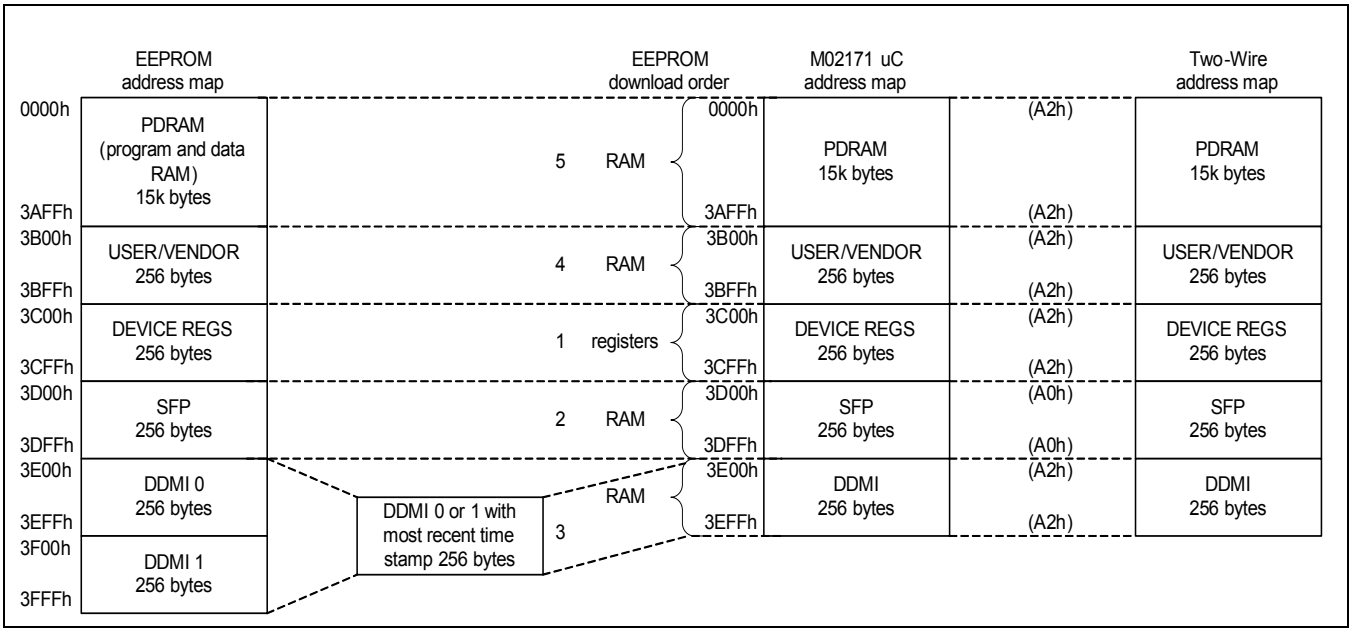
All on-chip memories can be accessed via the host two-wire interface using serial device addresses A0h and A2h. The on-chip memory is partitioned into 128 byte tables accessed using 8-bit addresses and a programmable table select byte where the memory partition is configurable to comply with the SFP/DDMI standards. The table select byte defaults upon power up to 00h. The table select byte is used as the MSB address bits and if the host attempts to write an invalid table select byte, nothing will be written and if an attempt is made to read using an invalid table select byte, the return value will be zero. The host interface memory map is defined in Table 4-1.

Note that the information at both two-wire addresses (A0h and A2h) may be accessed by using the appropriate address without the need for a special address change sequence. This means that accessing information at either address can be accomplished by the host at any time.

Figure 4-4 describes the device memory map to the EEPROM, internal device controller and the host two-wire serial interface.

Section 4.4.3, “Host Two-wire Serial Interface Block (see Table 1-12 and Table 1-14 for specifications),” on page 37 describes the DDMI and SFP memory maps in more detail.

Figure 4-4. Memory Mapping Table



4.4.1 NVRAM Controller Initial Data Download (see Table 1-12 and Table 1-14 for specifications)

The NVRAM Controller block is used to download all the 16 k external RAM from the NVRAM to the internal device registers and memories after power on reset.

During NVRAM download, the M02171 internal uC8051 is disabled while the NVRAM Controller is the master driving the 2-wire EEPROM (NVRAM1 and NVRAM2) bus. The NVRAM Controller first downloads the 256 byte device register data along with the SFP, DDMI and the program and data RAM (PDRAM) checksums (see the "EEPROM download order" column in Figure 4-4). The NVRAM Controller then downloads the 256 byte SFP data image. The SFP checksum is recomputed and compared with the downloaded checksum. (The checksum is defined as the modulo 256 sum of the SFP data.) If the two checksums are not equal, the SFP Checksum Error register bit is set. The M02171 SFP checksum data is held in the Device Registers section of its registers.

The download of the DDMI data is slightly different. The controller reads both data images DDMI 0 and DDMI 1. Each checksum is recomputed and compared with the downloaded checksum from the Device Register section. The controller also polls the DDMI status register STAT_DDMI to determine which DDMI is the most recent write back to the EEPROM. The DDMI data image containing the most recent data (based on STAT_DDMI) with a valid checksum is loaded into the DDMI memory. If neither checksum is correct the DDMI 0 and DDMI 1 Checksum Error register bit is set and the 256 bytes of data are still loaded into the internal DDMI memory based on the timestamp status bit.

Finally, the NVRAM Controller downloads the program and data image to the internal device RAM. If the checksum comparison fails, the download will be attempted two more times. If all three attempts fail, the download will remain in the internal RAM, the PDRAM Checksum Error register bit is set and the device will be put into host mode in which the device uC8051 is disabled and the only way to control the device is through the host two-wire serial interface. The download can also be initiated by a signal from uC watchdog timers and from the NVRAM Controller control register.

4.4.2 Uploading the Device Registers and Internal Memories (SFP, DDMI, 15 kbyte PDRAM) to the External EEPROM

The NVRAM Controller is allowed to write back device registers and internal memories to the external EEPROM. It can be initiated by either the device uC8051 or through the host two-wire serial interface. This is accomplished by writing to the NVRAM Controller control register.

The uC8051 and the host can be enabled to initiate a W/R backup of the SFP data, the DDMI data, and the device registers. Only the host is allowed to initiate a backup of the 15k PDRAM, user memory and vendor memory.

During the backup of the SFP data, the DDMI data, and the device registers, the finite state machine controller will send an interrupt to the uC8051 forcing the microcontroller into a wait state. To accomplish this, the uC memory bus has to communicate with the 15k PDRAM memory program code. During this time, the uC and the host are able to read the device register section. At the end of the backup, the interrupt is released, bringing the uC out of the wait state. During the write back operation, new checksums of the SFP data, the DDMI data and the 15k PDRAM have to be computed either by the device firmware or by the host controller.

A special case exists for updating the DDMI memory with calibration information. When either the device uC or host sends a command to write back the DDMI data, the NVRAM Controller toggles the STAT_DDMI status bit and writes the DDMI data into the corresponding image in the external EEPROM. The timestamp and checksum are also written to the appropriate locations in the EEPROM. During the backup time to the EEPROM, the host will have read only access (with the appropriate password) of the DDMI and SFP dual-port memories. At the end of the backup mode, the interrupt is released, bringing the uC out of the wait state and the clear on read status bit eeprom_access_done will be asserted when the EEPROM access is complete.

Whenever the host or device initiates a write back of the DDMI memory data to the external EEPROM, a dummy read should follow the write operation to force the device to increment the DDMI memory location in the EEPROM (DDMI 0 or 1) that it will next write back to. (The Mindspeed supplied firmware performs this function whenever it writes to the EEPROM DDMI memory).

4.4.3 Host Two-wire Serial Interface Block (see Table 1-12 and Table 1-14 for specifications)

- Slave operation only
- Supports 7-bit addressing on the two-wire serial bus
- Supports Standard and Fast Mode transfer rates
- During write back to the 15k program and data RAM (PDRAM), user memory and vendor memory, the NVRAM Controller will send a signal to disable the host acknowledge signal
- Reprogramming the Serial (Slave) device address is described in Section 4.7

The host accesses internal memories using serial device addresses A0h and A2h. Since the host has an 8 bit address interface, to access to all 16 k memory locations, the memory is partitioned into 128-byte tables. A table select byte (TSB) is used to provide indirect addressing to each table. The TSB must proceed each read or write access except when a consecutive read or write occurs within the same table already accessed.

The host interface memory map is defined in Table 4-1.

Table 4-1. SFP/DDMI Memory Map

Serial Device Address	Table	Data Address (decimal)	SFF-8472 Description	M02171 Description
A0h (SFP)	00h Lower	0-95	Serial ID	Serial ID
		96-127	Vendor Specific	Vendor Specific
	00h Upper	128-255	Reserved SFF-8079	Reserved SFF-8079
A2h (DDMI)	00h Lower	0-55	Alarm and Warning Thresholds	Diagnostics 1
		56-95	Calibration Constants	
		96-119	Real Time Diagnostic Interface	Diagnostics 2
		120-122	Vendor Specific	Firmware Revision
		123-126		Password Entry
		127		Table Select Byte
	00h Upper	128-247	User Writable Memory	User Memory
		248-255	Vendor Specific	Vendor Specific
A2h (DDMI)	01h Upper	128-255	N/A	User Memory
	02h Upper	128-255	N/A	Vendor Memory
	03h - 04h Upper	128-255	N/A	Device Registers
	05h - 7Ah Upper	128-255	N/A	Program and Data Memory

For serial device address A2h, the lower data addresses always reference the same information regardless of the actual Table Select Byte value (i.e., the diagnostic information is always accessible). The default table for serial device address A2h (or whatever it may be reprogrammed to be) is 00h (i.e. the DDMI specified data fields).

The memory is further partitioned into functional groups, each of which has configurable access permissions and password protection. There are four programmable password configurations. This flexible access methodology allows the module manufacturer to customize access models for a variety of purposes or intended users.

Table 4-2. M02171 DDMI Memory Partitioning (default serial device address A2h)

<table>
<tr><th rowspan="2">Data Address (decimal)</th><th colspan="6">Table Select Byte (TSB)</th></tr>
<tr><th colspan="2">00</th><th>01</th><th>02</th><th>03-04</th><th>05-7Ah</th></tr>
<tr><td>00

95</td><td>Diag 1</td><td rowspan="2">DDMI Diagnostics</td><td colspan="4" rowspan="2">All lower 128 bytes with table select byte > 0 map to the lower 128 bytes at TSB 00</td></tr>
<tr><td>96

119</td><td>Diag 2</td></tr>
<tr><td>120

127</td><td colspan="2">Vendor Specified
(used by Mindspeed)</td></tr>
<tr><td>128

247</td><td colspan="2">Reserved</td><td rowspan="2">User Memory</td><td rowspan="2">Vendor Memory</td><td rowspan="2">Device Registers</td><td rowspan="2">...Program/Data...
(PDRAM)</td></tr>
<tr><td>248

255</td><td colspan="2">Vendor Specified</td></tr>
</table>

Each memory partition is assigned a bit in the read and write access permission registers for each password level.

4.5 Password Protection

Passwords are entered by writing to the password entry bytes (see address A2h 123-126d in Table 4-1). These along with the table select byte are accessible without a password. The on-chip memory is protected from unauthorized access from the host interface by four levels (lowest to highest, 0 - 3) of 32-bit passwords.

The access restrictions for each password level is configurable to allow read or write access to different blocks of memory. The memory is partitioned into nine sections as listed in Table 4-3 with each level allowing unique password access.

Table 4-3. The Nine SFP/DDMI Memory Password Protection Partitions

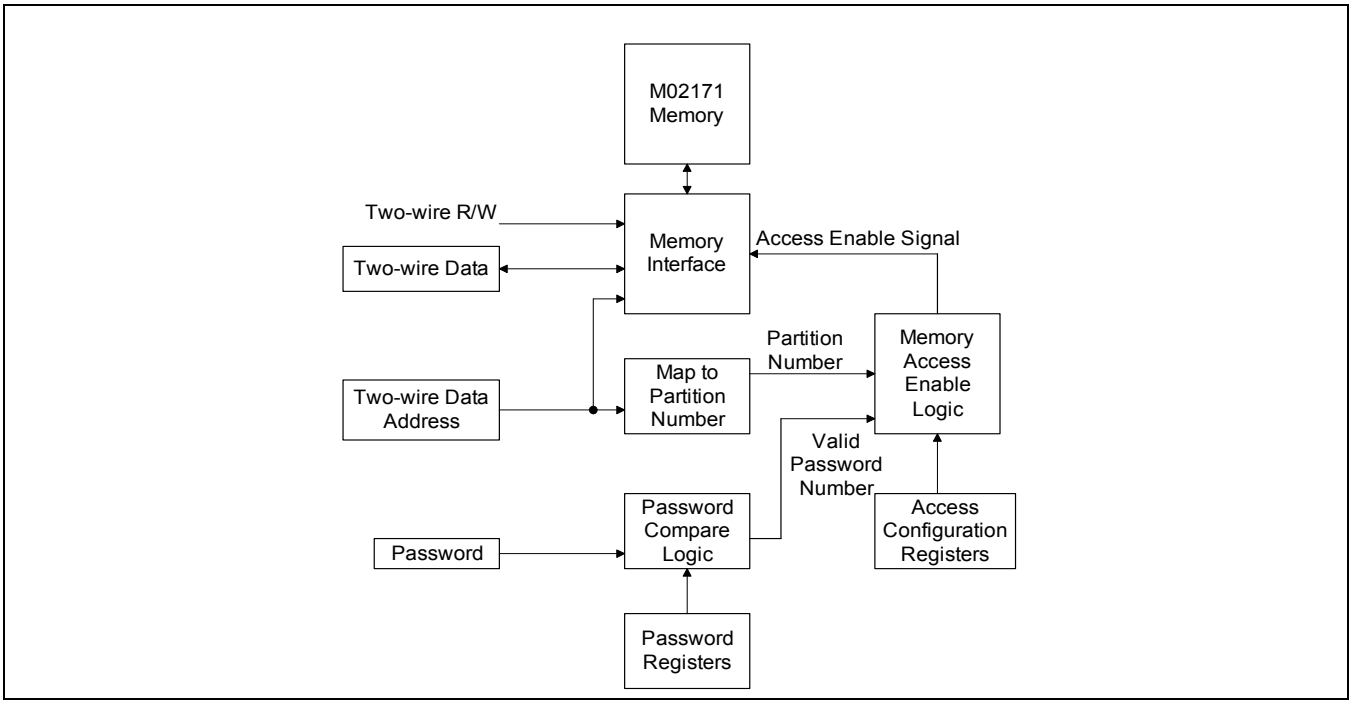
Memory Section	Data Address			Allowable Password Control Level
	Serial Device Address	Table	Address (decimal)	
Diagnostics 1	A2	00h Lower	0-95	0-3
Diagnostics 2	A2	00h Lower	96-119	
Serial ID	A0	00h Lower	0-95	
User	A2	00h Upper	128-247	
	A2	01h Upper	128-255	
Vendor	A0	00h Lower	96-127	
	A2	00h Lower	120-122	
	A2	00h Upper	248-255	
	A2	02h Upper	128-255	
Reserved	A0	00h Upper	128-255	
Program/Data	A2	≥05h Upper	128-255	
Device Registers 1	A2	03h Upper	128-255	
Device Registers 2	A2	04h Upper	128-255	

For each access level, there are internal configuration registers for read access and for write access. The control of access to the on-chip memory is illustrated in Figure 4-5. To access the memory, the host must write a 32-bit password to the appropriate DDMI memory location (see address A2h 123-126d in Table 4-1). The entered password is compared to the four passwords (one for each access level) stored internally. The current access level is defined as that corresponding to the matching password. If the entered password matches none of the stored passwords, access defaults to the lowest level (level 0 is the lowest level, level 3 is the highest level).

The access configuration registers for the current access level defines whether access is enabled to a given memory partition. When the host attempts to access the on-chip memory, the data address is first mapped to a memory partition number. The corresponding bit of the access configuration registers for the current access level are then checked to determine if access should be enabled for this partition. If access is enabled, the memory interface is then allowed to perform the requested access. An example of access definition, using the Mindspeed supplied software the vendor could configure the level 0 access for read-only for Diagnostics 1 and Diagnostics 2 while all memory is write protected.

Note that the vendor is given complete password control with the Mindspeed supplied M02171 configuration software. Using the supplied software, the vendor defines the password for each access level and the level of access for the nine SFP/DDMI Memory Password Protection Partitions shown in Table 4-3.

Figure 4-5. Password Access Control Architecture



4.6 Two-Wire Serial Interface

4.6.1 SFP Compliant interface

- SFP data read accessible via two-wire serial interface with serial device address A0h (reprogrammable)
- SFP data writable via two-wire serial interface with multiple levels of password protection
- SFP data downloaded from external EEPROM to on-chip RAM after module powers up
- M02171 internal device controller does not alter SFP data
- If the host alters the SFP data, it must supply a checksum at address 3Fh (automatic backup to external EEPROM initiated without interruption access from the host)

4.6.2 DDMI Compliant interface

- Fully SFF-8472 compliant
- DDMI data read accessible via two-wire interface with serial device address A2h (reprogrammable)
- DDMI data writable via two-wire serial interface with multiple levels of password protection
- DDMI data downloaded from external EEPROM to on-chip RAM after module powers up
- If the host alters the DDMI data, it must supply a checksum at address 3Fh and 5Fh (automatic backup to external EEPROM initiated without interruption access from the host)

4.6.3 HOST Interface Details

In accordance with SFP MSA and SFF-8472, the M02171 incorporates a two-wire interface that uses the serial EEPROM protocol defined for the Atmel AT24C01A/02/04 family of products. The interface consists of a serial input clock line (SCL, Mod Def 1) and a serial, bi-directional data line (SDA, Mod Def 2). SCL and SDA are each pulled up with an external resistor.

Table 4-4. Two-Wire Interface

Pin	Function	Description
MD1/SCL	Mod-Def 1/Serial Clock	Clock input (open drain)
MD2/SDA	Mod-Def 2/Serial Data	Data input/output (open drain)

During data transmission, SDA can only transition while SCL is low. Changes on SDA when SCL is high indicates a start or stop condition which initiates or terminates the transmission. A start condition occurs when SDA transitions from high to low when SCL is high. Conversely, a low to high transition on SDA when SCL is high indicates a stop condition. The start condition is followed by the device address (A0h for SFP and A2h for DDMI). The data address is transmitted following the device address which is followed by transmission of the data. The M02171 responds to each byte of data with an acknowledgement which is a zero following the received byte. The device can receive data a byte at a time or in sixteen byte sequences (page mode). The transmission is then terminated with the stop condition.

4.6.4 Four-wire SPI Interface Details

For those applications requiring faster programming and read back than an I2C interface can provide, an SPI interface is also provided. When SPI_Sel is high, the 4-wire SPI interface is selected. If SPI_Sel =0, the device returns to the existing 2-wire Interface (MOD_DEF1 and MOD_DEF2) with GPIO[1] and $\overline{SS}$ inputs ignored.

Table 4-5. Four-Wire Serial Interface Description

Pin	Function	Description
SS	Slave Select	Active Low. Allowing SS to return high, changes communication back to I2C
SCK	Serial Clock	10MHz maximum
SI	Slave Input	MOD_DEF2 (Data input)
SO	Slave Output	MOD_DEF1 (Data output)

After the transition high-to-low of $\overline{SS}$, the SPI Master will transfer a1 byte instruction (one of 4 instructions at table 1) following by a 1-byte address and 1-byte data for write mode and so forth. SI is sampled by the rising edge of SCK and SO is clocked out by falling edge of SCK. For an SPI Master, SO is sampled by the rising edge of SCK and SI is clocked out by the falling edge of SCK.

Table 4-6. SPI Instructions

Instruction Name	Instruction Format	$\overline{SS}$ at end of current read/write operation	Operation
R-Read	PDDDDx11	H	Random Read
R-Write	xxxxxx10	H	Random Write
S-Read	PDDDDx11	L	Sequential Read
S-Write	xxxxxx10	L	Sequential Write

As a result, the read command changes to: “PDDDD_X11; the Random/Sequence Read command. Where the P bit refers to whether or not the programmable delay mode is turned on or off. The DDDD bits represent the number of cycles by which the read is delayed. For reliable operation, it is recommended that 3 to 8 SPI clock cycles be programmed. (With a 10 MHZ SPI clock). The X’s are don't cares. When P=1, the programmable delay is turned on, and the read value is delayed by the number represented by DDDD bits. For example: If DDDD = 0100, then the read value is output after a 4 cycle delay. DDDD = 1000 means that the read value is output after an 8 cycle delay. When P = 0, the programmable mode is turned off, and the read value is output after a default 8 cycles delay.

SPI Timing Application Notes:

- If the two LSB of the instruction byte are not 11 or 10, no read/write cycle is executed and the SO pin remains tri-stated.
- There are no different instructions for Random R/W and sequential R/W. When slave select, $\overline{SS}$ is extended by n*8-spi clock cycles, and a Random R/W becomes a sequential R/W as in the sequential write timing diagram.
- The sequential R/W continues to roll over the 256 byte addresses if $\overline{SS}$ is extended low.
- A minimum of one SPI clock cycle pulse width is required for Slave Select ($\overline{SS}$) to be deselected between Read-Read, Read-Write, Write-Read, or Write-Write modes.
- At least one SPI clock cycle is required after Slave select $\overline{SS}$ is deasserted.
- As in the two wire slave interface, the SPI interface reserves HOST address 7Fh for table select. Each 128-byte table definition remains as before (at two wire slave address A2h). For example, writing 03h to table select address $7F, selects table #3, following by a R/W to any address from $80 to $FF, giving access to Host locations $80 to $FF.
- SPI Host Read/Writes to any lower addresses ($00 to $7E and $7F) are mapped to the 128 byte common area of Diagnostics 1, Diagnostics 2, Vendor specific, Password Entry and Table Select defined in the lower page.
- To access the 256-byte SFP (former two wire slave) address A0h(from two wire interface mode), writing **80h** (for the lower 128 bytes) and **81h** (for the upper 128 bytes) to table select is required. After writing **80h** or **81h** to table select, SPI host addresses ($80 to $FF) are mapped to the lower 128 bytes or upper 128 bytes of SFP memory.
- Note: it is up to the user to terminate the extension of $\overline{SS}$ in sequential write and change the table select since it can be rolled over 256 bytes address which can roll to lower addresses and data are written to the common area. For example, start writing at address $C0 in sequential Write: $C0, #C1 …….#FF, #00, #01 …….#7E (table select), #7F, #80, ……. #C0, #C1 …. #FF…….

Figure 4-6. SPI Random Read

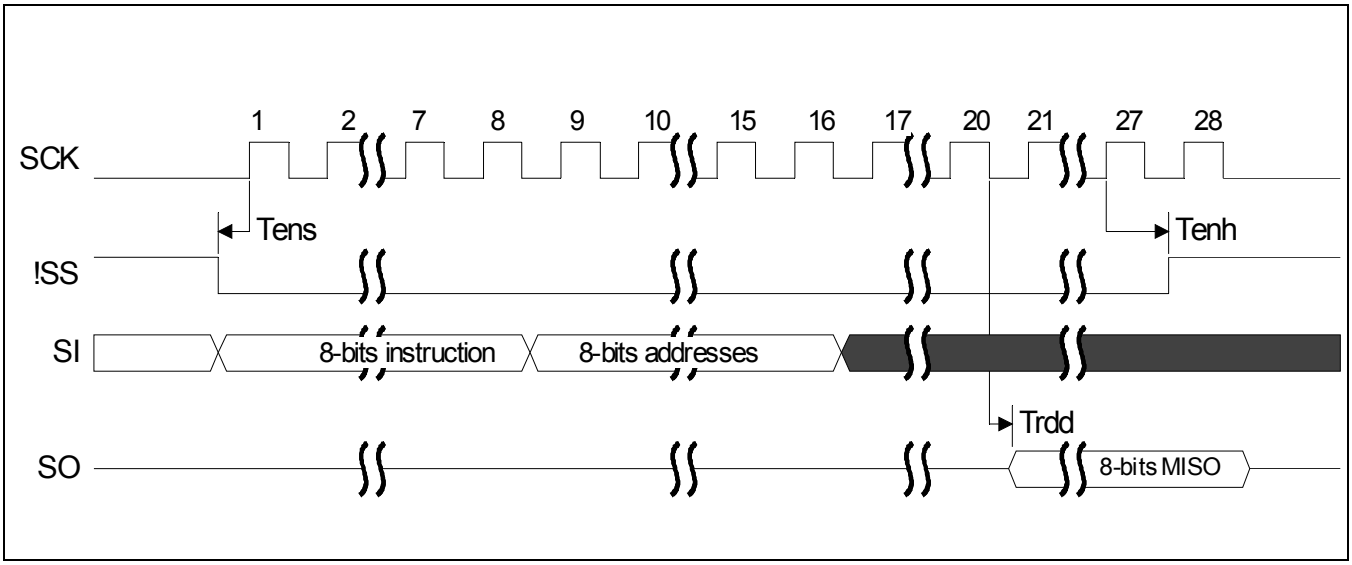


Figure 4-7. SPI Random Write

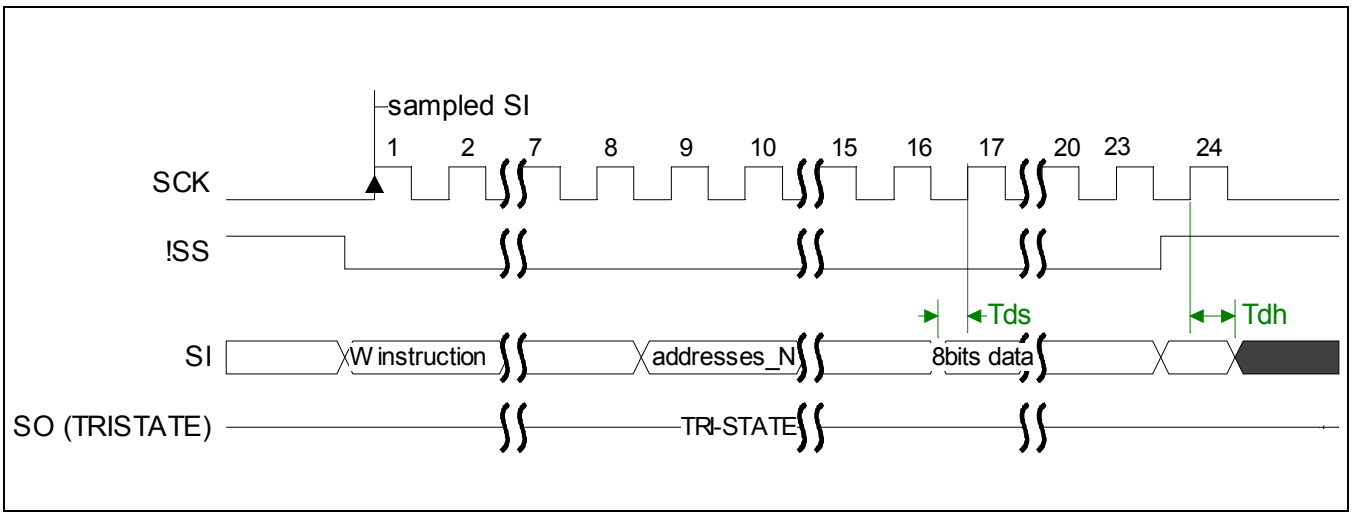


Figure 4-8. SPI Sequential Read

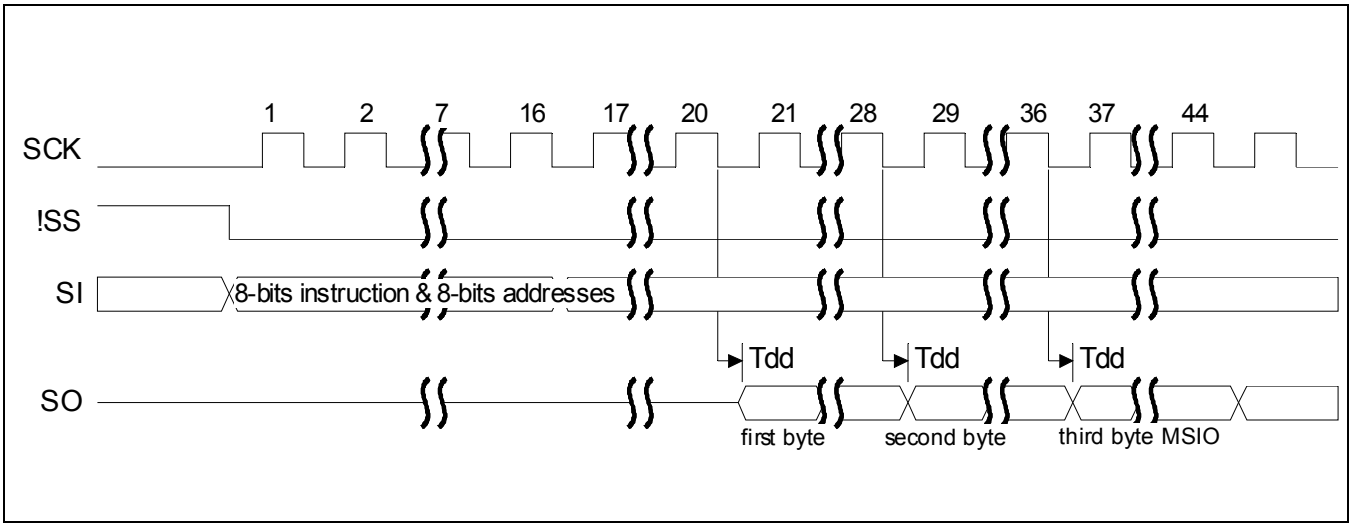
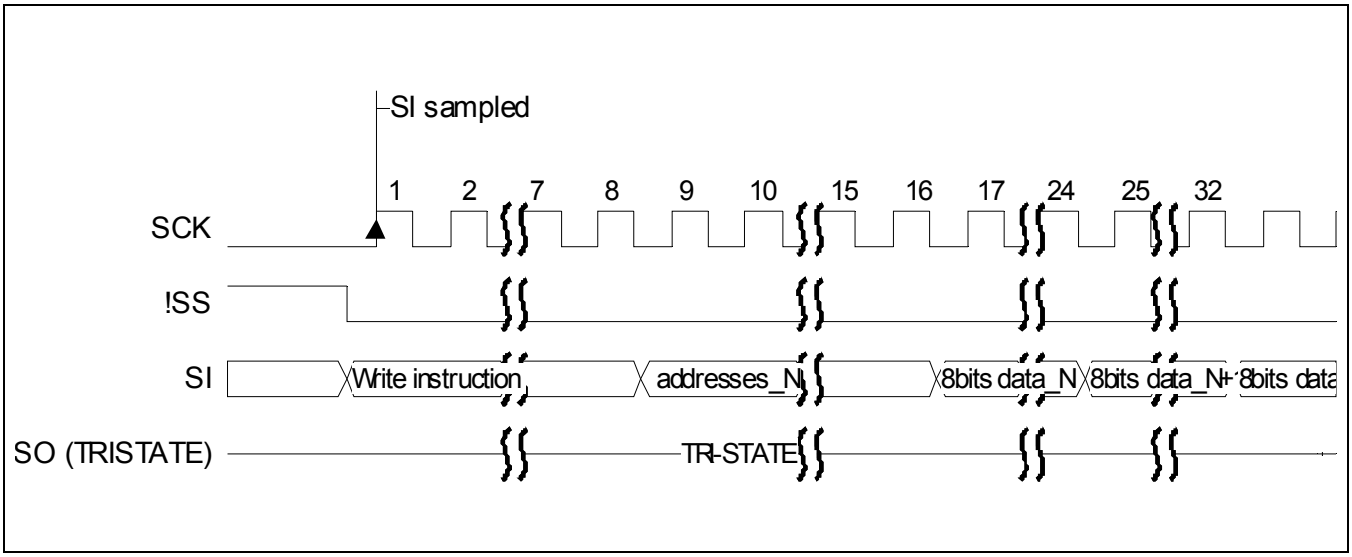


Figure 4-9. SPI Sequential Write



4.7 Reprogramming the Serial Device Address

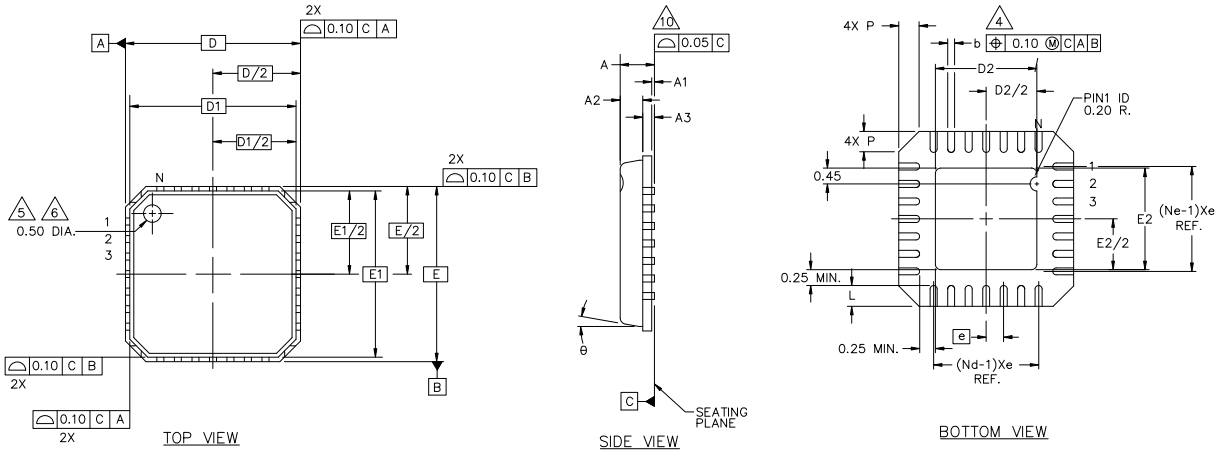
When more than one device is sharing the two-wire interface it will be necessary to change the serial device address of each module to allow the host independent access to each module. This is accomplished using the Two-wire Serial Control Register that when set, redefines how the TX_DIS pin is interpreted by the M02171. In this mode, if TX_DIS is high, the M02171 will not respond to any serial device address from the host interface. If TX_DIS is low, the M02171 will respond when the serial device address is its own, allowing the particular device to be accessed (TX_DIS is performing as a device select pin).

When the host sets this control bit, all modules will be placed in this reprogramming mode. Individually selecting a module through an individual module's TX_DIS pin allows the modules address to be uniquely programmed. Module addresses are 8 bit words. The LSB selects a read or write operation and is not part of the address. The second bit is defined to be a zero for SFP and a one for DDMI, thus DDMI addresses are always 2 greater than the SFP addresses in a module (e.g. A0h and A2h the default SFP and DDMI addresses). This means that the first six MSBs are what constitute the unique module address. The serial device address is held in the Physical Address Control Register. Only one address is written. The reprogrammed address is now the SFP serial device address. As detailed above, the DDMI serial device address is now an increment of 2 greater than the SFP address.

Once each module has had its address reprogrammed, to exit this reprogramming mode is accomplished by again using the Two-wire Serial Control Register to define the TX_DIS pin to its normal function. This operation must be performed on each module as they now each possess a unique serial device address.

5.0 Package Specification

Figure 5-1. QFN32 Package Information (Amkor)



Note: View is for a 28 pin package. All dimensions in the tables apply for the 32 pin package

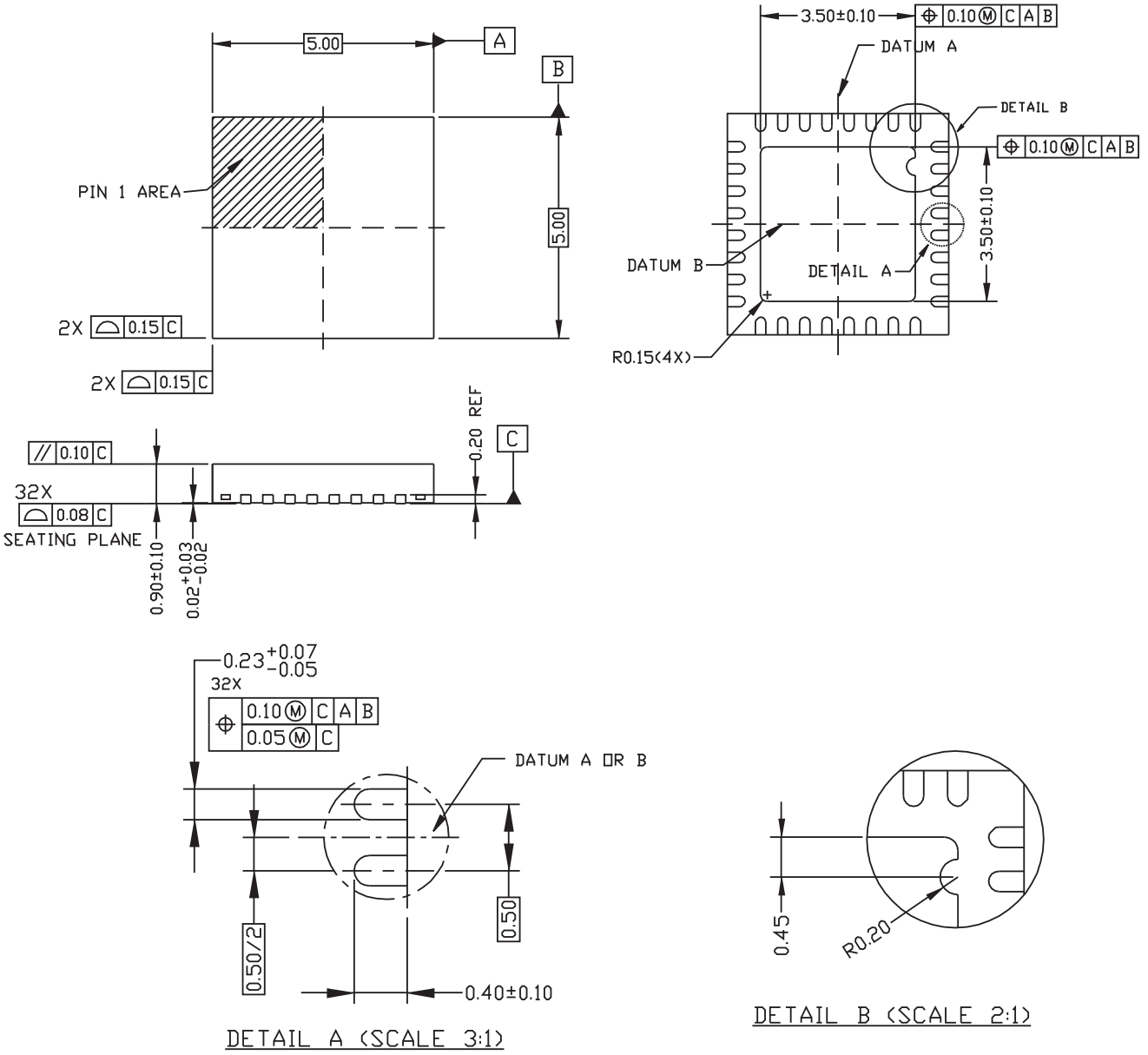
SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		32		3
Nd		8		3
Ne		8		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
Q	0.00	0.20	0.45	
D2	3.4	3.5	3.6	
E2	3.4	3.5	3.6	

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	-	0.85	**0.90**	
A1	0.00	0.01	0.05	11
A2	-	0.65	**0.70**	
A3		0.20 REF.		
D		5.00 BSC		
D1		4.75 BSC		
E		5.00 BSC		
E1		4.75 BSC		
θ			12°	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	

NOTES:

2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
    EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.

Figure 5-2. QFN32 Package Information (ASEM)



NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

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