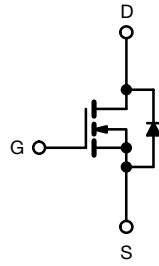
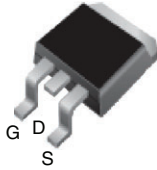




**THE DATASHEET OF
SIHL630STRL-GE3**



Power MOSFET

D²PAK (TO-263)


N-Channel MOSFET



RoHS*
Available
HALOGEN
FREE
Available

FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dv/dt rating
- Repetitive avalanche rated
- Logic-level gate drive
- R_{DS(on)} specified at V_{GS} = 4 V and 5 V
- 150 °C operating temperature
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface-mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface-mount application.

PRODUCT SUMMARY

V _{DS} (V)	200	
R _{DS(on)} (Ω)	V _{GS} = 5 V	0.40
Q _g max. (nC)	40	
Q _{gs} (nC)	5.5	
Q _{gd} (nC)	24	
Configuration	Single	

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHL630S-GE3	SiHL630STRR-GE3 ^a	SiHL630STRL-GE3 ^a
Lead (Pb)-free	IRL630SPbF	IRL630STRRPbF ^a	IRL630STRLPbF ^a

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	200	V
Gate-source Voltage	V _{GS}	± 10	
Continuous drain current	V _{GS} at 5 V	T _C = 25 °C	9.0
		T _C = 100 °C	5.7
Pulsed drain current ^a	I _{DM}	36	A
Linear derating factor		0.59	W/°C
Linear derating factor (PCB mount) ^e		0.025	
Single pulse avalanche energy ^b	E _{AS}	250	mJ
Avalanche current ^a	I _{AR}	9.0	A
Repetitive avalanche energy ^a	E _{AR}	7.4	mJ
Maximum power dissipation	P _D	T _C = 25 °C	74
Maximum power dissipation (PCB mount) ^e		T _A = 25 °C	3.1
Peak diode recovery dv/dt ^c	dv/dt	5.0	V/ns
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^d	For 10 s	300	

Notes

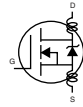

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- V_{DD} = 25 V, starting T_J = 25 °C, L = 4.6 mH, R_g = 25 Ω, I_{AS} = 9.0 A (see fig. 12)
- I_{SD} ≤ 9.0 A, di/dt ≤ 120 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material)



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	40	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.7	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0, I_D = 250\ \mu\text{A}$	200	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\ \text{mA}$	-	0.27	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0	-	2.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 10\ \text{V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 200\ \text{V}, V_{GS} = 0\ \text{V}$	-	-	25	μA
		$V_{DS} = 160\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 5.0\ \text{V}, I_D = 5.4\ \text{A}^b$	-	-	0.40	Ω
		$V_{GS} = 4.0\ \text{V}, I_D = 4.5\ \text{A}^b$	-	-	0.50	
Forward transconductance	g_{fs}	$V_{DS} = 50\ \text{V}, I_D = 5.4\ \text{A}^b$	4.8	-	-	S
Dynamic						
Input capacitance	C_{iss}	$V_{GS} = 0\ \text{V}, V_{DS} = 25\ \text{V}, f = 1.0\ \text{MHz}, \text{ see fig. 5}$	-	1100	-	pF
Output capacitance	C_{oss}		-	220	-	
Reverse transfer capacitance	C_{rss}		-	70	-	
Total gate charge	Q_g	$V_{GS} = 10\ \text{V}, I_D = 9.0\ \text{A}, V_{DS} = 160\ \text{V}, \text{ see fig. 6 and 13}^b$	-	-	40	nC
Gate-source charge	Q_{gs}		-	-	5.5	
Gate-drain charge	Q_{gd}		-	-	24	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 100\ \text{V}, I_D = 9.0\ \text{A}, R_g = 6.0\ \Omega, R_D = 11\ \Omega, \text{ see fig. 10}^b$	-	8.0	-	ns
Rise time	t_r		-	57	-	
Turn-off delay time	$t_{d(off)}$		-	38	-	
Fall time	t_f		-	33	-	
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal source inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	9.0	A
Pulsed diode forward current ^a	I_{SM}		-	-	36	
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 9.0\ \text{A}, V_{GS} = 0\ \text{V}^b$	-	-	2.0	V
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 9.0\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}^b$	-	230	350	ns
Body diode reverse recovery charge	Q_{rr}		-	1.7	2.6	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width $\leq 300\ \mu\text{s}$; duty cycle $\leq 2\ \%$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

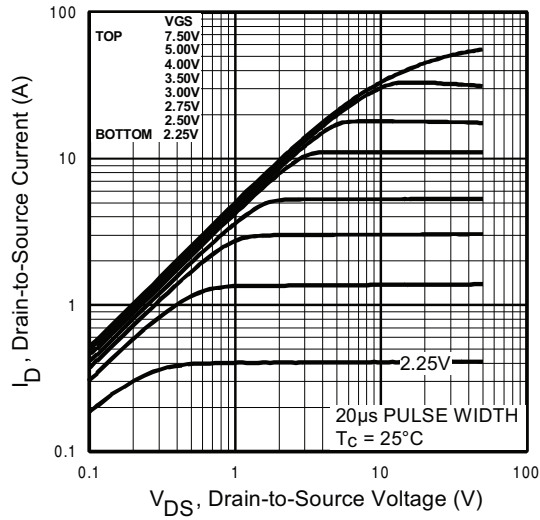


Fig. 1 - Typical Output Characteristics, $T_c = 25^\circ\text{C}$

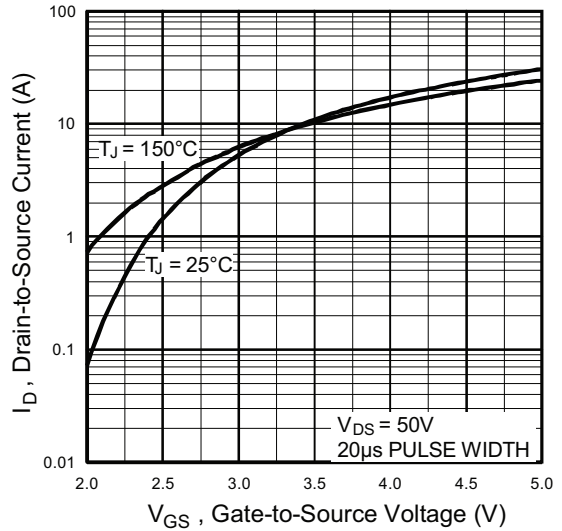


Fig. 3 - Typical Transfer Characteristics

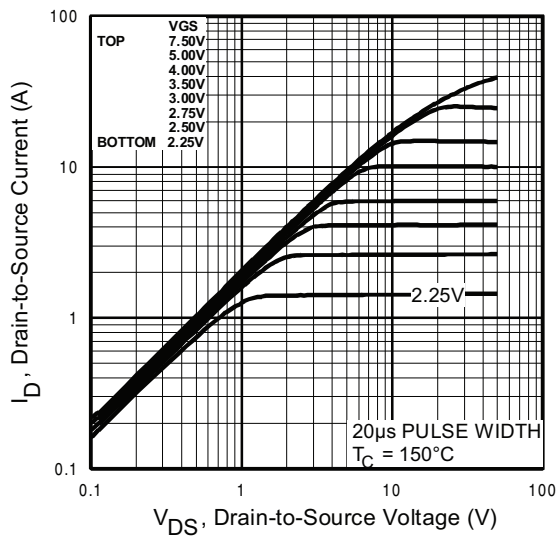


Fig. 2 - Typical Output Characteristics, $T_c = 150^\circ\text{C}$

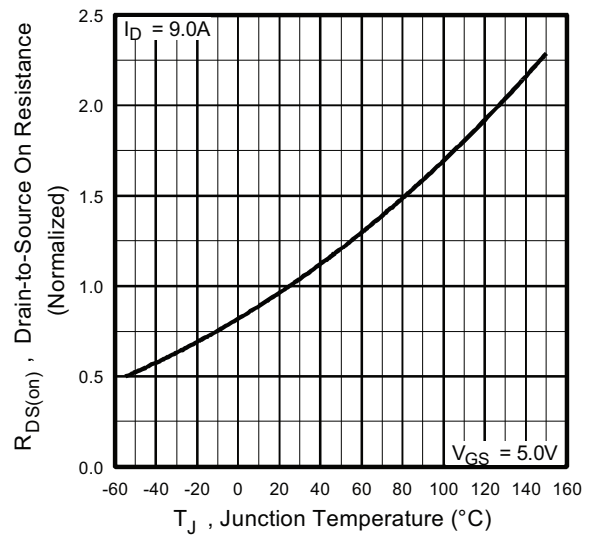


Fig. 4 - Normalized On-Resistance vs. Temperature

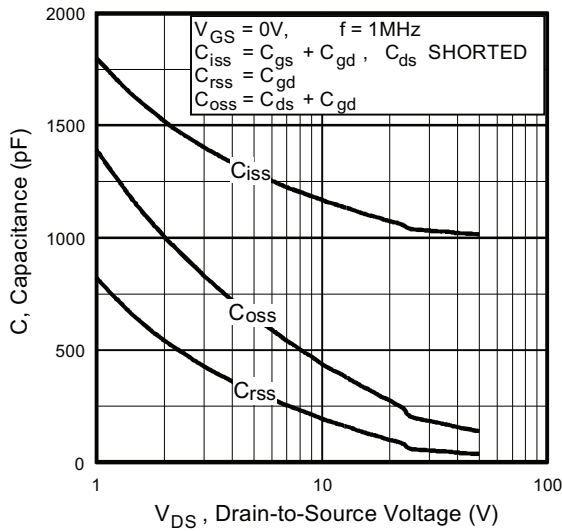


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

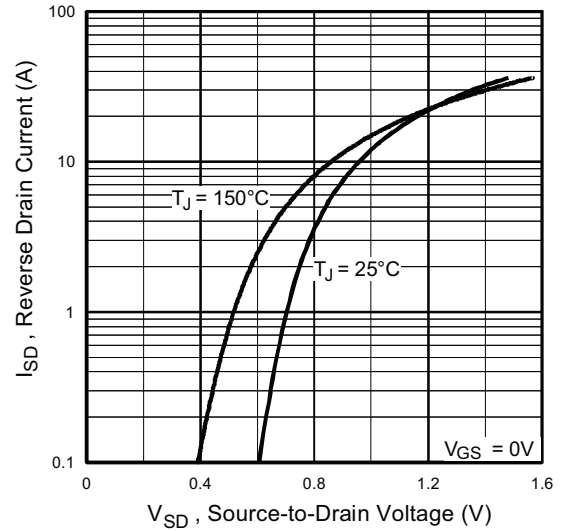


Fig. 7 - Typical Source-Drain Diode Forward Voltage

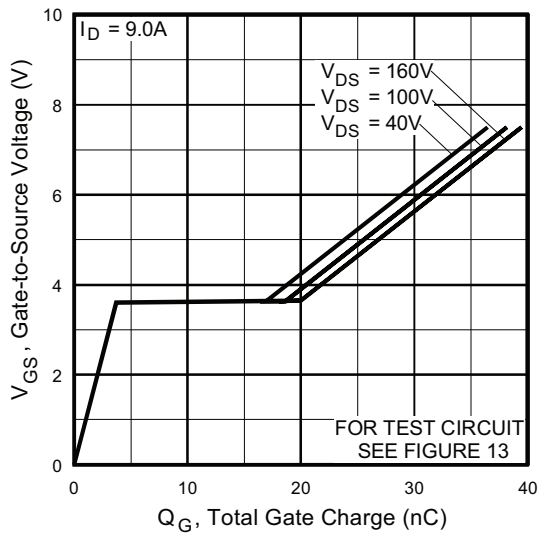


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

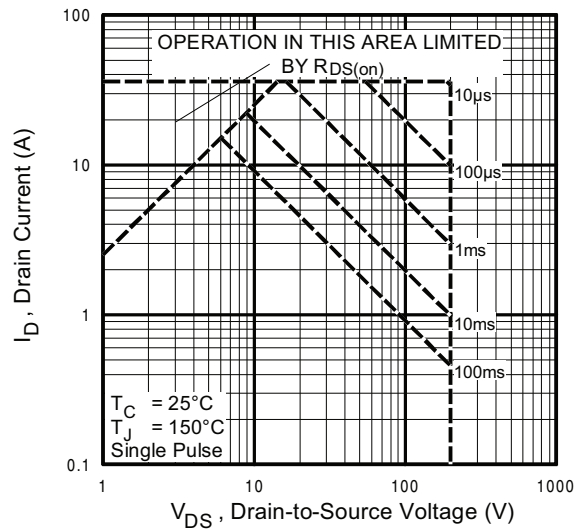


Fig. 8 - Maximum Safe Operating Area

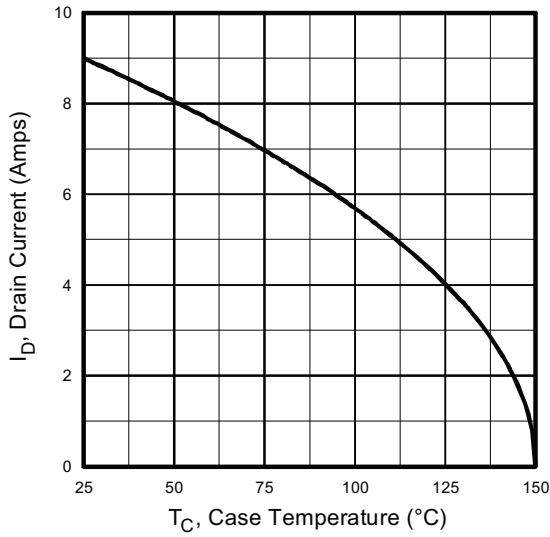


Fig. 9 - Maximum Drain Current vs. Case Temperature

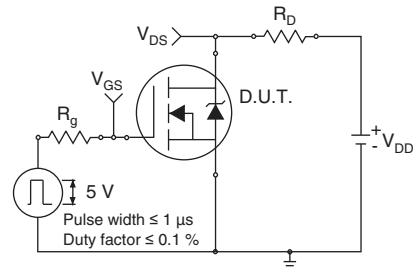


Fig. 10a - Switching Time Test Circuit

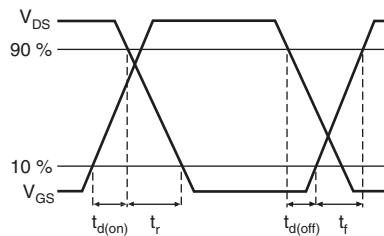


Fig. 10b - Switching Time Waveforms

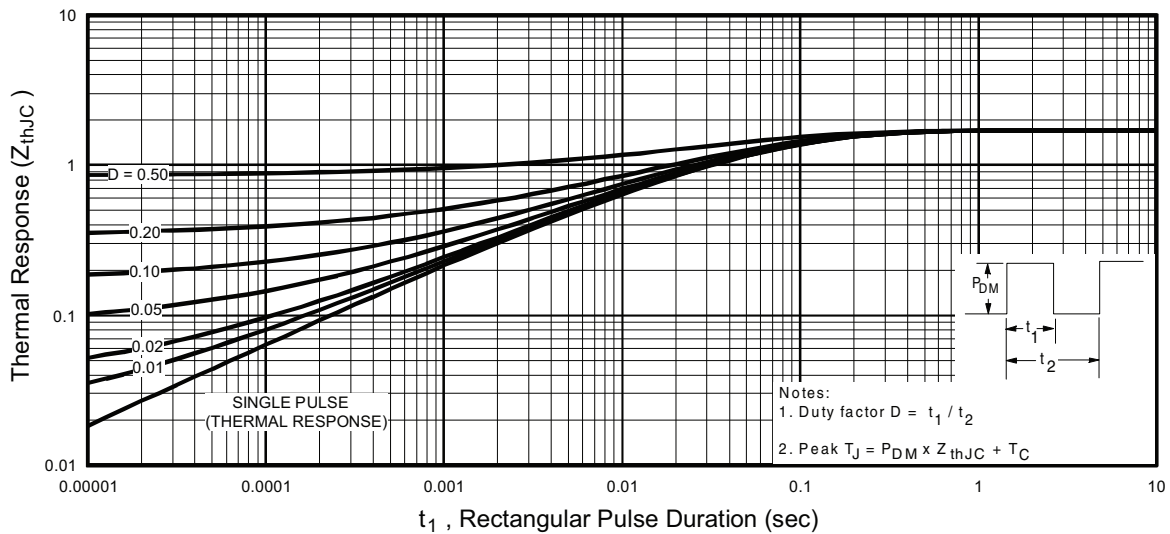
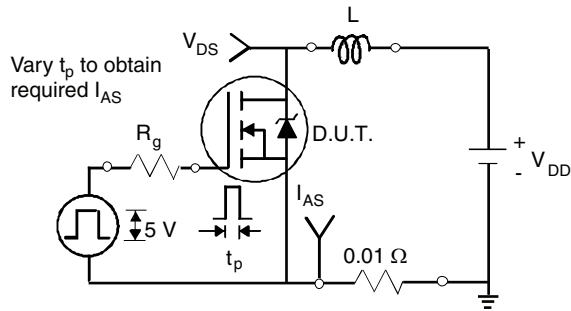
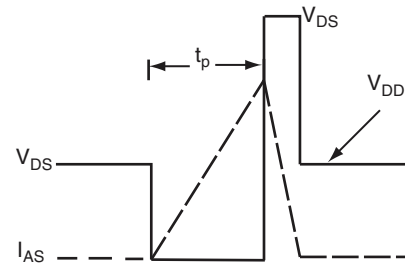
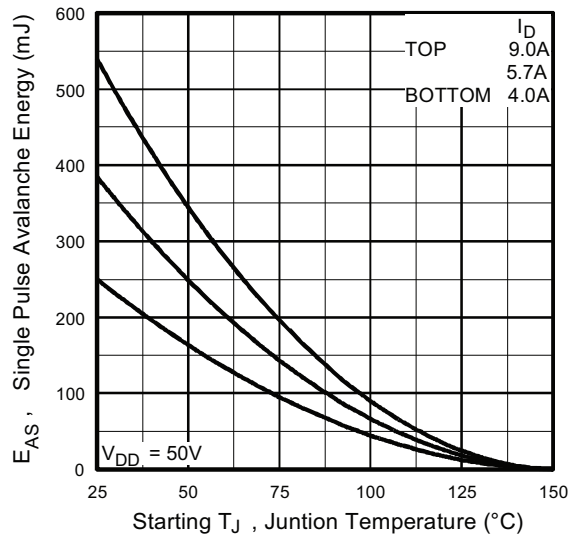
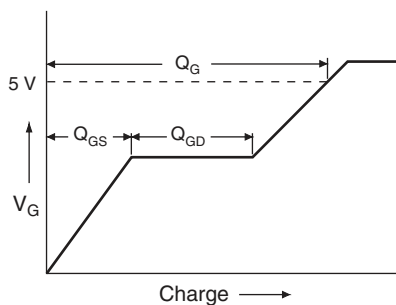
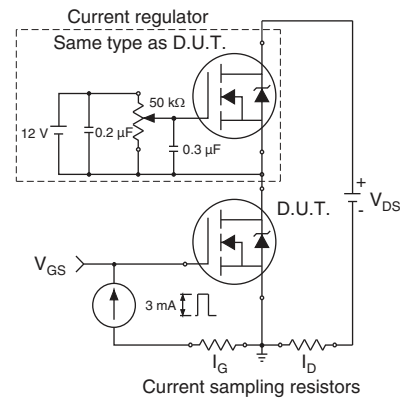
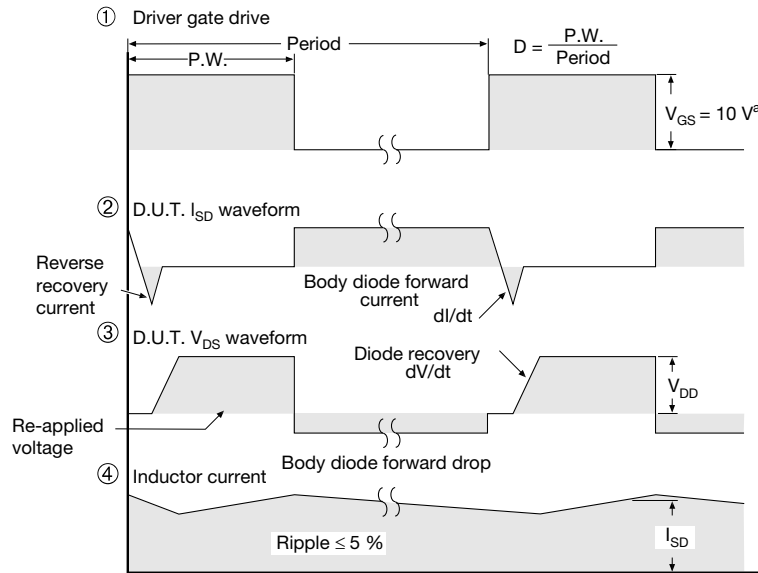
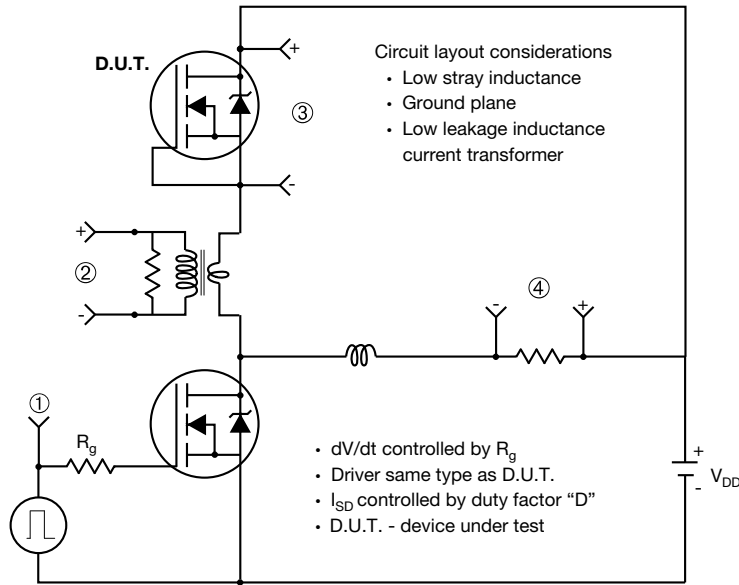


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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