THE DATASHEET OF

ATS668LSMTN-T

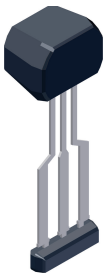
ATS668LSM

True Zero-Speed High-Accuracy Gear Tooth Sensor IC

FEATURES AND BENEFITS

- Three-wire back-biased speed sensor optimized for transmission speed-sensing applications
- Integrated in-package EMC protection circuit allows compliance to most automotive EMC environments without external circuitry
- Small-signal lockout for immunity to vibration
- Tight timing accuracy over full operating temperature range
- True zero-speed operation
- Air gap independent switch points
- Large operating air gaps achieved through use of gain and offset adjust circuitry
- Wide operating voltage range with undervoltage lockout (UVLO)
- Digital output representing target profile
- Single-chip sensing IC for high reliability
- High-speed startup

PACKAGE: 3-pin SIP (suffix SM)



Not to scale

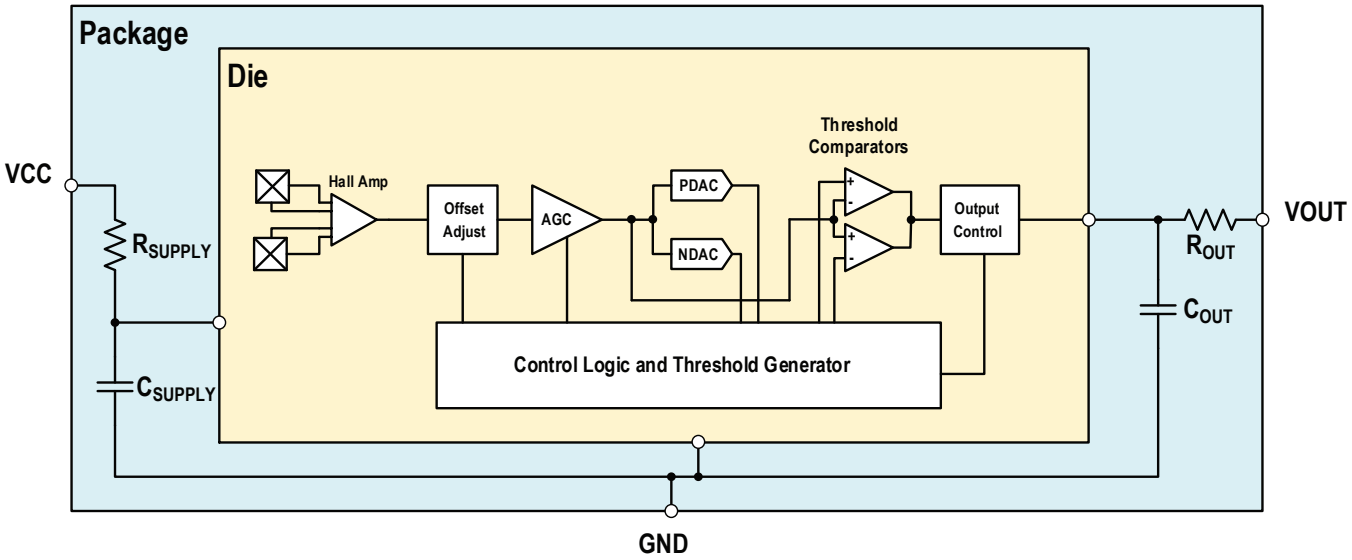
DESCRIPTION

The ATS668LSM is an optimized Hall-effect integrated circuit (IC) and permanent magnet pellet combination with integrated EMC protection components to provide a user-friendly solution for true zero-speed digital gear tooth sensing. The small package can be easily assembled and used in conjunction with a wide variety of gear tooth sensing applications.

The device incorporates a dual element Hall IC that switches in response to differential magnetic signals created by a ferromagnetic target. The IC contains a sophisticated compensating circuit designed to eliminate the detrimental effects of magnet and system offsets. Digital processing of the analog signal provides zero-speed performance independent of air gap and also dynamic adaptation of device performance to the typical operating conditions found in automotive applications (i.e. vibration immunity and runout tolerance). High-resolution peak detecting DACs are used to set the adaptive switching thresholds of the device. Hysteresis in the thresholds reduces the negative effects of any anomalies in the magnetic signal associated with system or target anomalies typically seen in many automotive applications.

This device is available in a lead (Pb) free 3-pin SIP package (SM) with matte-tin leadframe plating.

Functional Block Diagram



SELECTION GUIDE

Part Number	Package
ATS668LSMTN-T	3-pin SIP with matte-tin leadframe plating

*Contact Allegro™ marketing or your local sales representative for additional options.

RoHS COMPLIANT

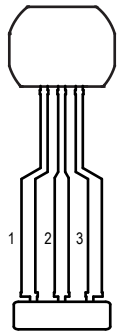
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		26.5	V
Reverse Supply Voltage	V_{RCC}		–18	V
Reverse Supply Current	I_{RCC}		50	mA
Reverse Output Voltage	V_{ROUT}		-0.5	V
Output Sink Current	I_{OUT}		25	mA
Operating Ambient Temperature	T_A	Range L, refer to Power Derating Curve	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

INTERNAL PASSIVE COMPONENTS RATINGS

Symbol	Characteristic	Rating	Unit
C_{SUPPLY}	Rated Nominal Capacitance	220	nF
C_{OUT}	Rated Nominal Capacitance	1.8	nF
R_{SUPPLY}	Rated Nominal Resistance	50	Ω
R_{OUT}	Rated Nominal Resistance	50	Ω

Pinout Diagram



Terminal List Table

Number	Name	Function
1	VCC	Supply voltage
2	GND	Ground
3	VOUT	Device output

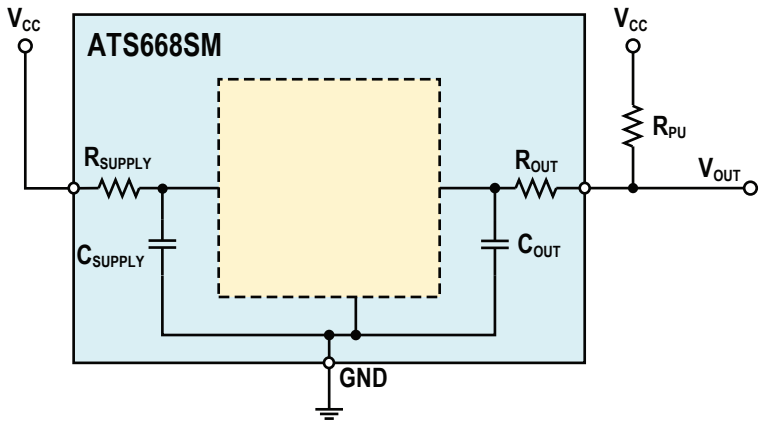


Figure 1: Typical Application

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OPERATING CHARACTERISTICS: Valid throughout full operating and temperature ranges, using Reference Target 60-0, unless otherwise noted.

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}	Operating, $T_J < T_J(max)$	4.6	–	24	V
Undervoltage Lockout	V_{UVLO}		–	4.1	4.55	V
Reverse Supply Current	I_{RCC}	V_{CC} = –18 V	–	–	–10	mA
Supply Current	I_{CC}		–	–	12	mA
Supply Zener Clamp Voltage	V_Z	$I_{CC} = I_{CC(MAX)} + 3$ mA	28.0	–	–	V
Supply Zener Current	I_Z	$T_J < T_J(max)$, V_{CC} = 27 V	–	–	15	mA
Reverse Supply Zener Clamp Voltage	V_{RZ}	I_{CC} = –3 mA, T_A = 25°C	–	–	–18	V
OUTPUT STAGE						
Low Output Voltage	V_{SAT}	I_{SINK} = 10 mA, Output = ON	–	750	1000	mV
Output Zener Clamp Voltage	V_{ZOUT}	I_{OUT} = 3 mA, T_A = 25°C	28.0	–	–	V
Output Current Limit	I_{LIM}	V_{OUT} = 12 V, $T_J < T_J(max)$	25	45	70	mA
Output Leakage Current	I_{OFF}	V_{OUT} = 24 V, Output = off state (V_{OUT} = High)	–	–	10	µA
Output Rise Time	t_r	R_{PU} = 1 kΩ, V_{PU} = 5 V	–	4	–	µs
Output Fall Time	t_f		–	6	–	µs

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MAGNETIC CHARACTERISTICS

Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
MAGNETIC CHARACTERISTICS						
Allowable Differential Signal Reduction	$B_{seq(min)}/B_{seq(max)}$	Over 60 cycles, see Figure 2	0.5	–	–	–
	$B_{seq(n+1)}/B_{seq(n)}$	Single cycle-to-cycle variation	0.6	–	–	–

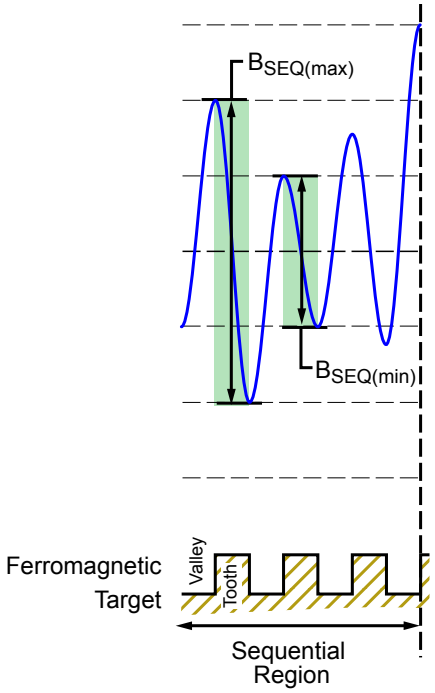

Figure 2: Differential Sequential Signal Variation

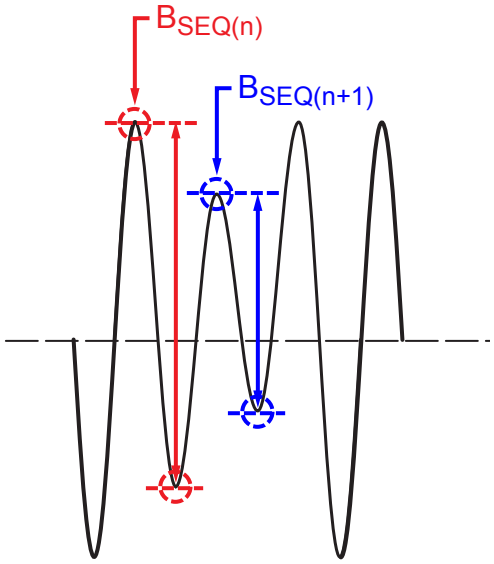

Figure 3: Sequential Pulse Variation

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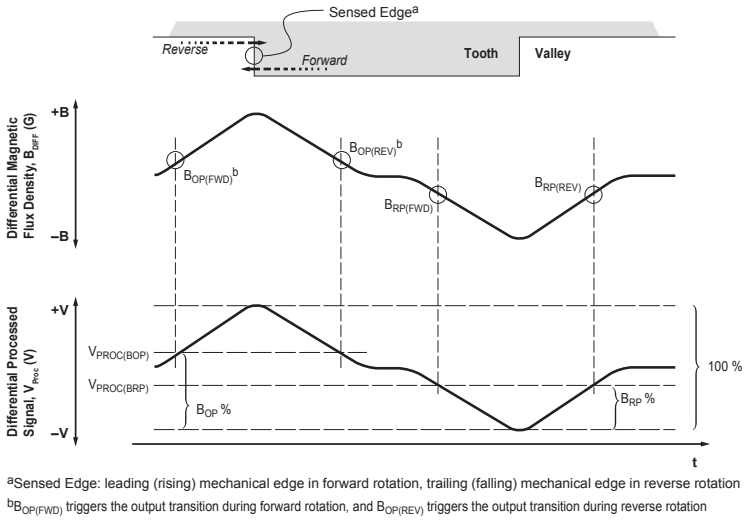
FUNCTIONAL CHARACTERISTICS

Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
POWER ON						
Power-On State	POS	V_{OUT} state at t > t_{PO}; see Figure 1	–	High	–	–
Power-On Time [1]	t_{PO}	f_{op} < 100 Hz	–	–	2	ms
AIR GAP						
Operating Air Gap Range		Guaranteed to operate within specification	0.5	–	2.5	mm
Extended Air Gap Range		Switching only—not guaranteed to operate within spec	2.5	–	3	mm
OFFSET						
Dynamic Offset Cancellation	$B_{DIFFEXT}$	Allowable user-induced offset	±60	–	–	G
CALIBRATION						
Initial Calibration [2]	CAL_I	Quantity of rising output edges required for accurate edge detection	–	2	3	edge
SWITCHING						
Operating Speed	f_{OP}		0	–	12	kHz
Analog Signal Bandwidth	BW		15	20	–	kHz
Operate Point	OP		–	70	–	%
Release Point	RP		–	30	–	%
OUTPUT DUTY CYCLE [3]						
Output Duty Cycle	DC	AG = 0.5 mm to 2.5 mm, Pin 3 to 1 target rotation	39	–	52	%
		AG = 2.5 mm to 3.0 mm, Pin 3 to 1 target rotation	39	–	56	%

[1] Power-On Time includes the time required to complete the internal automatic offset adjust. DAC is then ready for peak acquisition.
[2] For power-on frequency, f_{OP} < 200 Hz. Higher power-on frequencies may result in more input magnetic cycles until full output edge accuracy is achieved, including the possibility of missed output edges.
[3] Measured at f_{OP} = 2 kHz. Output rise and fall times should be considered when measuring duty cycle.



[a]Sensed Edge: leading (rising) mechanical edge in forward rotation, trailing (falling) mechanical edge in reverse rotation
[b]$B_{OP(FWD)}$ triggers the output transition during forward rotation, and $B_{OP(REV)}$ triggers the output transition during reverse rotation

Figure 4: Definition of Terms for Switch Points

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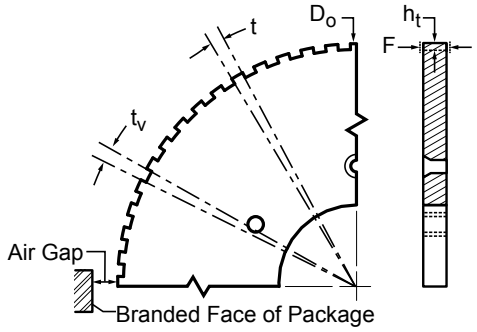
Reference Target 60-0 (60-Tooth Target)

Characteristics	Symbol	Test Conditions	Typ.	Units	Symbol Key
Outside Diameter	D_O	Outside diameter of target	120	mm	
Face Width	F	Breadth of tooth, with respect to sensor IC	6	mm	
Circular Tooth Length	t	Length of tooth, with respect to sensor IC; measured at D_O	3	degrees	
Circular Valley Width	t_v	Length of valley, with respect to sensor IC; measured at D_O	3	degrees	
Tooth Whole Depth	h_t		3	mm	
Material		Low Carbon Steel	–	–	

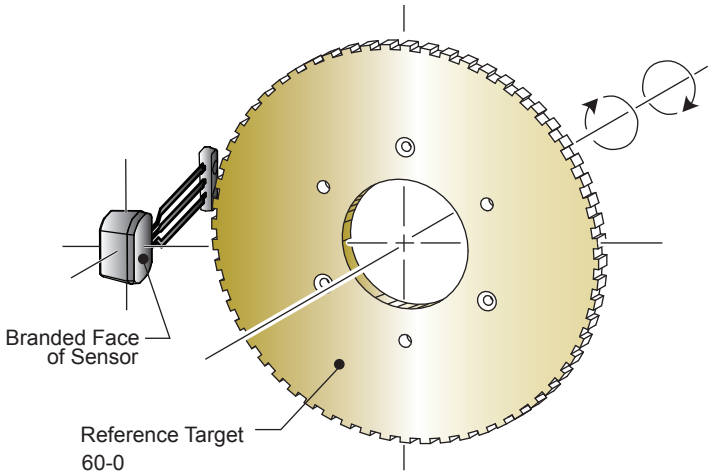


Figure 5: Reference Target Measurement Setup

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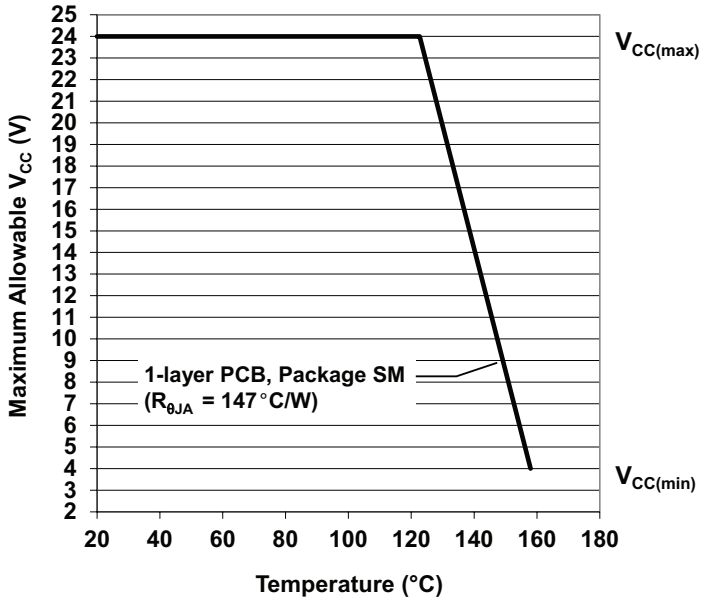
POWER DERATING

THERMAL CHARACTERISTICS: May require derating at maximum conditions, see Power Derating section

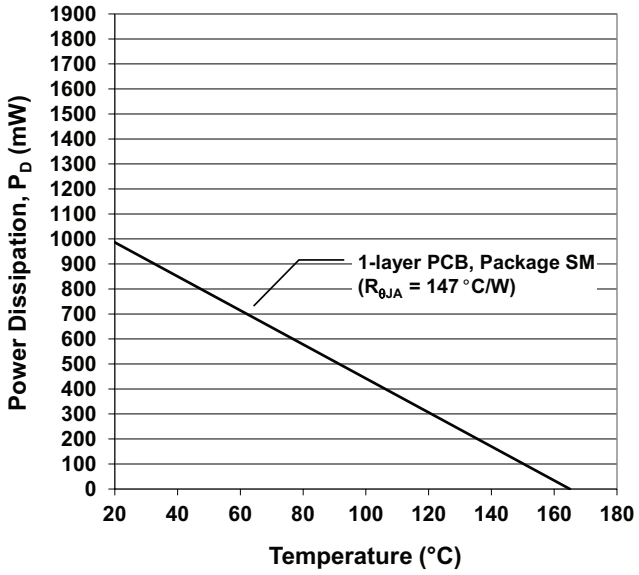
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Single layer PCB, with copper limited to solder pads	147	°C/W

*Additional thermal information available on the Allegro website

Power Derating Curve



Power Dissipation versus Ambient Temperature



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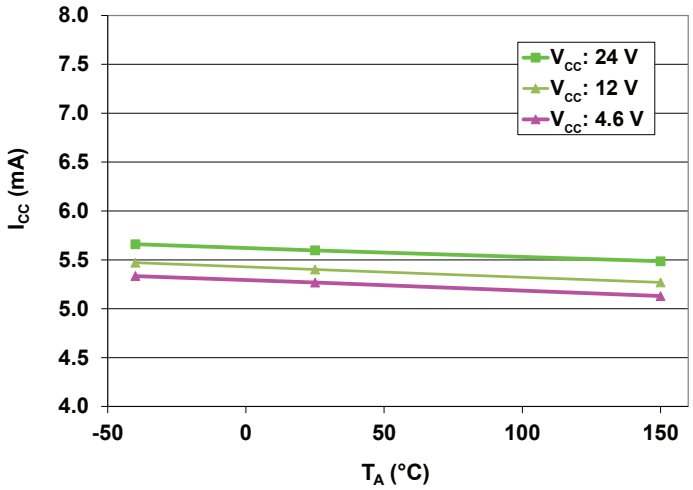
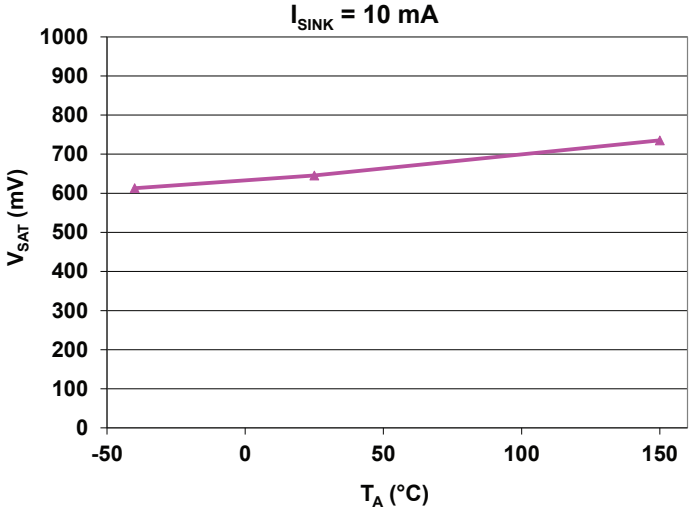
CHARACTERISTIC DATA

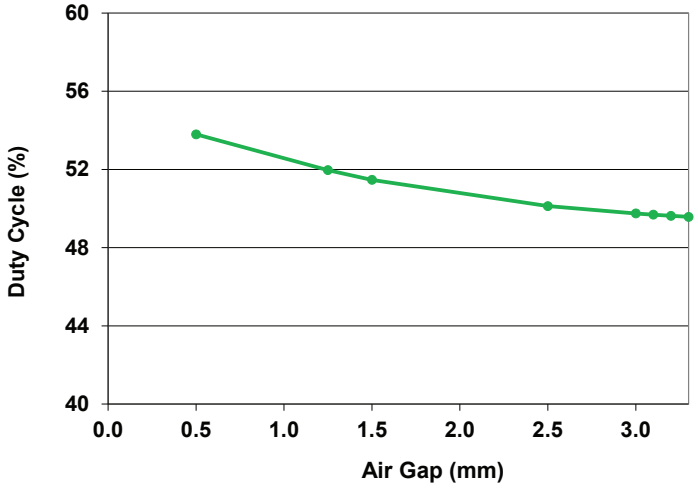
Supply Current versus Ambient Temperature



Output Voltage versus Ambient Temperature
I_{SINK} = 10 mA



Average Duty Cycle versus Air Gap
Pin 1 to 3 Rotation of Allegro Standard Target



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FUNCTIONAL DESCRIPTION

Sensing Technology

The ATS668 contains a single-chip differential Hall-effect sensor IC and a back-biasing pellet. The Hall IC supports a pair of Hall elements which sense the magnetic profile of the ferromagnetic gear target simultaneously, but at different points (spaced at a 2.2 mm pitch), generating a differential internal analog voltage, V_{PROC}, that is processed for precise switching of the digital output signal. The ATS668 is intended for use with ferromagnetic targets.

The Hall IC is self-calibrating and also possesses a temperature compensated amplifier and offset cancellation circuitry. Its voltage regulator provides supply noise rejection throughout the operating voltage range. Changes in temperature do not greatly affect this device due to the stable amplifier design and the offset compensation circuitry. The Hall transducers and signal processing electronics are integrated on the same silicon substrate, using a proprietary BiCMOS process

Target Profiling During Operation

An operating device is capable of providing digital information that is representative of the mechanical features of a rotating gear. The waveform diagram in Figure 7 presents the automatic translation of the mechanical profile, through the magnetic profile that it induces, to the digital output signal of the IC. No additional optimization is needed and minimal processing circuitry is required. This ease of use reduces design time and incremental assembly costs for most applications.

Determining Output Signal Polarity

In Figure 7, the top panel, labeled *Mechanical Position*, represents the mechanical features of the target gear and orientation to the device. The bottom panel, labeled *IC Output Signal*, displays the square waveform corresponding to the digital output signal that results from a rotating gear configured as shown in Figure 6 and electrically connected as in Figure 1. That direction of rotation (of the gear side adjacent to the package face) is: perpendicular to the leads, across the face of the device, from the pin 1 side to the pin 3 side. This results in the IC output switching from low state to high state as the leading edge of a tooth (a rising

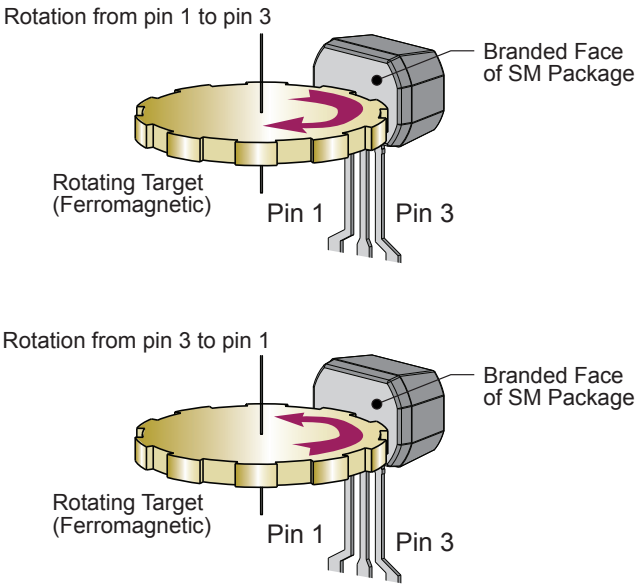

Figure 6: Sensor and target configuration. The output is low when a tooth of the target gear is nearest the branded face of the package.

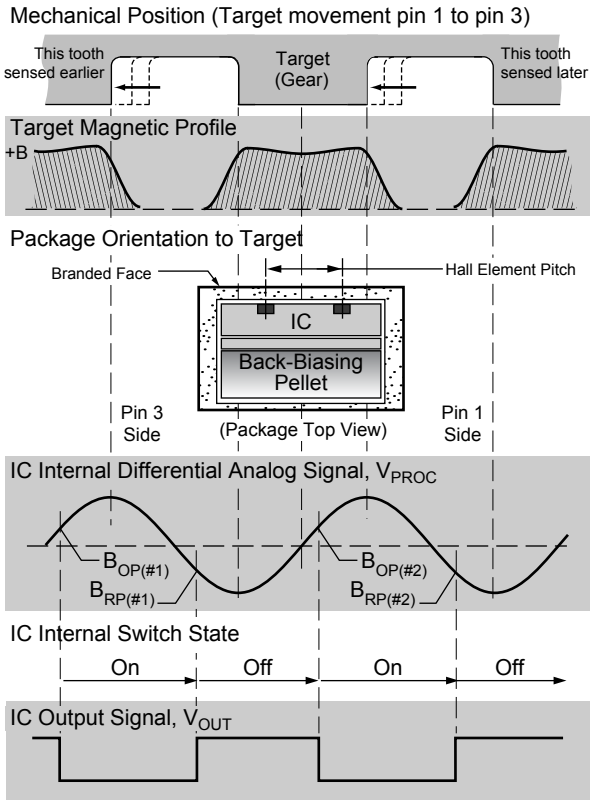

Figure 7: The magnetic profile reflects the features of the target, allowing the sensor IC to present an accurate digital representation of the target teeth.

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mechanical edge, as detected by the IC) passes the package face. In this configuration, the device output switches to its high polarity when a tooth is the target feature nearest to the package. If the direction of rotation is reversed, so that the gear rotates from the pin 3 side to the pin 1 side, then the output polarity inverts. That is, the output signal goes high when a falling edge is detected, and a valley is nearest to the package.

Undervoltage Lockout

When the supply voltage falls below the undervoltage lockout voltage, $V_{CC(min)}$, the device enters Reset, where the output state returns to the Power-On State (POS) until sufficient V_{CC} is supplied. This lockout feature prevents false signals, caused by undervoltage conditions, from propagating to the output of the IC.

Power Supply Protection

The device contains an on-chip regulator and can operate over a wide V_{CC} range. The device also includes integrated in-package EMC protection components virtually eliminating the need for additional external passive components.

Automatic Gain Control (AGC)

This feature allows the device to operate with an optimal internal electrical signal, regardless of the air gap (within the AG specification). At power-on, the device determines the peak-to-peak amplitude of the signal generated by the target. The gain of the IC is then automatically adjusted. Figure 8 illustrates the effect of this feature.

Automatic Offset Adjust (AOA)

The AOA circuitry automatically compensates for the effects of chip, magnet, and installation offsets. This circuitry is continuously active, including during both power-on mode and running mode, compensating for any offset drift (within the Allowable User-Induced Differential Offset). Continuous operation also allows it to compensate for offsets induced by temperature variations over time.

Running Mode Lockout

The ATS668 has a running mode lockout feature to prevent switching in response to small signals that are characteristic of vibration signals. The internal logic of the chip considers small-signal amplitudes below a certain level to be vibration. The output is held to the state prior to lockout until the amplitude of the signal returns to normal operational levels.

Watchdog

The ATS668 employs a watchdog circuit to prevent extended loss of output switching during sudden impulses and vibration in the system. If the system changes the magnetic input drastically such that target feature detection is terminated, the device will fully reset itself, allowing the chip to recalibrate properly on the new magnetic input signal.

Assembly Description

The ATS668 is integrally molded into a plastic body that has been optimized for size, ease of assembly, and manufacturability. High operating temperature materials are used in all aspects of construction.

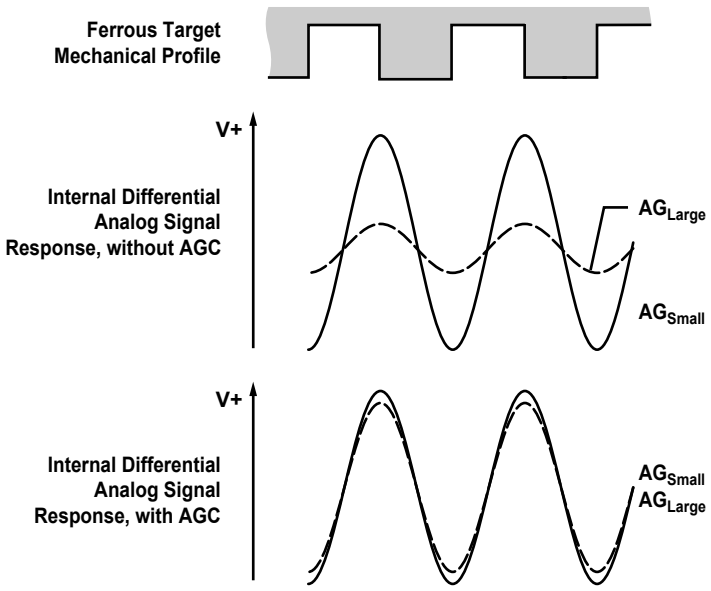

Figure 8: Automatic Gain Control (AGC). The AGC function corrects for variances in the air gap. Differences in the air gap cause differences in the magnetic field at the device, but AGC prevents that from affecting device performance, as shown in the lowest panel.

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POWER DERATING

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 6.5 mA, and $R_{\theta JA}$ = 147°C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 6.5\ mA = 78\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 78\ mW \times 147°C/W = 11.5°C$$

$$T_J = T_A + \Delta T = 25°C + 11.5°C = 36.5°C$$

A worst-case estimate, $P_D(max)$, represents the maximum allowable power level ($V_{CC}(max)$, $I_{CC}(max)$), without exceeding $T_J(max)$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=147°C/W, $T_J(max)$=165°C, $V_{CC}(max)$ = 24 V, and $I_{CC}(max)$ = 12 mA.

Calculate the maximum allowable power level, $P_D(max)$. First, invert equation 3:

$$\Delta T_{max} = T_J(max) - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_D(max) = \Delta T_{max} \div R_{\theta JA} = 15°C \div 147°C/W = 102\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC}(est) = P_D(max) \div I_{CC}(max) = 102\ mW \div 12\ mA = 8.5\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤V_{CC}(est).

Compare V_{CC}(est) to V_{CC}(max). If V_{CC}(est) ≤ V_{CC}(max), then reliable operation between V_{CC}(est) and V_{CC}(max) requires enhanced $R_{\theta JA}$. If V_{CC}(est) ≥ V_{CC}(max), then operation between V_{CC}(est) and V_{CC}(max) is reliable under these conditions.

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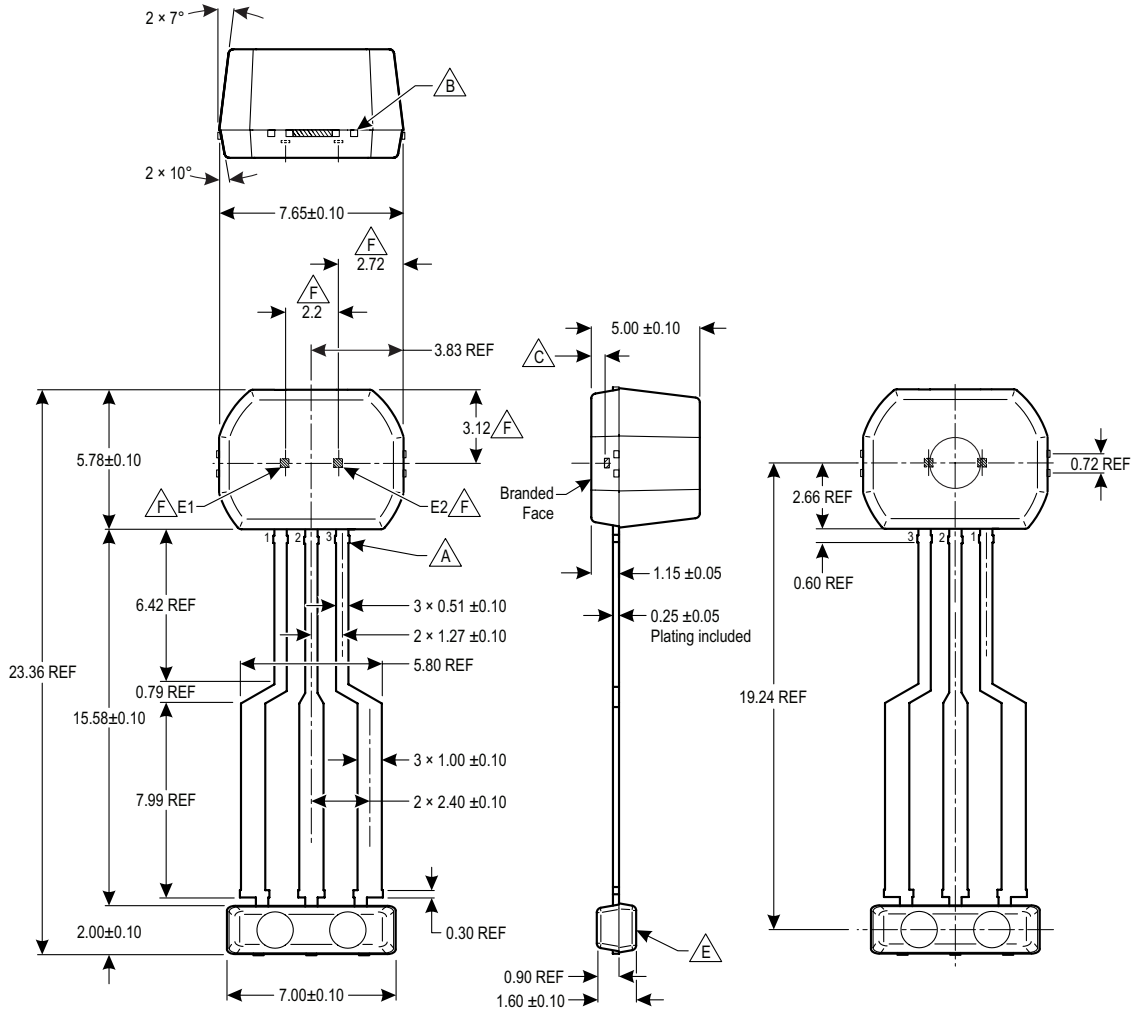
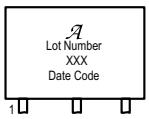
Package SM, 3-Pin SIP

For Reference Only – Not for Tooling Use

(Reference DWG-0000417, Rev. 3)
Dimensions in Millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





D Standard Branding Reference View

Lines 1, 2, 3, 4: Max. 10 characters per line

Line 1: Logo A
Line 2: Characters 5, 6, 7, 8, 9, 10, 11 of Assembly Lot Number
Line 3: Last 3 digits of Part Number; additional suffixes may be added to Part Number as required
Line 4: 4-digit Date Code

A Dambar removal protrusion (12×)
B Gate and tie bar burr area
C Active Area Depth 0.40 ±0.05 mm
D Branding scale and appearance at supplier discretion
E Molded lead bar for preventing damage to leads during shipment
F Hall elements (E1 and E2), not to scale

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Revision History

Number	Date	Description
–	March 17, 2017	Initial release
1	March 22, 2017	Updated Power Derating and Thermal Characteristics
2	April 24, 2017	Updated Electrical Characteristics table
3	July 2, 2019	Minor editorial updates
4	July 1, 2021	Updated Package Outline Drawing (page 12)

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