THE DATASHEET OF

ISL8117FVEZ-T7A

ISL8117

Synchronous Step-Down PWM Controller

The ISL8117 is a synchronous buck controller used to generate POL voltage rails and bias voltage rails for a wide variety of applications in industrial and general purpose segments. Its wide input and output voltage ranges make it suitable for telecommunication and after-market automotive applications.

The ISL8117 uses the valley current modulation technique to bring hassle-free power supply design with a minimal number of components and complete protection from unwanted events.

The ISL8117 offers programmable soft-start and enable functions along with a power-good indicator for ease of supply rail sequencing and other housekeeping requirements. In ideal situations, a complete power supply circuit can be designed with 10 external components and provide OV/OC/OT protections in a space conscious 16 Ld 4mmx4mm QFN or easy to assemble 6.4mmx5mm 16 Ld HTSSOP package. Both packages use an EPAD to improve thermal dissipation and noise immunity. Low pin count, fewer external components, and default internal values makes the ISL8117 an ideal solution for quick to market simple power supply designs. The ISL8117 uses internal loop compensation and single resistor settings for other functions such as operating frequency and overcurrent protection. Its current mode control with V_{IN} feed-forward enables it to cover various applications even with fixed internal compensations. The unique DEM/Skipping mode at light-load dramatically lowers standby power consumption with consistent output ripple over different load levels.

Features

- Wide input voltage range: 4.5V to 60V
- Wide output voltage range: 0.6V to 54V
- Light-load efficiency enhancement
  - Low ripple Diode Emulation mode with pulse skipping
- Programmable soft-start
- Supports prebiased output with SR soft-start
- Programmable frequency: 100kHz to 2MHz
- External sync
- PGOOD indicator
- Forced PWM
- Adaptive shoot-through protection
- No external current sense resistor
  - Use lower MOSFET $r_{DS(ON)}$
- Complete protection
  - Overcurrent, overvoltage, over-temperature, undervoltage
  - Pb-free (RoHS compliant)

Applications

- PLC and factory automation
- Amusement machines
- Security surveillance
- Servers and data centers
- Switchers and routers
- Telecom and datacom
- LED panels

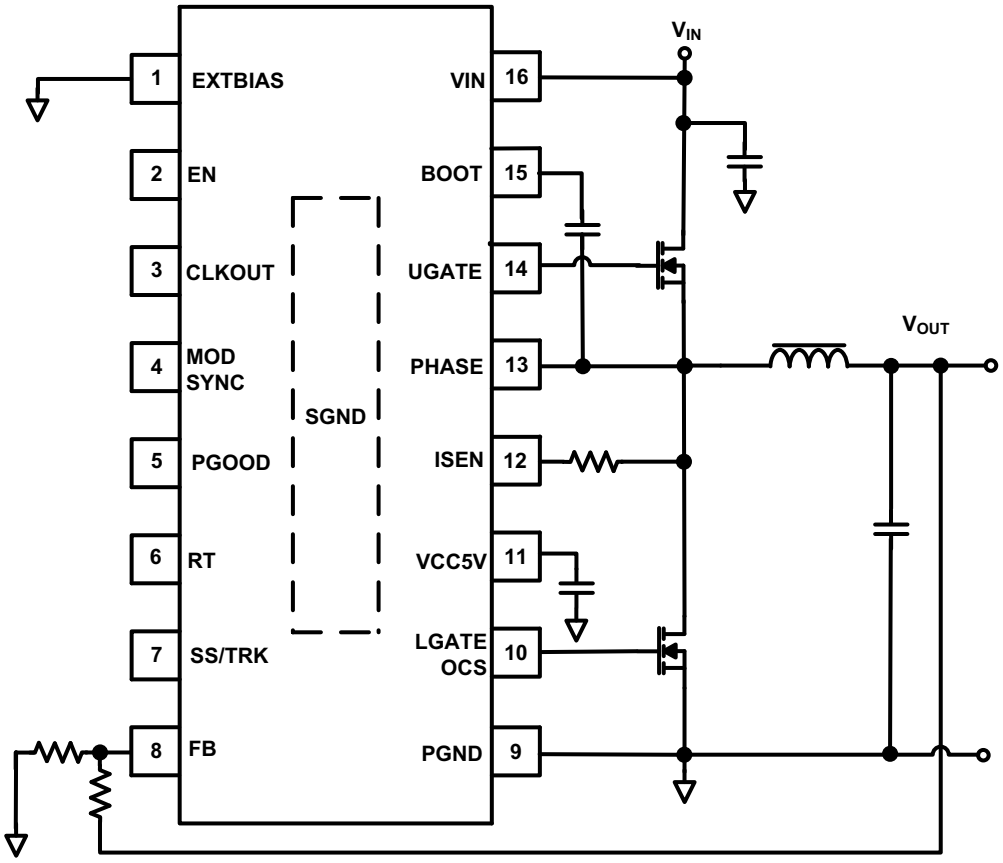


Figure 1. Typical Application

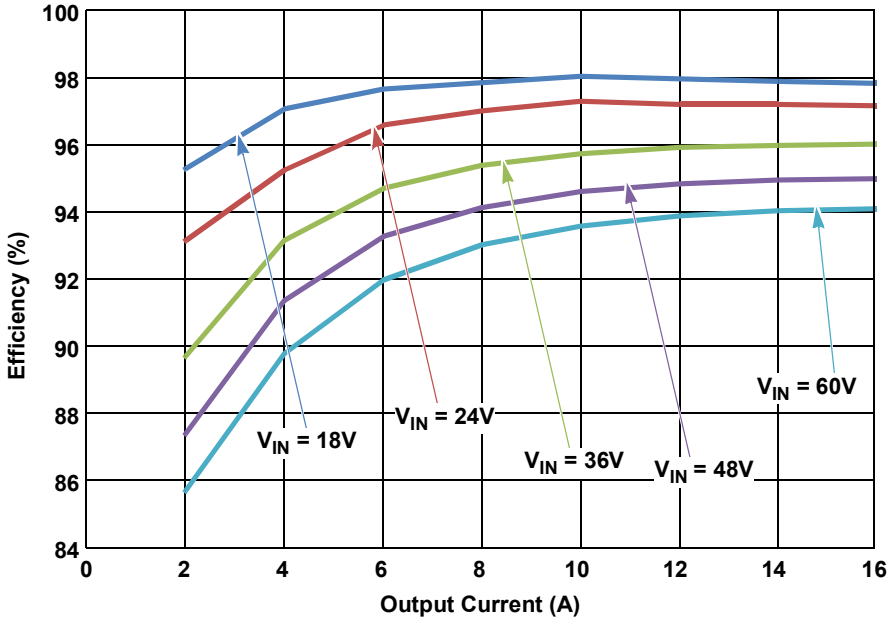


Figure 2. Efficiency

Contents

1. Overview

1.1 Block Diagram

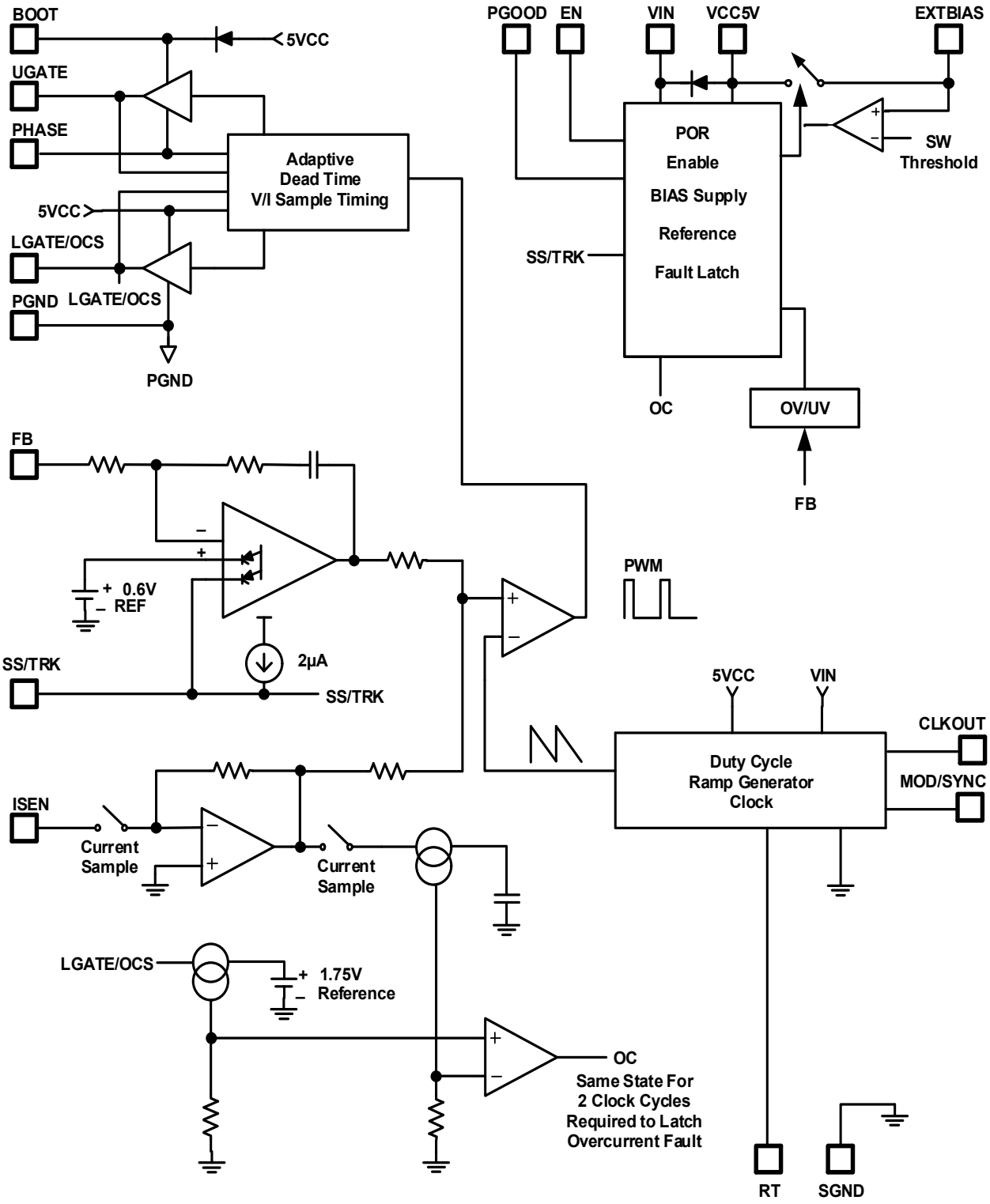


Figure 3. Block Diagram

1.2 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temp. Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL8117FRZ	81 17FRZ	-40 to +125	-	16 Ld 4x4 QFN	L16.4x4A
ISL8117FRZ-T	81 17FRZ	-40 to +125	6k	16 Ld 4x4 QFN	L16.4x4A
ISL8117FRZ-T7A	81 17FRZ	-40 to +125	250	16 Ld 4x4 QFN	L16.4x4A
ISL8117FVEZ	8117 FVEZ	-40 to +125	-	16 Ld HTSSOP	M16.173A
ISL8117FVEZ-T	8117 FVEZ	-40 to +125	2.5k	16 Ld HTSSOP	M16.173A
ISL8117FVEZ-T7A	8117 FVEZ	-40 to +125	250	16 Ld HTSSOP	M16.173A
ISL8117EVAL1Z	Evaluation Board for HTSSOP				
ISL8117EVAL2Z	Evaluation Board for QFN				
ISL8117DEMO1Z	Demonstration Board for HTSSOP				
ISL8117DEMO2Z	Demonstration Board for QFN				
ISL8117DEMO3Z	Demonstration Board for QFN				
ISL8117DEMO4Z	Demonstration Board for QFN				

Notes:

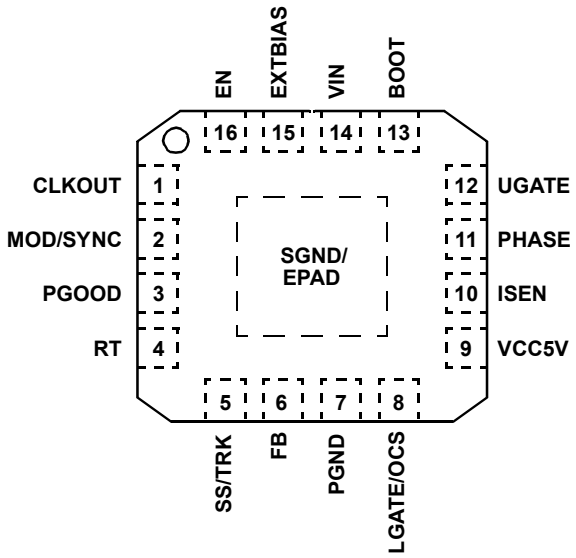
1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL8117 device page. For more information about MSL, see TB363.

Table 1. Key Differences Between Family of Parts

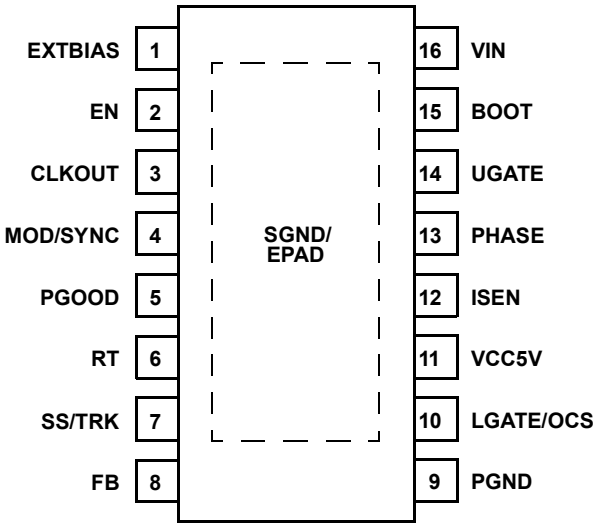
Part Number	Loop Compensation	Clock Output Signal	Package
ISL8117	Internal compensation without COMP pin	Clock Output Signal on CLKOUT pin	16 Ld 4x4 QFN,16 Ld HTSSOP
ISL8117A	External compensation with COMP pin	No clock output signal	16 Ld 4x4 QFN

1.3 Pin Configuration

16 LD 4x4 QFN
Top View



16 LD HTSSOP
Top View



1.4 Pin Descriptions

PIN # (QFN)	PIN # (HTSSOP)	PIN Name	Function
1	3	CLKOUT	Clock signal output. The frequency of the clock signal is the switching frequency set by the resistor from RT to ground.
2	4	MOD/ SYNC	Dual function pin. Connect this pin to VCC5V to select Diode Emulation mode with pulse skipping at light-load. While connected to ground or floating, the controller operates in PWM mode at light-load. Connect this pin to an external clock for synchronization. The controller operates in PWM mode at light-load when synchronized with an external clock.
3	5	PGOOD	Open-drain logic output used to indicate the status of output voltage. This pin is pulled down when the output is not within ±11% of the nominal voltage or the EN pin is pulled LOW.
4	6	RT	A resistor from this pin to ground adjusts the switching frequency from 100kHz to 2MHz. The switching frequency of the PWM controller is determined by the resistor, R_T as shown in Equation 1. (EQ. 1) $R_T = \left(\frac{39.2}{f_{SW}} - 1.96\right) \cdot k\Omega$ Where f_{SW} is the switching frequency in MHz. When this pin is tied to ground, the output frequency is set to 300kHz. When this pin is tied to VCC5V or floating, the output frequency is set to 600kHz.
5	7	SS/TRK	Dual function pin. When used for soft-starting control, a soft-start capacitor is connected from this pin to ground. A regulated 2µA soft-starting current charges up the soft-start capacitor. The value of the soft-start capacitor sets the output voltage ramp. When used for tracking control, an external supply rail is configured as the master and the output voltage of the master supply is applied to this pin using a resistor divider. The output voltage tracks the master supply voltage.
6	8	FB	Output feedback input. Connect FB to a resistive voltage divider from the output to SGND to adjust the output voltage.
7	9	PGND	Power ground connection. This pin should be connected to the sources of the lower MOSFETs and the (-) terminals of the external input capacitors.
8	10	LGATE/ OCS	Low-side MOSFET gate driver output and OC set pin. Connect a 1k to 30k resistor between this pin and ground to set the overcurrent threshold. If no resistor is connected from this pin to GND, the overcurrent threshold is automatically set to the same point as a 10k resistor.

PIN # (QFN)	PIN # (HTSSOP)	PIN Name	Function
9	11	VCC5V	Output of the internal 5V linear regulator. This output supplies bias for the IC, the low-side gate driver, and the internal boot circuitry for the high-side gate driver. The VCC5V pin must always be decoupled to power ground with a minimum of 4.7µF ceramic capacitor placed very close to the pin. Do not allow the voltage at VCC5V to exceed V_{IN} at any time. To prevent excessive current through the VCC5V pin to the VIN pin, a resistor can be connected from the VIN pin to the power supply.
10	12	ISEN	Current sense signal input. This pin is used to monitor the voltage drop across the lower MOSFET for current loop feedback and overcurrent protection.
11	13	PHASE	Phase node connection. This pin is connected to the junction of the upper MOSFET's source, output filter inductor, and lower MOSFET's drain.
12	14	UGATE	High-side MOSFET gate driver output.
13	15	BOOT	Bootstrap pin to provide bias for high-side driver. The positive terminal of the bootstrap capacitor connects to this pin. The bootstrap diode is integrated to help reduce total cost and reduce layout complexity.
14	16	VIN	Tie this pin should be tied to the input rail. This pin provides power to the internal linear drive circuitry and is also used by the feed-forward controller to adjust the amplitude of the PWM sawtooth. Decouple this pin with a small ceramic capacitor (0.1µF to 1µF) to ground.
15	1	EXTBIAS	Input from an optional external 5V bias supply. There is an internal switch from this pin to VCC5V. When voltage at EXTBIAS is higher than 4.7V (typical), this switch closes and supplies the IC power to bypass the internal linear regulator. Do not allow voltage at the EXTBIAS pin to exceed V_{IN} at any time. To prevent excessive current through the EXTBIAS pin to the V_{IN} pin, a resistor can be connected from the VIN pin to the power supply. Decouple this pin to ground with a small ceramic capacitor (0.1µF to 1µF) when it is in use, otherwise tie this pin to ground. DO NOT float this pin.
16	2	EN	Provides an enable/disable function. The output is disabled when the pin is pulled to ground. When the voltage on the pin reaches 1.6V, the output becomes active. When the pin is floating, it is enabled in default by internal pull-up.
-	-	SGND EPAD	Small-signal ground common to all control circuitry. Renesas recommends routing this ground separately from the high current ground (PGND). SGND and PGND can be tied together if there is one solid ground plane with no noisy currents around the chip. All voltage levels are measured with respect to this pin. EPAD at ground potential. EPAD is connected to SGND internally. However, it is highly recommended to solder the EPAD directly to ground plane for better thermal performance and noise immunity.

1.5 Typical Application Schematics

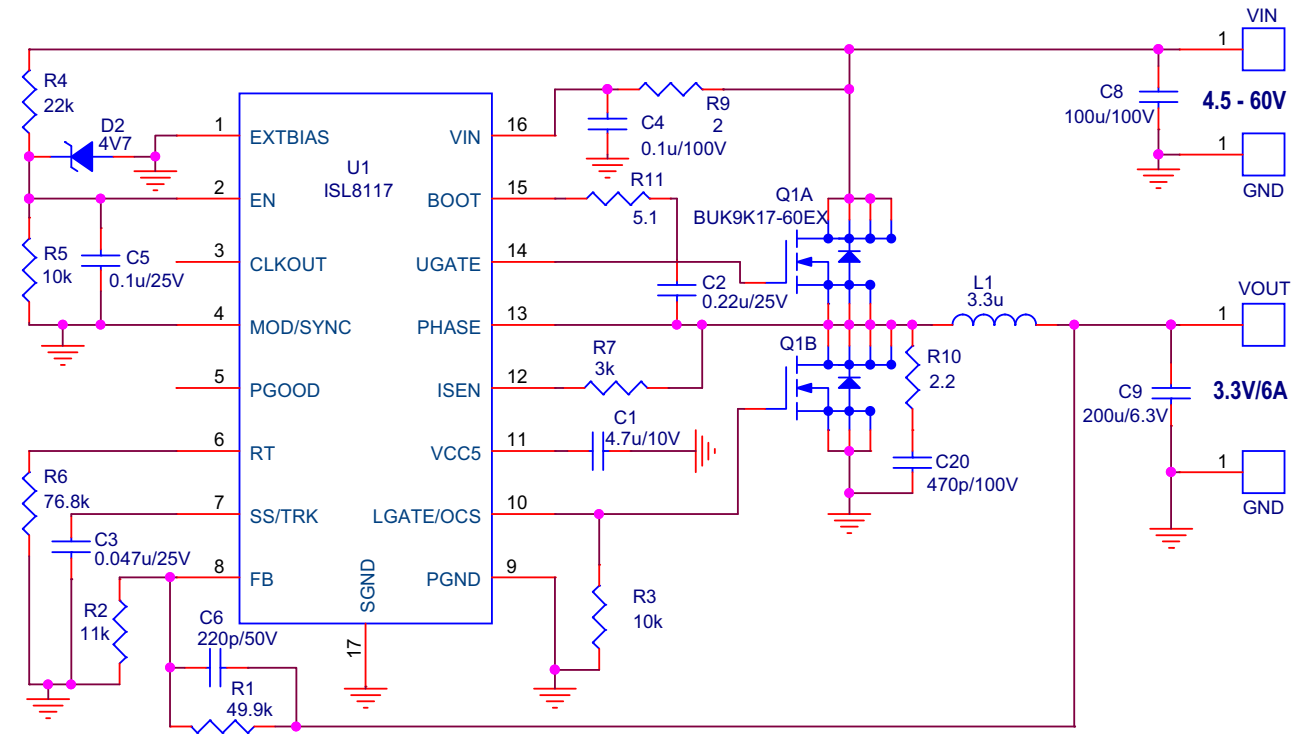


Figure 4. ISL8117EVAL1Z Evaluation Board Schematic

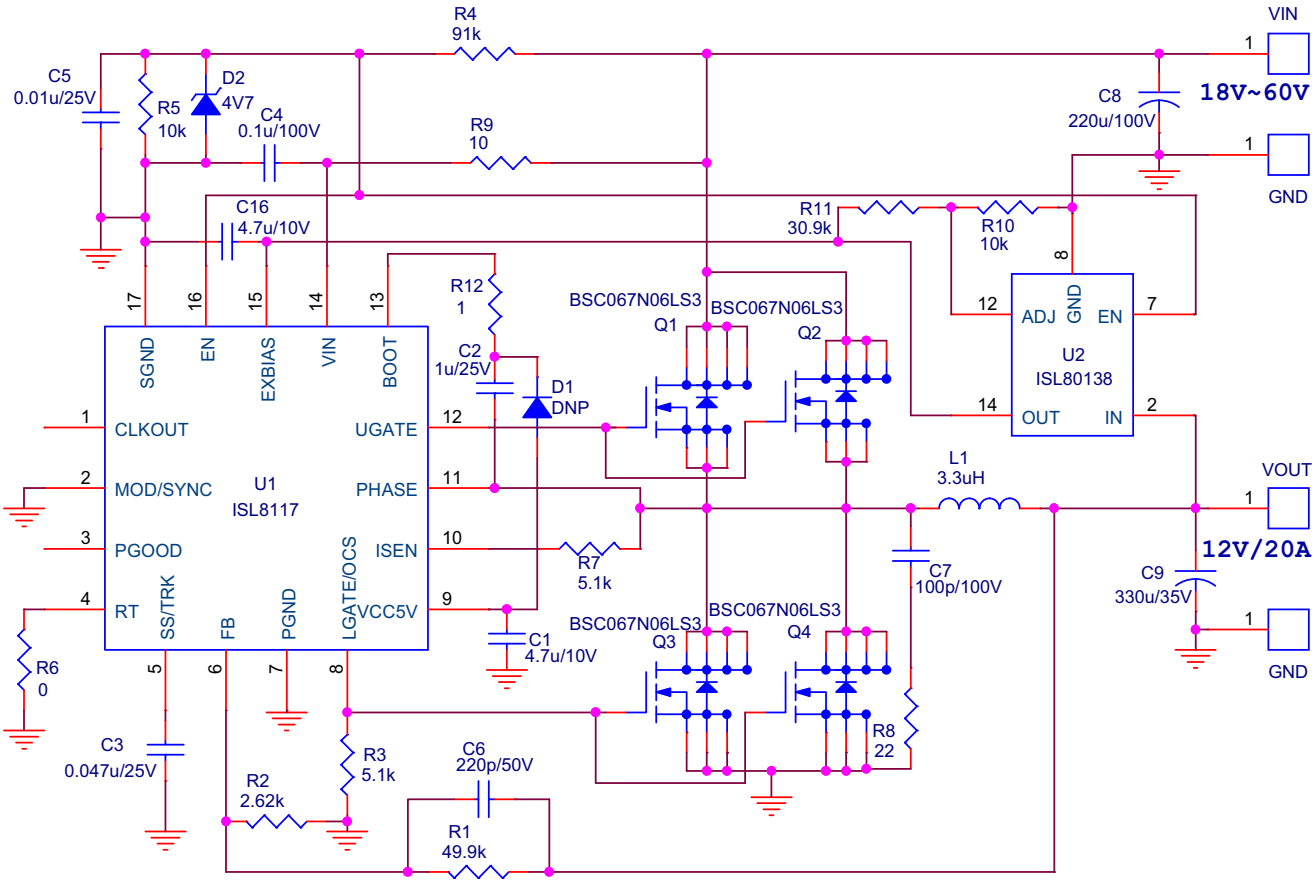


Figure 5. ISL8117EVAL2Z Evaluation Board Schematic

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VCC5V to GND	-0.3	+5.9	V
EXTBIAS to GND	-0.3	+5.9	V
VIN to GND	-0.3	+62.5	V
BOOT/UGATE to PHASE	-0.3	VCC5V + 0.3V	V
PHASE and ISEN to GND	-5V (<20ns) / -0.3 (DC)	+62.5	V
EN, PGOOD, SS/TRK, FB to GND	-0.3	VCC5V + 0.3	V
LGATE/OCS to GND	-0.3	VCC5V + 0.3	V
RT, MOD/SYNC, CLKOUT to GND	-0.3	VCC5V + 0.3	V
VCC5V Short-Circuit to GND Duration		1	s
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2010)	2		kV
Charge Device Model (Tested per JESD22-C101E)	0.75		kV
Latch-Up (Tested per JESD78E; Class 2, Level A, +125°C)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld QFN Package (Notes 4, 5)	40	2.5
16 Ld HTSSOP Package (Notes 4, 5)	35	4.5

Notes:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
5. For θ_{JC}, the case temperature location is the center of the ceramic on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-55	+150	°C
Maximum Operating Temperature	-40	+125	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Maximum	-40	+125	°C
VIN to GND	4.5	+60	V
VCC5V to GND	-0.1	+5.5	V
EXTBIAS to GND	-0.2	+5.5	V

2.4 Electrical Specifications

Recommended operating conditions unless otherwise noted. See Block Diagram and Typical Application Schematics. V_{IN} = 4.5V to 60V, or VCC5V = 5V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

Parameter	Symbol	Test Conditions	Min (Note 9)	Typ	Max (Note 9)	Unit
V_{IN} Supply						
Input Voltage Range	V_{IN}		**4.5**		**60.0**	V
V_{IN} Supply Current						
Shutdown Current (Note 6)	I_{VINQ}	EN = 0 PGOOD is floating		5	**10**	µA
Operating Current (Note 8)	I_{VINOP}	PGOOD is floating		2.5	**4**	mA
Vcc5v Supply (Note 6)						
Operation Voltage	V_{CC}	V_{IN} = 12V, I_L = 0mA	**4.85**	5.1	**5.4**	V
Internal LDO Output Voltage		V_{IN} = 4.5V, I_L = 30mA	**4.1**	4.4		V
Internal LDO Output Voltage		V_{IN} > 5.6V, I_L = 75mA	**4.75**	5.05		V
Maximum Supply Current of Internal LDO	I_{VCC_MAX}	V_{VCC5V} = 0V, V_{IN} = 12V		120		mA
EXTBIAS Supply (Note 6)						
Switch Over Threshold Voltage, Rising	V_{EXT_THR}	EXTBIAS voltage	**4.5**	4.7	**4.9**	V
Switch Over Threshold Voltage, Falling	V_{EXT_THF}	EXTBIAS voltage	**4.2**	4.5	**4.65**	V
Internal Switch ON-resistance	R_{EXT}	V_{IN} = 12V		1.5		Ω
Undervoltage Lockout						
Undervoltage Lockout, Rising	$V_{UVLOTHR}$	V_{IN} voltage, 0mA on VCC5V	**3.7**	3.90	**4.2**	V
Undervoltage Lockout, Falling	$V_{\overline{UVLOTHF}}$	V_{IN} voltage, 0mA on VCC5V	**3.35**	3.50	**3.85**	V
EN Threshold						
EN Rise Threshold	V_{ENSS_THR}	V_{IN} > 5.6V	**1.25**	1.60	**1.95**	V
EN Fall Threshold	V_{ENSS_THF}	V_{IN} > 5.6V	**1.05**	1.25	**1.55**	V
EN Hysteresis	V_{ENSS_HYST}	V_{IN} > 5.6V	**180**	350	**500**	mV
Soft-start Current						
SS/TRK Soft-Start Charge Current	I_{SS}	SS/TRK = 0V		2.00		µA
Default Internal Minimum Soft-starting						
Default Internal Output Ramping Time	t_{SS_MIN}	SS/TRK open		1.5		ms
Power-Good Monitors						
PGOOD Upper Threshold	V_{PGOV}		**109**	112.5	**115**	%
PGOOD Lower Threshold	V_{PGUV}		**85**	87.5	**92**	%
PGOOD Low Level Voltage	V_{PGLOW}	I_SINK = 2mA			**0.35**	V
PGOOD Leakage Current	I_{PGLKG}	PGOOD = 5V		20	**150**	nA
PGOOD Timing						
V_{OUT} Rising Threshold to PGOOD Rising (Note 11)	t_{PGR}			1.1	**5**	ms
V_{OUT} Falling Threshold to PGOOD Falling	t_{PGF}			75		µs
Reference Section						
Internal Reference Voltage	V_{REF}			0.600		V
Reference Voltage Accuracy		T_A = 0°C to +85°C	**-0.75**		**+0.75**	%
		T_A = -40°C to +125°C	**-1.00**		**+1.00**	%
GOOD	I_{FBLKG}		**-40**	0	**40**	nA

Recommended operating conditions unless otherwise noted. See Block Diagram and Typical Application Schematics. V_{IN} = 4.5V to 60V, or VCC5V = 5V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 9)	Typ	Max (Note 9)	Unit
PWM Controller Error Amplifiers						
DC Gain				88		dB
Gain-BW Product	GBW			8		MHz
Slew Rate	SR			2.0		V/µs
PWM Regulator						
Minimum Off Time	t_{OFF_MIN}			308		ns
Minimum On Time	t_{ON_MIN}			40		ns
Peak-to-Peak Sawtooth Amplitude	DV_{RAMP}	V_{IN} = 20V		1.0		V
		V_{IN} = 12.0V		0.6		V
Ramp Offset				1.0		V
Switching Frequency						
Switching Frequency	f_{SW}	R_T = 36k	**890**	1050	**1195**	kHz
Switching Frequency		R_T = 16.5k	**1650**	2000	**2375**	kHz
Switching Frequency		RT PIN connect to GND	**250**	300	**350**	kHz
Switching Frequency		RT PIN connect to VCC5V or FLOAT	**515**	600	**645**	kHz
RT Voltage	V_{RT}	R_T = 36k		770		mV
Clock Output and Synchronization						
CLKOUT Output High	VCLKH	I_{SOURCE} = 1mA	**VCC5V - 0.3**			V
CLKOUT Output Low	V_{CLKL}	I_{SINK} = 1mA			**0.3**	V
CLKOUT Frequency	f_{CLK}	R_T = VCC5V	**515**	600	**645**	kHz
SYNC Synchronization Range	f_{SYNC}	R_T = 36kΩ	**1230**		**2200**	kHz
Diode Emulation Mode Detection						
MOD/SYNC Threshold High	$V_{MODETHH}$		**1.1**	1.6	**2.1**	V
MOD/SYNC Hysteresis	$V_{MODEHYST}$			200		mV
Diode Emulation Phase Threshold (Note 10)	V_{CROSS}	V_{IN} = 12V		-3		mV
PWM Gate Driver						
Source Current	I_{GSRC}			2000		mA
Sink Current	I_{GSNK}			2000		mA
Upper Drive Pull-Up	R_{UG_UP}	VCC5V = 5.0V		1.5		Ω
Upper Drive Pull-Down	R_{UG_DN}	VCC5V = 5.0V		1.5		Ω
Lower Drive Pull-Up	R_{LG_UP}	VCC5V = 5.0V		1.0		Ω
Lower Drive Pull-Down	R_{LG_DN}	VCC5V = 5.0V		0.8		Ω
Upper Drive Rise Time	t_{GR_UP}	C_{OUT} = 1000pF		9.0		ns
Upper Drive Fall Time	t_{GF_UP}	C_{OUT} = 1000pF		8.0		ns
Lower Drive Rise Time	t_{GR_DN}	C_{OUT} = 1000pF		7.0		ns
Lower Drive Fall Time	t_{GF_DN}	C_{OUT} = 1000pF		6.1		ns
Overvoltage Protection						
OVP Threshold	V_{OVTH}		**116**	121	**127**	%
Overcurrent Protection						
OC Set Current Source	$I_{OCSET-CS}$	LGATE/OCS = 0V	**9**	10.5	**11.5**	µA

Recommended operating conditions unless otherwise noted. See Block Diagram and Typical Application Schematics. V_{IN} = 4.5V to 60V, or VCC5V = 5V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 9)	Typ	Max (Note 9)	Unit
Over-Temperature						
Over-Temperature Shutdown	T_{OT-TH}			160		°C
Over-Temperature Hysteresis	T_{OT-HYS}			15		°C

Notes:

6. In normal operation where the device is supplied with voltage on the VIN pin, the VCC5V pin provides a 5V output capable of 75mA (min). When the device is supplied by an external 5V supply on the EXTBIAS pin, the internal LDO regulator is disabled. The voltage at VCC5V should not exceed the voltage at VIN at any time. (See "Pin Descriptions" on page 6 for more details.)
7. This is the total shutdown current with V_{IN} = 5.6V and 60V.
8. Operating current is the supply current consumed when the device is active but not switching. It does not include gate drive current.
9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. Threshold voltage at PHASE pin for turning off the bottom MOSFET during DEM.
11. When soft-start time is less than 4.5ms, t_{PGR} increases. With internal soft-start (the fastest soft-start time), t_{PGR} increases close to its max limit 5ms.

3. Typical Performance Curves

Oscilloscope plots are taken using the ISL8117EVAL2Z evaluation board, V_{IN} = 18 to 60V, VOUT = 12V, I_{OUT} = 20A, unless otherwise noted.

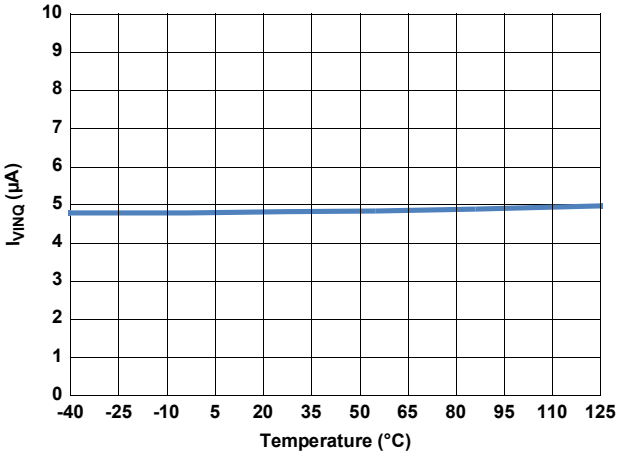


Figure 6. Shutdown Current Vs Temperature

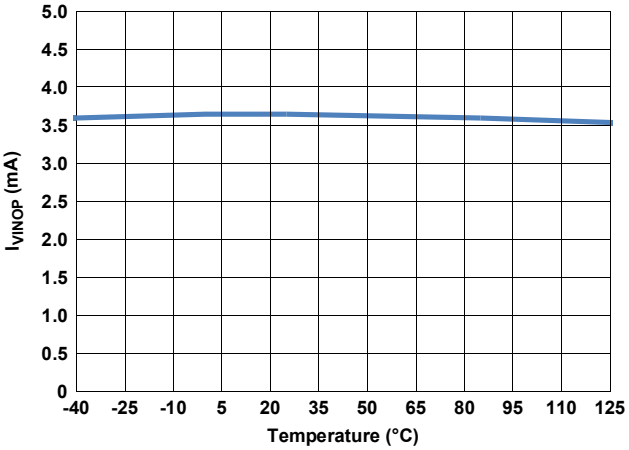


Figure 7. Quiescent Current vs Temperature

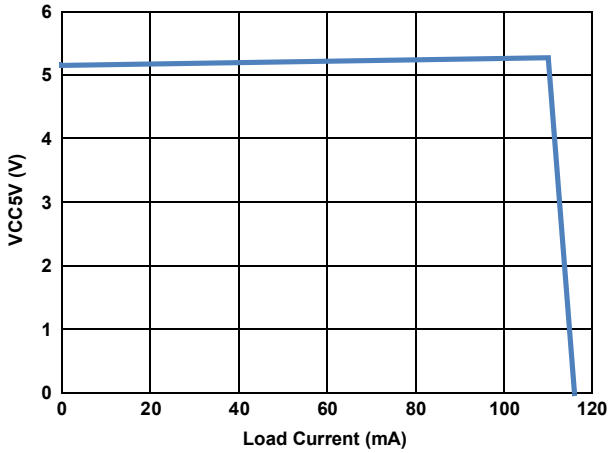


Figure 8. VCC5V Load Regulation

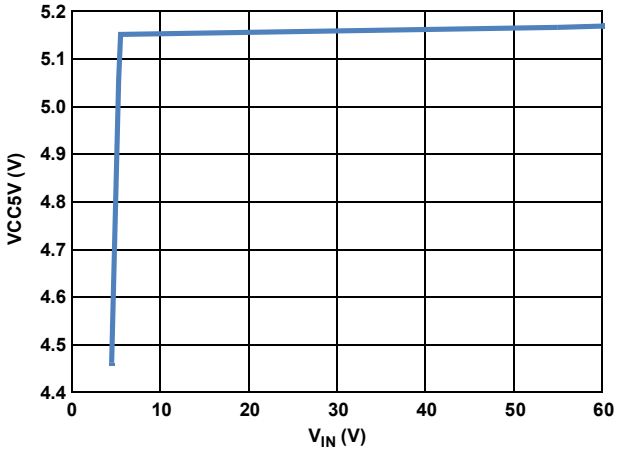


Figure 9. VCC5V Line Regulation

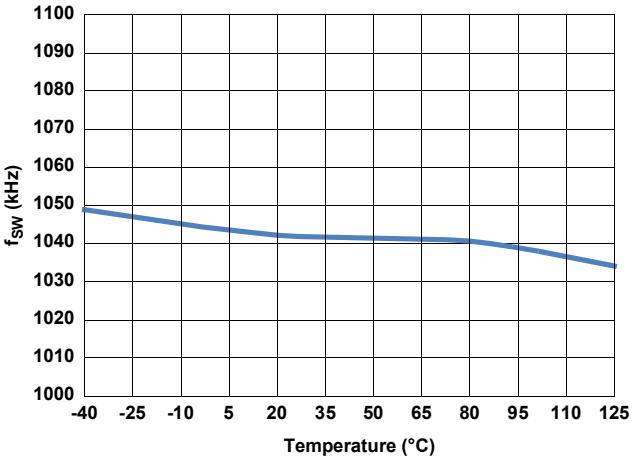


Figure 10. Switching Frequency vs Temperature (R_T = 36kΩ)

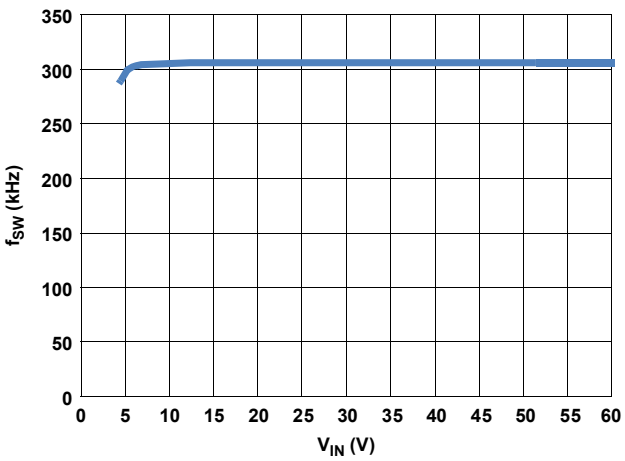


Figure 11. Switching Frequency vs V_{IN}

Oscilloscope plots are taken using the ISL8117EVAL2Z evaluation board, V_{IN} = 18 to 60V, VOUT = 12V, I_{OUT} = 20A, unless otherwise noted. **(Continued)**

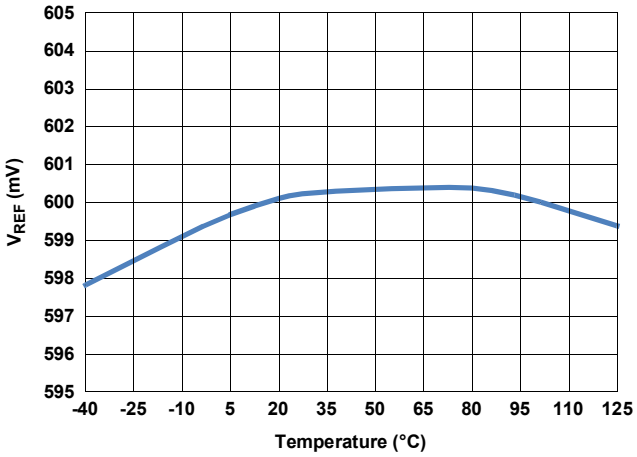


Figure 12. Reference Voltage vs Temperature

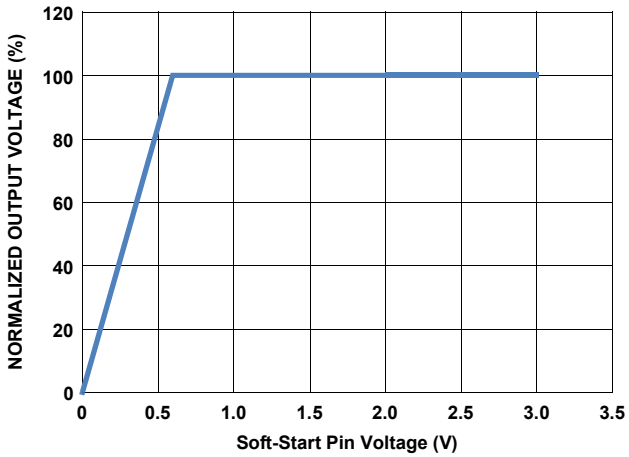


Figure 13. Normalized Output Voltage vs Voltage On Soft-Start Pin

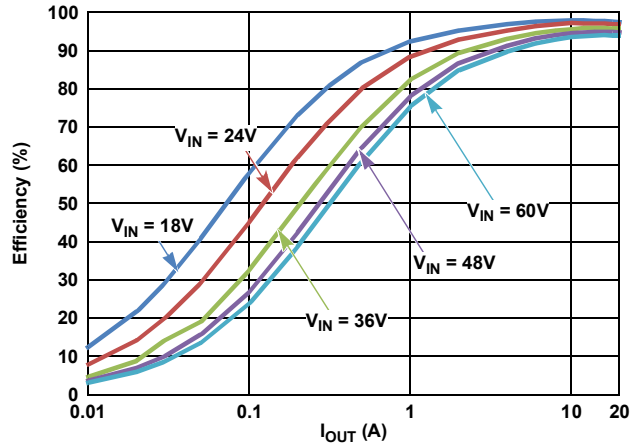


Figure 14. CCM Mode Efficiency

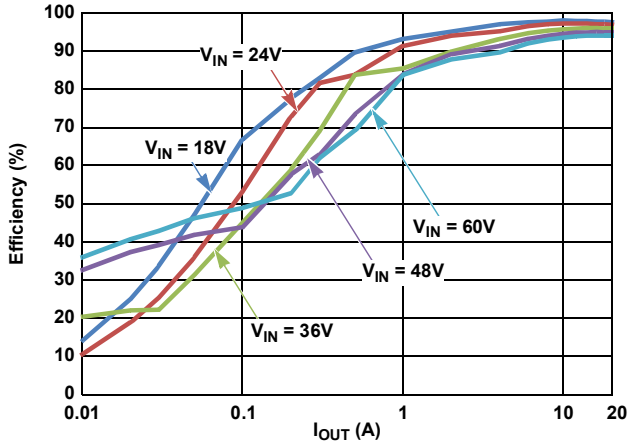


Figure 15. DEM Mode Efficiency

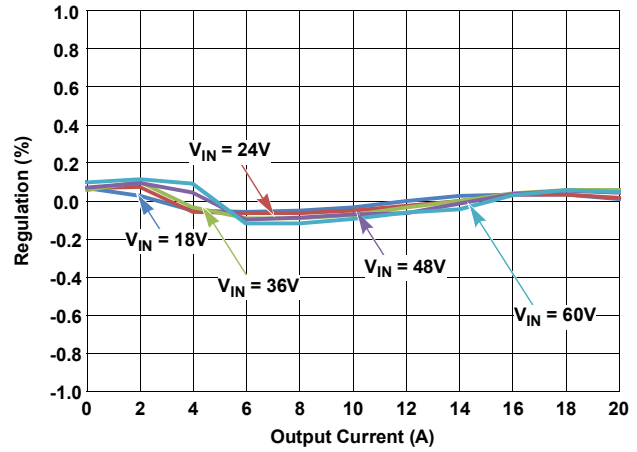


Figure 16. CCM Mode Load Regulation

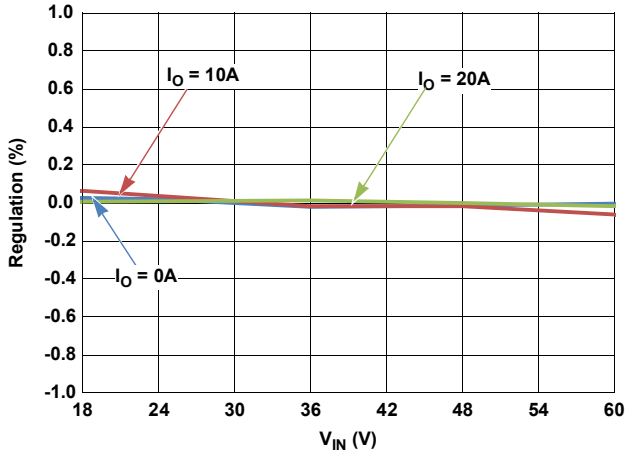


Figure 17. CCM Mode Line Regulation

Oscilloscope plots are taken using the ISL8117EVAL2Z evaluation board, V_{IN} = 18 to 60V, VOUT = 12V, I_{OUT} = 20A, unless otherwise noted. **(Continued)**

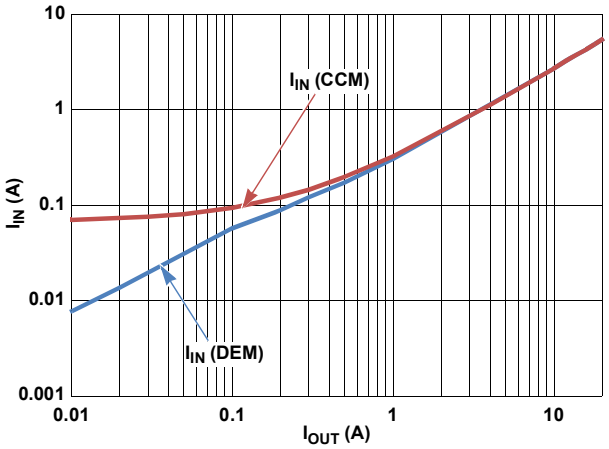


Figure 18. Input Current Comparison With Mode = CCM/DEM, V_{IN} = 48V

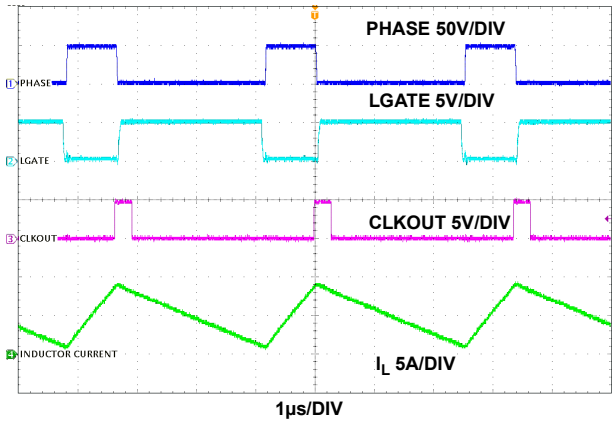


Figure 19. PHASE, LGATE, CLKOUT and Inductor Current Waveforms

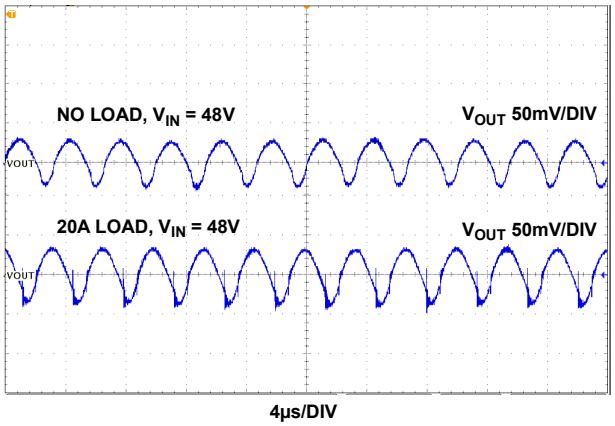


Figure 20. Output Ripple, Mode = CCM

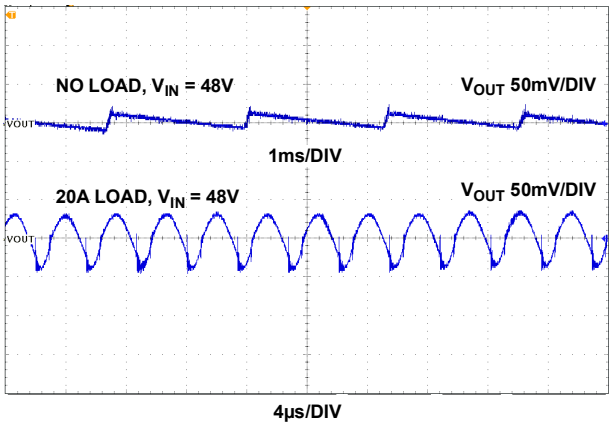


Figure 21. Output Ripple, Mode = DEM

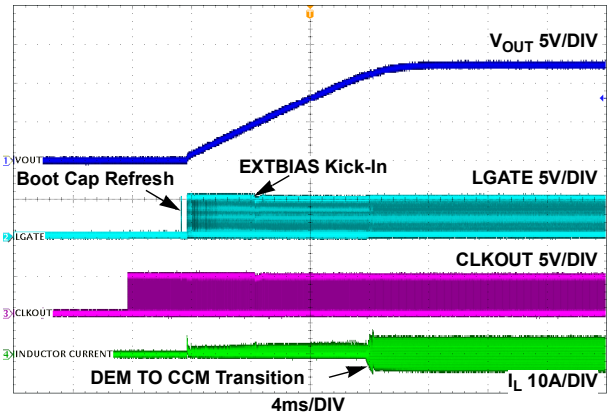


Figure 22. Start-Up Waveforms; Mode = CCM, Load = 0A, V_{IN} = 48V

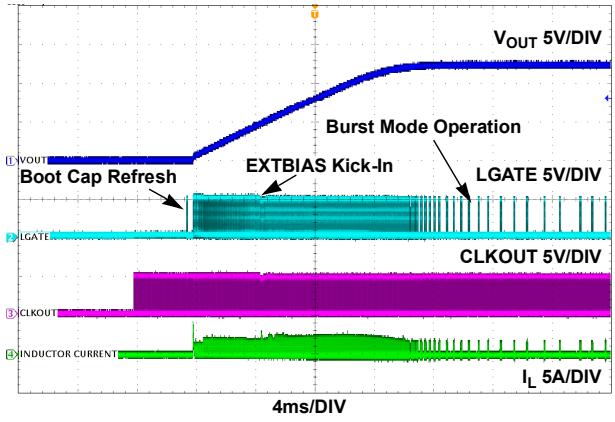


Figure 23. Start-Up Waveforms; Mode = DEM, Load = 0A, V_{IN} = 48V

Oscilloscope plots are taken using the ISL8117EVAL2Z evaluation board, V_{IN} = 18 to 60V, VOUT = 12V, I_{OUT} = 20A, unless otherwise noted. **(Continued)**

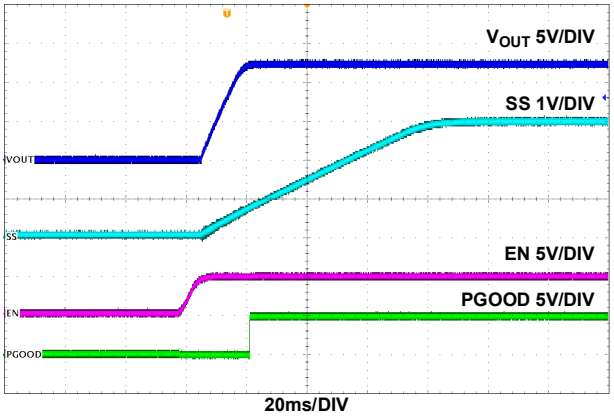


Figure 24. Start-Up Waveforms; Mode = CCM, Load = 0A, V_{IN} = 48V

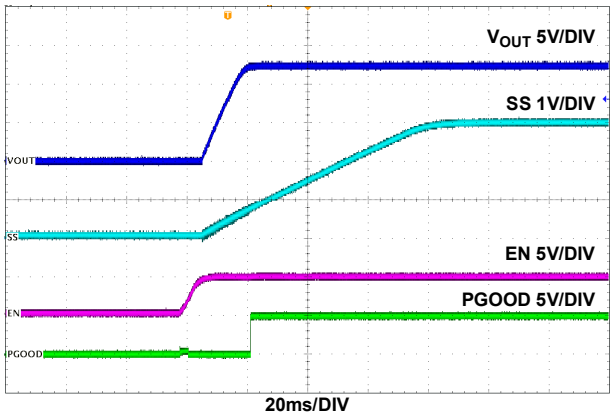


Figure 25. Start-Up Waveforms; Mode = DEM, Load = 0A, V_{IN} = 48V

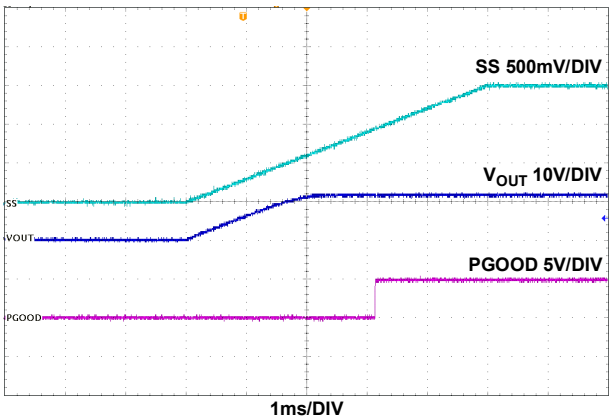


Figure 26. Tracking; V_{IN} = 48V, Load = 0A, Mode = CCM

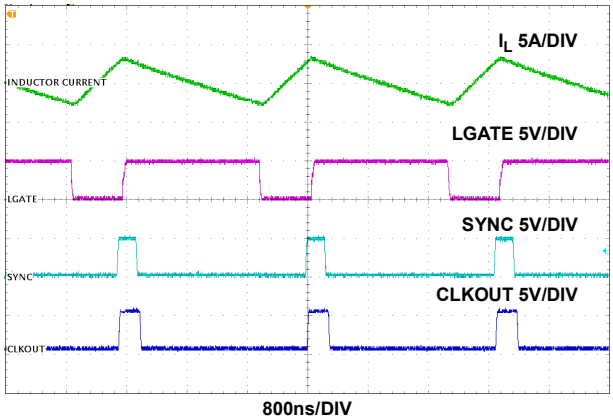


Figure 27. Frequency Synchronization; V_{IN} = 48V, Load = 0A, Default f_{SW} = 300kHz, SYNC f_{SW} = 400kHz

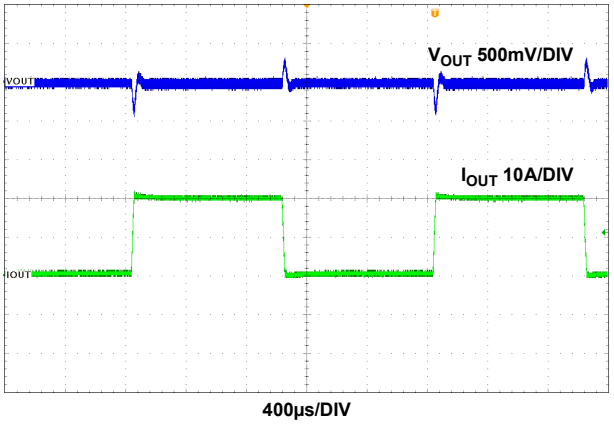


Figure 28. LOAD Transient Response; V_{IN} = 48V, 0A to 20A 1A/µs Step Load, CCM Mode

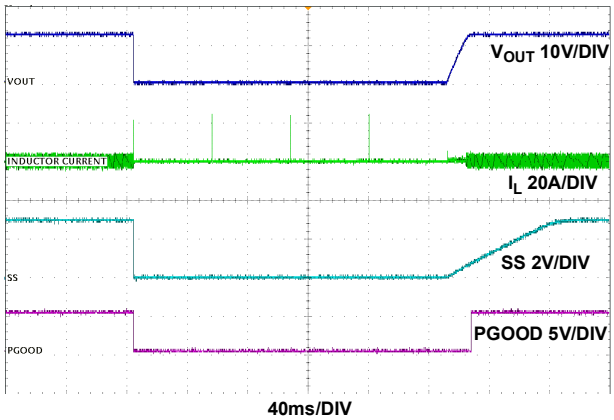


Figure 29. OCP Response, Output Short-Circuited From No Load to Ground and Released, CCM Mode, V_{IN} = 48V

4. Functional Description

4.1 General Description

The ISL8117 integrates control circuits for a synchronous buck converter. The driver and protection circuits are also integrated to simplify the end design.

The part has an independent enable/disable control line EN, which provides a flexible power-up sequencing and a simple VIN UVP implementation. The soft-start time is programmable by adjusting the soft-start capacitor connected from SS/TRK.

The valley current mode control scheme with input voltage feed-forward ramp simplifies loop compensation and provides excellent rejection to input voltage variation.

4.2 Input Voltage Range

The ISL8117 is designed to operate from input supplies ranging from 4.5V to 60V.

The input voltage range can be effectively limited by the available minimum PWM off-time as shown in Equation 2.

(EQ. 2) $$V_{IN(min)} \geq \left(\frac{V_{OUT} + V_{d1}}{1 - t_{OFF(min)} \times Frequency} \right) + V_{d2} - V_{d1}$$

where,
V_{d1} = sum of the parasitic voltage drops in the inductor discharge path, including the lower FET, inductor and PC board.
V_{d2} = sum of the voltage drops in the charging path, including the upper FET, inductor and PC board resistances.
$t_{OFF(min)}$ = 308ns.

The maximum input voltage and minimum output voltage is limited by the minimum on-time ($t_{ON(min)}$) as shown in Equation 3.

(EQ. 3) $$V_{IN(max)} \leq \left(\frac{V_{OUT}}{t_{ON(min)} \times Frequency} \right)$$

where, $t_{ON(min)}$ = 40ns in CCM (continuous conduction mode) and 60ns in DEM (diode emulation mode).

4.3 Internal 5V Linear Regulator (VCC5V) and External VCC Bias Supply (EXTBIAS)

All the ISL8117 functions can be internally powered from an on-chip, low dropout 5V regulator or an external 5V bias voltage through the EXTBIAS pin. Bypass the linear regulator's output (VCC5V) with a 4.7µF capacitor to the power ground. The ISL8117 also employs an undervoltage lockout circuit that disables all regulators when VCC5V falls below 3.5V.

The internal LDO can source over 75mA to supply the IC, power the low-side gate driver, and charge the boot capacitor. When driving large FETs at high switching frequency, little or no regulator current may be available for external loads.

For example, a single large FET with 15nC total gate charge requires 15nC x 300kHz = 4.5mA (15nC x 600kHz = 9mA). Also, at higher input voltages with larger FETs, the power dissipation across the internal 5V increases. Excessive dissipation across this regulator must be avoided to prevent junction temperature rise. Thermal protection may be triggered if die temperature increases above +160°C due to excessive power dissipation.

When large MOSFETs are used, an external 5V bias voltage can be applied to the EXTBIAS pin to alleviate excessive power dissipation. Voltage at the EXTBIAS pin must always be lower than the voltage at the VIN pin to prevent biasing of the power stage through EXTBIAS and VCC5V. An external UVLO circuit might be necessary to ensure smooth soft-starting.

The internal LDO has an overcurrent limit of typically 120mA. For better efficiency, connect VCC5V to VIN for 5V ±10% input applications.

4.4 Enable and Soft-Start Operation

Pulling the EN pin high or low can enable or disable the controller. When the EN pin voltage is higher than 1.6V, the controller is enabled to initialize its internal circuit. After the VCC5V pin reaches the UVLO threshold, ISL8117 soft-start circuitry becomes active. The internal 2µA charge current begins charging up the soft-start capacitor connected from the SS/TRK pin to GND. The voltage error amplifier reference voltage is clamped to the voltage on the SS/TRK pin. The output voltage therefore rises from 0V to regulation as SS/TRK rises from 0V to 0.6V. Charging of the soft-start capacitor continues until the voltage on the SS/TRK pin reaches 3V.

Typical applications for the ISL8117 use programmable analog soft-start or the SS/TRK pin for tracking. The soft-start time can be set by the value of the soft-start capacitor connected from the SS/TRK the to GND. Inrush current during start-up can be alleviated by adjusting the soft-starting time.

The typical soft-start time is set according to Equation 4:

$$t_{SS} = 0.6V\left(\frac{C_{SS}}{2\mu A}\right) \quad \text{(EQ. 4)}$$

When the soft-starting time set by external C_{SS} or tracking is less than 1.5ms, an internal soft-start circuit of 1.5ms takes over the soft-start.

PGOOD toggles to high when the corresponding output is up and in regulation.

Pulling the EN pin low disables the PWM output and internal LDO to achieve low standby current. The SS/TRK pin also discharges to GND by an internal MOSFET with 70Ω $r_{DS(ON)}$.

4.5 Output Voltage Programming

The ISL8117 provides a precision 0.6V internal reference voltage to set the output voltage. Based on this internal reference, the output voltage can be set from 0.6V up to a level determined by the input voltage, the maximum duty cycle, and the conversion efficiency of the circuit.

A resistive divider from the output to ground sets the output voltage. Connect the center point of the divider to the FB pin. The output voltage value is determined by Equation 5.

$$V_{OUT} = 0.6V\left(\frac{R_1 + R_2}{R_2}\right) \quad \text{(EQ. 5)}$$

where R_1 is the top resistor of the feedback divider network and R_2 is the bottom resistor connected from FB to ground.

4.6 Tracking Operation

The ISL8117 can be set up to track an external supply. To implement tracking, a resistive divider is connected between the external supply output and ground. The center point of the divider shall be connected to the SS/TRK pin of the ISL8117. The resistive divider ratio sets the ramping ratio between the two voltage rails. To implement coincident tracking, set the tracking resistive divider ratio exactly the same as the ISL8117 output resistive divider given by Equation 5. Make sure that the voltage at SS/TRK is greater than 0.6V when the master rail reaches regulation.

To minimize the impact of the 2µA soft-start current on the tracking function, Renesas recommends using resistors of less than 10kΩ for the tracking resistive divider.

When overcurrent protection (OCP) is triggered, the internal minimum soft-start circuit determines the OCP soft-start hiccup.

4.7 Light-Load Efficiency Enhancement

When MOD/SYNC is tied to VCC5V, the ISL8117 operates in high efficiency Diode Emulation mode and Pulse Skipping mode in light-load condition. The inductor current is not allowed to reverse (discontinuous operation). At very light-loads, the converter goes into diode emulation and triggers the pulse skipping function. In Pulse Skipping mode, the upper MOSFET remains off until the output voltage drops to the point the error amplifier output goes above the pulse skipping mode threshold. The minimum t_{ON} in the pulse skipping mode is 60ns.

4.8 Prebiased Power-Up

The ISL8117 has the ability to soft-start with a prebiased output. The output voltage is not pulled down during prebiased start-up. The PWM is not active until the soft-start ramp reaches the output voltage times the resistive divider ratio.

Overvoltage protection is active during soft-start.

4.9 Frequency Selection

Switching frequency selection is a trade-off between efficiency and component size. Low switching frequency improves efficiency by reducing MOSFET switching loss. To meet the output ripple and load transient requirements, operation at a low switching frequency requires larger inductance and output capacitance. The switching frequency of the ISL8117 is set by a resistor connected from the RT pin to GND according to Equation 1.

The frequency setting curve shown in Figure 30 assists in selecting the correct value for R_T.

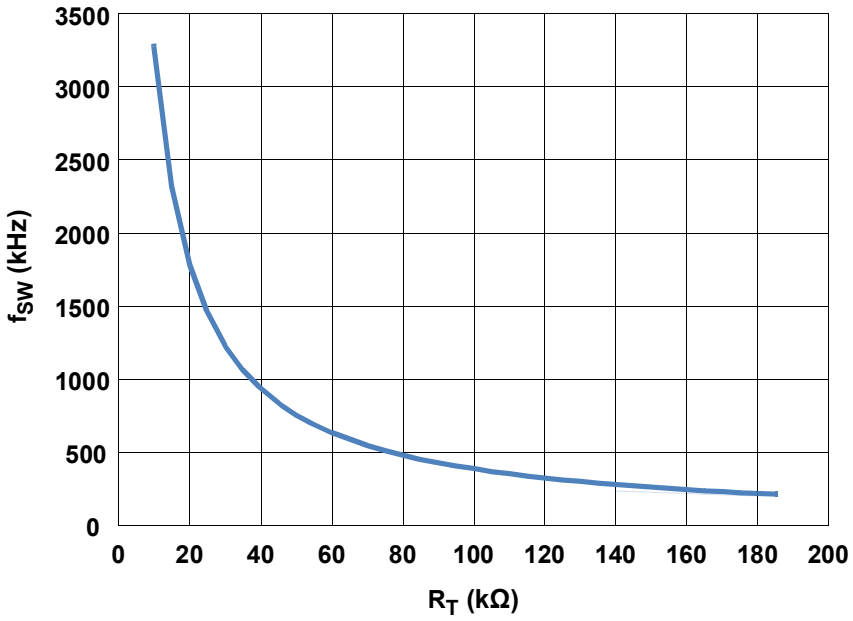


Figure 30. R_T vs Switching Frequency f_{SW}

4.10 Frequency Synchronization

The MOD/SYNC pin can be used to synchronize the ISL8117 to an external clock or the CLKOUT pin of another ISL8117. When the MOD/SYNC pin is connected to the CLKOUT pin of another ISL8117, the two controllers operate in synchronization.

When the MOD/SYNC pin is connected to an external clock, the ISL8117 synchronizes to the external clock frequency. For proper operation, the frequency set by resistor R_T should be lower than the external clock frequency.

When frequency synchronization is in action, the controllers enter forced continuous current mode at light-load.

The CLKOUT pin outputs a clock signal with a 280ns pulse width. The signal frequency is the same as the frequency set by the resistor from RT pin to ground. The signal rising edge is in line with the PWM falling edge.

4.11 Gate Control Logic

The gate control logic translates the PWM signal into gate drive signals providing amplification, level shifting, and shoot-through protection. The gate driver has circuitry that helps optimize the IC performance over a wide range of operational conditions. MOSFET switching times can vary dramatically from type to type and with input voltage, the gate control logic provides adaptive dead time by monitoring real gate waveforms of both the upper and the lower MOSFETs. Shoot-through control logic provides a 16ns dead time to ensure that both the upper and lower MOSFETs do not turn on simultaneously and cause a shoot-through condition.

4.12 Gate Driver

The low-side gate driver is supplied from VCC5V and provides a 2A peak sink and source current. The high-side gate driver is capable of delivering the same currents as the low-side gate driver. Gate-drive voltage for the upper N-channel MOSFET is generated by a flying capacitor boot circuit. A boot capacitor connected from the BOOT pin to the PHASE node provides power to the high-side MOSFET driver. To limit the peak current in the IC, an external resistor can be placed between the BOOT pin and the boot capacitor. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

At start-up, the low-side MOSFET turns on first and forces PHASE to ground in order to charge the BOOT capacitor to 5V. After the low-side MOSFET turns off, the high-side MOSFET is turned on by closing an internal switch between BOOT and UGATE. The closing of the internal switch provides the necessary gate-to-source voltage to turn on the upper MOSFET, an action that boosts the 5V gate drive signal above V_{IN}. The current required to drive the upper MOSFET is drawn from the internal 5V regulator.

For optimal EMI performance or reducing phase node ringing, a small resistor can be placed between the BOOT pin to the positive terminal of the bootstrap capacitor.

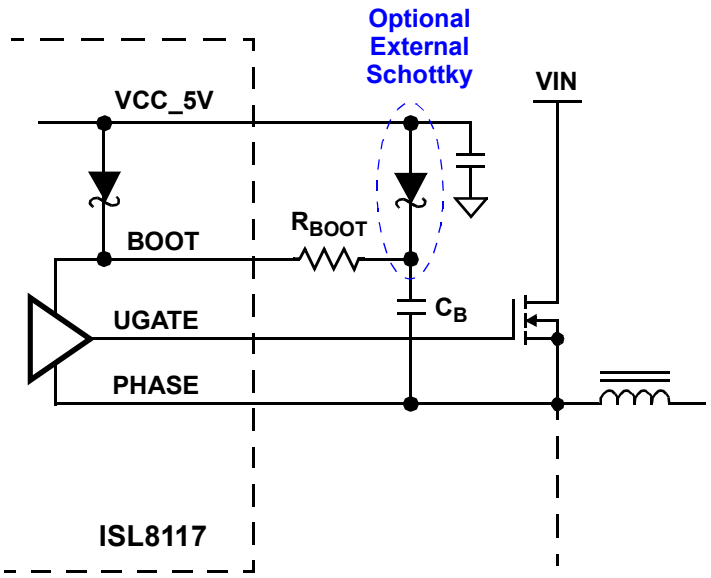


Figure 31. Upper Gate Driver Circuit

4.13 Adaptive Dead Time

The ISL8117 incorporates an adaptive dead time algorithm on the synchronous buck PWM controller that optimizes operation with varying MOSFET conditions. This algorithm provides approximately 16ns dead time between the switching of the upper and lower MOSFETs. This dead time is adaptive and allows operation with different MOSFETs without having to externally adjust the dead time using a resistor or capacitor. During turn-off of the lower MOSFET, the LGATE voltage is monitored until it reaches a threshold of 1V, at which time the UGATE is released to rise. Adaptive dead time circuitry monitors the upper MOSFET gate voltage during UGATE turn-off. Once the upper MOSFET gate-to-source voltage has dropped below a threshold of 1V, the LGATE is allowed to rise. It is recommended to not use a resistor between UGATE and LGATE and the respective MOSFET gates as it may interfere with the dead time circuitry.

4.14 Internal Bootstrap Diode

The ISL8117 has an integrated bootstrap diode to help reduce total cost and reduces layout complexity. Add an external capacitor across the BOOT and PHASE pins to complete the bootstrap circuit. The bootstrap capacitor can be chosen from Equation 6.

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{BOOT}} \quad \text{(EQ. 6)}$$

where Q_{GATE} is the amount of gate charge required to fully charge the gate of the upper MOSFET. ΔV_{BOOT} is defined as the allowable droop in the rail of the upper drive.

As an example, suppose an upper MOSFET has a gate charge (Q_{GATE}) of 25nC at 5V and assume the droop in the drive voltage over a PWM cycle is 200mV. Based on the calculation, a bootstrap capacitance of at least 0.125µF is required. The next larger standard value capacitance of 0.22µF should be used. A good quality ceramic capacitor is recommended.

The internal bootstrap Schottky diode has a resistance of 1.5Ω (typical) at 800mA. Combined with the resistance R_{BOOT}, this could lead to the boot capacitor charging insufficiently in cases where the bottom MOSFET is turned on for a very short period of time. If such circumstances are expected, an additional external Schottky diode can be added from VCC5V to the positive of the boot capacitor. R_{BOOT} may still be necessary to lower EMI due to fast turn-on of the upper MOSFET.

4.15 Power-Good Indicator

The power-good pin can be used to monitor the status of the output voltage. PGOOD is true (open drain) 1.1ms after the FB pin is within ±11% of the reference voltage.

There is no extra delay when the PGOOD pin is pulled LOW.

5. Protection Circuits

The converter output is monitored and protected against overload, light-load, and undervoltage conditions.

5.1 Undervoltage Lockout

The ISL8117 includes UVLO protection, which keeps the device in a reset condition until a proper operating voltage is applied. It also shuts down the ISL8117 if the operating voltage drops below a predefined value. The controller is disabled when UVLO is asserted. When UVLO is asserted, PGOOD is valid and is deasserted.

5.2 Overcurrent Protection

The controller uses the ON-resistance, $r_{DS(ON)}$, of the low-side MOSFET to monitor the inductor current in the low-side MOSFET On period. The sensed lowside MOSFET $r_{DS(ON)}$ voltage drop is instantly proportional to the inductor down ramp current. Theoretically, the inductor peak current can be sensed at the low-side MOSFET turn-on moment. In reality, due to the internal sense circuit delay, the maximum sensed inductor current is slightly lower than the peak current.

The sensed low-side MOSFET $r_{DS(ON)}$ voltage drop is compared with a threshold set by a resistor R_{OCSET} connected from the LGATE/OCS pin to ground during the initiation stage before soft-start. During the initiation stage, a typical 10.5µA current source $I_{OCSET-CS}$ from the LGATE/OCS pin creates a voltage drop on R_{OCSET}. The voltage drop is then read and stored as the OCP comparator reference. R_{OCSET} can be calculated by Equation 7.

$$R_{OCSET} = \frac{(r_{DS(ON)})(I_{OC})}{0.7 + 3.5R_{CS}} \quad \text{(EQ. 7)}$$

where I_{OC} is the required overcurrent protection threshold which should be sufficiently higher than the maximum output load current. As the current is sensed between peak and valley of the inductor current, the ripple current should be included while calculating maximum output current. Half of the inductor ripple current is the worst case scenario.

R_{CS} is the value of the current sense resistor connected to the ISEN pin. The unit for $r_{DS(ON)}$ is mΩ, R_{CS} is kΩ, and I_{OC} is A.

Because $I_{OCSET-CS}$ varies from minimum 9µA to maximum 11.5µA, with the calculated R_{OCSET} by Equation 7, the actual I_{OC} varies from -14.3% to +9.5%.

If an overcurrent is detected, the upper MOSFET remains off and the lower MOSFET remains on until the next cycle. As a result, the converter skips a pulse. When the overload condition is removed, the converter resumes normal operation.

If an overcurrent is detected for two consecutive clock cycles, the IC enters in a Hiccup mode by turning off the gate driver and entering soft-start. The IC stays off for 50ms before trying to restart. The IC continues to cycle through soft-start until the overcurrent condition is removed. Hiccup mode is active during soft-start, so care must be taken to ensure that the peak inductor current does not exceed the overcurrent threshold during soft-start.

Because of the nature of this current sensing technique, and to accommodate a wide range of $r_{DS(ON)}$ variations, the value of the overcurrent threshold should represent an overload current about 180% of the maximum operating current, assuming approximately 40% variation in MOSFET $r_{DS(ON)}$. If more accurate current protection is needed, place a current sense resistor in series with the lower MOSFET source.

When OCP is triggered, the SS/TRK pin is pulled to ground by an internal MOSFET for hiccup restart. When configured to track another voltage rail, the SS/TRK pin rises up much faster than the internal minimum soft-start ramp. The voltage reference then clamps to the internal minimum soft-start ramp. Therefore, smooth soft-start hiccup is achieved even with the tracking function.

For applications with large inductor ripple current, it is recommended to use a larger R_{CS} to reduce the current ripple into the ISEN pin to less than 6µA which is the OCP comparator hysteresis. Otherwise, when the load current approaches to the OCP trip point, the OCP comparator can trip and reset in one switching cycle. The overcurrent condition cannot last for two consecutive cycles to force the IC into Hiccup mode. Instead, the IC runs in a half frequency PWM mode leading to a larger output ripple.

5.3 Overvoltage Protection

The overvoltage set point is set at 121% of the nominal output voltage set by the feedback resistors. In the case of an overvoltage event, the IC attempts to bring the output voltage back into regulation by keeping the upper MOSFET turned off and the lower MOSFET turned on. If the overvoltage condition has been corrected and the output voltage returns to 110% of the nominal output voltage, both upper and lower MOSFETs turn off until the output voltage drops to the nominal voltage to start work in normal PWM switching.

For lower control loop bandwidth applications, such as very low output voltage or very low switching frequency designs, the full load to no load transient response may be slow to cause an OVP false trigger. When OVP is triggered, the long LGATE on-time creates a high negative inductor current leading to a higher than normal sink in current to the ISEN pin. It is recommended to limit the ISEN pin sink in current to less than 16µA. Otherwise, a false OCP hiccup operation may be triggered to cause the output to shut down.

5.4 Over-Temperature Protection

The IC incorporates an over-temperature protection circuit that shuts the IC down when a die temperature of +160°C is reached. Normal operation resumes when the die temperature drops below +145°C through the initiation of a full soft-start cycle. During OTP shutdown, the IC consumes only 100µA of current. When the controller is disabled, thermal protection is inactive, which helps achieve a very low shutdown current of 5µA.

6. Feedback Loop Compensation

To reduce the number of external components and to simplify the process of determining compensation components, the controller is designed with an internally compensated error amplifier. To make internal compensation possible, several design measures were taken.

First, the ramp signal applied to the PWM comparator is proportional to the input voltage provided at the VIN pin, which keeps the modulator gain constant with varying input voltages. Next, the load current proportional signal is derived from the voltage drop across the lower MOSFET during the $\overline{PWM}$ time interval, and it is subtracted from the amplified error signal on the comparator input, which creates an internal current control loop. The resistor R_{CS} connected to the ISEN pin sets the gain in the current feedback loop. The following expression estimates the required value of the current sense resistor depending on the maximum operating load current and the value of the MOSFET $r_{DS(ON)}$ as shown in Equation 8.

$$R_{CS} \geq \frac{(I_{MAX})(r_{DS(ON)})}{30\mu A} \quad \text{(EQ. 8)}$$

Choosing R_{CS} to provide 30µA of current to the current sample and hold circuitry is recommended but values down to 2µA and up to 100µA can be used.

Due to the current loop feedback, the modulator has a single pole response with -20dB slope at a frequency determined by the load by using Equation 9.

$$F_{PO} = \frac{1}{2\pi \cdot R_O \cdot C_O} \quad \text{(EQ. 9)}$$

where R_O is load resistance and C_O is load capacitance. For this type of modulator, a Type 2 compensation circuit is usually sufficient.

Figure 32 shows a Type 2 amplifier and its response, along with the responses of the current mode modulator and the converter. The Type 2 amplifier, in addition to the pole at origin, has a zero-pole pair that causes a flat gain region at frequencies between the zero and the pole.

$$F_Z = \frac{1}{2\pi \cdot R_2 \cdot C_1} = 10kHz \quad \text{(EQ. 10)}$$

$$F_P = \frac{1}{2\pi \cdot R_2 \cdot C_2} = 600kHz \quad \text{(EQ. 11)}$$

High amplifier zero frequency gain and modulator gain are chosen to satisfy most typical applications. The crossover frequency appears at the point where the modulator attenuation equals the amplifier high frequency gain. The only task that the system designer has to complete is to specify the output filter capacitors to position the load main pole somewhere within one decade lower than the amplifier zero frequency. With this type of compensation, plenty of phase margin is easily achieved due to zero-pole pair phase ‘boost’.

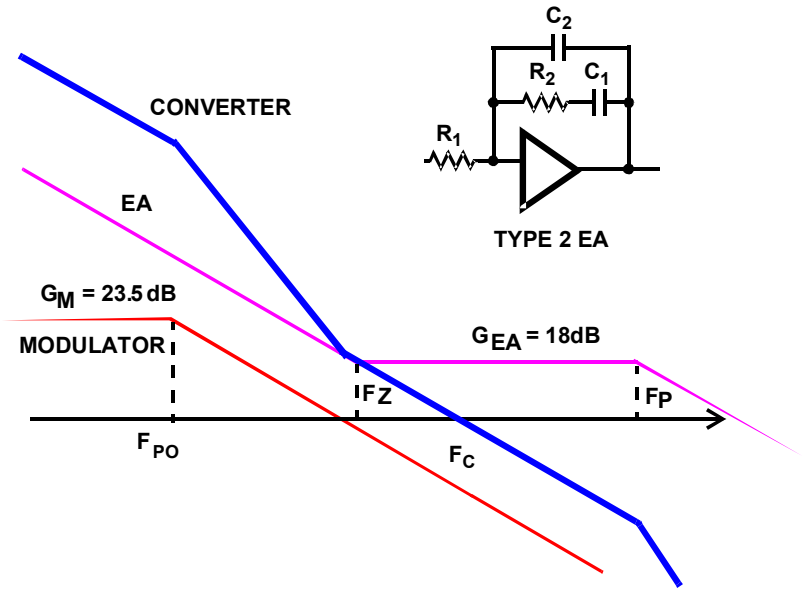


Figure 32. Feedback Loop Compensation

Conditional stability may occur only when the main load pole is positioned to the extreme left side on the frequency axis due to excessive output filter capacitance. In this case, the ESR zero placed within the 1.2kHz to 30kHz range gives some additional phase ‘boost’. Some phase boost can also be achieved by connecting capacitor C_3 in parallel with the upper resistor R_1 of the divider that sets the output voltage value. See Output Voltage Programming.

7. Layout Guidelines

Careful attention to layout requirements is necessary for successful implementation of an ISL8117 based DC/DC converter. The ISL8117 switches at a very high frequency and therefore the switching times are very short. At these switching frequencies, even the shortest trace has significant impedance. Also, the peak gate drive current rises significantly in an extremely short time. Transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, and increase device overvoltage stress and ringing. Careful component selection and proper PCB layout minimizes the magnitude of these voltage spikes.

There are three sets of critical components in a DC/DC converter using the ISL8117:

- Controller
- Switching power components
- Small signal components

The switching power components are the most critical from a layout point of view because they switch a large amount of energy, which tends to generate a large amount of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bias currents. A multilayer PCB is recommended.

7.1 Layout Considerations

1. The input capacitors, upper FET, lower FET, inductor, and output capacitor should be placed first. Isolate these power components on dedicated areas of the board with their ground terminals adjacent to one another. Place the input high frequency decoupling ceramic capacitors very close to the MOSFETs.
2. If signal components and the IC are placed in a separate area to the power train, it is recommended to use full ground planes in the internal layers with shared SGND and PGND to simplify the layout design. Otherwise, use separate ground planes for the power ground and small signal ground. Connect the SGND and PGND together close to the IC. DO NOT connect them together anywhere else.
3. The loop formed by the input capacitor, the top FET, and the bottom FET must be kept as small as possible.
4. Ensure the current paths from the input capacitor to the MOSFET, to the output inductor and the output capacitor are as short as possible with maximum allowable trace widths.
5. Place the PWM controller IC close to the lower FET. The LGATE connection should be short and wide. Place the IC over a quiet ground area. Avoid switching ground loop currents in this area.
6. Place the VCC5V bypass capacitor very close to the VCC5V pin of the IC and connect its ground to the PGND plane.
7. Place the gate drive components - optional BOOT diode and BOOT capacitors - together near the controller IC.
8. The output capacitors should be placed as close to the load as possible. Use short wide copper regions to connect output capacitors to load to avoid inductance and resistance.
9. Use copper filled polygons or wide short traces to connect the junction of upper FET, lower FET, and output inductor. Also keep the PHASE node connection to the IC short. DO NOT unnecessarily oversize the copper islands for the PHASE node. Because the phase nodes are subjected to very high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry tends to couple switching noise.
10. Route all high speed switching nodes away from the control circuitry.
11. Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. All small signal grounding paths including feedback resistors, current limit setting resistor, soft-starting capacitor, and EN pull-down resistor should be connected to this SGND plane.
12. Separate the current sensing trace from the PHASE node connection.
13. Ensure the feedback connection to the output capacitor is short and direct.

7.2 General PowerPAD Design Considerations

The following is an example of how to use vias to remove heat from the IC.

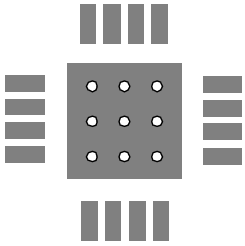


Figure 33. PCB Via Pattern

It is recommended to fill the thermal pad area with vias. A typical via array fills the thermal pad footprint such that their centers are 3x the radius apart from each other. Keep the vias small but not so small that their inside diameter prevents solder wicking through during reflow.

Connect all vias to the ground plane. It is important the vias have a low thermal resistance for efficient heat transfer. It is important to have a complete connection of the plated through-hole to each plane.

8. Component Selection Guideline

8.1 MOSFET Considerations

The logic level MOSFETs are chosen for optimum efficiency given the potentially wide input voltage range and output power requirement. Two N-channel MOSFETs are used in the synchronous-rectified buck converters. These MOSFETs should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management considerations.

Power dissipation includes two loss components: conduction loss and switching loss. These losses are distributed between the upper and lower MOSFETs according to duty cycle (see Equations 12 and 13). The conduction losses are the main component of power dissipation for the lower MOSFET. Only the upper MOSFET has significant switching losses, because the lower device turns on and off into near zero voltage. The equations assume linear voltage current transitions and do not model power loss due to the reverse recovery of the lower MOSFET's body diode.

(EQ. 12) $$P_{UPPER} = \frac{(I_O^2)(r_{DS(ON)})(V_{OUT})}{V_{IN}} + \frac{(I_O)(V_{IN})(t_{SW})(f_{SW})}{2}$$

(EQ. 13) $$P_{LOWER} = \frac{(I_O^2)(r_{DS(ON)})(V_{IN} - V_{OUT})}{V_{IN}}$$

A large gate-charge increases the switching time, t_{SW}, which increases the upper MOSFET's switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications.

8.2 Output Inductor Selection

The PWM converter requires an output inductor. The output inductor is selected to meet the output voltage ripple requirements. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current and the output capacitor(s) ESR. The ripple voltage expression is given in the capacitor selection section and the ripple current is approximated by Equation 14:

(EQ. 14) $$\Delta I_L = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_{SW})(L)(V_{IN})}$$

The ripple current ratio is usually from 30% to 70% of the full output load.

8.3 Output Capacitor Selection

The output capacitors for each output have unique requirements. In general, the output capacitors should be selected to meet the dynamic regulation requirements including ripple voltage and load transients. Selection of output capacitors is also dependent on the output inductor, so some inductor analysis is required to select the output capacitors.

One of the parameters limiting the converter's response to a load transient is the time required for the inductor current to slew to its new level. The ISL8117 provides either 0% or maximum duty cycle in response to a load transient.

The response time is the time interval required to slew the inductor current from an initial current value to the load current level. During this interval, the difference between the inductor current and the transient current level must be supplied by the output capacitor(s). Minimizing the response time can minimize the output capacitance required. Also, if the load transient rise time is slower than the inductor response time, as in a hard drive or CD drive, it reduces the requirement on the output capacitor.

The minimum capacitor value required to provide the full, rising step, transient load current during the response time of the inductor is shown in Equation 15:

$$C_{OUT} = \frac{(L_O)(I_{TRAN})^2}{2(V_{IN} - V_O)(DV_{OUT})} \quad \text{(EQ. 15)}$$

where C_{OUT} is the output capacitor(s) required, L_O is the output inductor, I_{TRAN} is the transient load current step, V_{IN} is the input voltage, V_O is output voltage, and DV_{OUT} is the drop in output voltage allowed during the load transient.

High frequency capacitors initially supply the transient current and slow the load rate of change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the Equivalent Series Resistance (ESR) and voltage rating requirements as well as actual capacitance requirements.

The output voltage ripple is due to the inductor ripple current and the ESR of the output capacitors as defined by Equation 16:

$$V_{RIPPLE} = \Delta I_L(ESR) \quad \text{(EQ. 16)}$$

where ΔI_L is calculated in Equation 14.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load circuitry for specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching regulator applications for the bulk capacitors. In most cases, multiple small case electrolytic capacitors perform better than a single large case capacitor.

The stability requirement on the selection of the output capacitor is that the ‘ESR zero’ (f_Z) is between 2kHz and 60kHz. This range is set by an internal, single compensation zero at 8.8kHz. The ESR zero can be a factor of five on either side of the internal zero and still contribute to increased phase margin of the control loop.

This requirement is shown in Equation 17:

$$C_{OUT} = \frac{1}{2\pi(ESR)(f_Z)} \quad \text{(EQ. 17)}$$

In conclusion, the output capacitors must meet the following criteria:

- They must have sufficient bulk capacitance to sustain the output voltage during a load transient while the output inductor current is slewing to the value of the load transient.
- The ESR must be sufficiently low to meet the desired output voltage ripple due to the output inductor current.
- The ESR zero should be placed in a rather large range, to provide additional phase margin.

The recommended output capacitor value for the ISL8117 is between 100µF to 680µF, to meet the stability criteria with external compensation. Use of aluminum electrolytic (POSCAP) or tantalum type capacitors is recommended. Use of low ESR ceramic capacitors is possible with loop analysis to ensure stability.

8.4 Input Capacitor Selection

The important parameters for the input capacitor(s) are the voltage rating and the RMS current rating. For reliable operation, select input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and 1.5 times is a conservative guideline. The AC RMS input current varies with the load given in Equation 18:

(EQ. 18) $$I_{RMS} = \sqrt{DC - DC^2} \cdot I_O$$

where DC is duty cycle of the PWM.

The maximum RMS current supplied by the input capacitance occurs at V_{IN} = 2 X V_{OUT}, DC = 50% as shown in Equation 19:

(EQ. 19) $$I_{RMS} = \frac{1}{2} \times I_O$$

Use a mix of input bypass capacitors to control the voltage ripple across the MOSFETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the MOSFETs to suppress the voltage induced in the parasitic circuit impedances.

Solid tantalum capacitors can be used, but use caution with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge current at power-up.

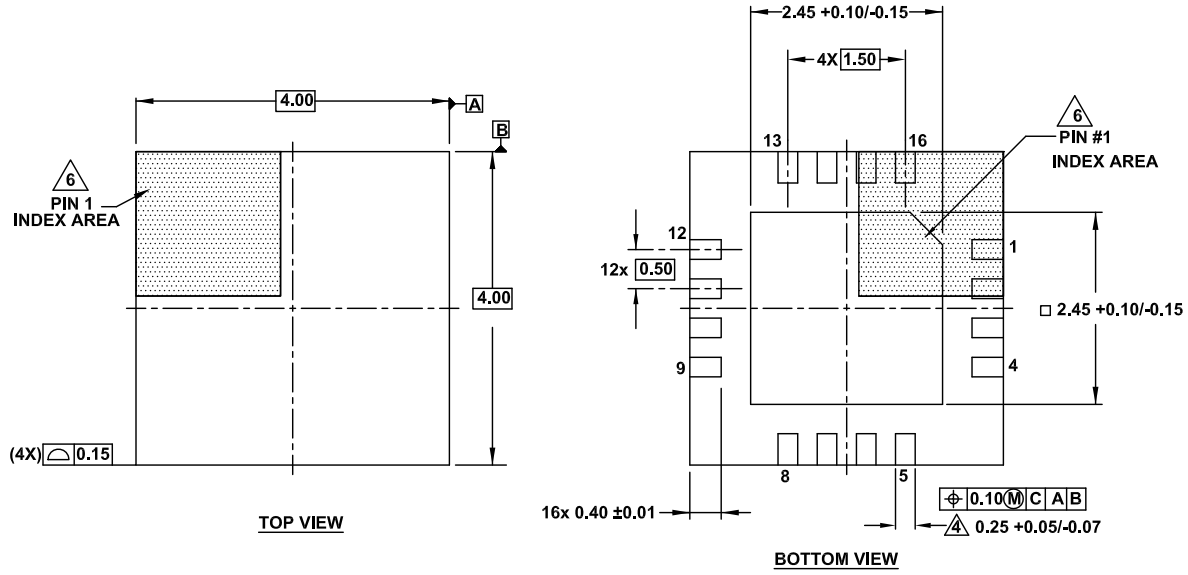
9. Revision History

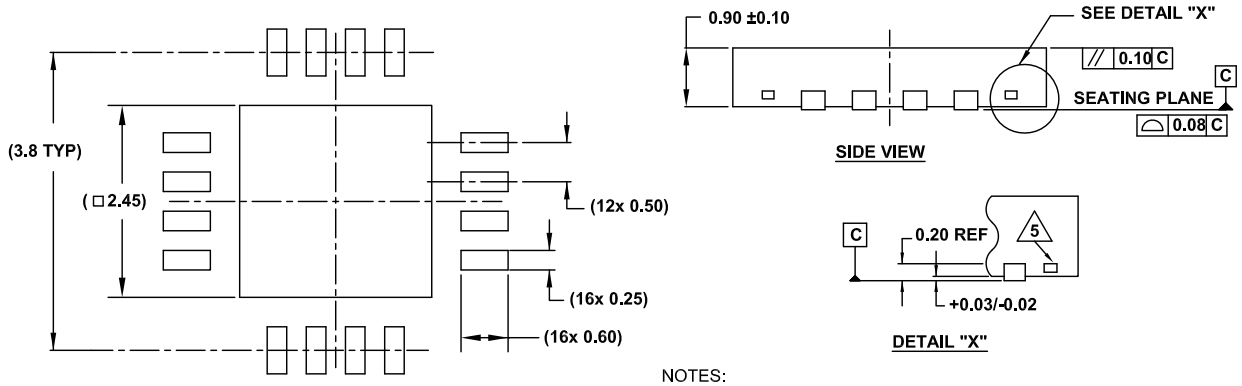
Date	Revision	Change
Feb.23.24	FN8666.7	Updated ESD Ratings in section 2.1. Removed Related Literature.
Oct.23.20	FN8666.6	Updated Figure 3 Block Diagram, Figures 4 and 5 eval board schematics Abs Max Ratings, BOOT/UGATE to PHASE - change Max +0.3 to VCC5V + 0.3V Overcurrent Protection section updated. Updated Disclaimer
Jun.11.19	FN8666.5	Formatting updated. Table, Key Differences Between Family of Parts, added on page 6.
Apr.19.18	FN8666.4	Updated Related Literature on page 1. Ordering Information table on page 3: Added Tape and Reel parts and Tape and Reel column. Updated Note 1. Added ISL8117DEMO3Z and ISL8117DEMO4Z. Page 19: Output Capacitor Selection section, fourth paragraph, first sentence: Changed “The maximum capacitor value. . .” to: “The minimum capacitor value. . .” Removed About Intersil section. Updated Disclaimer. Updated POD L16.4x4A from rev 3 to rev 4, changes since rev 3: Updated bottom view: 2.40 to 2.45 +0.10/-0.152.45 (2 dimensions) Updated typical recommend land pattern: 2.40 to 2.45
Jun.4.15	FN8666.3	Description, page 1 - changed "with 13 external components" to "with 10 external components". On page 6, EN pin description - changed "When the voltage on the pin reaches 1.3V, the output becomes active" to "When the voltage on the pin reaches 1.6V, the output becomes active". On page 18, right column, changed "Thermal protection may be triggered if die temperature increases above +150°C due to excessive power dissipation" to "Thermal protection may be triggered if die temperature increases above +160°C due to excessive power dissipation". On page 18, right column, changed "When the EN pin voltage is higher than 1.3V, the controller is enabled to initialize its internal circuit" to "When the EN pin voltage is higher than 1.6V, the controller is enabled to initialize its internal circuit".
May.12.15	FN8666.2	Replaced Figures 1, 6, and 7. Updated the MOD/SYNC Pin description on page 6.
May.6.15	FN8666.1	Added HTSSOP package/part information throughout datasheet. On page 10, updated “IVINOP” parameter Typical value from “3mA” to “2.5mA”. Added 2nd Paragraph to “Overvoltage Protection” section on page 23.
Apr.10.15	FN8666.0	Initial Release

10. Package Outline Drawings

For the most recent package outline drawing, see L16.4x4A.

L16.4x4A
16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 7/17



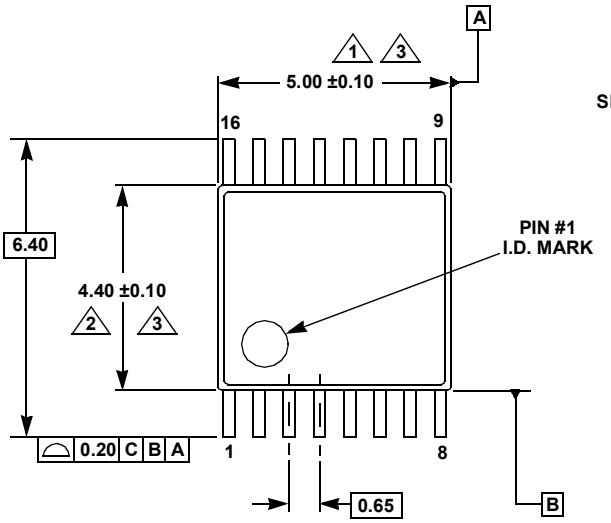


NOTES:

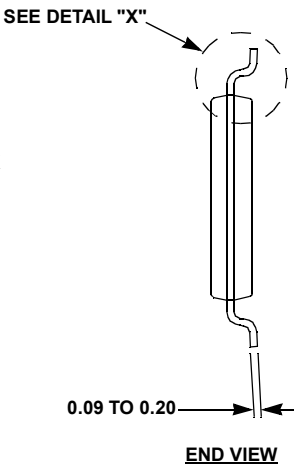
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ±0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

M16.173A
16 LEAD HEATSINK THIN SHRINK SMALL OUTLINE PACKAGE (HTSSOP)
Rev 1, 2/15

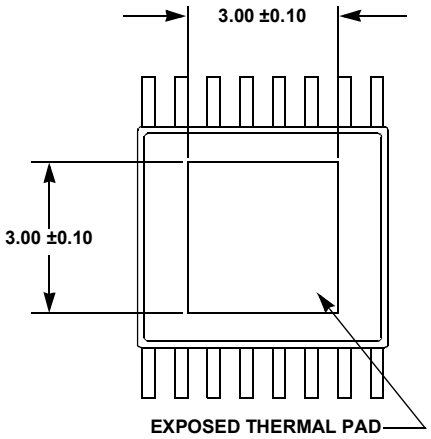
For the most recent package outline drawing, see M16.173A.



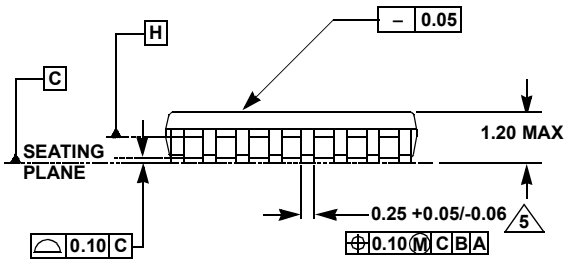
TOP VIEW



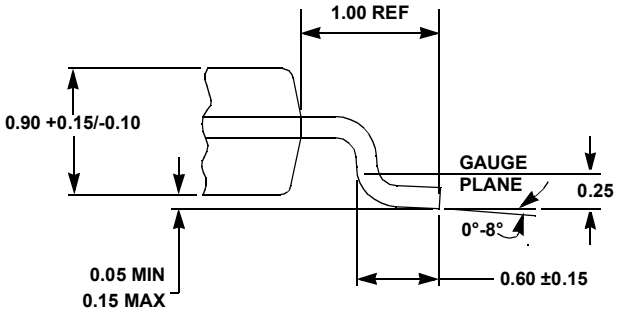
END VIEW



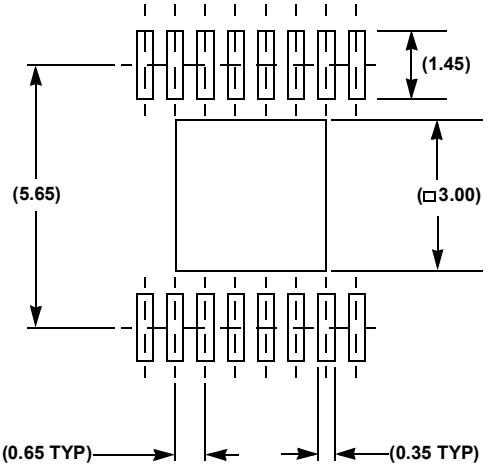
BOTTOM VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

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