THE DATASHEET OF

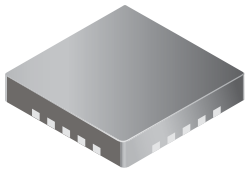
APEK4490EES-01-T-DK

Triple Output Step-Down Switching Regulator

Features and Benefits

- Three buck converters
- 4.5 to 34 V input voltage range
- 550 kHz fixed frequency
- Multiphase switching
- Independent control of each converter
- Power-on-reset flag
- Internal compensation
- 4 × 4 mm QFN Package, small PCB footprint

Package: 20-contact QFN (suffix ES)



Approximate size

Description

Designed to provide the power supply requirements of printers, office automation, industrial, and portable equipment, the A4490 provides three high current, high performance, switching regulator outputs with independent soft start.

High frequency switching allows selection of inexpensive inductors and small ceramic output capacitors. The turn-on cycles of the regulators are interleaved to minimize stresses on the input capacitors and to reduce EMI. A charge pump is used to provide the supply for driving the power switches, ensuring operation at very wide operating duty cycles and avoiding the need for power-draining clamp circuits.

A power-on-reset circuit with user configurable delay indicates when enabled regulators are in specification. The power-on-reset flag also indicates when the input voltage drops below specification, giving the system controller advance warning while the switchers continue to operate down to the shutdown level.

Internal diagnostics provide comprehensive protection against overloads, input undervoltages, and overtemperatures.

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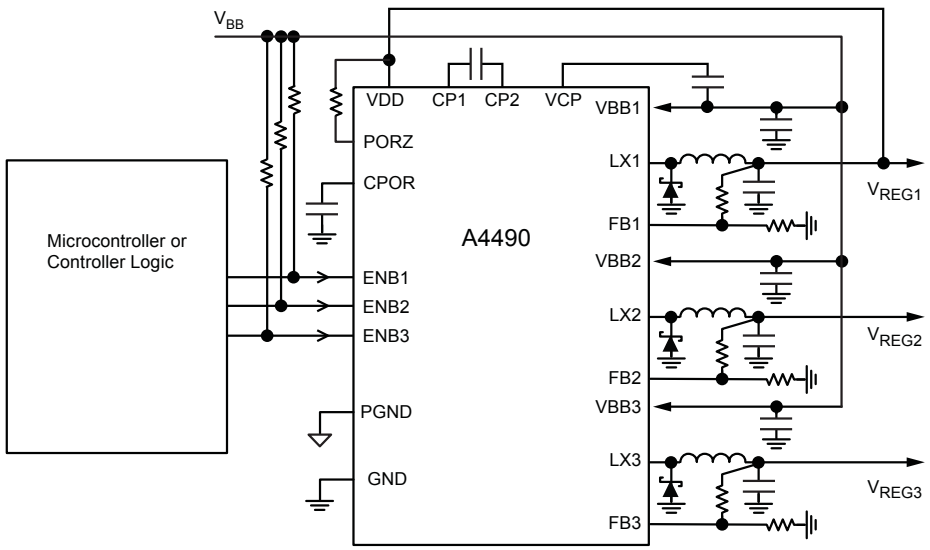
Typical Application



Description (continued)

The A4490 is provided in a 20-contact, 4 mm × 4 mm, 0.75 mm nominal overall height QFN, with exposed pad for enhanced thermal dissipation. It is lead (Pb) free, with 100% matte tin leadframe plating.

Applications include the following:

- Photo, inkjet, and portable printers
- Industrial
- Hand-held devices
- Portable applications

Selection Guide

Part Number	Packing	Operating Temperature Range (°C)
A4490EESTR-T	1500 pieces per 7-in. reel	–40 to 85

Absolute Maximum Ratings (reference to GND)

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		36	V
LX1, LX2, and LX3 Pins	V_{LXn}		–1 to 36	V
PORZ and VDD Pins	V_{IN}		–0.3 to 7	V
ENBx Pin Input Current	I_{ENBx}	Driven by a current-limited voltage source	1	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Recommended Operating Conditions

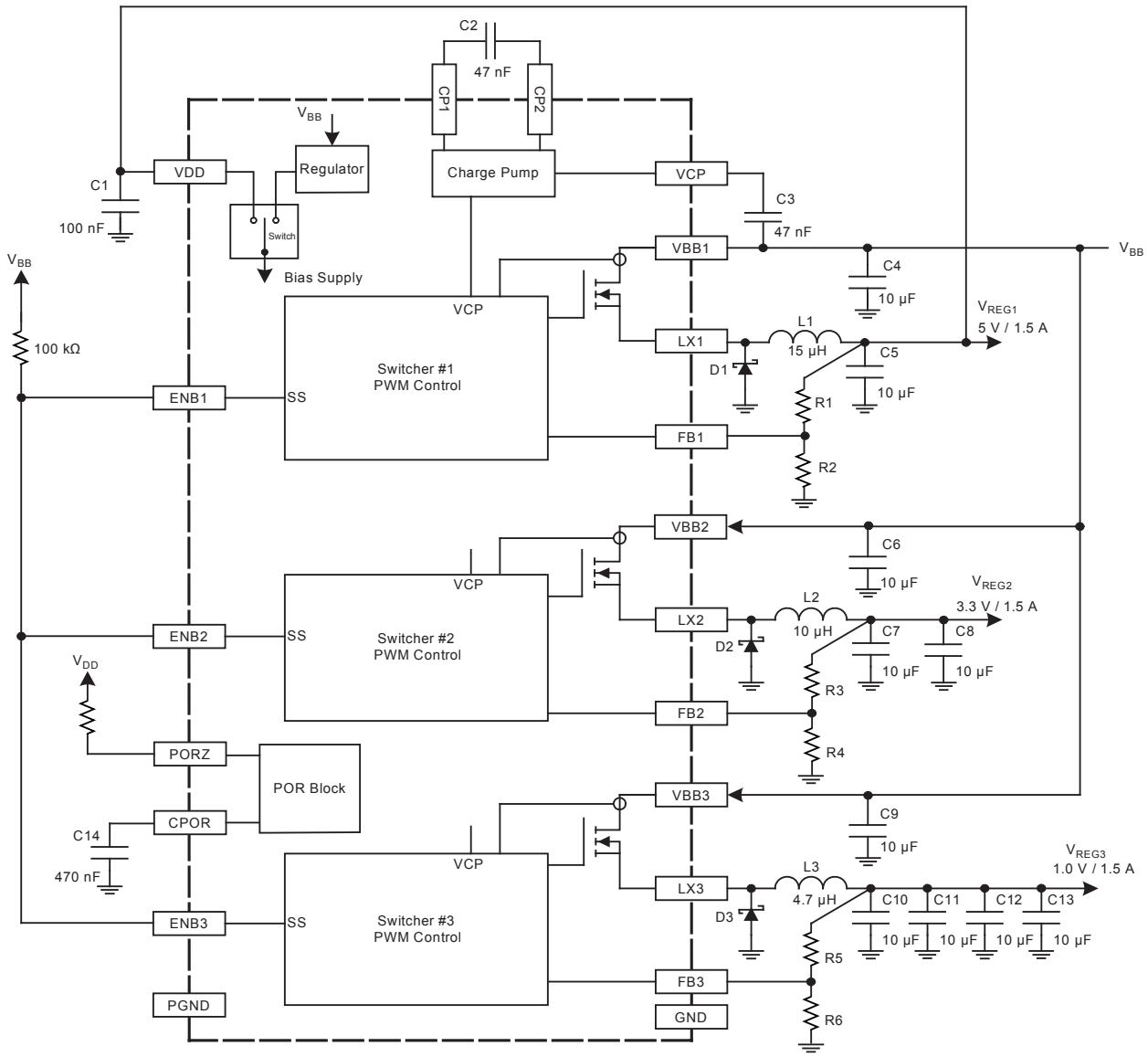
Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Units
Load Supply Voltage	V_{BB}	To operate at V_{BB} < 6 V, connect V_{DD} supply to the V_{BB} supply. See Powering Configurations section.	4.5	–	34	V
LX1, LX2, and LX3 Pins	V_{LXn}		–0.7	–	34	V
Operating Ambient Temperature	T_A		–40	–	85	ºC
Junction Temperature	T_J		–40	–	125	ºC

Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	37	ºC/W

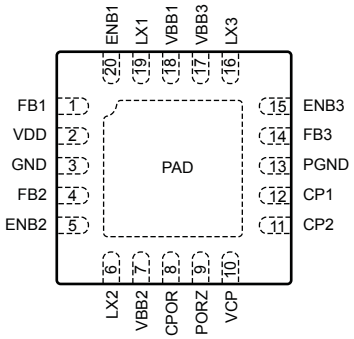
*Additional thermal information available on the Allegro website.

Functional Block Diagram



Note: All capacitors ceramic X5R.

Pin-out Diagram



Terminal List

Number	Name	Function
1	FB1	Feedback REG1
2	VDD	Bias supply
3	GND[1]	Ground
4	FB2	Feedback REG2
5	ENB2	Enable REG2, logic input, active high
6	LX2	Switch node REG2
7	VBB2[2]	Input supply for REG2
8	CPOR	POR delay adjustment
9	PORZ	Power on reset output, active low
10	VCP	Charge pump reservoir
11	CP2	Charge pump capacitor terminal
12	CP1	Charge pump capacitor terminal
13	PGND[1]	Ground for charge pump circuitry
14	FB3	Feedback REG3
15	ENB3	Enable REG3, logic input, active high
16	LX3	Switch node REG3
17	VBB3[2]	Input supply for REG3
18	VBB1[2]	Input supply for REG1
19	LX1	Switch node REG1
20	ENB1	Enable REG1, logic input, active high
–	PAD[3]	Exposed pad for enhanced thermal dissipation

[1]GND and PGND should be connected externally.
[2]The three VBBx pins should be connected together externally.
[3]Thermal pad should be connected to the ground (0 V) plane using thermal vias.

ELECTRICAL CHARACTERISTICS[1,2] at T_A = 25°C, V_{BB} = 6.0 to 34 V, V_{DD} supplied externally, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
General						
VBB Quiescent Current	I_{BBON}	ENBx = high, I_{LOAD} = 0 mA, V_{BB} = 12 V, current drawn by feedback resistors ignored	–	1	2	mA
	I_{BBOFF}	ENBx = 0 V	–	1	–	µA
VDD Supply Range	V_{DD}		3.3	–	5.5	V
VDD Quiescent Current	I_{DD}	ENBx = high	–	–	6	mA
		ENBx = 0 V	–	1	–	µA
REG1, REG2, and REG3						
Feedback Input Bias Current	I_{BIAS}		–400	–100	100	nA
Feedback Voltage	V_{FB}	With respect to 0.8 V target voltage	–	±1.5	–	%
Output Voltage Regulation[3]	V_{OUT}	V_{REGx} = 5 V, I_{OUT} = 0 to 1.5 A, T_A = –20°C to 85°C	–2.5	–	2.5	%
		V_{REGx} = 5 V, I_{OUT} = 0 to 1.5 A, T_A = –40°C to 85°C	–3.5	–	3.5	%
PWM Frequency	f_{SW}		470	550	630	kHz
Maximum Duty Cycle	D_{max}		90	–	–	%
Minimum Duty Cycle	D_{min}		–	5	–	%
Buck Switch On-Resistance	$R_{DS(on)}$	T_J = 25°C, I_{LOAD} = 1.5 A, V_{BB} = 6.0 V	–	450	–	mΩ
		T_J = 125°C, I_{LOAD} = 1.5 A, V_{BB} = 6.0 V	–	700	–	mΩ
		T_J = 25°C, I_{LOAD} = 1.5 A, V_{BB} = 4.5 V	–	560	–	mΩ
		T_J = 125°C, I_{LOAD} = 1.5 A, V_{BB} = 4.5 V	–	870	–	mΩ
Current Limit Threshold	I_{LIM}	Peak current through switch with D = 0.9	2.0			A
Soft Start Duration	t_{ss}		0.625	1.25	1.875	ms
Logic Inputs and Outputs						
ENBx Input Voltage	V_{IL}		–	–	0.8	V
	V_{IH}		2.0	–	–	V
ENBx Input Hysteresis	$V_{I(hys)}$		300	500	–	mV
ENBx Input Current	I_{IL}	$V_{IH} \leq$ 5 V	–1	–	1	µA
PORZ Output (Open Drain)	V_{PORZL}	I_{PORZL} = 1 mA, fault asserted	–	–	0.4	V
PORZ Output Leakage Current	I_{PORZH}	V_{PORZ} = 5 V, fault not asserted	–1	–	1	µA
Power-On Reset Duration	t_{POR}	C_{POR} = 470 nF	75	115	155	ms

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ELECTRICAL CHARACTERISTICS[1,2] (continued) at T_A = 25°C, V_{BB} = 6.0 to 34 V, V_{DD} supplied externally, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Protection						
VREGx Undervoltage Lockout Startup	$V_{REGUV(su)}$	FB1, FB2, and FB3 rising	–	85	–	$\%V_{FB}$
VREGx Undervoltage Lockout Shutdown	$V_{REGUV(sd)}$	FB1, FB2, and FB3 falling	–	80	–	$\%V_{FB}$
VREGx Undervoltage Lockout Startup Hysteresis	$V_{REGUV(suhys)}$		–	5	–	%
VBB Undervoltage Lockout Startup	$V_{BBUV(su)}$	No external VDD supply, V_{BB} rising	3.7	4.3	4.7	V
	$V_{BBCPUV(su)}$	External VDD supply, V_{BB} rising	3.8	4.2	4.6	V
VBB Undervoltage Lockout Shutdown	$V_{BBUV(sd)}$	No external VDD supply, V_{BB} falling	3.6	4.1	4.7	V
	$V_{BBCPUV(sd)}$	External VDD supply, V_{BB} falling	3.0	3.5	4.3	V
VBB Undervoltage Lockout Shutdown Hysteresis	$V_{BBUV(sdhys)}$	No external VDD supply	–	500	–	mV
	$V_{BBCPUV(sdhys)}$	External VDD supply	–	600	–	mV
VBB Undervoltage Warning Threshold	$V_{BBUV(por)}$	V_{BB} falling (forces PORZ low); switchers continue to operate	–	3.6	–	V
Junction Overtemperature Shutdown	T_{JTSD}	Temperature rising	–	165	–	°C
Junction Overtemperature Shutdown Hysteresis	$T_{JTSD(hys)}$	Recovery = $T_{JTSD} - T_{JTSD(hys)}$	–	15	–	°C

[1]For input and output current specifications, negative current is defined as coming out of (sourcing) the specified pin.
[2]Specifications over the junction temperature range of –40°C to 125°C are assured by design and characterization.
[3]Average value of V_{OUT} relative to target voltage. The effects of the feedback resistors are not taken into account.

Functional Description

Basic Operation

The A4490 contains three fixed frequency, buck switching converters with peak current-mode control, including slope compensation. Each converter can be independently turned on and off via the enable inputs (EN1, EN2, and EN3), which are active high. When enabled, the corresponding output is brought-up under the control of a soft start routine, which avoids output voltage overshoot and minimizes input inrush current.

The output voltage is typically divided down by an external potential divider, and is compared against an internal reference voltage to produce an error signal, also known as the *current demand signal*. The current signal through the buck switch is converted into a voltage. This signal is then compared against the current demand signal to create the required duty cycle.

At the beginning of each switching cycle, the buck switch is turned on. When the current signal through the switch reaches the level of the current demand signal, the on-time of the switch is terminated. On the next switching cycle, the switch is turned on again and the cycle is repeated.

One shared clock is used to define the switching frequency for each regulator. Each of the three switching cycles (REG1, REG2, and REG3) are phase shifted with respect to one another by 120° in an attempt to minimize the pulsed current drawn from the input filter capacitors. Under certain conditions, for example at low V_{BB} conditions and relatively high user-set output voltages, switching overlap between channels is inevitable.

Under conditions, such as light loads or high V_{BB} voltages, that cause duty cycles (DC) of less than the minimum value, the converter enters a pulse-skipping mode to ensure regulation is maintained.

A charge pump regulator is provided to ensure a sufficient gate drive is available for all three power switches across the full input voltage range. This regulator allows operation even at very wide operating duty cycles. On initial power-up, an internal regulator is used to provide the bias supply for on-chip control functions.

Each regulator channel utilizes pulse-by-pulse current limiting in the event of either a short circuit or an overload. If the overload is applied long enough, the IC temperature may rise sufficiently to cause the thermal shutdown circuit to operate. The part will auto-restart under control of the soft start circuit after the thermal disable condition is removed, and assuming all other conditions are met. See the Shutdown section for more information.

Power Configuration

The A4490 supports alternative schemes for providing logic supply voltage on the VDD pin. In addition, the IC can be powered up and down using either the VBB or ENB pins.

Powering VDD To minimize power dissipation, especially at high input voltages, it is recommended that an external supply be applied to the VDD input pin. Typically, this voltage is derived from one of the three regulated outputs that are set-up for between 3.3 and 5 V (V_{REGx}).

Another advantage of powering the VDD externally is that the VBB undervoltage lockout level is lowered. To maximize the run time of the switchers during a VBB power-down condition, two alternative undervoltage shutdown conditions are supported, depending on which VDD-powering configuration has been implemented. When no external VDD is applied, the minimum V_{BB}, $V_{BBUV(sd)}$, is 4.1 V typical. When an external VDD is applied, the minimum V_{BB}, $V_{BBCPUV(sd)}$, is 3.5 V typical.

One note of caution when deriving VDD from a VREG output: during initial application of V_{BB}, the internal bias supply automatically starts from the internal regulator because VREG has not yet reached regulation. This means the startup threshold is determined by $V_{BBUV(su)}$ (4.3 V typical) because there is no external VDD. When VREG has begun to supply VDD externally, the shutdown threshold reduces to $V_{BBCPUV(sd)}$ (3.5 V typical). This assumes that V_{REG} is present.

Powering Up and Down with VBB Referring to figure 1, each of the enable inputs (ENBx) are held high by being tied to the V_{BB} rail via a 100 kΩ resistor and the VDD is supplied from one of the regulator outputs. When the V_{BB} voltage reaches the minimum threshold, $V_{BBUV(su)}$, the charge pump supply (VCP) ramps up. When $V_{BB} + V_{CP}$ has reached the minimum threshold $V_{BBCPUV(su)}$, the soft start routines are initiated (t_{SS}) for all three regulator channels (VREGx). When all three regulators have reached the 85% FBx threshold, the power-on-reset timer is initiated. After the power-on-reset period, t_{POR}, has elapsed, PORZ goes high, indicating that all the regulators and V_{BB} are in specification.

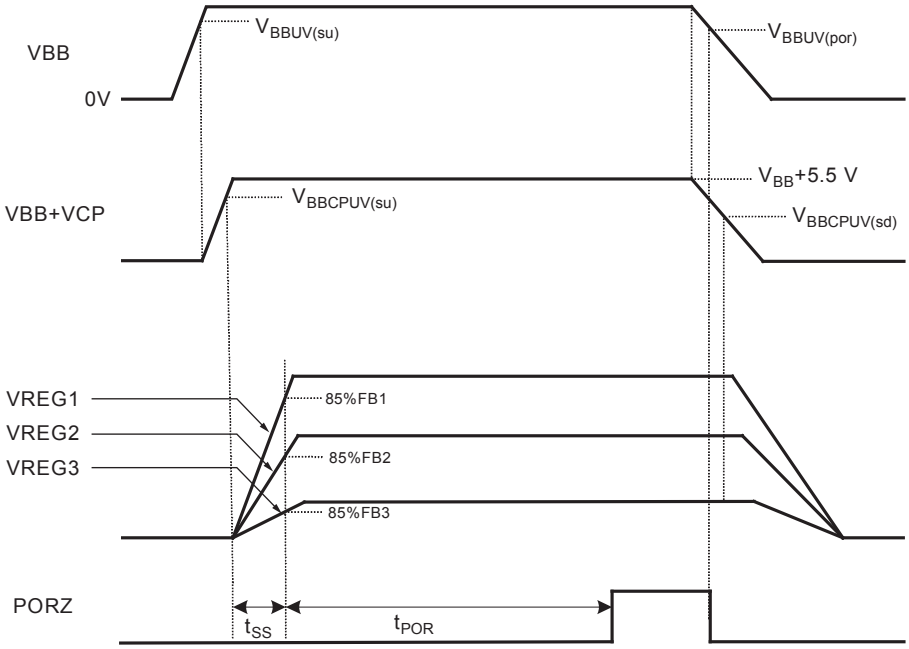


Figure 1. Timing diagram for powering up and down using the VBB pin

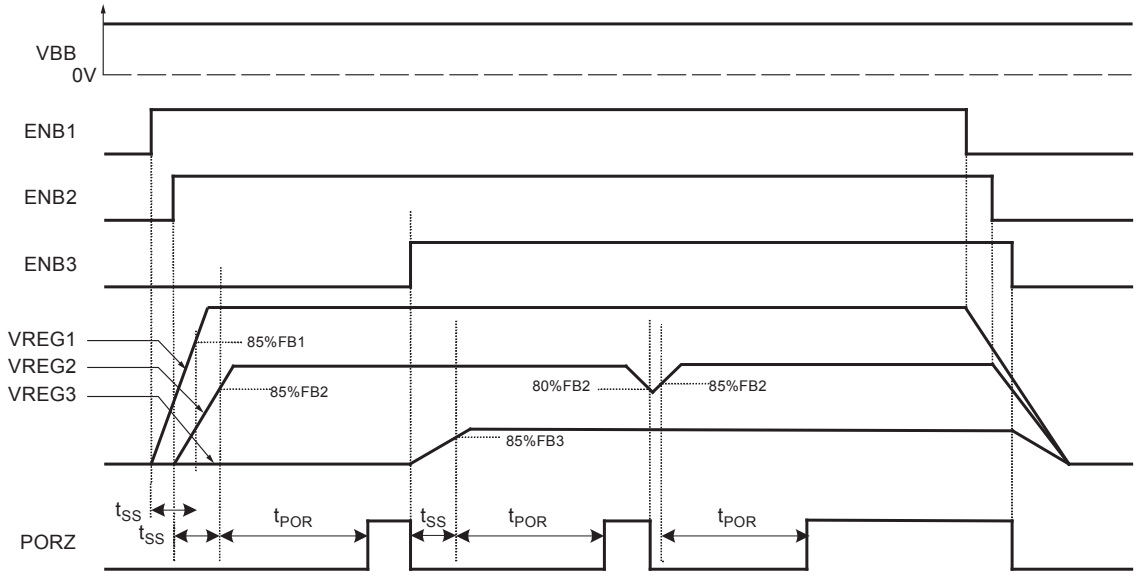


Figure 2. Timing diagram for powering up and down using the ENB pin

When the V_{BB} voltage starts to fall below the undervoltage warning level, $V_{BBUV(por)}$, of 3.6 V typical, the PORZ flag resets. This gives advance warning to the system controller that the V_{BB} voltage is falling. Note that this feature is only guaranteed when VDD is supplied externally. During this interval, the three switchers continue to operate.

While V_{BB} falls further, the VCP supply also tends to fall, which degrades the drive voltage to the series switches. In addition, the higher voltage rails start to fall out of regulation first, as the corresponding maximum duty cycle (D_{max}) for these particular converters is reached.

The regulators that have the lower output voltages achieve some level of steady state, before the A4490 powers down when all of the corresponding V_{BB} undervoltage thresholds have been reached. For example, it may be possible for a 1 V output to continue to operate down to a V_{BB} of 3.4 V typical, if the VDD supply is derived externally. The extent of this effect depends on a myriad of factors, including input and output filter capacitance, output loads, gate drive amplitude, MOSFET $R_{DS(on)}$, and so forth.

Powering Up and Down with Enable Referring to figure 2, V_{BB} is present and the UVLO start-up thresholds, $V_{BBUV(su)}$ and $V_{BBCPUV(su)}$ have been reached. Each of the regulators are enabled in turn. Initially, VREG1 is enabled and is brought-up under the control of the soft start circuit (t_{SS}). Before VREG1 reaches 85% FB1, VREG2 is enabled and is brought-up under a separate soft start control.

When both regulators have reached their respective 85% FB thresholds, the power-on-reset (POR) timer is initiated. Note that the POR timer is only enabled after all of the enabled regulators reach their corresponding 85% FB levels. After the power-on-reset time, t_{POR}, has elapsed, if the FB levels of VREG1 and VREG2 are not below their respective 80% FB levels, then the PORZ signal will go high.

At some point later, if VREG3 is enabled, then the PORZ is reset and VREG3 is brought-up under the control of the soft start circuit. When the 85% FB3 threshold is reached, the POR timer is initiated. After t_{POR} has elapsed, if all the FB levels are above their respective 80% FB levels, then the PORZ signal will go high.

Note that if any regulator channel is not enabled, the channel will not influence PORZ. To avoid multiple signal changes of the PORZ signal, it is recommended that the system be designed such that all three regulator channels are within specification before t_{POR} has elapsed.

If any regulator channel drops below 80% FB, the PORZ signal will be reset. If the voltage then recovers to within 85% FB, the POR timer is initiated again. Note that a soft start is not initiated when the feedback voltage drops below the 80% FB level. This is to allow a rapid auto-restart in the event of an overload or similar fault. If a soft start is required, it is recommended that on receipt of the PORZ reset signal, the system controller disables and then re-enables the relevant regulator channels again. As soon as the last regulator is disabled the PORZ signal is reset.

Power on Reset The power-on-reset duration, t_{POR}, is determined by selecting an appropriate capacitor connected to the CPOR pin. The value of t_{POR} can be determined by the following formula:

$$t_{POR} = 2.131 \times 10^5 \times C_{POR} \quad . \qquad (1)$$

The PORZ output goes high when both V_{BB} is above the undervoltage warning levels, and the FB pins of the regulators that are enabled are > 85% of the V_{REG} voltage.

Because the external capacitor is charged via a 5 µA current source, care must be taken in the layout to avoid additional leakage paths. The capacitor should be positioned adjacent to the CPOR pin, and the ground connection to the A4490 GND pin should be as short as possible.

It is recommended that the t_{POR} period be set to exceed the start-up phases of all three regulators, to avoid the possibility of multiple triggerings of the PORZ output.

Output Voltage Selection The output voltage on each of the three regulators is set by the following relationship, shown here for the VREG1 channel:

$$R_1 = R_2 \left(\frac{V_{REG1}}{V_{FB}} - 1 \right) \quad , \qquad (2)$$

where R2 (connected between GND and the FB1 pin) should be a value between 4.7 and 12 kΩ. R1 is connected between the output rail and the FB1 pin. V_{REG1} is the set output regulator voltage. V_{FB} is the reference voltage.

The tolerances of the feedback resistors influence the voltage setpoint. It is therefore important to consider the tolerance selection when targeting an overall regulation figure.

The bias current, I_{BIAS}, flowing out of the FB1 node into R2, will introduce a small voltage offset to the output.

Enable Each regulator channel can be individually enabled via the corresponding ENBx pin. If any channel is required to start-up automatically after the VBB voltage is applied, that particular channel should have the ENB pin tied to the VBB rail via a pullup resistor.

This resistor should be selected to limit the current to less than the maximum specified value, 1 mA. This prevents the internal protection clamps from turning on. It is recommended that a 100 kΩ pull-up resistor be used. This would ensure the current remains below the maximum value when V_{BB} = 36 V.

Soft Start Each regulator channel contains a soft start circuit. A soft start cycle is initiated when the appropriate regulator enable input is set to high; the V_{BB}, charge pump, and bias supply voltages are above the minimum values; and no thermal shutdown condition exists. Note that an overload or short circuit will not cause a soft start cycle, unless a thermal shutdown event occurs.

During a soft start cycle, the reference voltage is ramped from 0 to 0.8 V typical, which in turn forces the current demand signal to increase in a linear fashion.

Shutdown All converter channels are disabled in the event of either a thermal shutdown event or an undervoltage on VBB ($V_{BBUV(sd)}$ or $V_{BBCPUV(sd)}$).

As soon as the above fault conditions have been removed, and assuming the ENB inputs are enabled, the appropriate channels will auto-restart under control of the soft start.

Current Limit The typical peak current limit for each channel is specified as 2.5 A minimum, with a duty cycle of 0.9. The minimum current limit occurs at maximum duty cycle (0.9), because the slope compensation has a maximum effect under this condition. As the duty cycle reduces, the current limit increases. This means for applications that operate with a narrow duty cycle, it is possible to operate with a load current greater than 2.0 A.

Figure 3 illustrates the typical peak current limit versus duty cycle. For example, it is possible to operate with a peak current limit of 3.75 A with a duty cycle of 0.3.

As well as ensuring the peak current limit is not exceeded, under worst case load and input voltage conditions, it is also important to check the implications on the thermal performance. See the Thermal Considerations section.

Component Selection

Inductor The inductance value, L, determines the ripple current. It is important to ensure that the minimum current limit is not exceeded under worst-case conditions: V_{BB}(min), I_{LOAD}(max), f_{SW}(min), and L(min).

It is recommended that gapped ferrite solutions be used as opposed to powdered iron solutions, the latter of which exhibit relatively high core losses that can have a large impact on long term reliability.

Inductors are typically specified at two current levels, rms current and saturation current. With regard to the rms current, it is important to understand how the rms current level is specified, in terms of ambient temperature. Some manufacturers quote an ambient only, whilst others quote a temperature that includes a self-induced temperature rise. For example, if an inductor is rated for 85°C and includes a self-induced temperature rise of 25°C at maximum load, then the inductor cannot be safely operated beyond an ambient temperature of 60°C at full load. The rms current can be assumed to be simply the maximum load current, with perhaps some margin to allow for overloads, and so forth.

The first stage of determining the inductor value is to specify a peak-to-peak ripple current of typically about 20% to 25% of the maximum load.

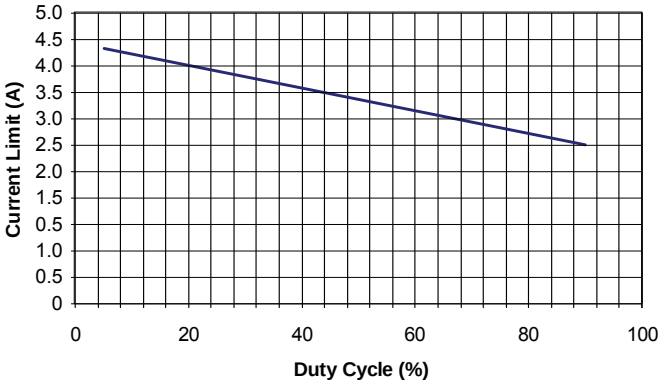


Figure 3. Current limit versus duty cycle

The maximum peak-to-peak ripple current, I_{RIPPLE}, occurs at the maximum input voltage. Therefore the duty cycle, D, should be found under these conditions (for the VREG1 channel):

$$D(min) = \frac{V_{REG1}+V_f}{V_{BB}(max)+V_f} \quad . \quad (3)$$

where V_f is the forward voltage drop of the recirculation diode.

The required inductance can be found:

$$L(min) = \frac{V_{BB}(max) - V_{REG1}}{I_{RIPPLE}} \times D(min) \times \frac{1}{f_{SW}(min)} \quad , \quad (4)$$

Note that the manufacturers inductance tolerance should also be taken into account. This value may be as high as ±20%. The peak-to-peak current should not exceed 1 A, to avoid instability in the innermost circuit loops due to insufficient slope compensation.

The maximum peak current can be found from to ensure that the saturation current level of the chosen inductor is not exceeded:

$$I_{sat} = I_{LOAD} + \frac{I_{RIPPLE}}{2} \quad . \quad (5)$$

Recommended inductor manufacturers and ranges are:

- Taiyo Yuden: NR6045 series for 1.5 A outputs
- Taiyo Yuden: NRG4026 series for 1.0 A outputs
- Sumida: CDH74 series for 1.5 A outputs

Output Capacitor In the interests of size, cost and performance, it is highly recommended that ceramic X5R or X7R capacitor types be used. When using ceramic capacitors another important consideration is the E-field effects on the actual value of the capacitor. To minimize the effects of the capacitance reducing with output voltage, it is recommended that the working voltage of the capacitor be considerably more than the set output voltage. As a suggestion, it is recommended that 6.3 V-rated capacitors should be used for output voltages of 3.3 V and below. For output voltages of 5 V, a 10 V-rated capacitor should be used.

The output capacitor determines the output voltage ripple and is used to close the control loop. To guarantee stability, the capacitance has to increase as the output voltage is reduced. This is actually reasonable from a ripple voltage point of view, as the ripple voltage is typically specified as a percentage of output voltage.

The following table outlines what the minimum output capacitance should be for a given output voltage:

Output Voltage (V)	Minimum Output Capacitance (µF)
15	3.3
12	4.7
5	10
3.3	20
1.8 to 2.5	30
<1.8	40

Capacitance values with greater than the above values can be used with the effect of reducing the bandwidth. This may be necessary in systems that have extremely low ripple/noise requirements.

The output ripple is largely determined by the output capacitance and the effects of ESR and ESL can largely be ignored assuming good layout practice is observed.

The output voltage ripple can be approximated to:

$$V_{RIPPLE} \approx \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}} \quad , \quad (6)$$

When using ceramic capacitors, there is generally no need to consider the current carrying capability due to the negligible heating effects of the ESR. Also, the rms current flowing into the output capacitor is extremely low.

Input Capacitor Again it is highly recommended that ceramic, X5R or X7R capacitors be used.

The value of the input capacitance determines the amount of current ripple (EMI) that appears at the source (V_{BB} supply) terminals. The amounts of current flowing in and out of the input capacitor depend on the relative impedances between the input capacitor impedance and the source impedance. To achieve a low impedance filter solution it is recommended to place at least two capacitors in parallel.

Again, there is generally no need to consider the heating effects of the rms current flowing through the ESR. Also, the phase-shifting of the input current drawn by each of the regulators helps to reduce the overall rms current.

Flyback Diode This diode conducts during the switch off-time. A Schottky diode is recommended to minimize both the forward drop and switching losses.

The worst case dissipation occurs at maximum V_{BB}, when the duty cycle, D, is a minimum. The average current through the diode can be found:

$$I_{DIODE(av)} = I_{LOAD} \times (1 - D(min)) \quad . \qquad (7)$$

The forward voltage drop, V_f, can be found from the diode characteristics by using the actual load current (not the average current).

The static power dissipation can be found:

$$P_{STAT} = I_{LOAD(av)} \times V_f \quad . \qquad (8)$$

It is also important to take into account the thermal rating of the package, $R_{\theta JA}$, and the ambient temperature, to ensure that enough heatsinking is provided to maintain the diode junction temperature within the safe operating area for the device.

To minimize the heating effects from the A4490 on the diode and vice-versa, it is recommended that the diode be mounted on the reverse side of the printed circuit board.

Support Components POR capacitor (C11), charge pump capacitor (C1), reservoir capacitor (C2) and VDD filter capacitor (C12) should be ceramic X5R or X7R.

Thermal Considerations

To ensure the A4490 operates in the safe operating area, which effectively means restricting the junction temperature to less than 150°C, several checks should be made. The general approach is to work out what thermal impedance ($R_{\theta JA}$) is required to maintain the junction temperature at a given level, for a particular power dissipation.

Another factor worth considering is that other power dissipating components on the system PCB may influence the thermal performance of the A4490. For example, the power loss contribution from the recirculation diode and the sense resistor may cause the junction temperature of the A4490 to be higher than expected.

The following steps can be used as a guideline for determining a suitable thermal solution. It should be noted that this process is usually an iterative one to achieve the optimum solution. These factors can be considered as follows:

Step 1. Estimate the maximum ambient temperature, $T_A(max)$, of the application.

Step 2. Define the maximum junction temperature, $T_J(max)$. Note that the absolute maximum is 150°C.

Step 3. Determine the worst case power dissipation, $P_D(max)$.

The evaluation should consider these at maximum load and minimum V_{BB}. Contributors are switch static and dynamic losses, and control losses. These are described in the following sections

Switch Static Losses The following steps can be used to determine switch static losses:

Estimate the maximum duty cycle:

$$D(max) = \frac{V_{REG} + V_f}{V_{BB}(min) + V_f} \quad , \qquad (9)$$

where V_f is the forward voltage drop of the Schottky diode under the given load current.

Estimate the $R_{DS(on)}$ of the each regulator switch at the given junction temperature:

$$R_{DS(on)TJ} = R_{DS(on)25C}\left(1 + \frac{T_J - 25}{200}\right) \quad . \qquad (10)$$

Note that if the V_{BB} range is restricted to between 4.5 and 5.5 V, the $R_{DS(on)}$ increases. For example, the $R_{DS(on)}$ at 25°C with a V_{BB} greater than 6 V is 450 mΩ typical, as stated in the Electrical Characteristics table. Under the same temperature conditions, with the V_{BB} = 4.5 V, the $R_{DS(on)}$ is 560 mΩ typical. For VBB voltages between 4.5 and 6 V, the $R_{DS(on)}$ can be found by linear approximation. For more information on operating the A4490 between a V_{BB} voltage of 4.5 and 5.5 V, see the Power Configurations section.

The static loss for each switch can be determined:

$$P_{STAT} = I_{LOAD}^2 \times D(max) \times R_{DS(on)TJ} \quad , \qquad (11)$$

where I_{LOAD} is the load for that particular regulator channel.

Switch Dynamic Losses The following can be used to determine switch dynamic losses:

Both turn on and turn off losses can be estimated:

$$P_{DYN} = V_{BB}(\min) \times \frac{I_{LOAD}}{2} \times 30\times10^{-9} \times f_{SW} \quad , \qquad (12)$$

where f_{SW} is the switching frequency.

Control Losses The following steps can be used to determine control losses:

$$P_{VBB} = I_{BBON} \times V_{BB} \quad , \qquad (13)$$

where I_{BBON} is the quiescent current assuming all three regulators are on.

$$P_{VDD} = I_{VDD} \times V_{DD} \quad , \qquad (14)$$

where I_{VDD} and is the quiescent current on VDD.

Total Losses The total losses can now be estimated:

$$P_{TOTAL} = P_{STAT1} + P_{STAT2} + P_{STAT2} + P_{DYN1} + P_{DYN2} + P_{DYN3} + P_{VBB} + P_{VDD} \quad . \qquad (15)$$

Thermal Impedance The thermal impedance required for the solution can now be determined:

$$R_{\theta JA} = \frac{T_J - T_A}{P_{TOTAL}} \quad . \qquad (16)$$

Example

Selected parameters:

V_{BB}(min) = 6 V
V_{REG1} = 5 V at 1 A
V_{REG2} = 3.3 V at 1 A
V_{REG3} = 1.8 V at 800 mA
T_A= 70°C
T_J = 115°C
V_f = 0.4 V

(a) Switch static losses

V_{REG1} duty cycle, $D_1 = \frac{5+0.4}{6+0.4} = 0.84$

V_{REG2} duty cycle, $D_2 = \frac{3.3+0.4}{6+0.4} = 0.58$

V_{REG3} duty cycle, $D_3 = \frac{1.8+0.4}{6+0.4} = 0.34$

The $R_{DS(on)}$ of each switch can be found:

$$R_{DS(on)TJ} = 450\times10^{-3}\left(1+\frac{115-25}{200}\right) = 0.653\ \Omega$$

The static loss of each switch can be found:

$P_{STAT1} = 1^2 \times 0.84 \times 0.653 = 0.55$ W
$P_{STAT2} = 1^2 \times 0.58 \times 0.653 = 0.379$ W
$P_{STAT3} = 0.8^2 \times 0.34 \times 0.653 = 0.14$ W

(b) Switch dynamic losses

$$P_{DYN1} = 6 \times \frac{1}{2} \times 30\times10^{-9} \times 500\times10^{3} = 0.045\ \text{W}$$

$$P_{DYN2} = 6 \times \frac{1}{2} \times 30\times10^{-9} \times 500\times10^{3} = 0.045\ \text{W}$$

$$P_{DYN3} = 6 \times \frac{0.8}{2} \times 30\times10^{-9} \times 500\times10^{3} = 0.036\ \text{W}$$

(c) Control losses

$P_{VBB} = 0.005 \times 6 = 0.03$ W
$P_{VDD} = 0.001 \times 3.3 = 0.003$ W

(d) The total power dissipation can now be found:

$P_{TOTAL} = 0.55 + 0.379 + 0.14 + 0.045 + 0.045 + 0.036 + 0.03 + 0.003 = 1.228$ W

(e) The thermal impedance required for the solution can be found:

$$R_{\theta JA} = \frac{115-70}{1.228} = 36.6\ ^\circ\text{C/W}$$

For this particular solution a high thermal efficiency board is required to ensure the junction temperature is kept below 115°C. For maximum effectiveness, the PCB pad area underneath the thermal pad of the A4490 should be exposed copper. Several thermal vias (say between 4 and 8) should be used to connect the thermal pad to the internal ground plane. If possible, an additional thermal copper plane should be applied to the bottom side of the PCB and connected to the thermal pad of the A4490 through the vias.

This calculation assumes no thermal influence from other components. If possible, it is advisable to mount the flyback diodes on the reverse side of the printed circuit board. Ensure low impedance electrical connections are implemented between board layers.

PCB Layout Guidelines The ground plane is largely dictated by the thermal requirements described in the previous section. The ground referenced power components should be referenced to a star ground, located away from the A4490 to minimize ground bounce issues.

A small, local, relatively quiet ground plane near the A4490 should be used for the ground referenced support components, to minimize interference effects of ground noise from the power circuitry. Figure 4 illustrates the recommended grounding architecture.

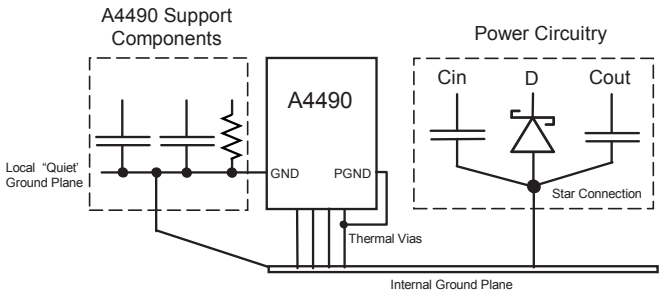


Figure 4. Ground plane configurations

To avoid ground bounce and offset issues, it is highly recommended that the ground referenced feedback resistors (R2, R4, and R6) should be connected as close to the GND connection of the A4490 as possible.

A local quiet ground plane around these components can be implemented, however, this ground plane should have a high impedance connection to the star connection of the power stages.

If a ground plane is used, it is recommended that it does not overlap the switching nodes (LX1, LX2, and LX3) to avoid the possibility of noise pick-up. To minimize the possibility of noise injection issues, it is recommended to isolate the ground plane around high impedance nodes such as: FBx, ENBx and CPOR.

In terms of grounding the power components, a star connection should be made to minimize the ground loop impedances. Note that although a ground plane may be required to meet the thermal characteristics of the solution it is still imperative to implement a ground star connection for the power components. The ground for the charge pump (PGND) should be connected to the thermal vias.

Figures 5 and 6 below illustrates the importance of keeping the ground connections as short as possible and forming good star connections.

Figure 5 also illustrates the current conduction paths during the on-cycle of the switching FET. The following points should be noted:

• The capacitor C_{IN} should be placed as close as possible to the VBB terminals. The capacitance should be split between the VBB terminals for V_{REG1} and V_{REG3} and the VBB terminal for V_{REG2}.

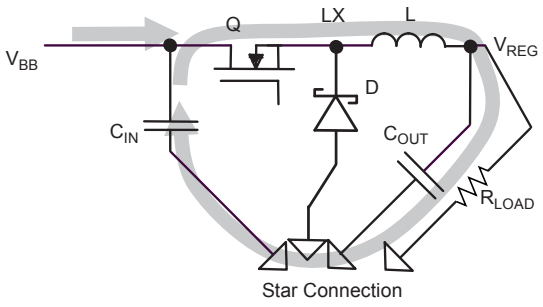


Figure 5. FET on-cycle current conduction paths

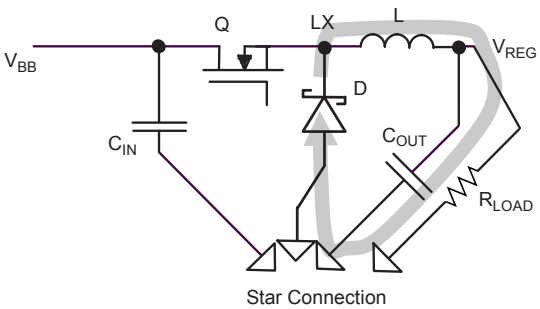


Figure 6. FET off-cycle current conduction paths

The VBB terminals for V_{REG1} and V_{REG2} should be connected via short and wide traces to the VBB terminal for V_{REG3}.

• Each inductor should be connected as close as possible to the respective switching FET (LX1, LX2, and LX3) and output capacitors.

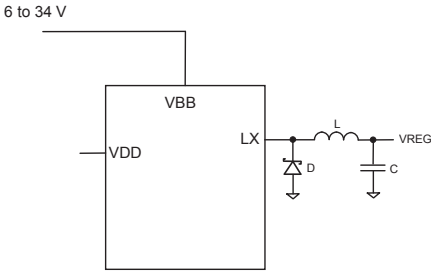
Figure 6 shows the current conduction path during the off-cycle of the switching FET. The following points should be noted:

• The diode D should be placed as close as possible to both the switching FET and the inductor.

• Support components: POR capacitor (C11), charge pump capacitor (C1), reservoir capacitor (C2), and VDD filter capacitor (C12) should be located as close as possible to their respective terminal connections. The ground referenced capacitors should be connected as close to the GND terminal as possible.

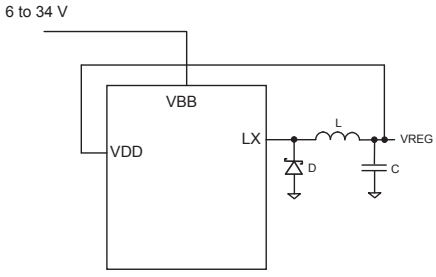
Powering Configurations The following three diagrams show typical configurations for providing power to the application. The middle diagram corresponds to the typical application shown on the front page.

Only VBB supplied



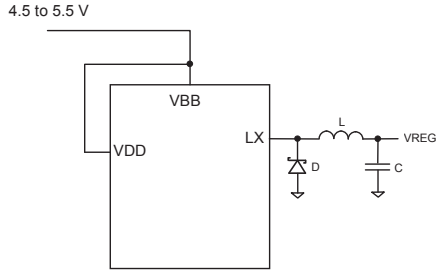
Comments:
- **Simple configuration, only one supply required**
- **Increased power losses at higher VBB voltages**
- **V_{BB} start-up = 4.3 V (typical), shutdown = 4.1 V (typical)**

VDD applied externally (first option)



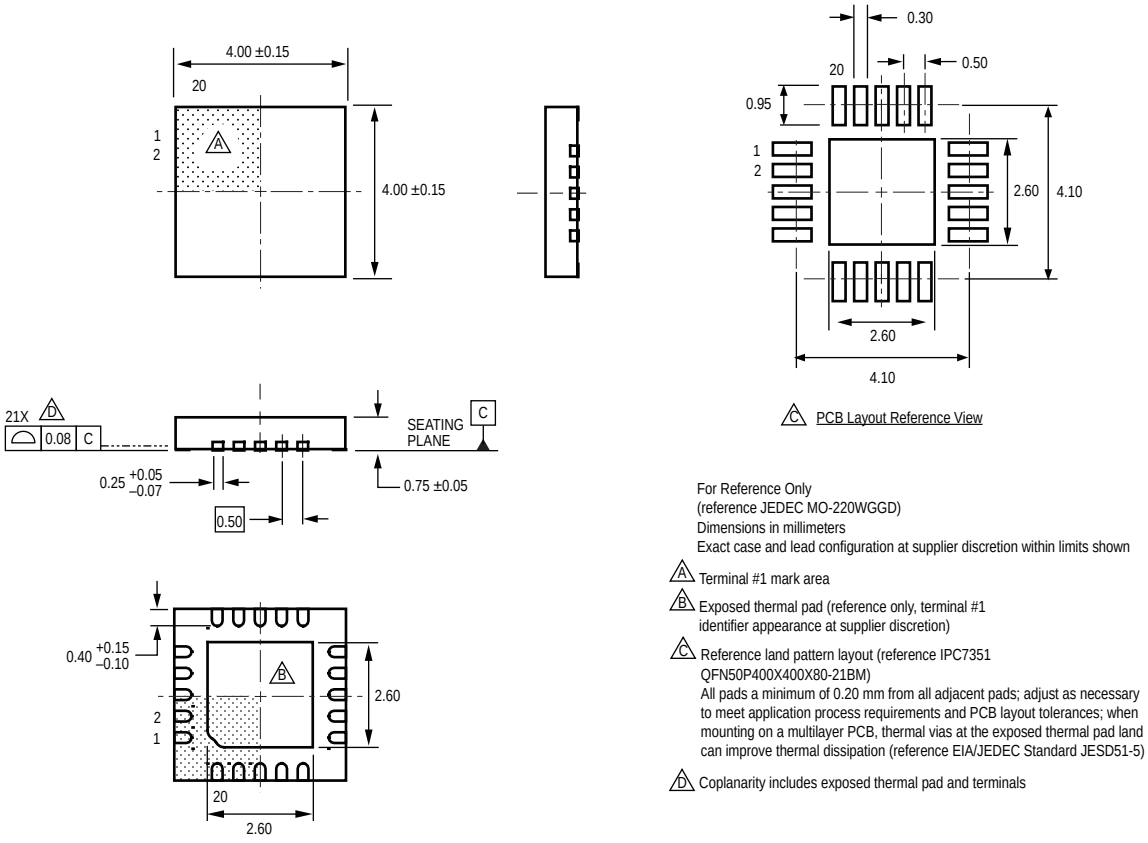
Comments:
- **Reduced power losses at higher VBB voltages**
- **V_{BB} start-up = 4.3 V (typical), shutdown = 3.5 V (typical). In this case, the start-up threshold ($V_{BBUV(su)}$) is higher because V_{REG} is not present**

VDD applied externally (second option)



Comments:
- **Power restricted as V_{BB} < 6 V, due to increase in $R_{DS(on)}$ of buck switches**
- **V_{BB} start-up = 4.2 V (typical), shutdown = 3.5 V (typical)**

Package ES, 20-Pin QFN



For Reference Only
(reference JEDEC MO-220WGGD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-21BM)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Revision History

Revision	Revision Date	Description of Revision
Rev. 10	June 26, 2012	Update I_{DD} and undervoltage lockout

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