THE DATASHEET OF

UJA1168ATK/X/0Z

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UJA1168A

Mini high-speed CAN system basis chip for partial networking

Rev. 1 — 23 August 2019 Product data sheet

1. General description

The UJA1168A is a mini high-speed CAN System Basis Chip (SBC) containing an ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant HS-CAN transceiver and an integrated 5 V/100 mA supply for a microcontroller. It also features a watchdog and a Serial Peripheral Interface (SPI). The UJA1168A can be operated in very-low-current Standby and Sleep modes with bus and local wake-up capability and supports ISO 11898-2:2016 compliant CAN partial networking by means of a selective wake-up function. The microcontroller supply is switched off in Sleep mode.

The UJA1168ATK and UJA1168ATK/F variants contain a battery-related high-voltage output (INH) for controlling an external voltage regulator, while the UJA1168ATK/X and UJA1168ATK/XF are equipped with a 5 V sensor supply (VEXT).

A dedicated implementation of the partial networking protocol has been embedded into the UJA1168ATK/F and UJA1168ATK/XF variants (see Section 7.8.2 for further details on CAN FD). This function is called ‘FD-passive’ and is the ability to ignore CAN FD frames while waiting for a valid wake-up frame in Sleep/Standby mode. This additional feature of partial networking is the perfect fit for networks that support both CAN FD and standard CAN 2.0 communications. It allows normal CAN controllers that do not need to communicate CAN FD messages to remain in partial networking Sleep/Standby mode during CAN FD communication without generating bus errors.

This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

A number of configuration settings are stored in non-volatile memory, allowing the SBC to be adapted for use in a specific application. This makes it possible to configure the power-on behavior of the UJA1168A to meet the requirements of different applications.

2. Features and benefits

2.1 General

- ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant high-speed CAN transceiver
- Hardware and software compatible with the UJA116x product family and with improved EMC performance
- Loop delay symmetry timing enables reliable communication at data rates up to 5 Mbit/s in the CAN FD fast phase
- Autonomous bus biasing according to ISO 11898-6
- Fully integrated 5 V/100 mA low-drop voltage regulator for 5 V microcontroller supply (V1)

- Bus connections are truly floating when power to pin BAT is off
- No ‘false’ wake-ups due to CAN FD frame detection in UJA1168ATK/F and UJA1168ATK/XF

2.2 Designed for automotive applications

- ±8 kV ElectroStatic Discharge (ESD) protection, according to the Human Body Model (HBM) on the CAN bus pins
- ±6 kV ESD protection, according to IEC TS 62228 on the CAN bus pins, the sensor supply output VEXT and on pins BAT and WAKE
- CAN bus pins short-circuit proof to ±58 V
- Battery and CAN bus pins protected against automotive transients according to ISO 7637-3
- Very low quiescent current in Standby and Sleep modes with full wake-up capability
- Leadless HVSON14 package (3.0 mm × 4.5 mm) with improved Automated Optical Inspection (AOI) capability and low thermal resistance
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.3 Low-drop voltage regulator for 5 V microcontroller supply (V1)

- 5 V nominal output; ±2 % accuracy
- 100 mA output current capability
- Current limiting above 150 mA
- On-resistance of 5 Ω (max)
- Support for microcontroller RAM retention down to a battery voltage of 2 V
- Undervoltage reset with selectable detection thresholds: 60 %, 70 %, 80 % or 90 % of output voltage
- Excellent transient response with a 4.7 μF ceramic output capacitor
- Short-circuit to GND/overload protection on pin V1
- Turned off in Sleep mode

2.4 Power Management

- Standby mode featuring very low supply current; voltage V1 remains active to maintain the supply to the microcontroller
- Sleep mode featuring very low supply current with voltage V1 switched off
- Remote wake-up capability via standard CAN wake-up pattern or via ISO 11898-6 compliant selective wake-up frame detection, including CAN FD-passive support in /F and /XF variants
- Bit rates of 50 kbit/s, 100 kbit/s, 125 kbit/s, 250 kbit/s, 500 kbit/s and 1 Mbit/s supported during selective wake-up
- Local wake-up via the WAKE pin
- Wake-up source recognition
- Local and/or remote wake-up can be disabled to reduce current consumption
- High-voltage output (INH) for controlling an external voltage (UJA1168ATK and UJA1168ATK/F)

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2.5 System control and diagnostic features

- Mode control via the Serial Peripheral Interface (SPI)
- Overtemperature warning and shutdown
- Watchdog with independent clock source
- Watchdog can be operated in Window, Timeout and Autonomous modes
- Optional cyclic wake-up in watchdog Timeout mode
- Watchdog automatically re-enabled when wake-up event captured
- Watchdog period selectable between 8 ms and 4 s
- Supports remote flash programming via the CAN bus
- 16-, 24- and 32-bit SPI for configuration, control and diagnosis
- Bidirectional reset pin with variable power-on reset length to support a variety of microcontrollers
- Configuration of selected functions via non-volatile memory

2.6 Sensor supply voltage (pin VEXT of UJA1168ATK/X and UJA1168ATK/XF)

- 5 V nominal output; ±2 % accuracy
- 30 mA output current capability
- Current limiting above 30 mA
- Excellent transient response with a 4.7 μF ceramic output load capacitor
- Protected against short-circuits to GND and to the battery
- High ESD robustness of ±6 kV according to IEC TS 62228
- Can handle negative voltages as low as −18 V

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3. Product family overview

Table 1. Feature overview of UJA1168A SBC family

Device	Modes			Supplies			Host Interface		Additional Features				
	Normal & Standby modes	Sleep mode	Reset mode	V1: 5 V, µC and CAN	VEXT: 5 V, external loads	INH: high-voltage output	SPI: for control & diagnostics	RSTN: reset pin	Watchdog	Local WAKE pin	Non-volatile memory	CAN partial networking	CAN FD passive
UJA1168ATK	●	●	●	●		●	●	●	●	●	●	●	
UJA1168ATK/X	●	●	●	●	●		●	●	●	●	●	●	
UJA1168ATK/F	●	●	●	●		●	●	●	●	●	●	●	●
UJA1168ATK/XF	●	●	●	●	●		●	●	●	●	●	●	●

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
UJA1168ATK[1]	HVSON14	plastic thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm	SOT1086-2
UJA1168ATK/X[2]			
UJA1168ATK/F[1][3]			
UJA1168ATK/XF[2][3]			

[1] UJA1168ATK and UJA1168ATK/F contain a high-voltage output for controlling an external voltage regulator.

[2] UJA1168ATK/X and UJA1168ATK/XF include a 5 V/30 mA sensor supply.

[3] UJA1168ATK/F and UJA1168ATK/XF can be configured to recognize CAN FD frames as valid data frames, but will not wake up when a CAN FD frame is received (CAN FD-passive).

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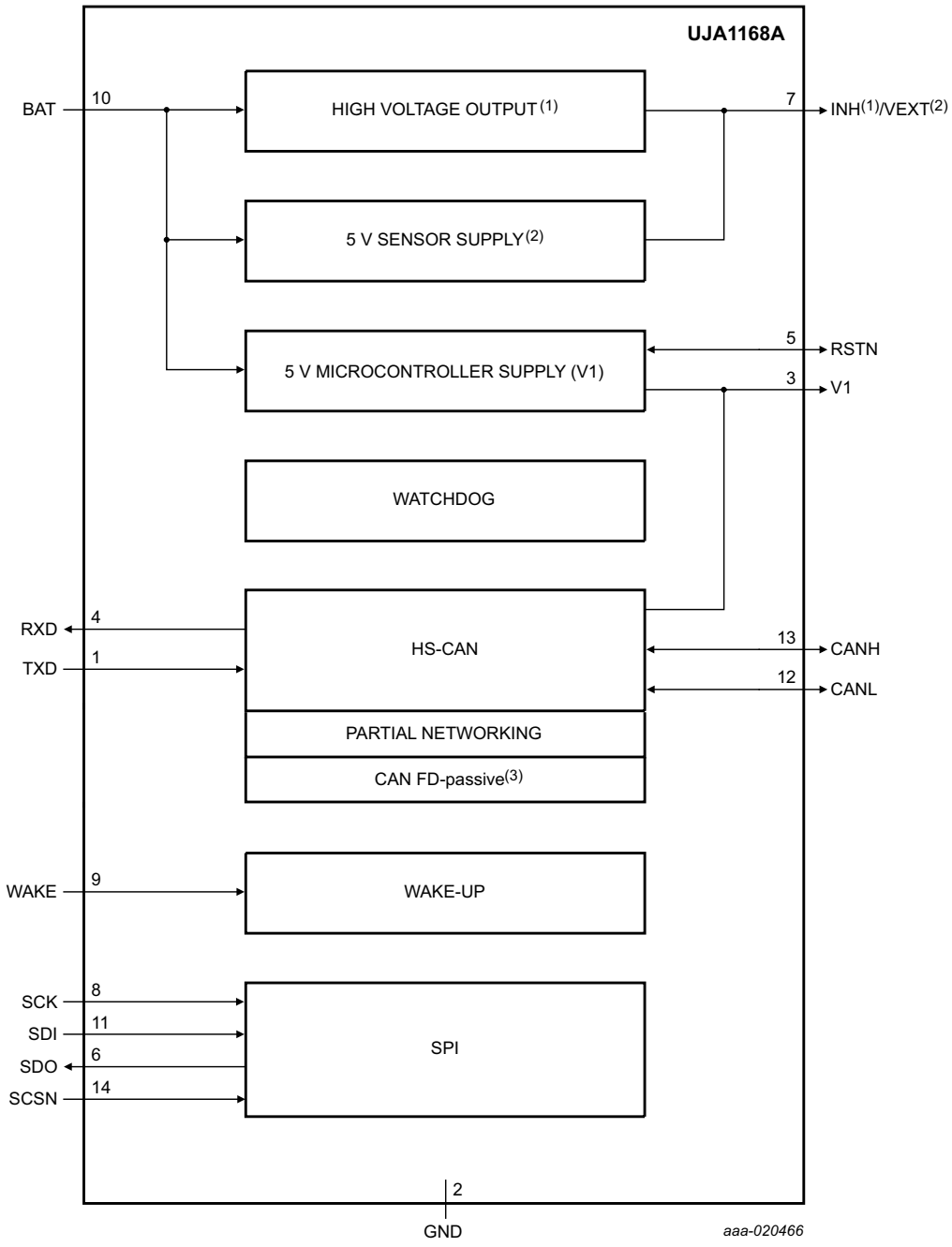
5. Block diagram



(1) UJA1168ATK and UJA1168ATK/F only.

(2) UJA1168ATK/X and UJA1168ATK/XF only.

(3) UJA1168ATK/F and UJA1168ATK/XF only.

Fig 1. Block diagram of UJA1168A

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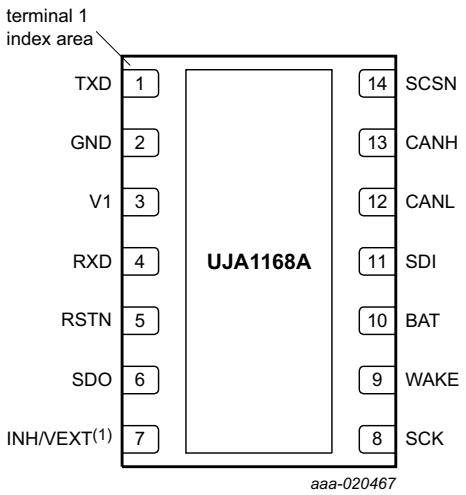
6. Pinning information

6.1 Pinning



Transparent top view

(1) INH in the UJA1168ATK and UJA1168ATK/F; VEXT in the UJA1168ATK/X and UJA1168ATK/XF

Fig 2. Pin configuration diagram

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
TXD	1	transmit data input
GND	2[1]	ground
V1	3	5 V microcontroller supply voltage
RXD	4	receive data output; reads out data from the bus lines
RSTN	5	reset input/output
SDO	6	SPI data output
INH	7	high-voltage output for switching external regulators (UJA1168ATK and UJA1168ATK/F only)
VEXT	7	sensor supply voltage (UJA1168ATK/X and UJA1168ATK/XF only)
SCK	8	SPI clock input
WAKE	9	local wake-up input
BAT	10	battery supply voltage
SDI	11	SPI data input
CANL	12	LOW-level CAN bus line
CANH	13	HIGH-level CAN bus line
SCSN	14	SPI chip select input

[1] The exposed die pad at the bottom of the package allows for better heat dissipation and grounding from the SBC via the printed circuit board. For enhanced thermal and electrical performance, it is recommended to solder the exposed die pad to GND.

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7. Functional description

7.1 System controller

The system controller manages register configuration and controls the internal functions of the UJA1168A. Detailed device status information is collected and made available to the microcontroller.

7.1.1 Operating modes

The system controller contains a state machine that supports seven operating modes: Normal, Standby, Sleep, Reset, Forced Normal, Overtemp and Off. The state transitions are illustrated in Figure 3.

7.1.1.1 Normal mode

Normal mode is the active operating mode. In this mode, all the hardware on the device is available and can be activated (see Table 4). Voltage regulator V1 is enabled to supply the microcontroller.

The CAN interface can be configured to be active and thus to support normal CAN communication. Depending on the SPI register settings, the watchdog may be running in Window or Timeout mode and the INH/VEXT output may be active.

Normal mode can be selected from Standby mode via an SPI command (MC = 111).

7.1.1.2 Standby mode

Standby mode is the first-level power-saving mode of the UJA1168A, offering reduced current consumption. The transceiver is unable to transmit or receive data in Standby mode. The SPI remains enabled and V1 is still active; the watchdog is active (in Timeout mode) if enabled. The behavior of INH/VEXT is determined by the SPI setting.

If remote CAN wake-up is enabled (CWE = 1; see Table 38), the receiver monitors bus activity for a wake-up request. The bus pins are biased to GND (via $R_{i(cm)}$) when the bus is inactive for $t > t_{to(silence)}$ and at approximately 2.5 V when there is activity on the bus (autonomous biasing). CAN wake-up can occur via a standard wake-up pattern or via a selective wake-up frame (selective wake-up is enabled when CPNC = PNCOK = 1; otherwise standard wake-up is enabled).

Pin RXD is forced LOW when any enabled wake-up event is detected. This can be either a regular wake-up (via the CAN bus or pin WAKE) or a diagnostic wake-up such as an overtemperature event (see Section 7.11).

The UJA1168A switches to Standby mode via Reset mode:

- from Off mode if the battery voltage rises above the power-on detection threshold ($V_{th(det)pon}$)
- from Overtemp mode if the chip temperature falls below the overtemperature protection release threshold, $T_{th(rel)otp}$
- from Sleep mode on the occurrence of a regular or diagnostic wake-up event

Standby mode can also be selected from Normal mode via an SPI command (MC = 100).

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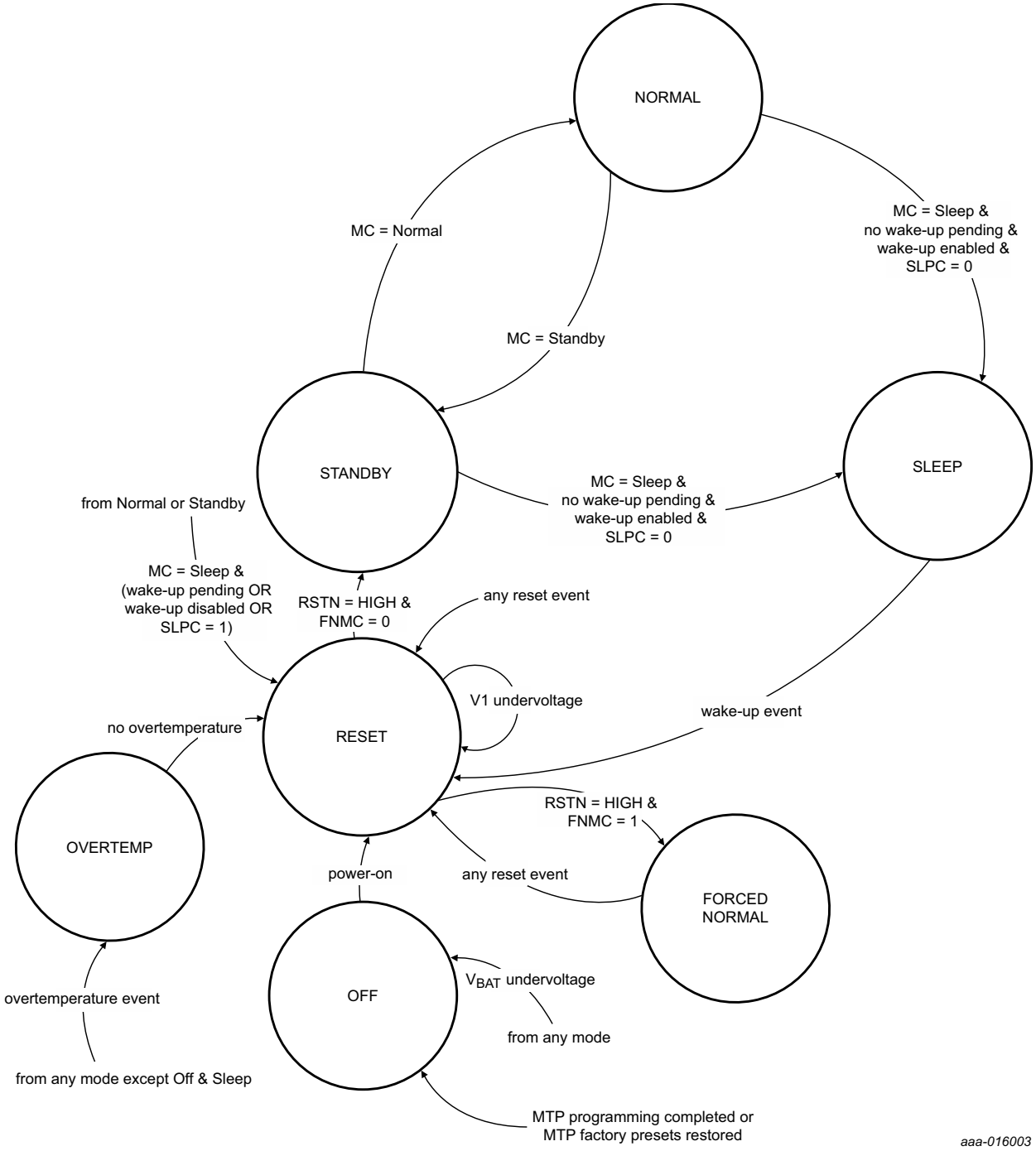

Fig 3. UJA1168A system controller state diagram

7.1.1.3 Sleep mode

Sleep mode is the second-level power-saving mode of the UJA1168A. The difference between Sleep and Standby modes is that V1 is off in Sleep mode and temperature protection is inactive.

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Any enabled regular wake-up via CAN or WAKE or any diagnostic wake-up event will cause the UJA1168A to wake up from Sleep mode. The behavior of INH/VEXT is determined by the SPI settings. The SPI is disabled. Autonomous bus biasing is active. See Table 7 for a description of watchdog behavior in Sleep mode.

Sleep mode can be selected from Normal or Standby mode via an SPI command (MC = 001). The UJA1168A will switch to Sleep mode on receipt of this command, provided there are no pending wake-up events and at least one regular wake-up source is enabled. Any attempt to enter Sleep mode while one of these conditions has not been met will cause the UJA1168A to switch to Reset mode and set the reset source status bits (RSS) to 10100 (‘illegal Sleep mode command received’; see Table 6).

Since V1 is off in Sleep mode, the only way the SBC can exit Sleep mode is via a wake-up event (see Section 7.11).

Sleep mode can be permanently disabled in applications where, for safety reasons, the supply voltage to the host controller must never be cut off. Sleep mode is permanently disabled by setting the Sleep control bit (SLPC) in the SBC configuration register (see Table 9) to 1. This register is located in the non-volatile memory area of the device. When SLPC = 1, a Sleep mode SPI command (MC = 001) triggers an SPI failure event instead of a transition to Sleep mode.

7.1.1.4 Reset mode

Reset mode is the reset execution state of the SBC. This mode ensures that pin RSTN is pulled down for a defined time to allow the microcontroller to start up in a controlled manner.

The transceiver is unable to transmit or receive data in Reset mode. The behavior of INH/VEXT is determined by the settings of bits VEXTC and VEXTSUC (see Section 7.6). The SPI is inactive; the watchdog is disabled; V1 and overtemperature detection are active.

The UJA1168A switches to Reset mode from any mode in response to a reset event (see Table 6 for a list of reset sources).

The UJA1168A exits Reset mode:

- and switches to Standby mode if pin RSTN is released HIGH
- and switches to Forced Normal mode if bit FNMC = 1
- if the SBC is forced into Off or Overtemp mode

If a V1 undervoltage event forced the transition to Reset mode, the UJA1168A will remain in Reset mode until the voltage on pin V1 has recovered.

7.1.1.5 Off mode

The UJA1168A switches to Off mode when the battery is first connected or from any mode when $V_{BAT} < V_{th(det)poff}$. Only power-on detection is enabled; all other modules are inactive. The UJA1168A starts to boot up when the battery voltage rises above the power-on detection threshold $V_{th(det)pon}$ (triggering an initialization process) and switches to Reset mode after $t_{startup}$. In Off mode, the CAN pins disengage from the bus (zero load; high-ohmic).

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7.1.1.6 Overtemp mode

Overtemp mode is provided to prevent the UJA1168A being damaged by excessive temperatures. The UJA1168A switches immediately to Overtemp mode from any mode (other than Off mode or Sleep mode) when the global chip temperature rises above the overtemperature protection activation threshold, $T_{th(act)otp}$.

To help prevent the loss of data due to overheating, the UJA1168A issues a warning when the IC temperature rises above the overtemperature warning threshold ($T_{th(warn)otp}$). When this happens, status bit OTWS is set and an overtemperature warning event is captured (OTW = 1), if enabled (OTWE = 1).

In Overtemp mode, the CAN transmitter and receiver are disabled and the CAN pins are in a high-ohmic state. No wake-up event will be detected, but a pending wake-up will still be signalled by a LOW level on pin RXD, which will persist after the overtemperature event has been cleared. V1 is off and pin RSTN is driven LOW.

VEXT is off in variants with a VEXT pin. In variants with an INH pin, INH remains unchanged when the SBC enters Overtemp mode.

The UJA1168A exits Overtemp mode:

- and switches to Reset mode if the chip temperature falls below the overtemperature protection release threshold, $T_{th(rel)otp}$
- if the device is forced to switch to Off mode ($V_{BAT} < V_{th(det)poff}$)

7.1.1.7 Forced Normal mode

Forced Normal mode simplifies SBC testing and is useful for initial prototyping and failure detection, as well as first flashing of the microcontroller. The watchdog is disabled in Forced Normal mode. The low-drop voltage regulator (V1) is active, VEXT/INH is enabled and the CAN transceiver is active.

Bit FNMC is factory preset to 1, so the UJA1168A initially boots up in Forced Normal mode (see Table 9). This allows a newly installed device to be run in Normal mode without a watchdog. So the microcontroller can be flashed via the CAN bus in the knowledge that a watchdog timer overflow will not trigger a system reset.

The register containing bit FNMC (address 74h) is stored in non-volatile memory (see Section 7.12). So once bit FNMC is programmed to 0, the SBC will no longer boot up in Forced Normal mode, allowing the watchdog to be enabled.

Even in Forced Normal mode, a reset event (e.g. an external reset or a V1 undervoltage) will trigger a transition to Reset mode with normal Reset mode behavior (except that the transmitter remains active if there is no V1 undervoltage). However, the UJA1168A will return to Forced Normal mode instead of switching to Standby mode when it exits Reset mode.

In Forced Normal mode, only the Main status register, the Watchdog status register, the Identification register and registers stored in non-volatile memory can be read. The non-volatile memory area is fully accessible for writing as long as the UJA1168A is in the factory preset state (for details see Section 7.12).

The UJA1168A switches from Reset mode to Forced Normal mode if bit FNMC = 1.

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7.1.1.8 Hardware characterization for the UJA1168A operating modes

Table 4. Hardware characterization by functional block

Block	Operating mode						
	Off	Forced Normal	Standby	Normal	Sleep	Reset	Overtemp
V1	off[1]	on	on	on	off	on	off
VEXT/INH	off	on	determined by bits VEXTC and VEXTSUC (see Table 13)	determined by bits VEXTC and VEXTSUC	determined by bits VEXTC and VEXTSUC	determined by bits VEXTC and VEXTSUC	VEXT off; INH unchanged
RSTN	LOW	HIGH	HIGH	HIGH	LOW	LOW	LOW
SPI	disabled	active	active	active	disabled	disabled	disabled
Watchdog	off	off	determined by bits WMC (see Table 8)[2]	determined by bits WMC	determined by bits WMC[2]	off	off
CAN	off	Active	Offline	Active/ Offline/ Listen-only (determined by bits CMC; see Table 15)	Offline	Offline	off
RXD	V1 level	CAN bit stream	V1 level/LOW if wake-up detected	CAN bit stream if CMC = 01/10/11; otherwise same as Standby/Sleep	V1 level/LOW if wake-up detected	V1 level/LOW if wake-up detected	V1 level/LOW if wake-up detected

[1] When the SBC switches from Reset, Standby or Normal mode to Off mode, V1 behaves as a current source during power down while V_{BAT} is between 3 V and 2 V.

[2] Window mode is only active in Normal mode.

7.1.2 System control registers

The operating mode is selected via bits MC in the Mode control register. The Mode control register is accessed via SPI address 0x01 (see Section 7.16).

Table 5. Mode control register (address 01h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:0	MC	R/W		mode control:
			001	Sleep mode
			100	Standby mode
			111	Normal mode

The Main status register can be accessed to monitor the status of the overtemperature warning flag and to determine whether the UJA1168A has entered Normal mode after initial power-up. It also indicates the source of the most recent reset event.

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Table 6. Main status register (address 03h)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	
6	OTWS	R		overtemperature warning status:
			0	IC temperature below overtemperature warning threshold
			1	IC temperature above overtemperature warning threshold
5	NMS	R		Normal mode status:
			0	UJA1168A has entered Normal mode (after power-up)
			1	UJA1168A has powered up but has not yet switched to Normal mode
4:0	RSS	R		reset source status:
			00000	exited Off mode (power-on)
			00001	CAN wake-up in Sleep mode
			00100	wake-up via WAKE pin in Sleep mode
			01100	watchdog overflow in Sleep mode (Timeout mode)
			01101	diagnostic wake-up in Sleep mode
			01110	watchdog triggered too early (Window mode)
			01111	watchdog overflow (Window mode or Timeout mode with WDF = 1)
			10000	illegal watchdog mode control access
			10001	RSTN pulled down externally
			10010	exited Overtemp mode
			10011	V1 undervoltage
			10100	illegal Sleep mode command received
			10110	wake-up from Sleep mode due to a frame detect error

7.2 Watchdog

The UJA1168A contains a watchdog that supports three operating modes: Window, Timeout and Autonomous. In Window mode (available only in SBC Normal mode), a watchdog trigger event within a closed watchdog window resets the watchdog timer. In Timeout mode, the watchdog runs continuously and can be reset at any time within the timeout time by a watchdog trigger. Watchdog timeout mode can also be used for cyclic wake-up of the microcontroller. In Autonomous mode, the watchdog can be off or in Timeout mode (see Section 7.2.4).

The watchdog mode is selected via bits WMC in the Watchdog control register (Table 8). The SBC must be in Standby mode when the watchdog mode and/or period is changed. If Window mode is selected (WMC = 100), the watchdog will remain in (or switch to) Timeout mode until the SBC enters Normal mode. Any attempt to change the watchdog operating mode (via WMC) or period (via NWP) while the SBC is in Normal mode will cause the UJA1168A to switch to Reset mode. The reset source status bits (RSS) will be set to 10000 (‘illegal watchdog mode control access’; see Table 6) and an SPI failure (SPIF) event triggered, if enabled.

Eight watchdog periods are supported, from 8 ms to 4096 ms. The watchdog period is programmed via bits NWP. The selected period is valid for both Window and Timeout modes. The default watchdog period is 128 ms.

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A watchdog trigger event resets the watchdog timer. A watchdog trigger event is any valid write access to the Watchdog control register. If the watchdog mode or the watchdog period have changed as a result of the write access, the new values are immediately valid.

Table 7. Watchdog configuration

Operating/watchdog mode						
FNMC (Forced Normal mode control)		0	0	0	0	1
SDMC (Software Development mode control)		x	x	0	1	x
WMC (watchdog mode control)		100 (Window)	010 (Timeout)	001 (Autonomous)	001 (Autonomous)	n.a.
SBC Operating Mode	Normal mode	Window	Timeout	Timeout	off	off
	Standby mode (RXD HIGH)[1]	Timeout	Timeout	off	off	off
	Standby mode (RXD LOW)[1]	Timeout	Timeout	Timeout	off	off
	Sleep mode	Timeout	Timeout	off	off	off
	Other modes	off	off	off	off	off

[1] RXD LOW signals a pending wake-up.

Table 8. Watchdog control register (address 00h)

Bit	**Symbol**	**Access**	**Value**	**Description**
7:5	WMC	R/W		watchdog mode control:
			001[1]	Autonomous mode
			010[2]	Timeout mode
			100[3]	Window mode
4	reserved	R	-	
3:0	NWP	R/W		nominal watchdog period
			1000	8 ms
			0001	16 ms
			0010	32 ms
			1011	64 ms
			0100[2]	128 ms
			1101	256 ms
			1110	1024 ms
			0111	4096 ms

[1] Default value if SDMC = 1 (see Section 7.2.1)

[2] Default value.

[3] Selected in Standby mode but only activated when the SBC switches to Normal mode.

The watchdog is a valuable safety mechanism, so it is critical that it is configured correctly. Two features are provided to prevent watchdog parameters being changed by mistake:

- redundant states of configuration bits WMC and NWP
- reconfiguration protection in Normal mode

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Redundant states associated with control bits WMC and NWP ensure that a single bit error cannot cause the watchdog to be configured incorrectly (at least two bits must be changed to reconfigure WMC or NWP). If an attempt is made to write an invalid code to WMC or NWP (e.g. 011 or 1001 respectively), the SPI operation is abandoned and an SPI failure event is captured, if enabled (see Section 7.11).

Two operating modes have a major impact on the operation of the watchdog: Forced Normal mode and Software Development mode (Software Development mode is provided for test purposes and is not an SBC operating mode; the UJA1168A can be in any mode with Software Development mode enabled; see Section 7.2.1). These modes are enabled and disabled via bits FNMC and SDMC respectively in the SBC configuration control register (see Table 9). Note that this register is located in the non-volatile memory area (see Section 7.11). In Forced Normal mode (FNM), the watchdog is completely disabled. In Software Development mode (SDM), the watchdog can be disabled or activated for test purposes.

Information on the status of the watchdog is available from the Watchdog status register (Table 10). This register also indicates whether Forced Normal and Software Development modes are active.

Table 9. SBC configuration control register (address 74h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	-	
5:4	V1RTSUC	R/W		V1 reset threshold (defined by bit V1RTC) at start-up:
			00[1]	V1 undervoltage detection at 90 % of nominal value at start-up (V1RTC = 00)
			01	V1 undervoltage detection at 80 % of nominal value at start-up (V1RTC = 01)
			10	V1 undervoltage detection at 70 % of nominal value at start-up (V1RTC = 10)
			11	V1 undervoltage detection at 60 % of nominal value at start-up (V1RTC = 11)
3	FNMC	R/W		Forced Normal mode control:
			0	Forced Normal mode disabled
			1[1]	Forced Normal mode enabled
2	SDMC	R/W		Software Development mode control:
			0[1]	Software Development mode disabled
			1	Software Development mode enabled
1	reserved	R	-	
0	SLPC	R/W		Sleep control:
			0[1]	the SBC supports Sleep mode
			1	Sleep mode commands will be ignored

[1] Factory preset value.

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Table 10. Watchdog status register (address 05h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	
3	FNMS	R	0	SBC is not in Forced Normal mode
			1	SBC is in Forced Normal mode
2	SDMS	R	0	SBC is not in Software Development mode
			1	SBC is in Software Development mode
1:0	WDS	R		watchdog status:
			00	watchdog is off
			01	watchdog is in first half of window
			10	watchdog is in second half of window
			11	reserved

7.2.1 Software Development mode

Software Development mode is provided to simplify the software design process. When Software Development mode is enabled, the watchdog starts up in Autonomous mode (WMC = 001) and is inactive after a system reset, overriding the default value (see Table 8). The watchdog is always off in Autonomous mode if Software Development mode is enabled (SDMC = 1; see Table 11).

Software can be run without a watchdog in Software Development mode. However, it is possible to activate and deactivate the watchdog for test purposes by selecting Window or Timeout mode via bits WMC while the SBC is in Standby mode (note that Window mode will only be activated when the SBC switches to Normal mode). Software Development mode is activated via bits SDMC in non-volatile memory (see Table 9).

7.2.2 Watchdog behavior in Window mode

The watchdog runs continuously in Window mode. The watchdog will be in Window mode if WMC = 100 and the UJA1168A is in Normal mode.

In Window mode, the watchdog can only be triggered during the second half of the watchdog period. If the watchdog overflows, or is triggered in the first half of the watchdog period (before $t_{trig(wd)1}$), a system reset is performed. After the system reset, the reset source (either ‘watchdog triggered too early’ or ‘watchdog overflow’) can be read via the reset source status bits (RSS) in the Main Status register (Table 6). If the watchdog is triggered in the second half of the watchdog period (after $t_{trig(wd)1}$ but before $t_{trig(wd)2}$), the watchdog timer is restarted.

7.2.3 Watchdog behavior in Timeout mode

The watchdog runs continuously in Timeout mode. The watchdog will be in Timeout mode if WMC = 010 and the UJA1168A is in Normal, Standby or Sleep mode. The watchdog will also be in Timeout mode if WMC = 100 and the UJA1168A is in Standby or Sleep mode. If Autonomous mode is selected (WMC = 001), the watchdog will be in Timeout mode if one of the conditions for Timeout mode listed in Table 11 has been satisfied.

In Timeout mode, the watchdog timer can be reset at any time by a watchdog trigger. If the watchdog overflows, a watchdog failure event (WDF) is captured. If a WDF is already pending when the watchdog overflows, a system reset is performed. In Timeout mode, the

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watchdog can be used as a cyclic wake-up source for the microcontroller when the UJA1168A is in Standby or Sleep mode. In Sleep mode, a watchdog overflow generates a wake-up event.

When the SBC is in Sleep mode with watchdog Timeout mode selected, a wake-up event is generated after the nominal watchdog period (NWP). If bit WDF is set, RXD is forced LOW and V1 is turned on. The application software can then clear the WDF bit and trigger the watchdog before it overflows.

7.2.4 Watchdog behavior in Autonomous mode

Autonomous mode is selected when WMC = 001. In Autonomous mode, the watchdog is either off or in Timeout mode, according to the conditions detailed in Table 11.

Table 11. Watchdog status in Autonomous mode

UJA1168A operating mode	Watchdog status	
	SDMC = 0	SDMC = 1
Normal	Timeout mode	off
Standby; RXD HIGH	off	off
Sleep	off	off
any other mode	off	off
Standby; RXD LOW	Timeout mode	off

When Autonomous mode is selected, the watchdog will be in Timeout mode if the SBC is in Normal mode or Standby mode with RXD LOW, provided Software Development mode has been disabled (SDMC = 0). Otherwise the watchdog will be off.

In Autonomous mode, the watchdog will not be running when the SBC is in Standby (RXD HIGH) or Sleep mode. If a wake-up event is captured, pin RXD is forced LOW to signal the event and the watchdog is automatically restarted in Timeout mode. If the SBC was in Sleep mode when the wake-up event was captured, it switches to Standby mode.

7.3 System reset

When a system reset occurs, the SBC switches to Reset mode and initiates process that generates a low-level pulse on pin RSTN.

7.3.1 Characteristics of pin RSTN

Pin RSTN is a bidirectional open drain low side driver with integrated pull-up resistance, as shown in Figure 4. With this configuration, the SBC can detect the pin being pulled down externally, e.g. by the microcontroller. The input reset pulse width must be at least $t_{w(rst)}$.

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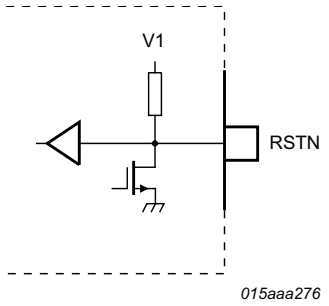

Fig 4. RSTN internal pin configuration

7.3.2 Selecting the output reset pulse width

The duration of the output reset pulse is selected via bits RLC in the Start-up control register (Table 12). The SBC distinguishes between a cold start and a warm start. A cold start is performed if the reset event was combined with a V1 undervoltage event (power-on reset, reset during Sleep mode, over-temperature reset, V1 undervoltage before entering or while in Reset mode). The output reset pulse width for a cold start is determined by the setting of bits RLC.

If any other reset event occurs without a V1 undervoltage (external reset, watchdog failure, watchdog change attempt in Normal mode, illegal Sleep mode command) the SBC uses the shortest reset length ($t_{w(rst)}$ = 1 ms to 1.5 ms). This is called a warm start of the microcontroller.

Table 12. Start-up control register (address 73h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	-	
5:4	RLC	R/W		RSTN output reset pulse width:
			00[1]	$t_{w(rst)}$ = 20 ms to 25 ms
			01	$t_{w(rst)}$ = 10 ms to 12.5 ms
			10	$t_{w(rst)}$ = 3.6 ms to 5 ms
			11	$t_{w(rst)}$ = 1 ms to 1.5 ms
3	VEXTSUC	R/W		VEXT/INH start-up control:
			0[1]	bits VEXTC set to 00 at power-up
			1	bits VEXTC set to 11 at power-up
2:0	reserved	R	-	

[1] Factory preset value.

7.3.3 Reset sources

The following events will cause the UJA1168A to switch to Reset mode:

- V_{V1} drops below the selected V1 undervoltage threshold defined by bits V1RTC
- pin RSTN is pulled down externally
- the watchdog overflows in Window mode
- the watchdog is triggered too early in Window mode (before $t_{trig(wd)1}$)
- the watchdog overflows in Timeout mode with WDF = 1 (watchdog failure pending)

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- an attempt is made to reconfigure the Watchdog control register while the SBC is in Normal mode
- the SBC leaves Off mode
- local or CAN bus wake-up in Sleep mode
- diagnostic wake-up in Sleep mode
- the SBC leaves Overtemp mode
- illegal Sleep mode command received
- wake-up from Sleep mode due to a frame detect error

7.4 Global temperature protection

The temperature of the UJA1168A is monitored continuously, except in Sleep and Off modes. The SBC switches to Overtemp mode if the temperature exceeds the overtemperature protection activation threshold, $T_{th(act)otp}$. In addition, pin RSTN is driven LOW and V1, VEXT and the CAN transceiver are switched off. When the temperature drops below the overtemperature protection release threshold, $T_{th(rel)otp}$, the SBC switches to Standby mode via Reset mode.

In addition, the UJA1168A provides an overtemperature warning. When the IC temperature rises about the overtemperature warning threshold ($T_{th(warn)otp}$), status bit OTWS is set and an overtemperature warning event is captured (OTW = 1).

7.5 Power supplies

7.5.1 Battery supply voltage (V_{BAT})

The internal circuitry is supplied from the battery via pin BAT. The device needs to be protected against negative supply voltages, e.g. by using an external series diode. If V_{BAT} falls below the power-off detection threshold, $V_{th(det)poff}$, the SBC switches to Off mode. However, the microcontroller supply voltage (V1) remains active until V_{BAT} falls below 2 V.

The SBC switches from Off mode to Reset mode $t_{startup}$ after the battery voltage rises above the power-on detection threshold, $V_{th(det)pon}$. Power-on event status bit PO is set to 1 to indicate the UJA1168A has powered up and left Off mode (see Table 32).

7.5.2 Low-drop voltage supply for 5 V microcontroller (V1)

V1 is intended to supply the microcontroller and the internal CAN transceiver and delivers up to 150 mA at 5 V. The output voltage on V1 is monitored. A system reset is generated if the voltage on V1 drops below the selected undervoltage threshold (60 %, 70 %, 80 % or 90 % of the nominal V1 output voltage, selected via V1RTC in the V1 and INH/VEXT control register; see Table 13).

The internal CAN transceiver consumes 50 mA (max) when the bus is continuously dominant, leaving 100 mA available for the external load on pin V1. In practice, the typical current consumption of the CAN transceiver is lower (≈25 mA), depending on the application, leaving more current available for the load.

The default value of the undervoltage threshold at power-up is determined by the value of bits V1RTSUC in the SBC configuration control register (Table 9). The SBC configuration control register is in non-volatile memory, allowing the user to define the undervoltage threshold (V1RTC) at start-up.

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In addition, an undervoltage warning (a V1U event; see Section 7.11) is generated if the voltage on V1 falls below 90 % of the nominal value (and V1U event detection is enabled, V1UE = 1; see Table 37). This information can be used as a warning, when the 60 %, 70 % or 80 % threshold is selected, to indicate that the level on V1 is outside the nominal supply range. The status of V1, whether it is above or below the 90 % undervoltage threshold, can be read via bit V1S in the Supply voltage status register (Table 14).

Table 13. V1 and INH/VEXT control register (address 10h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	
3:2	VEXTC[1]	R/W		VEXT/INH configuration:
			00	VEXT/INH off in all modes
			01	VEXT/INH on in Normal mode
			10	VEXT/INH on in Normal, Standby and Reset modes
			11	VEXT/INH on in Normal, Standby, Sleep and Reset modes
1:0	V1RTC[2]	R/W		set V1 reset threshold:
			00	reset threshold set to 90 % of V1 nominal output voltage
			01	reset threshold set to 80 % of V1 nominal output voltage
			10	reset threshold set to 70 % of V1 nominal output voltage
			11	reset threshold set to 60 % of V1 nominal output voltage

[1] Default value at power-up defined by setting of bits VEXTSUC (see Table 12).

[2] Default value at power-up defined by setting of bits V1RTSUC (see Table 9).

Table 14. Supply voltage status register (address 1Bh)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:1	VEXTS[1]	R		VEXT status:
			00[2]	VEXT voltage ok
			01	VEXT output voltage below undervoltage threshold
			10	VEXT output voltage above overvoltage threshold
			11	VEXT disabled
0	V1S	R		V1 status:
			0[2]	V1 output voltage above 90 % undervoltage threshold
			1	V1 output voltage below 90 % undervoltage threshold

[1] Variants with a VEXT pin only; status will always be 00 in other variants.

[2] Default value at power-up.

7.6 High voltage output and external sensor supply

Depending on the device version, pin 7 is a high voltage output (INH) or an external sensor supply (VEXT).

In the UJA1168ATK and UJA1168ATK/F, the INH pin can be used to control external devices, such as voltage regulators. Depending on the setting of bits VEXTC, pin INH will either be disabled (to disable external devices) or at a battery-related HIGH level (to

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enable external devices) in selected SBC operating modes (see Table 13). To ensure external devices are not disabled due to an overtemperature event, pin INH does not change state when the SBC switches to Overtemp mode.

In the UJA1168ATK/X and UJA1168ATK/XF, the VEXT pin is a voltage output intended to supply external components, delivering up to 30 mA at 5 V. Like INH, VEXT is also configured via bits VEXTC in the V1 and INH/VEXT control register (Table 13).

The default value of VEXTC at power-on is defined by bits VEXTSUC in non-volatile memory (see Section 7.12).

In contrast to pin INH, pin VEXT is disabled when the SBC switches to Overtemp mode. The status of VEXT can be read from the Supply voltage status register (Table 14).

7.7 High-speed CAN transceiver

The integrated high-speed CAN transceiver is designed for active communication at bit rates up to 1 Mbit/s, providing differential transmit and receive capability to a CAN protocol controller. The transceiver is ISO 11898-2:2016 compliant (defining high-speed CAN with selective wake-up functionality and autonomous biasing). The CAN transmitter is supplied from V1. The UJA1168A includes additional timing parameters on loop delay symmetry to ensure reliable communication in fast phase at data rates up to 5 Mbit/s, as used in CAN FD networks.

The CAN transceiver supports autonomous CAN biasing, which helps to minimize RF emissions. CANH and CANL are always biased to 2.5 V when the transceiver is in Active or Listen-only modes (CMC = 01/10/11).

Autonomous biasing is active in CAN Offline mode - to 2.5 V if there is activity on the bus (CAN Offline Bias mode) and to GND if there is no activity on the bus for $t > t_{to(silence)}$ (CAN Offline mode).

This is useful when the node is disabled due to a malfunction in the microcontroller or when CAN partial networking is enabled. The SBC ensures that the CAN bus is correctly biased to avoid disturbing ongoing communication between other nodes. The autonomous CAN bias voltage is derived directly from V_{BAT}.

7.7.1 CAN operating modes

The integrated CAN transceiver supports four operating modes: Active, Listen-only, Offline and Offline Bias (see Figure 5). The CAN transceiver operating mode depends on the UJA1168A operating mode and on the setting of bits CMC in the CAN control register (Table 15).

When the UJA1168A is in Normal mode, the CAN transceiver operating mode (Active, Listen-only or Offline) can be selected via bits CMC in the CAN control register (Table 15). When the UJA1168A is in Standby or Sleep modes, the transceiver is forced to Offline or Offline Bias mode (depending on bus activity).

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7.7.1.1 CAN Active mode

In CAN Active mode, the transceiver can transmit and receive data via CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data, which is output on pin RXD. The transmitter converts digital data generated by the CAN controller (input on pin TXD) into analog signals suitable for transmission over the CANH and CANL bus lines.

CAN Active mode is selected when CMC = 01 or 10. When CMC = 01, V1/CAN undervoltage detection is enabled and the transceiver will go to CAN Offline or CAN Offline Bias mode when the voltage on V1 drops below the 90 % threshold. When CMC = 10, V1/CAN undervoltage detection is disabled. The transmitter will remain active until the voltage on V1 drops below the V1 reset threshold (selected via bits V1RTC). The SBC will then switch to Reset mode and the transceiver will switch to CAN Offline or CAN Offline Bias mode.

The CAN transceiver is in Active mode when:

- the UJA1168A is in Normal mode (MC = 111) and the CAN transceiver has been enabled by setting bits CMC in the CAN control register to 01 or 10 (see Table 15) and:
  - if CMC = 01, the voltage on pin V1 is above the 90 % undervoltage threshold
  - if CMC = 10, the voltage on pin V1 is above the V1 reset threshold

If pin TXD is held LOW (e.g. by a short-circuit to GND) when CAN Active mode is selected via bits CMC, the transceiver will not enter CAN Active mode but will switch to or remain in CAN Listen-only mode. It will remain in Listen-only mode until pin TXD goes HIGH in order to prevent a hardware and/or software application failure from driving the bus lines to an unwanted dominant state.

In CAN Active mode, the CAN bias voltage is derived from V1.

The application can determine whether the CAN transceiver is ready to transmit/receive data or is disabled by reading the CAN Transceiver Status (CTS) bit in the Transceiver Status Register (Table 16).

7.7.1.2 CAN Listen-only mode

CAN Listen-only mode allows the UJA1168A to monitor bus activity while the transceiver is inactive, without influencing bus levels. This facility could be used by development tools that need to listen to the bus but do not need to transmit or receive data or for software-driven selective wake-up. Dedicated microcontrollers could be used for selective wake-up, providing an embedded low-power CAN engine designed to monitor the bus for potential wake-up events.

In Listen-only mode the CAN transmitter is disabled, reducing current consumption. The CAN receiver and CAN biasing remain active. This enables the host microcontroller to switch to a low-power mode in which an embedded CAN protocol controller remains active, waiting for a signal to wake up the microcontroller.

The CAN transceiver is in Listen-only mode when:

- the UJA1168A is in Normal mode and CMC = 11

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The CAN transceiver will not leave Listen-only mode while TXD is LOW or CAN Active mode is selected with CMC = 01 while the voltage on V1 is below the 90 % undervoltage threshold.

7.7.1.3 CAN Offline and Offline Bias modes

In CAN Offline mode, the transceiver monitors the CAN bus for a wake-up event, provided CAN wake-up detection is enabled (CWE = 1). CANH and CANL are biased to GND.

CAN Offline Bias mode is the same as CAN Offline mode, with the exception that the CAN bus is biased to 2.5 V. This mode is activated automatically when activity is detected on the CAN bus while the transceiver is in CAN Offline mode. The transceiver will return to CAN Offline mode if the CAN bus is silent (no CAN bus edges) for longer than $t_{to(silence)}$.

The CAN transceiver switches to CAN Offline mode from CAN Active mode or CAN Listen-only mode if:

- the SBC switches to Reset or Standby or Sleep mode OR
- the SBC is in Normal mode and CMC = 00

provided the CAN-bus has been inactive for at least $t_{to(silence)}$. If the CAN-bus has been inactive for less than $t_{to(silence)}$, the CAN transceiver switches first to CAN Offline Bias mode and then to CAN Offline mode once the bus has been silent for $t_{to(silence)}$.

The CAN transceiver switches to CAN Offline/Offline Bias mode from CAN Active mode if CMC = 01 and the voltage on V1 drops below the 90 % undervoltage threshold or CMC = 10 and the voltage on V1 drops below the V1 reset threshold.

The CAN transceiver switches to CAN Offline mode:

- from CAN Offline Bias mode if no activity is detected on the bus (no CAN edges) for $t > t_{to(silence)}$ OR
- when the SBC switches from Off or Overtemp mode to Reset mode

The CAN transceiver switches from CAN Offline mode to CAN Offline Bias mode if:

- a standard wake-up pattern is detected on the CAN bus OR
- the SBC is in Normal mode, CMC = 01 or 10 and $V_{V1} < 90$ %

7.7.1.4 CAN Off mode

The CAN transceiver is switched off completely with the bus lines floating when:

- the SBC switches to Off or Overtemp mode OR
- V_{BAT} falls below the CAN receiver undervoltage detection threshold, $V_{uvd(CAN)}$

It will be switched on again on entering CAN Offline mode when V_{BAT} rises above the undervoltage recovery threshold ($V_{uvr(CAN)}$) and the SBC is no longer in Off/Overtemp mode. CAN Off mode prevents reverse currents flowing from the bus when the battery supply to the SBC is lost.

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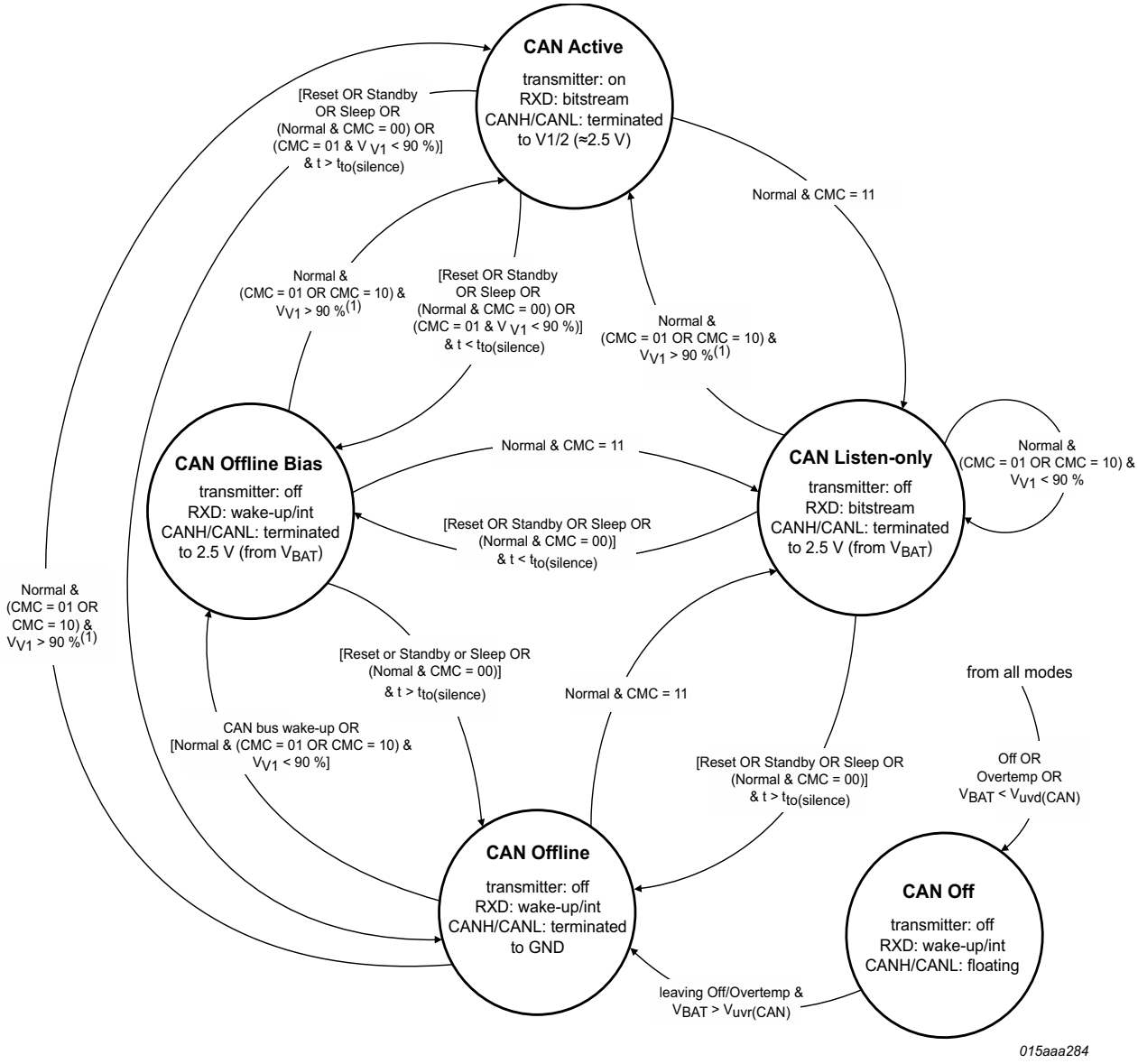

(1) To prevent the bus lines being driven to a permanent dominant state, the transceiver will not switch to CAN Active mode or CAN Listen-only mode if pin TXD is held LOW (e.g. by a short-circuit to GND)

Fig 5. CAN transceiver state machine (with FNMC = 0)

7.7.2 CAN standard wake-up (partial networking not enabled)

If the CAN transceiver is in Offline mode and CAN wake-up is enabled (CWE = 1), but CAN selective wake-up is disabled (CPNC = 0 or PNCOK = 0), the UJA1168A will monitor the bus for a wake-up pattern.

A filter at the receiver input prevents unwanted wake-up events occurring due to automotive transients or EMI. A dominant-recessive-dominant wake-up pattern must be transmitted on the CAN bus within the wake-up timeout time ($t_{to(wake)}$) to pass the wake-up

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filter and trigger a wake-up event (see Figure 6; note that additional pulses may occur between the recessive/dominant phases). The recessive and dominant phases must last at least $t_{wake(busrec)}$ and $t_{wake(busdom)}$, respectively.

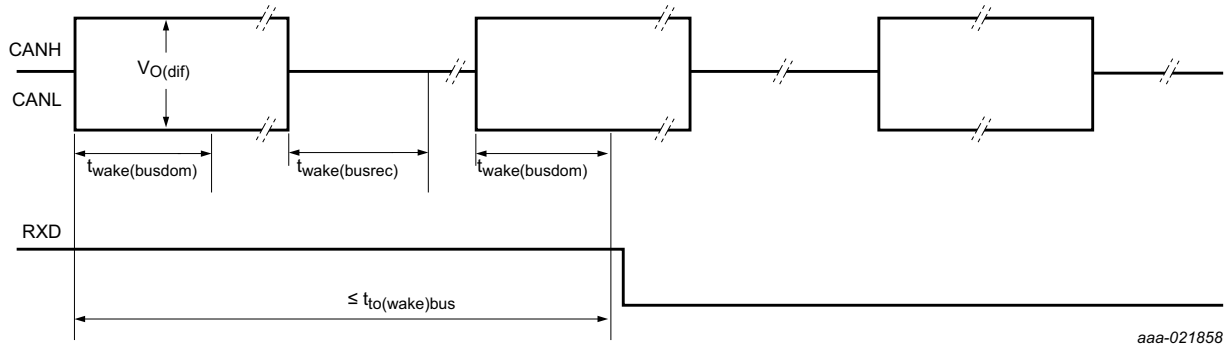

Fig 6. CAN wake-up timing

When a valid CAN wake-up pattern is detected on the bus, wake-up bit CW in the Transceiver event status register is set (see Table 34) and pin RXD is driven LOW. If the SBC was in Sleep mode when the wake-up pattern was detected, V1 is enabled to supply the microcontroller and the SBC switches to Standby mode via Reset mode.

7.7.3 CAN control and Transceiver status registers

Table 15. CAN control register (address 20h)

Bit	Symbol	Access	Value	Description
7	reserved	R/W	-	
6	CFDC	R/W		CAN FD tolerance (UJA1168ATK/F and UJA1168ATK/XF only; otherwise ignored)
			0	CAN FD tolerance disabled
			1	CAN FD tolerance enabled
5	PNCOK	R/W		CAN partial networking configuration registers:
			0	partial networking register configuration invalid (wake-up via standard wake-up pattern only)
			1	partial networking registers configured successfully
4	CPNC	R/W		CAN selective wake-up; when enabled, node is part of a partial network:
			0	disable CAN selective wake-up
			1	enable CAN selective wake-up
3:2	reserved	R	-	
1:0	CMC	R/W		CAN transceiver operating mode selection (available when UJA1168A is in Normal mode; MC = 111):
			00	Offline mode
			01	Active mode; see Section 7.7.1.1 and Section 7.7.1.3
			10	Active mode; see Section 7.7.1.1 and Section 7.7.1.3
			11	Listen-only mode

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Table 16. Transceiver status register (address 22h)

Bit	Symbol	Access	Value	Description
7	CTS	R	0	CAN transceiver not in Active mode
			1	CAN transceiver in Active mode
6	CPNERR	R	0	no CAN partial networking error detected (PNFDE = 0 AND PNCOK = 1)
			1	CAN partial networking error detected (PNFDE = 1 OR PNCOK = 0; wake-up via standard wake-up pattern only)
5	CPNS	R	0	CAN partial networking configuration error detected (PNCOK = 0)
			1	CAN partial networking configuration ok (PNCOK = 1)
4	COSCS	R	0	CAN partial networking oscillator not running at target frequency
			1	CAN partial networking oscillator running at target frequency
3	CBSS	R	0	CAN bus active (communication detected on bus)
			1	CAN bus inactive (for longer than $t_{to(silence)}$)
2	reserved	R	-	
1	VCS[1]	R	0	the output voltage on V1 is above the 90 % threshold
			1	the output voltage on V1 is below the 90 % threshold
0	CFS	R	0	no TXD dominant timeout event detected
			1	CAN transmitter disabled due to a TXD dominant timeout event

[1] Only active when CMC = 01.

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7.8 CAN partial networking

Partial networking allows nodes in a CAN network to be selectively activated in response to dedicated wake-up frames (WUF). Only nodes that are functionally required are active on the bus while the other nodes remain in a low-power mode until needed.

If both CAN wake-up (CWE = 1) and CAN selective wake-up (CPNC = 1) are enabled, and the partial networking registers are configured correctly (PNCOK = 1), the transceiver monitors the bus for dedicated CAN wake-up frames.

7.8.1 Wake-up frame (WUF)

A wake-up frame is a CAN frame according to ISO11898-1:2015, consisting of an identifier field (ID), a Data Length Code (DLC), a data field and a Cyclic Redundancy Check (CRC) code including the CRC delimiter.

The wake-up frame format, standard (11-bit) or extended (29-bit) identifier, is selected via bit IDE in the Frame control register (Table 26).

A valid WUF identifier is defined and stored in the ID registers (Table 18 to Table 21). An ID mask can be defined to allow a group of identifiers to be recognized as valid by an individual node. The identifier mask is defined in the ID mask registers (Table 22 to Table 25), where a 1 means ‘don’t care’.

In the example illustrated in Figure 7, based on the standard frame format, the 11-bit identifier is defined as 0x1A0. The identifier is stored in ID registers 2 and 3 (Table 20 and Table 21). The three least significant bits of the ID mask (bits 2 to 4 of ID mask register 2; Table 24) are ‘don’t care’. This means that any of eight different identifiers will be recognized as valid in the received WUF (from 0x1A0 to 0x1A7).

Fig 7. Evaluating the ID field in a selective wake-up frame

The data field indicates the nodes to be woken up. Within the data field, groups of nodes can be predefined and associated with bits in a data mask. By comparing the incoming data field with the data mask, multiple groups of nodes can be woken up simultaneously with a single wake-up message.

The data length code (bits DLC in the Frame control register; Table 26) determines the number of data bytes (between 0 and 8) expected in the data field of a CAN wake-up frame. If one or more data bytes are expected (DLC ≠ 0000), at least one bit in the data

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field of the received wake-up frame must be set to 1 and at least one equivalent bit in the associated data mask register in the transceiver (see Table 27) must also be set to 1 for a successful wake-up. Each matching pair of 1s indicates a group of nodes to be activated (since the data field is up to 8 bytes long, up to 64 groups of nodes can be defined). If DLC = 0, a data field is not expected.

In the example illustrated in Figure 8, the data field consists of a single byte (DLC = 1). This means that the data field in the incoming wake-up frame is evaluated against data mask 7 (stored at address 6Fh; see Table 27 and Figure 9). Data mask 7 is defined as 10101000 in the example, indicating that the node is assigned to three groups (Group1, Group 3 and Group 5).

The received message shown in Figure 8 could, potentially, wake up four groups of nodes: groups 2, 3, 4 and 5. Two matches are found (groups 3 and 5) when the message data bits are compared with the configured data mask (DM7).

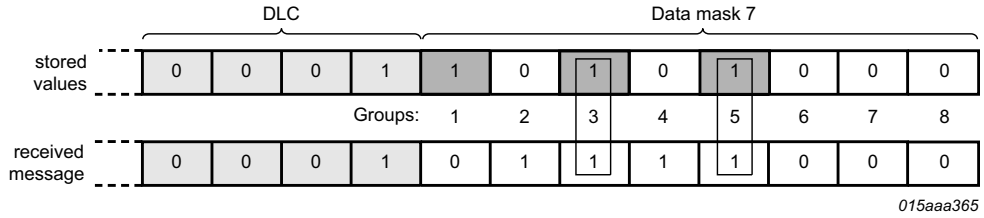

Fig 8. Evaluating the Data field in a selective wake-up frame

Optionally, the data length code and the data field can be excluded from the evaluation of the wake-up frame. If bit PNDM = 0, only the identifier field is evaluated to determine if the frame contains a valid wake-up message. If PNDM = 1 (the default value), the data field is included for wake-up filtering.

When PNDM = 0, a valid wake-up message is detected and a wake-up event is captured (and CW is set to 1) when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error

When PNDM = 1, a valid wake-up message is detected when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- the frame is not a Remote frame AND
- the data length code in the received message matches the configured data length code (bits DLC) AND
- if the data length code is greater than 0, at least one bit in the data field of the received frame is set and the corresponding bit in the associated data mask register is also set AND
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error

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If the UJA1168A receives a CAN message containing errors (e.g. a ‘stuffing’ error) that are transmitted in advance of the ACK field, an internal error counter is incremented. If a CAN message is received without any errors appearing in front of the ACK field, the counter is decremented. Data received after the CRC delimiter and before the next SOF is ignored by the partial networking module. If the counter overflows (counter > 31), a frame detect error is captured (PNFDE = 1) and the device wakes up; the counter is reset to zero when the bias is switched off and partial networking is re-enabled.

Partial networking is assumed to be configured correctly when PNCOK is set to 1 by the application software. The UJA1168A clears PNCOK after a write access to any of the CAN partial networking configuration registers (see Section 7.8.3).

If selective wake-up is disabled (CPNC = 0) or partial networking is not configured correctly (PNCOK = 0), and the CAN transceiver is in Offline mode with wake-up enabled (CWE = 1), then any valid wake-up pattern according to ISO 11898-2:2016 will trigger a wake-up event.

If the CAN transceiver is not in Offline mode (CMC $\neq$ 00) or CAN wake-up is disabled (CWE = 0), all wake-up patterns on the bus will be ignored.

CAN bit rates of 50kbit/s, 100kbit/s, 125kbit/s, 250kbit/s, 500kbit/s and 1Mbit/s are supported during selective wake-up. The bit rate is selected via bits CDR (see Table 17).

7.8.2 CAN FD frames

CAN FD stands for ‘CAN with Flexible Data-Rate’. It is based on the CAN protocol as specified in ISO 11898-1:2015.

CAN FD is being gradually introduced into automotive market. In time, all CAN controllers will be required to comply with the new standard (enabling ‘FD-active’ nodes) or at least to tolerate CAN FD communication (enabling ‘FD-passive’ nodes). The UJA1168ATK/F and UJA1168ATK/XF variants support FD-passive features by means of a dedicated implementation of the partial networking protocol.

These variants can be configured to recognize CAN FD frames as valid frames. When CFDC = 1, the error counter is decremented every time the control field of a CAN FD frame is received. The UJA1168A remains in low-power mode (CAN FD-passive) with partial networking enabled. CAN FD frames are never recognized as valid wake-up frames, even if PNDM = 0 and the frame contains a valid ID. After receiving the control field of a CAN FD frame, the UJA1168A ignores further bus signals until idle is again detected.

CAN FD passive is supported up to a ratio of one-to-eight between arbitration and data bit rates, without unwanted wake-ups. The CAN FD filter parameter defined in ISO 11898-2:2016 and SAE J2284 is supported up to a ratio of one-to-four, with a maximum supported bit data bit rate of 2 Mbit/s and a maximum arbitration speed of 500 kbit/s.

CAN FD frames are interpreted as frames with errors by the partial networking module in the UJA1168ATK and UJA1168ATK/X, and in the CAN FD variants when CFDC = 0. So the error counter is incremented when a CAN FD frame is received. If the ratio of CAN FD frames to valid CAN frames exceeds the threshold that triggers error counter overflow, bit PNFDE is set to 1 and the device wakes up.

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7.8.3 CAN partial networking configuration registers

Dedicated registers are provided for configuring CAN partial networking.

Table 17. Data rate register (address 26h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:0	CDR	R/W		CAN data rate selection:
			000	50 kbit/s
			001	100 kbit/s
			010	125 kbit/s
			011	250 kbit/s
			100	reserved (intended for future use; currently selects 500 kbit/s)
			101	500 kbit/s
			110	reserved (intended for future use; currently selects 500 kbit/s)
			111	1000 kbit/s

Table 18. ID register 0 (address 27h)

Bit	Symbol	Access	Value	Description
7:0	ID07:ID00	R/W	-	bits ID07 to ID00 of the extended frame format

Table 19. ID register 1 (address 28h)

Bit	Symbol	Access	Value	Description
7:0	ID15:ID08	R/W	-	bits ID15 to ID08 of the extended frame format

Table 20. ID register 2 (address 29h)

Bit	Symbol	Access	Value	Description
7:2	ID23:ID18	R/W	-	bits ID23 to ID18 of the extended frame format bits ID05 to ID00 of the standard frame format
1:0	ID17:ID16	R/W	-	bits ID17 to ID16 of the extended frame format

Table 21. ID register 3 (address 2Ah)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	
4:0	ID28:ID24	R/W	-	bits ID28 to ID24 of the extended frame format bits ID10 to ID06 of the standard frame format

Table 22. ID mask register 0 (address 2Bh)

Bit	Symbol	Access	Value	Description
7:0	M07:M00	R/W	-	mask bits ID07 to ID00 of the extended frame format

Table 23. ID mask register 1 (address 2Ch)

Bit	Symbol	Access	Value	Description
7:0	M15:M08	R/W	-	mask bits ID15 to ID08 of the extended frame format

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Table 24. ID mask register 2 (address 2Dh)

Bit	Symbol	Access	Value	Description
7:2	M23:M18	R/W	-	mask bits ID23 to ID18 of the extended frame format mask bits ID05 to ID00 of the standard frame format
1:0	M17:M16	R/W	-	mask bits ID17 to ID16 of the extended frame format

Table 25. ID mask register 3 (address 2Eh)

Bit	Symbol	Access	Value	Description
7:5	reserved	R		
4:0	M28:M24	R/W	-	mask bits ID28 to ID24 of the extended frame format mask. bits ID10 to ID06 of the standard frame format

Table 26. Frame control register (address 2Fh)

Bit	Symbol	Access	Value	Description
7	IDE	R/W	-	identifier format:
			0	standard frame format (11-bit)
			1	extended frame format (29-bit)
6	PNDM	R/W	-	partial networking data mask:
			0	data length code and data field are ‘don’t care’ for wake-up
			1	data length code and data field are evaluated at wake-up
5:4	reserved	R	-	
3:0	DLC	R/W		number of data bytes expected in a CAN frame:
			0000	0
			0001	1
			0010	2
			0011	3
			0100	4
			0101	5
			0110	6
			0111	7
			1000	8
			1001 to 1111	tolerated, 8 bytes expected

Table 27. Data mask registers (addresses 68h to 6Fh)

Addr.	Bit	Symbol	Access	Value	Description
68h	7:0	DM0	R/W	-	data mask 0 configuration
69h	7:0	DM1	R/W	-	data mask 1 configuration
6Ah	7:0	DM2	R/W	-	data mask 2 configuration
6Bh	7:0	DM3	R/W	-	data mask 3 configuration
6Ch	7:0	DM4	R/W	-	data mask 4 configuration

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Table 27. Data mask registers (addresses 68h to 6Fh) *…continued*

Addr.	Bit	Symbol	Access	Value	Description
6Dh	7:0	DM5	R/W	-	data mask 5 configuration
6Eh	7:0	DM6	R/W	-	data mask 6 configuration
6Fh	7:0	DM7	R/W	-	data mask 7 configuration

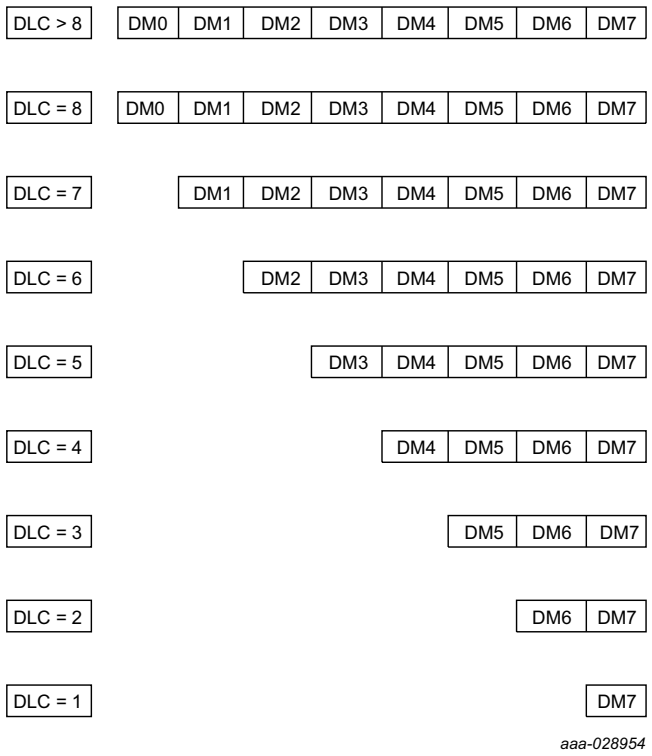

Fig 9. Data mask register usage for different values of DLC

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7.9 CAN fail-safe features

7.9.1 TXD dominant timeout

A TXD dominant time-out timer is started when pin TXD is forced LOW while the transceiver is in CAN Active Mode. If the LOW state on pin TXD persists for longer than the TXD dominant time-out time ($t_{to(dom)TXD}$), the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD goes HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 4.4 kbit/s.

When the TXD dominant time-out time is exceeded, a CAN failure event is captured (CF = 1; see Table 34), if enabled (CFE = 1; see Table 38). In addition, the status of the TXD dominant timeout can be read via the CFS bit in the Transceiver status register (Table 16) and bit CTS is cleared.

7.9.2 Pull-up on TXD pin

Pin TXD has an internal pull-up towards V1 to ensure a safe defined recessive driver state in case the pin is left floating.

7.9.3 V1 undervoltage event

When CMC = 01, a CAN failure event is captured (CF = 1) and status bit VCS is set to 1 when the supply to the CAN transceiver (V_{V1}) falls below 90 % of its nominal value (assuming CAN failure detection is enabled; CFE = 1).

7.9.4 Loss of power at pin BAT

A loss of power at pin BAT has no influence on the bus lines or on the microcontroller. No reverse currents will flow from the bus.

7.10 Local wake-up via WAKE pin

Local wake-up is enabled via bits WPRE and WPFE in the WAKE pin event capture enable register (see Table 39). A wake-up event is triggered by a LOW-to-HIGH (if WPRE = 1) and/or a HIGH-to-LOW (if WPFE = 1) transition on the WAKE pin. This arrangement allows for maximum flexibility when designing a local wake-up circuit. In applications that don't make use of the local wake-up facility, local wake-up should be disabled and the WAKE pin connected to GND to ensure optimal EMI performance.

Table 28. WAKE status register (address 4Bh)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	
1	WPVS	R		WAKE pin status:
			0	voltage on WAKE pin below switching threshold ($V_{th(sw)}$)
			1	voltage on WAKE pin above switching threshold ($V_{th(sw)}$)
0	reserved	R	-	

While the SBC is in Normal mode, the status of the voltage on pin WAKE can always be read via bit WPVS. Otherwise, WPVS is only valid if local wake-up is enabled (WPRE = 1 and/or WPFE = 1).

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7.11 Wake-up and interrupt event diagnosis via pin RXD

Wake-up and interrupt event diagnosis in the UJA1168A is intended to provide the microcontroller with information on the status of a range of features and functions. This information is stored in the event status registers (Table 32 to Table 34) and is signaled on pin RXD, if enabled.

A distinction is made between regular wake-up events and interrupt events (at least one regular wake-up source must be enabled to allow the UJA1168A to switch to Sleep mode; see Section 7.1.1.3).

Table 29. Regular events

Symbol	Event	Power-on	Description
CW	CAN wake-up	disabled	a CAN wake-up event was detected while the transceiver was in CAN Offline mode.
WPR	rising edge on WAKE pin	disabled	a rising-edge wake-up was detected on pin WAKE
WPF	falling edge on WAKE pin	disabled	a falling-edge wake-up was detected on pin WAKE

Table 30. Diagnostic events

Symbol	Event	Power-on	Description
PO	power-on	always enabled	the UJA1168A has exited Off mode (after battery power has been restored/connected)
OTW	overtemperature warning	disabled	the IC temperature has exceeded the overtemperature warning threshold (not in Sleep mode)
SPIF	SPI failure	disabled	SPI clock count error (only 16-, 24- and 32-bit commands are valid), illegal WMC, NWP or MC code or attempted write access to locked register (not in Sleep mode)
WDF	watchdog failure	always enabled	watchdog overflow in Window or Timeout mode or watchdog triggered too early in Window mode; a system reset is triggered immediately in response to a watchdog failure in Window mode; when the watchdog overflows in Timeout mode, a system reset is only performed if a WDF is already pending (WDF = 1)
VEXTO[1]	VEXT overvoltage	disabled	VEXT overvoltage detected
VEXTU[1]	VEXT undervoltage	disabled	VEXT undervoltage detected
V1U	V1 undervoltage	disabled	voltage on V1 has dropped below the 90 % undervoltage threshold when V1 is active (event is not captured in Sleep mode because V1 is off). V1U event capture is independent of the setting of bits V1RTC.
PNFDE	PN frame detection error	always enabled	partial networking frame detection error
CBS	CAN bus silence	disabled	no activity on CAN bus for $t_{to(silence)}$ (detected only when CBSE = 1 while bus active)
CF	CAN failure	disabled	one of the following CAN failure events detected: - CAN transceiver deactivated due to a V1 undervoltage - CAN transceiver deactivated due to a dominant clamped TXD (not in Sleep mode)

[1] UJA1168ATK/X and UJA1168ATK/XF only.

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PO, WDF and PNFDE interrupts are always captured. Wake-up and interrupt detection can be enabled/disabled for the remaining events individually via the event capture enable registers (Table 36 to Table 38).

If an event occurs while the associated event capture function is enabled, the relevant event status bit is set. If the transceiver is in CAN Offline mode with V1 active (SBC Normal or Standby mode), pin RXD is forced LOW to indicate that a wake-up or interrupt event has been detected. If the UJA1168A is in sleep mode when the event occurs, the microcontroller supply, V1, is activated and the SBC switches to Standby mode (via Reset mode).

The microcontroller can monitor events via the event status registers. An extra status register, the Global event status register (Table 31), is provided to help speed up software polling routines. By polling the Global event status register, the microcontroller can quickly determine the type of event captured (system, supply, transceiver or WAKE pin) and then query the relevant table (Table 32, Table 33, Table 34 or Table 35 respectively).

After the event source has been identified, the status flag should be cleared (set to 0) by writing 1 to the relevant bit (writing 0 will have no effect). A number of status bits can be cleared in a single write operation by writing 1 to all relevant bits.

It is strongly recommended to clear only the status bits that were set to 1 when the status registers were last read. This precaution ensures that events triggered just before the write access are not lost.

7.11.1 Interrupt/wake-up delay

If interrupt or wake-up events occur very frequently while the transceiver is in CAN Offline mode, they can have a significant impact on the software processing time (because pin RXD is repeatedly driven LOW, requiring a response from the microcontroller each time an interrupt/wake-up is generated). The UJA1168A incorporates an event delay timer to limit the disturbance to the software.

When one of the event capture status bits is cleared, pin RXD is released (HIGH) and a timer is started. If further events occur while the timer is running, the relevant status bits are set. If one or more events are pending when the timer expires after $t_{d(event)}$, pin RXD goes LOW again to alert the microcontroller.

In this way, the microcontroller is interrupted once to process a number of events rather than several times to process individual events.

If all events are cleared while the timer is running, RXD remains HIGH after the timer expires, since there are no pending events. The event capture registers can be read at any time.

The event capture delay timer is stopped immediately when pin RSTN goes low (triggered by a HIGH-to-LOW transition on the pin). RSTN is driven LOW when the SBC enters Reset, Sleep, Overtemp and Off modes. A pending event is signaled on pin RXD when the SBC enters Sleep mode.

7.11.2 Sleep mode protection

The wake-up event capture function is critical when the UJA1168A is in Sleep mode, because the SBC will only leave Sleep mode in response to a captured wake-up event. To avoid potential system deadlocks, the SBC distinguishes between regular and diagnostic

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events (see Section 7.11). Wake-up events (via the CAN bus or the WAKE pin) are classified as regular events; diagnostic events signal failure/error conditions or state changes. At least one regular wake-up event must be enabled before the UJA1168A can switch to Sleep mode. Any attempt to enter Sleep mode while all regular wake-up events are disabled will trigger a system reset.

Another condition that must be satisfied before the UJA1168A can switch to Sleep mode is that all event status bits must be cleared. If an event is pending when the SBC receives a Sleep mode command (MC = 001), it will immediately switch to Reset mode. This condition applies to both regular and diagnostic events.

Sleep mode can be permanently disabled in applications where, for safety reasons, the supply voltage to the host controller must never be cut off. Sleep mode is permanently disabled by setting the Sleep control bit (SLPC) in the SBC configuration register (see Table 9) to 1. This register is located in the non-volatile memory area of the device. When SLPC = 1, a Sleep mode SPI command (MC = 001) will trigger an SPI failure event instead of a transition to Sleep mode.

7.11.3 Event status and event capture registers

After an event source has been identified, the status flag should be cleared (set to 0) by writing 1 to the relevant status bit (writing 0 will have no effect).

Table 31. Global event status register (address 60h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	
3	WPE	R	0	no pending WAKE pin event
			1	WAKE pin event pending at address 0x64
2	TRXE	R	0	no pending transceiver event
			1	transceiver event pending at address 0x63
1	SUPE	R	0	no pending supply event
			1	supply event pending at address 0x62
0	SYSE	R	0	no pending system event
			1	system event pending at address 0x61

Table 32. System event status register (address 61h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	
4	PO	R/W	0	no recent power-on
			1	the UJA1168A has left Off mode after power-on
3	reserved	R	-	
2	OTW	R/W	0	overtemperature not detected
			1	the global chip temperature has exceeded the overtemperature warning threshold ($T_{th(warn)otp}$)
1	SPIF	R/W	0	no SPI failure detected
			1	SPI failure detected
0	WDF	R/W	0	no watchdog failure event captured
			1	watchdog failure event captured

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Table 33. Supply event status register (address 62h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2	VEXTO[1]	R/W	0	no VEXT overvoltage event captured
			1	VEXT overvoltage event captured
1	VEXTU[1]	R/W	0	no VEXT undervoltage event captured
			1	VEXT undervoltage event captured
0	V1U	R/W	0	no V1 undervoltage event captured
			1	V1 undervoltage event captured

[1] Variants with a VEXT pin only; reserved in other variants.

Table 34. Transceiver event status register (address 63h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	-	
5	PNFDE	R/W	0	no partial networking frame detection error detected
			1	partial networking frame detection error detected
4	CBS	R/W	0	CAN bus active
			1	no activity on CAN bus for $t_{to(silence)}$
3:2	reserved	R	-	
1	CF	R/W	0	no CAN failure detected
			1	(CMC = 01 & CAN transceiver deactivated due to V1 undervoltage) OR dominant clamped TXD
0	CW	R/W	0	no CAN wake-up event detected
			1	CAN wake-up event detected while the transceiver is in CAN Offline Mode

Table 35. WAKE pin event capture status register (address 64h)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	
1	WPR	R/W	0	no rising edge detected on WAKE pin
			1	rising edge detected on WAKE pin
0	WPF	R/W	0	no falling edge detected on WAKE pin
			1	falling edge detected on WAKE pin

Table 36. System event capture enable register (address 04h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2	OTWE	R/W		overtemperature warning event capture:
			0	overtemperature warning disabled
			1	overtemperature warning enabled

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Table 36. System event capture enable register (address 04h)

Bit	Symbol	Access	Value	Description
1	SPIFE	R/W		SPI failure detection:
			0	SPI failure detection disabled
			1	SPI failure detection enabled
0	reserved	R	-	

Table 37. Supply event capture enable register (address 1Ch)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2	VEXTOE[1]	R/W		VEXT overvoltage detection:
			0	VEXT overvoltage detection disabled
			1	VEXT overvoltage detection enabled
1	VEXTUE[1]	R/W		VEXT undervoltage detection:
			0	VEXT undervoltage detection disabled
			1	VEXT undervoltage detection enabled
0	V1UE	R/W		V1 undervoltage detection:
			0	V1 undervoltage detection disabled
			1	V1 undervoltage detection enabled

[1] Variants with a VEXT pin only; reserved in other variants.

Table 38. Transceiver event capture enable register (address 23h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	
4	CBSE	R/W		CAN bus silence detection:
			0	CAN bus silence detection disabled
			1	CAN bus silence detection enabled
3:2	reserved	R	-	
1	CFE	R/W		CAN failure detection
			0	CAN failure detection disabled
			1	CAN failure detection enabled
0	CWE	R/W		CAN wake-up detection:
			0	CAN wake-up detection disabled
			1	CAN wake-up detection enabled

Table 39. WAKE pin event capture enable register (address 4Ch)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	
1	WPRE	R/W		rising-edge detection on WAKE pin:
			0	rising-edge detection on WAKE pin disabled
			1	rising-edge detection on WAKE pin enabled

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Table 39. WAKE pin event capture enable register (address 4Ch) *…continued*

Bit	Symbol	Access	Value	Description
0	WPFE	R/W		falling-edge detection on WAKE pin:
			0	falling-edge detection on WAKE pin disabled
			1	falling-edge detection on WAKE pin enabled

7.12 Non-volatile SBC configuration

The UJA1168A contains Multiple Time Programmable Non-Volatile (MTPNV) memory cells that allow some of the default device settings to be reconfigured. The MTPNV memory address range is from 0x73 to 0x74. An overview of the MTPNV registers is given in Table 40.

Table 40. Overview of MTPNV registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x73	Start-up control (see Table 12)	reserved		RLC		VEXTSUC	reserved		
0x74	SBC configuration control (see Table 9)	reserved		V1RTSUC		FNMC	SDMC	reserved	SLPC

7.12.1 Programming MTPNV cells

The UJA1168A must be in Forced Normal mode and the MTPNV cells must contain the factory preset values before the non-volatile memory can be reprogrammed. The UJA1168A will switch to Forced Normal mode after a reset event (e.g. pin RSTN LOW) when the MTPNV cells contain the factory preset values (since FNMC = 1).

The factory presets may need to be restored before reprogramming can begin (see Section 7.12.2). When the factory presets have been restored, a system reset is generated automatically and UJA1168A switches to Forced Normal mode. This ensures that the programming cycle cannot be interrupted by the watchdog.

Programming of the non-volatile memory registers is performed in two steps. First, the required values are written to addresses 0x73 and 0x74. In the second step, reprogramming is confirmed by writing the correct CRC value to the MTPNV CRC control register (see Section 7.12.1.1). The SBC starts reprogramming the MTPNV cells as soon as the CRC value has been validated. If the CRC value is not correct, reprogramming is aborted. On completion, a system reset is generated to indicate that the MTPNV cells have been reprogrammed successfully. Note that the MTPNV cells cannot be read while they are being reprogrammed.

After an MTPNV programming cycle has been completed, the non-volatile memory is protected from being overwritten via a standard SPI write operation.

The MTPNV cells can be reprogrammed a maximum of 200 times ($N_{cy(W)MTP}$; see Table 59). Bit NVMPS in the MTPNV status register (Table 41) indicates whether the non-volatile cells can be reprogrammed. This register also contains a write counter, WRCNTS, that is incremented each time the MTPNV cells are reprogrammed (up to a maximum value of 111111; there is no overflow; performing a factory reset also increments the counter). This counter is provided for information purposes only; reprogramming will not be rejected when it reaches its maximum value.

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An error correction code status bit, ECCS, is set to indicate that the CRC check mechanism in the SBC has detected a single bit failure in non-volatile memory. If more than one bit failure is detected, the SBC will not restart after MTPNV reprogramming. Check the ECCS flag at the end of the production cycle to verify the content of non-volatile memory. When this flag is set, it indicates a device or ECU failure.

Table 41. MTPNV status register (address 70h)

Bit	Symbol	Access	Value	Description
7:2	WRCNTS	R		write counter status:
			xxxxxx	contains the number of times the MTPNV cells were reprogrammed
1	ECCS	R		error correction code status:
			0	no bit failure detected in non-volatile memory
			1	bit failure detected and corrected in non-volatile memory
0	NVMPS	R		non-volatile memory programming status:
			0	MTPNV memory cannot be overwritten
			1[1]	MTPNV memory is ready to be reprogrammed

[1] Factory preset value.

7.12.1.1 Calculating the CRC value for MTP programming

The cyclic redundancy check value stored in bits CRCC in the MTPNV CRC control register is calculated using the data written to registers 0x73 and 0x74.

Table 42. MTPNV CRC control register (address 75h)

Bit	Symbol	Access	Value	Description
7:0	CRCC	R/W	-	CRC control data

The CRC value is calculated using the data representation shown in Figure 10 and the modulo-2 division with the generator polynomial: $X^8 + X^5 + X^3 + X^2 + X + 1$. The result of this operation must be bitwise inverted.

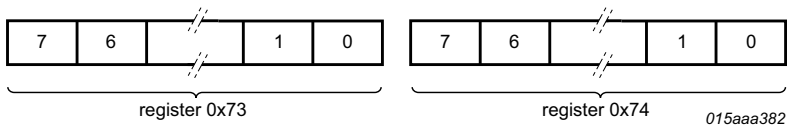

Fig 10. Data representation for CRC calculation

The following parameters can be used to calculate the CRC value (e.g. via the Autosar method):

Table 43. Parameters for CRC coding

Parameter	Value
CRC result width	8 bits
Polynomial	0x2F
Initial value	0xFF

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Table 43. Parameters for CRC coding

Parameter	Value
Input data reflected	no
Result data reflected	no
XOR value	0xFF

Alternatively, the following algorithm can be used:

```
data = 0   // unsigned byte
crc = 0xFF
for i = 0 to 1
     data = content_of_address(0x73 + i) EXOR crc
     for j = 0 to 7
          if data ≥ 128
               data = data * 2  // shift left by 1
               data = data EXOR 0x2F
          else
               data = data * 2 // shift left by 1
     next j
     crc = data
next i
crc = crc EXOR 0xFF
```

7.12.2 Restoring factory preset values

Factory preset values are restored if the following conditions apply for at least $t_{d(MTPNV)}$ during power-up:

- pin RSTN is held LOW
- CANH is pulled up to V_{BAT}
- CANL is pulled down to GND

After the factory preset values have been restored, the SBC performs a system reset and enters Forced normal Mode. Since the CAN bus is clamped dominant, pin RXDC is forced LOW. During the factory preset restore process, this pin is forced HIGH; a falling edge on this pin caused by bit PO being set after power-on then clearly indicates that the process has been completed.

Note that the write counter, WRCNTS, in the MTPNV status register is incremented every time the factory presets are restored.

7.13 Device ID

A byte is reserved at address 0x7E for a UJA1168A identification code.

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Table 44. Identification register (address 7Eh)

Bit	Symbol	Access	Value	Description
7:0	IDS[7:0]	R		device identification code
			F8h	UJA1168ATK
			FCh	UJA1168ATK/F
			E8h	UJA1168ATK/X
			ECh	UJA1168ATK/XF

7.14 Lock control register

Sections of the register address area can be write-protected to protect against unintended modifications. Note that this facility only protects locked bits from being modified via the SPI and will not prevent the UJA1168A updating status registers etc.

Table 45. Lock control register (address 0Ah)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	cleared for future use
6	LK6C	R/W		lock control 6: address area 0x68 to 0x6F
			0	SPI write-access enabled
			1	SPI write-access disabled
5	LK5C	R/W		lock control 5: address area 0x50 to 0x5F
			0	SPI write-access enabled
			1	SPI write-access disabled
4	LK4C	R/W		lock control 4: address area 0x40 to 0x4F - WAKE pin control
			0	SPI write-access enabled
			1	SPI write-access disabled
3	LK3C	R/W		lock control 3: address area 0x30 to 0x3F
			0	SPI write-access enabled
			1	SPI write-access disabled
2	LK2C	R/W		lock control 2: address area 0x20 to 0x2F - transceiver control
			0	SPI write-access enabled
			1	SPI write-access disabled
1	LK1C	R/W		lock control 1: address area 0x10 to 0x1F - regulator control
			0	SPI write-access enabled
			1	SPI write-access disabled
0	LK0C	R/W		lock control 0: address area 0x06 to 0x09 - general purpose memory
			0	SPI write-access enabled
			1	SPI write-access disabled

7.15 General purpose memory

UJA1168A allocates 4 bytes of RAM as general purpose registers for storing user information. The general purpose registers can be accessed via the SPI at address 0x06 to 0x09 (see Table 46).

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7.16 SPI

7.16.1 Introduction

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller, supporting multi-slave operations. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing registers to be read back by the application without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

- SCSN: SPI chip select; active LOW
- SCK: SPI clock; default level is LOW due to low-power concept (pull-down)
- SDI: SPI data input
- SDO: SPI data output; floating when pin SCSN is HIGH

Bit sampling is performed on the falling edge of the clock and data is shifted in/out on the rising edge, as illustrated in Figure 11.

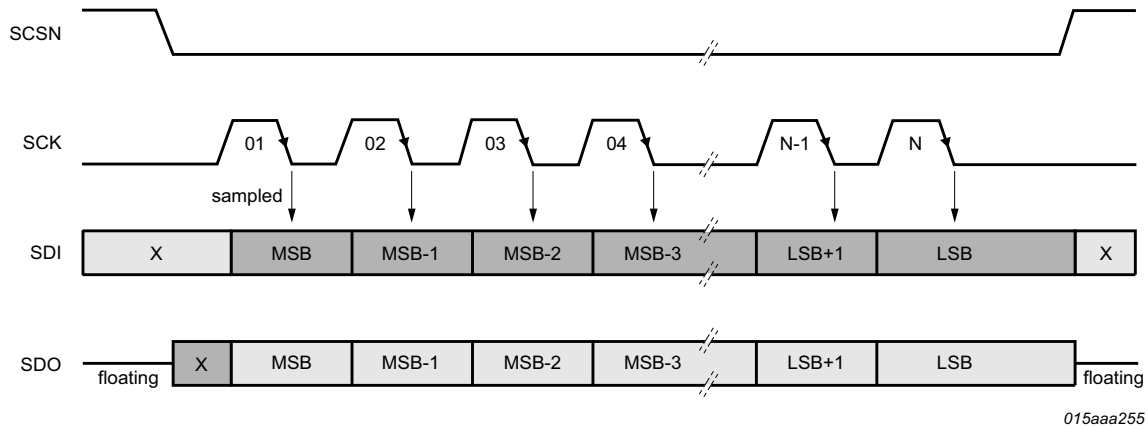

Fig 11. SPI timing protocol

The SPI data in the UJA1168A is stored in a number of dedicated 8-bit registers. Each register is assigned a unique 7-bit address. Two bytes must be transmitted to the SBC for a single register write operation. The first byte contains the 7-bit address along with a ‘read-only’ bit (the LSB). The read-only bit must be 0 to indicate a write operation (if this bit is 1, a read operation is assumed and any data on the SDI pin is ignored). The second byte contains the data to be written to the register.

24- and 32-bit read and write operations are also supported. The register address is automatically incremented, once for a 24-bit operation and twice for a 32-bit operation, as illustrated in Figure 12.

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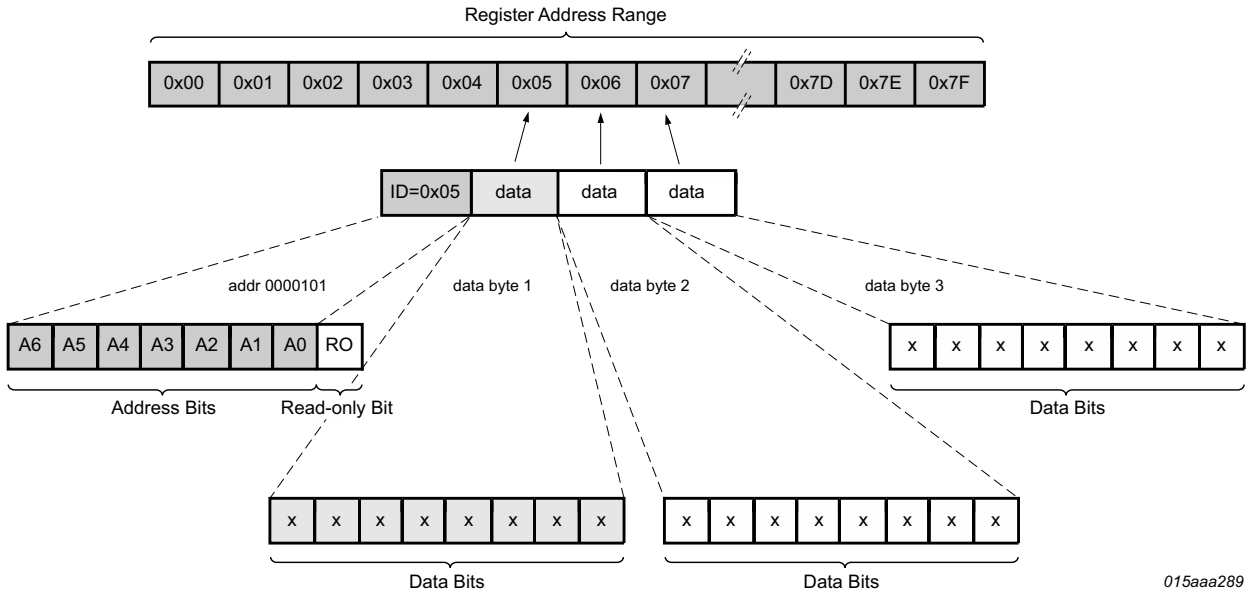

Fig 12. SPI data structure for a write operation (16-, 24- or 32-bit)

During an SPI data read or write operation, the contents of the addressed register(s) is returned via pin SDO.

The UJA1168A tolerates attempts to write to registers that don't exist. If the available address space is exceeded during a write operation, the data above the valid address range is ignored (without generating an SPI failure event).

During a write operation, the UJA1168A monitors the number of SPI bits transmitted. If the number recorded is not 16, 24 or 32, then the write operation is aborted and an SPI failure event is captured (SPIF = 1).

If more than 32 bits are clocked in on pin SDI during a read operation, the data stream on SDI is reflected on SDO from bit 33 onwards.

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7.16.2 Register map

The addressable register space contains 128 registers with addresses from 0x00 to 0x7F. An overview of the register mapping is provided in Table 46 to Table 55. The functionality of individual bits is discussed in more detail in relevant sections of the data sheet.

Table 46. Overview of primary control registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x00	Watchdog control	WMC			reserved	NWP			
0x01	Mode control	reserved					MC		
0x03	Main status	reserved	OTWS	NMS	RSS				
0x04	System event enable	reserved					OTWE	SPIFE	reserved
0x05	Watchdog status	reserved				FNMS	SDMS	WDS	
0x06	Memory 0	GPM[7:0]							
0x07	Memory 1	GPM[15:8]							
0x08	Memory 2	GPM[23:16]							
0x09	Memory 3	GPM[31:24]							
0x0A	Lock control	reserved	LK6C	LK5C	LK4C	LK3C	LK2C	LK1C	LK0C

Table 47. Overview of V1 and INH/VEXT control registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x10	V1 and INH/VEXT control	reserved				VEXTC		V1RTC	
0x1B	Supply status	reserved					VEXTS		V1S
0x1C	Supply event enable	reserved					VEXTOE	VEXTUE	V1UE

Table 48. Overview of transceiver control and partial networking registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x20	CAN control	reserved	CFDC[1]	PNCOK	CPNC	reserved		CMC	
0x22	Transceiver status	CTS	CPNERR	CPNS	COSCS	CBSS	reserved	VCS	CFS
0x23	Transceiver event enable	reserved			CBSE	reserved		CFE	CWE
0x26	Data rate	reserved					CDR		
0x27	Identifier 0	ID[7:0]							
0x28	Identifier 1	ID[15:8]							
0x29	Identifier 2	ID[23:16]							
0x2A	Identifier 3	reserved			ID[28:24]				
0x2B	Mask 0	M[7:0]							
0x2C	Mask 1	M[15:8]							
0x2D	Mask 2	M[23:16]							
0x2E	Mask 3	reserved			M[28:24]				
0x2F	Frame control	IDE	PNDM	reserved		DLC			
0x68	Data mask 0	DM0[7:0]							
0x69	Data mask 1	DM1[7:0]							

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Table 48. Overview of transceiver control and partial networking registers *…continued*

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x6A	Data mask 2	DM2[7:0]							
0x6B	Data mask 3	DM3[7:0]							
0x6C	Data mask 4	DM4[7:0]							
0x6D	Data mask 5	DM5[7:0]							
0x6E	Data mask 6	DM6[7:0]							
0x6F	Data mask 7	DM7[7:0]							

[1] UJA1168ATK/F and UJA1168ATK/XF only; otherwise reserved.

Table 49. Overview of WAKE pin control and status registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x4B	WAKE pin status	reserved						WPVS	reserved
0x4C	WAKE pin enable	reserved						WPRE	WPFE

Table 50. Overview of event capture registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x60	Global event status	reserved				WPE	TRXE	SUPE	SYSE
0x61	System event status	reserved			PO	reserved	OTW	SPIF	WDF
0x62	Supply event status	reserved					VEXTO	VEXTU	V1U
0x63	Transceiver event status	reserved		PNFDE	CBS	reserved		CF	CW
0x64	WAKE pin event status	reserved						WPR	WPF

Table 51. Overview of MTPNV status register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x70	MTPNV status	WRCNTS						ECCS	NVMPS

Table 52. Overview of Startup control register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x73	Startup control	reserved		RLC		VEXTSUC	reserved		

Table 53. Overview of SBC configuration control register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x74	SBC configuration control	reserved		V1RTSUC		FNMC	SDMC	reserved	SLPC

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Table 54. Overview of CRC control register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x75	MTPNV CRC control	CRCC[7:0]							

Table 55. Overview of Identification register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x7E	Identification	IDS[7:0]							

7.16.3 Register configuration in UJA1168A operating modes

A number of register bits may change state automatically when the UJA1168A switches from one operating mode to another. This is particularly evident when the UJA1168A switches to Off mode. These changes are summarized in Table 56. If an SPI transmission is in progress when the UJA1168A changes state, the transmission is ignored (automatic state changes have priority).

Table 56. Register bit settings in UJA1168A operating modes

Symbol	Off (power-on default)	Standby	Normal	Sleep	Overtemp	Reset
CBS	0	no change	no change	no change	no change	no change
CBSE	0	no change	no change	no change	no change	no change
CBSS	1	actual state	actual state	no change	actual state	actual state
CDR	101	no change	no change	no change	no change	no change
CF	0	no change	no change	no change	no change	no change
CFDC	0	no change	no change	no change	no change	no change
CFE	0	no change	no change	no change	no change	no change
CFS	0	actual state	actual state	actual state	actual state	actual state
CMC	00	no change	no change	no change	no change	no change
COSCS	0	actual state	actual state	actual state	actual state	actual state
CPNC	0	no change	no change	no change	no change	no change
CPNERR	1	actual state	actual state	actual state	actual state	actual state
CPNS	0	actual state	actual state	actual state	actual state	actual state
CRCC	00000000	no change	no change	no change	no change	no change
CTS	0	0	actual state	0	0	0
CW	0	no change	no change	no change	no change	no change
CWE	0	no change	no change	no change	no change	no change
DMn	11111111	no change	no change	no change	no change	no change
DLC	0000	no change	no change	no change	no change	no change
ECCS	actual state	actual state	actual state	actual state	actual state	actual state
FNMC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
FNMS	0	actual state	actual state	actual state	actual state	actual state
GPMn	00000000	no change	no change	no change	no change	no change
IDn	00000000	no change	no change	no change	no change	no change
IDE	0	no change	no change	no change	no change	no change

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Table 56. Register bit settings in UJA1168A operating modes *…continued*

Symbol	Off (power-on default)	Standby	Normal	Sleep	Overtemp	Reset
IDS	see Table 44	no change	no change	no change	no change	no change
LKnC	0	no change	no change	no change	no change	no change
MC	100	100	111	001	don't care	100
NMS	1	no change	0	no change	no change	no change
NVMPS	actual state	actual state	actual state	actual state	actual state	actual state
NWP	0100	no change	no change	no change	0100	0100
OTW	0	no change	no change	no change	no change	no change
OTWE	0	no change	no change	no change	no change	no change
OTWS	0	actual state	actual state	actual state	actual state	actual state
PNCOK	0	no change	no change	no change	no change	no change
PNDM	1	no change	no change	no change	no change	no change
PNFDE	0	no change	no change	no change	no change	no change
PO	1	no change	no change	no change	no change	no change
RLC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
RSS	00000	no change	no change	no change	10010	reset source
SDMC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
SDMS	0	actual state	actual state	actual state	actual state	actual state
SLPC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
SPIF	0	no change	no change	no change	no change	no change
SPIFE	0	no change	no change	no change	no change	no change
SUPE	0	no change	no change	no change	no change	no change
SYSE	1	no change	no change	no change	no change	no change
TRXE	0	no change	no change	no change	no change	no change
V1RTC	defined by V1RTSUC	no change	no change	no change	no change	no change
V1RTSUC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
V1S	0	actual state	actual state	actual state	actual state	actual state
V1UE	0	no change	no change	no change	no change	no change
V1U	0	no change	no change	no change	no change	no change
VCS	0	actual state	actual state	actual state	actual state	actual state
VEXTC	defined by VEXTSUC	no change	no change	no change	no change	no change
VEXTO[1]	0	no change	no change	no change	no change	no change
VEXTOE[1]	0	no change	no change	no change	no change	no change
VEXTS[1]	00	actual state	actual state	actual state	actual state	actual state
VEXTSUC	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV	MTPNV
VEXTU[1]	0	no change	no change	no change	no change	no change
VEXTUE[1]	0	no change	no change	no change	no change	no change
WDF	0	no change	no change	no change	no change	no change
WDS	0	actual state	actual state	actual state	actual state	actual state
WMC	[2]	no change	no change	no change	no change	[2]

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Table 56. Register bit settings in UJA1168A operating modes *…continued*

Symbol	Off (power-on default)	Standby	Normal	Sleep	Overtemp	Reset
WPE	0	no change	no change	no change	no change	no change
WPF	0	no change	no change	no change	no change	no change
WPR	0	no change	no change	no change	no change	no change
WPFE	0	no change	no change	no change	no change	no change
WPRE	0	no change	no change	no change	no change	no change
WPVS	0	no change	no change	no change	no change	no change
WRCNTS	actual state	actual state	actual state	actual state	actual state	actual state

[1] Only in variants with a VEXT pin.

[2] 001 if SDMC = 1; otherwise 010.

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8. Limiting values

Table 57. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x[1]	pin V1 [2]	−0.2	+6	V
		pins TXD, RXD, SDI, SDO, SCK, SCSN, RSTN [3]	−0.2	V_{V1} + 0.2	V
		pins INH, VEXT, WAKE	−18	+40	V
		pin BAT	−0.2	+40	V
		pins CANH and CANL with respect to any other pin	−58	+58	V
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		−40	+40	V
V_{trt}	transient voltage	on pins CANL, CANH, WAKE, VEXT, BAT [4]			
		pulse 1	−100	-	V
		pulse 2a	-	75	V
		pulse 3a	−150	-	V
		pulse 3b	-	100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω) discharge circuit [5]			
		on pins CANH and CANL; pin BAT with capacitor; pin WAKE with 10 nF capacitor and 10 kΩ resistor; pin VEXT with 2.2 μF capacitor	−6	+6	kV
		Human Body Model (HBM)			
		on any pin [6]	−2	+2	kV
		on pins BAT, WAKE, VEXT [7]	−4	+4	kV
		on pins CANH, CANL [8]	−8	+8	kV
		Machine Model (MM) [9]			
		on any pin	−100	+100	V
		Charged Device Model (CDM) [10]			
		on corner pins	−750	+750	V
		on any other pin	−500	+500	V
T_{vj}	virtual junction temperature	[11]	−40	+150	°C
		when programming the MTPNV cells	0	+125	°C
T_{stg}	storage temperature		−55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] When the device is not powered up, I_{V1} (max) = 25 mA.

[3] Maximum voltage should never exceed 6 V.

[4] Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO7637 part 2.

[5] Verified by an external test house according to IEC TS 62228, Section 4.3.

[6] According to AEC-Q100-002.

[7] Pins stressed to reference group containing all grounds, emulating the application circuit (Figure 17). HBM pulse as specified in AEC-Q100-002 used.

[8] Pins stressed to reference group containing all ground and supply pins, emulating the application circuit (Figure 17). HBM pulse as specified in AEC-Q100-002 used.

[9] According to AEC-Q100-003.

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[10] According to AEC-Q100-011.

[11] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value used in the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

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9. Thermal characteristics

Table 58. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(vj-a)}$	thermal resistance from virtual junction to ambient	HVSON14 [1]	60	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 μm).

10. Static characteristics

Table 59. Static characteristics

T_{vj} = −40 °C to +150 °C; V_{BAT} = 3 V to 28 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin BAT						
$V_{th(det)pon}$	power-on detection threshold voltage	V_{BAT} rising	4.2	-	4.55	V
$V_{th(det)poff}$	power-off detection threshold voltage	V_{BAT} falling	2.8	-	3	V
$V_{uvr(CAN)}$	CAN undervoltage recovery voltage	V_{BAT} rising	4.5	-	5	V
$V_{uvd(CAN)}$	CAN undervoltage detection voltage	V_{BAT} falling	4.2	-	4.55	V
I_{BAT}	battery supply current	Normal mode; MC = 111; CAN Active mode				
		CAN recessive; V_{TXD} = V_{V1}	-	4	7.5	mA
		CAN dominant; V_{TXD} = 0 V	-	46	67	mA
		Sleep mode; MC = 001; CAN Offline mode; V_{BAT} = 7 V to 18 V; −40 °C < T_{vj} < 85 °C	-	[2]	65	μA
		Standby mode; MC = 100; CWE = 1; CAN Offline mode; I_{V1} = 0 μA; V_{BAT} = 7 V to 18 V; −40 °C < T_{vj} < 85 °C	-	[2]	91	μA
		additional current in CAN Offline Bias mode; −40 °C < T_{vj} < 85 °C	-	38	55	μA
		additional current in CAN Offline Bias mode with active partial networking decoder; Standby or Sleep mode; −40 °C < T_{vj} < 85 °C [3]		0.4	0.65	mA
		additional current from WAKE input; WPRE = WPFE = 1; −40 °C < T_{vj} < 85 °C		2	3	μA

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Table 59. Static characteristics *…continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 3 V to 28 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage source: pin V1						
V_O	output voltage	V_{BAT} = 5.5 V to 28 V; I_{V1} = −120 mA to 0 mA; V_{TXD} = V_{V1}	4.9	5	5.1	V
		V_{BAT} = 5.65 V to 28 V; I_{V1} = −150 mA to 0 mA; V_{TXD} = V_{V1}	4.9	5	5.1	V
		V_{BAT} = 5.65 V to 28 V; I_{V1} = −100 mA to 0 mA; V_{TXD} = 0 V; V_{CANH} = 0 V	4.9	5	5.1	V
$\Delta V_{ret(RAM)}$	RAM retention voltage difference	between V_{BAT} and V_{V1}				
		V_{BAT} = 2 V to 3 V; I_{V1} = −2 mA	-	-	100	mV
		V_{BAT} = 2 V to 3 V; I_{V1} = −200 µA [3]			10	mV
$R_{(BAT-V1)}$	resistance between pin BAT and pin V1	V_{BAT} = 4 V to 6 V; I_{V1} = −120 mA	-	-	5	Ω
		V_{BAT} = 3 V to 4 V; I_{V1} = −40 mA	-	2.625	-	Ω
V_{uvd}	undervoltage detection voltage	$V_{uvd(nom)}$ = 90 %	4.5	-	4.75	V
		$V_{uvd(nom)}$ = 80 %	4	-	4.25	V
		$V_{uvd(nom)}$ = 70 %	3.5		3.75	V
		$V_{uvd(nom)}$ = 60 %	3	-	3.25	V
V_{uvr}	undervoltage recovery voltage		4.5	-	4.75	V
$I_{O(sc)}$	short-circuit output current		−300	-	−150	mA
$I_{CAN(int)V1}$	internal CAN supply current from V1	Normal mode; MC = 111; CAN Active mode; CAN dominant; V_{TXD} = 0 V; short-circuit on bus lines; −3 V < (V_{CANH} = V_{CANL}) < +18 V	-	-	59	mA
Voltage source: VEXT (UJA1168ATK/X and UJA1168ATK/XF only)						
V_O	output voltage	V_{BAT} = 6.5 V to 28 V; I_{VEXT} = −30 mA to 0 mA	4.9	5	5.1	V
V_{uvd}	undervoltage detection voltage		4.5	-	4.75	V
V_{ovd}	overvoltage detection voltage		6.5	-	7	V
$I_{O(sc)}$	short-circuit output current		−125	-	−30	mA
Voltage source: INH (UJA1168ATK and UJA1168ATK/F only)						
V_O	output voltage	I_{INH} = −180 µA	V_{BAT} − 0.8	-	V_{BAT}	V
R_{pd}	pull-down resistance	Sleep mode	3	4	5	MΩ
Serial peripheral interface inputs; pins SDI, SCK and SCSN						
$V_{th(sw)}$	switching threshold voltage		0.25V_{V1}	-	0.75V_{V1}	V
$V_{th(sw)hys}$	switching threshold voltage hysteresis		0.05V_{V1}	-	-	V
$R_{pd(SCK)}$	pull-down resistance on pin SCK		40	60	80	kΩ
$R_{pu(SCSN)}$	pull-up resistance on pin SCSN		40	60	80	kΩ
$R_{pd(SDI)}$	pull-down resistance on pin SDI	V_{SDI} < $V_{th(sw)}$	40	60	80	kΩ
$R_{pu(SDI)}$	pull-up resistance on pin SDI	V_{SDI} > $V_{th(sw)}$	40	60	80	kΩ

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Table 59. Static characteristics *…continued*

T_{vj} = –40 °C to +150 °C; V_{BAT} = 3 V to 28 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Serial peripheral interface data output; pin SDO						
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	V_{V1} – 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
$I_{LO(off)}$	off-state output leakage current	V_{SCSN} = V_{V1}; V_O = 0 V to V_{V1}	–5	-	+5	µA
CAN transmit data input; pin TXD						
$V_{th(sw)}$	switching threshold voltage		0.25V_{V1}	-	0.75V_{V1}	V
$V_{th(sw)hys}$	switching threshold voltage hysteresis		0.05V_{V1}	-	-	V
R_{pu}	pull-up resistance		40	60	80	kΩ
CAN receive data output; pin RXD						
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	V_{V1} – 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
R_{pu}	pull-up resistance	CAN Offline mode	40	60	80	kΩ
Local wake input; pin WAKE						
$V_{th(sw)r}$	rising switching threshold voltage		2.8	-	4.1	V
$V_{th(sw)f}$	falling switching threshold voltage		2.4	-	3.75	V
$V_{hys(i)}$	input hysteresis voltage		250	-	800	mV
I_i	input current	T_{vj} = –40 °C to +85 °C	-	-	1.5	µA
High-speed CAN bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	CAN Active mode; V_{TXD} = 0 V; t < $t_{to(dom)TXD}$				
		pin CANH; R_L = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANL; R_L = 50 Ω to 65 Ω	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym}$ = V_{V1} – V_{CANH} – V_{CANL}; V_{V1} = 5 V	–400	-	+400	mV
V_{TXsym}	transmitter voltage symmetry	V_{TXsym} = V_{CANH} + V_{CANL}; f_{TXD} = 250 kHz, 1 MHz or 2.5 MHz; C_{SPLIT} = 4.7 nF [3] [4]	0.9V_{V1}	-	1.1V_{V1}	V
$V_{O(dif)}$	differential output voltage	CAN Active mode (dominant); V_{TXD} = 0 V; V_{V1} = 4.75 V to 5.5 V; t < $t_{to(dom)TXD}$				
		R_L = 50 Ω to 65 Ω	1.5	-	3	V
		R_L = 45 Ω to 70 Ω	1.4	-	3.3	V
		R_L = 2240 Ω	1.5	-	5	V
		recessive; R_L = no load				
		CAN Active/Listen-only/Offline Bias mode; V_{TXD} = V_{V1}	–50	-	+50	mV
		CAN Offline mode	–0.2	-	+0.2	V

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Table 59. Static characteristics *...continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 3 V to 28 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(rec)}$	recessive output voltage	CAN Active mode; V_{TXD} = V_{V1} R_L = no load	2	$0.5V_{V1}$	3	V
		CAN Offline mode; R_L = no load	−0.1	-	+0.1	V
		CAN Offline Bias/Listen-only modes; R_L = no load	2	2.5	3	V
$I_{O(sc)dom}$	dominant short-circuit output current	CAN Active mode; V_{TXD} = 0 V; V_{V1} = 5 V				
		pin CANH; V_{CANH} = −3 V to +27 V	−55	-	-	mA
		pin CANL; V_{CANL} = −15 V to +18 V	-	-	+55	mA
$I_{O(sc)rec}$	recessive short-circuit output current	V_{CANL} = V_{CANH} = −27 V to +32 V; V_{TXD} = V_{V1}	−3	-	+3	mA
$V_{th(RX)dif}$	differential receiver threshold voltage	−12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V				
		CAN Active/Listen-only modes	0.5	0.7	0.9	V
		CAN Offline mode	0.4	0.7	1.15	V
$V_{rec(RX)}$	receiver recessive voltage	−12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V				
		CAN Active/Listen-only modes	−4[3]	-	+0.5	V
		CAN Offline/Offline Bias modes	−4[3]	-	+0.4	V
$V_{dom(RX)}$	receiver dominant voltage	−12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V				
		CAN Active/Listen-only modes	0.9	-	9.0[3]	V
		CAN Offline/Offline Bias modes	1.15	-	9.0[3]	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	CAN Active/Listen-only modes; −12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V	1	30	60	mV
R_i	input resistance	−2 V ≤ V_{CANL} ≤ +7 V; −2 V ≤ V_{CANH} ≤ +7 V	9	15	28	kΩ
ΔR_i	input resistance deviation	0 V ≤ V_{CANL} ≤ +5 V; 0 V ≤ V_{CANH} ≤ +5 V	−1	-	+1	%
$R_{i(dif)}$	differential input resistance	−2 V ≤ V_{CANL} ≤ +7 V; −2 V ≤ V_{CANH} ≤ +7 V	19	30	52	kΩ
$C_{i(cm)}$	common-mode input capacitance	[3]	-	-	20	pF
$C_{i(dif)}$	differential input capacitance	[3]	-	-	10	pF
I_L	leakage current	V_{BAT} = V_{V1} = 0 V or V_{BAT} = V_{V1} = shorted to ground via 47 kΩ; V_{CANH} = V_{CANL} = 5 V	−5	-	+5	µA
Temperature protection						
$T_{th(act)otp}$	overtemperature protection activation threshold temperature		167	177	187	°C

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Table 59. Static characteristics *…continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 3 V to 28 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.[1]

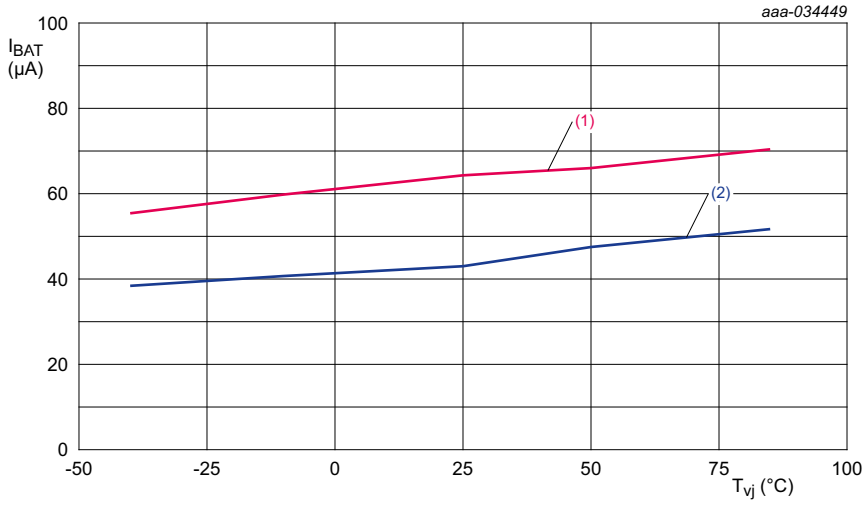
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{th(rel)otp}$	overtemperature protection release threshold temperature		127	137	147	°C
$T_{th(warn)otp}$	overtemperature protection warning threshold temperature		127	137	147	°C
Reset output; pin RSTN						
V_{OL}	LOW-level output voltage	V_{V1} = 1.0 V to 5.5 V; pull-up resistor to V_{V1} ≥ 900 Ω	0	-	$0.2V_{V1}$	V
R_{pu}	pull-up resistance		40	60	80	kΩ
$V_{th(sw)}$	switching threshold voltage		$0.25V_{V1}$	-	$0.75V_{V1}$	V
$V_{th(sw)hys}$	switching threshold voltage hysteresis		$0.05V_{V1}$	-	-	V
MTP non-volatile memory						
$N_{cy(W)MTP}$	number of MTP write cycles	V_{BAT} = 6 V to 28 V; T_{vj} = 0 °C to +125 °C	-	-	200	-

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] See Figure 13.

[3] Not tested in production; guaranteed by design.

[4] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 20.



(1) Standby Mode: MC = 100, CWE = 1, CAN Offline mode, V_{BAT} = 12 V, I_{V1} = 0 µA.

(2) Sleep mode: MC = 001, CAN Offline mode, V_{BAT} = 12 V.

Fig 13. UJA1168A typical Standby and Sleep mode quiescent current (µA)

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11. Dynamic characteristics

Table 60. Dynamic characteristics

T_{vj} = −40 °C to +150 °C; V_{BAT} = 3 V to 28 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage source; pin V1						
$t_{startup}$	start-up time	from V_{BAT} exceeding the power-on detection threshold until V_{V1} exceeds the 90 % undervoltage threshold; C_{V1} = 4.7 µF	-	2.8	4.7	ms
$t_{d(uvd)}$	undervoltage detection delay time		6	-	54	µs
$t_{d(uvd-RSTNL)}$	delay time from undervoltage detection to RSTN LOW	undervoltage on V1	-	-	63	µs
$t_{d(buswake-VOH)}$	delay time from bus wake-up to HIGH-level output voltage	HIGH = 0.8$V_{O(V1)}$; $I_{V1} \leq$ 100 mA	-	-	5	ms
Voltage source; pin VEXT						
$t_{d(uvd)}$	undervoltage detection delay time		6	-	39	µs
$t_{d(ovd)}$	overvoltage detection delay time		6	-	39	µs
Serial peripheral interface timing; pins SCSN, SCK, SDI and SDO; see Figure 16						
$t_{cy(clk)}$	clock cycle time		250	-	-	ns
$t_{SPILEAD}$	SPI enable lead time		50	-	-	ns
t_{SPILAG}	SPI enable lag time		50	-	-	ns
$t_{clk(H)}$	clock HIGH time		100	-	-	ns
$t_{clk(L)}$	clock LOW time		100	-	-	ns
$t_{su(D)}$	data input set-up time		50	-	-	ns
$t_{h(D)}$	data input hold time		50	-	-	ns
$t_{v(Q)}$	data output valid time	pin SDO; C_L = 20 pF	-	-	50	ns
$t_{d(SDI-SDO)}$	SDI to SDO delay time	SPI address bits and read-only bit; C_L = 20 pF	-	-	50	ns
$t_{WH(S)}$	chip select pulse width HIGH	pin SCSN	250	-	-	ns
$t_{d(SCKL-SCSNL)}$	delay time from SCK LOW to SCSN LOW		50	-	-	ns
CAN transceiver timing; pins CANH, CANL, TXD and RXD						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	[2]	-	80	-	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	[2]	-	80	-	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	[2]	-	105	-	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	[2]	-	120	-	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	$t_{bit(TXD)}$ = 200 ns [3]	-	-	255	ns

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Table 60. Dynamic characteristics *...continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 3 V to 28 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	$t_{bit(TXD)}$ = 200 ns [3]	-	-	255	ns
$t_{bit(bus)}$	transmitted recessive bit width	$t_{bit(TXD)}$ = 500 ns [3]	435	-	530	ns
		$t_{bit(TXD)}$ = 200 ns [3]	155	-	210	ns
$t_{bit(RXD)}$	bit time on pin RXD	$t_{bit(TXD)}$ = 500 ns [3]	400	-	550	ns
		$t_{bit(TXD)}$ = 200 ns [3]	120	-	220	ns
Δt_{rec}	receiver timing symmetry	$t_{bit(TXD)}$ = 500 ns	−65	-	+40	ns
		$t_{bit(TXD)}$ = 200 ns	−45	-	+15	ns
$t_{wake(busdom)}$	bus dominant wake-up time	first pulse (after first recessive) for wake-up on pins CANH and CANL; CAN Offline mode	0.5	-	1.8	µs
		second pulse for wake-up on pins CANH and CANL	0.5	-	1.8	µs
$t_{wake(busrec)}$	bus recessive wake-up time	first pulse for wake-up on pins CANH and CANL; CAN Offline mode	0.5	-	1.8	µs
		second pulse (after first dominant) for wake-up on pins CANH and CANL	0.5	-	1.8	µs
$t_{to(wake)bus}$	bus wake-up time-out time	between first and second dominant pulses; CAN Offline mode	0.8	-	10	ms
$t_{to(dom)TXD}$	TXD dominant time-out time	CAN Active mode; V_{TXD} = 0 V	2.7	-	3.3	ms
$t_{to(silence)}$	bus silence time-out time	recessive time measurement started in all CAN modes	0.95	-	1.17	s
$t_{d(busact-bias)}$	delay time from bus active to bias		-	-	200	µs
$t_{startup(CAN)}$	CAN start-up time	when switching to Active mode (CTS = 1)	-	-	220	µs
CAN partial networking						
$N_{bit(idle)}$	number of idle bits	before a new SOF is accepted; CFDC = 1 [4]	6	-	10	-
$t_{fltr(bit)dom}$	dominant bit filter time	arbitration data rate ≤ 500 kbit/s; CFDC = 1 [5] [4]	5	-	17.5	%
Pin RXD: event capture timing (valid in CAN Offline mode only)						
$t_{d(event)}$	event capture delay time	CAN Offline mode	0.9	-	1.1	ms
t_{blank}	blanking time	when switching from Offline to Active/Listen-only mode	-	-	25	µs
Watchdog						
$t_{trig(wd)1}$	watchdog trigger time 1	Normal mode; watchdog Window mode only [6]	0.45 × NWP[7]	-	0.55 × NWP[7]	ms
$t_{trig(wd)2}$	watchdog trigger time 2	Normal/Standby mode [8]	0.9 × NWP[7]	-	1.11 × NWP[7]	ms
$t_{d(SCSNH-RSTNL)}$	delay time from SCSN HIGH to RSTN LOW	rising edge to falling edge; watchdog in window mode, triggered in the first half of the watchdog period (before $t_{trig(wd)1}$) [4]	-	-	0.2	ms

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Table 60. Dynamic characteristics *…continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 3 V to 28 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pin RSTN: reset pulse width						
$t_{w(rst)}$	reset pulse width	output pulse width				
		RLC = 00	20	-	25	ms
		RLC = 01	10	-	12.5	ms
		RLC = 10	3.6	-	5	ms
		RLC = 11	1	-	1.5	ms
		input pulse width	18	-	-	µs
Pin WAKE						
t_{wake}	wake-up time		50	-	-	µs
MTP non-volatile memory						
$t_{ret(data)}$	data retention time	T_{vj} = 90 °C	20	-	-	year
$t_{prog(MTPNV)}$	MTPNV programming time	correct CRC code received at address 0x75; V_{BAT} = 6 V to 28 V	10	12	14	ms
$t_{d(MTPNV)}$	MTPNV delay time	before factory presets are restored; V_{BAT} = 6 V to 28 V	0.9	-	1.1	s
Mode transition						
$t_{d(act)norm}$	normal mode activation delay time	MC = 111; delay before CAN transceiver gets activated after the SBC switches to Normal mode	-	-	320	µs

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] See Figure 14 and Figure 19.

[3] See Figure 15 and Figure 19.

[4] Not tested in production; guaranteed by design.

[5] Up to 2 Mbit/s data speed.

[6] A system reset will be performed if the watchdog is in Window mode and is triggered less than $t_{trig(wd)1}$ after the start of the watchdog period (or in the first half of the watchdog period).

[7] The nominal watchdog period is programmed via the NWP control bits.

[8] The watchdog will be reset if it is in window mode and is triggered at least $t_{trig(wd)1}$, but not more than $t_{trig(wd)2}$, after the start of the watchdog period (or in the second half of the watchdog period). A system reset will be performed if the watchdog is triggered more than $t_{trig(wd)2}$ after the start of the watchdog period (watchdog overflows).

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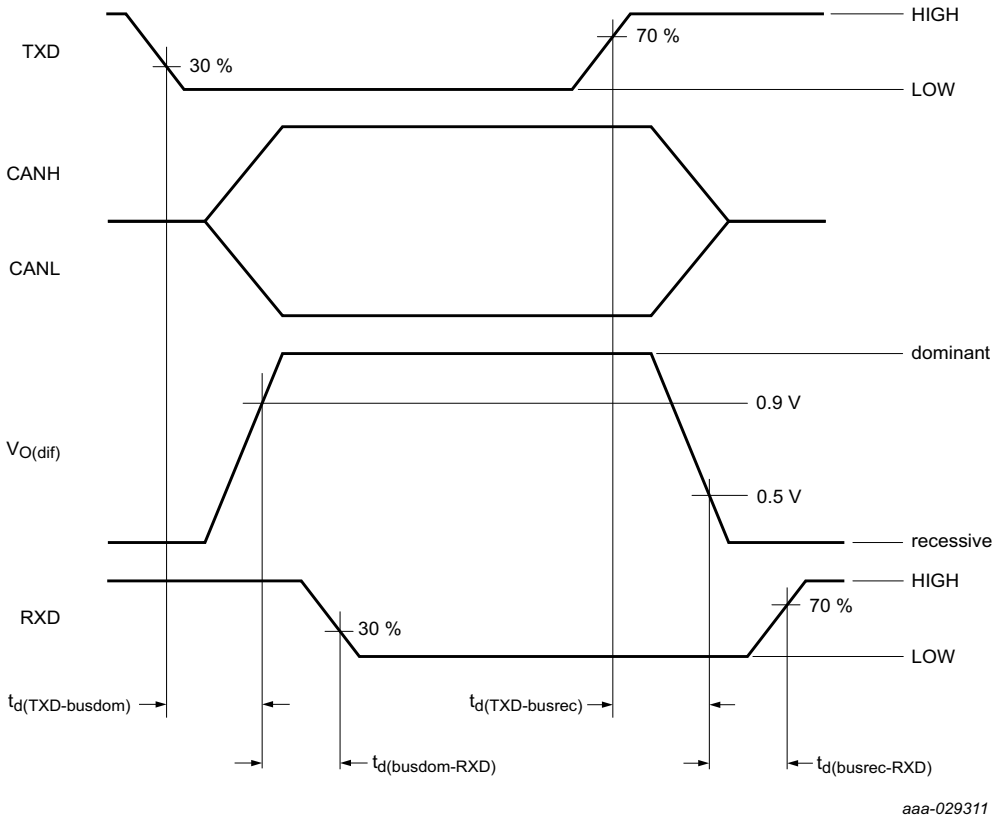

Fig 14. CAN transceiver timing diagram

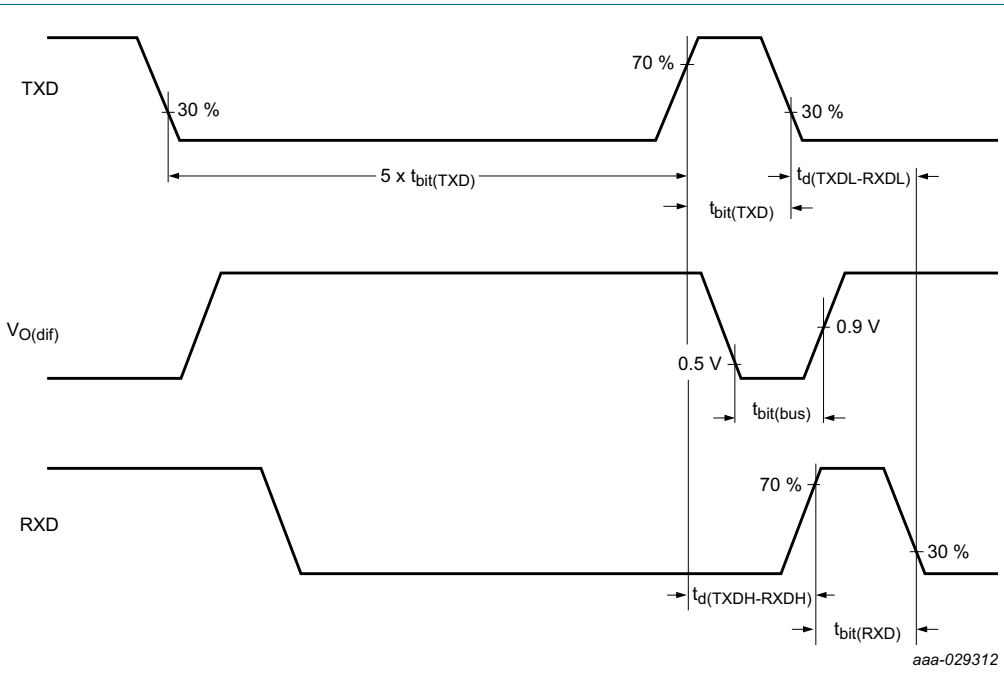

Fig 15. CAN FD timing definitions according to ISO 11898-2:2016

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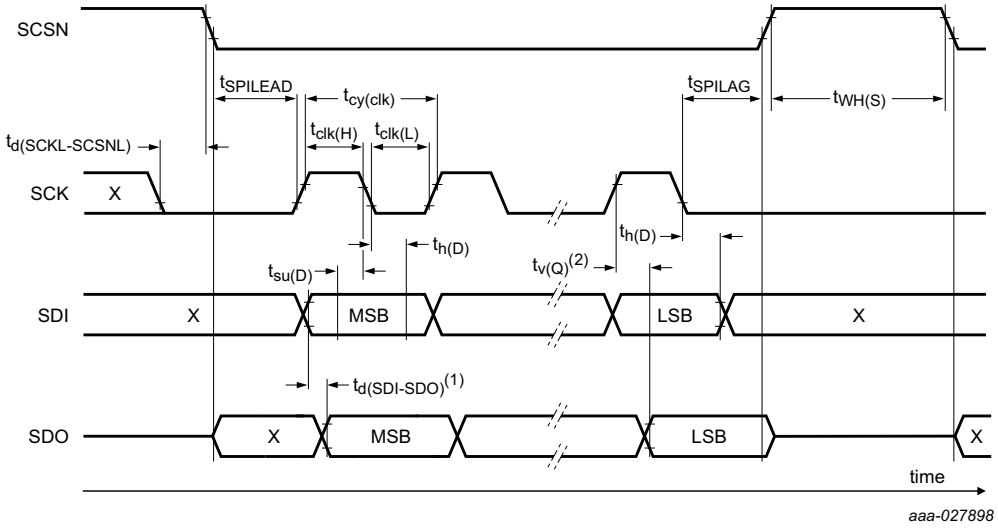

(1) The SDI to SDO delay time is valid for SPI address bits and the read-only bit.

(2) The data output valid time is valid for the SPI data bits.

Fig 16. SPI timing diagram

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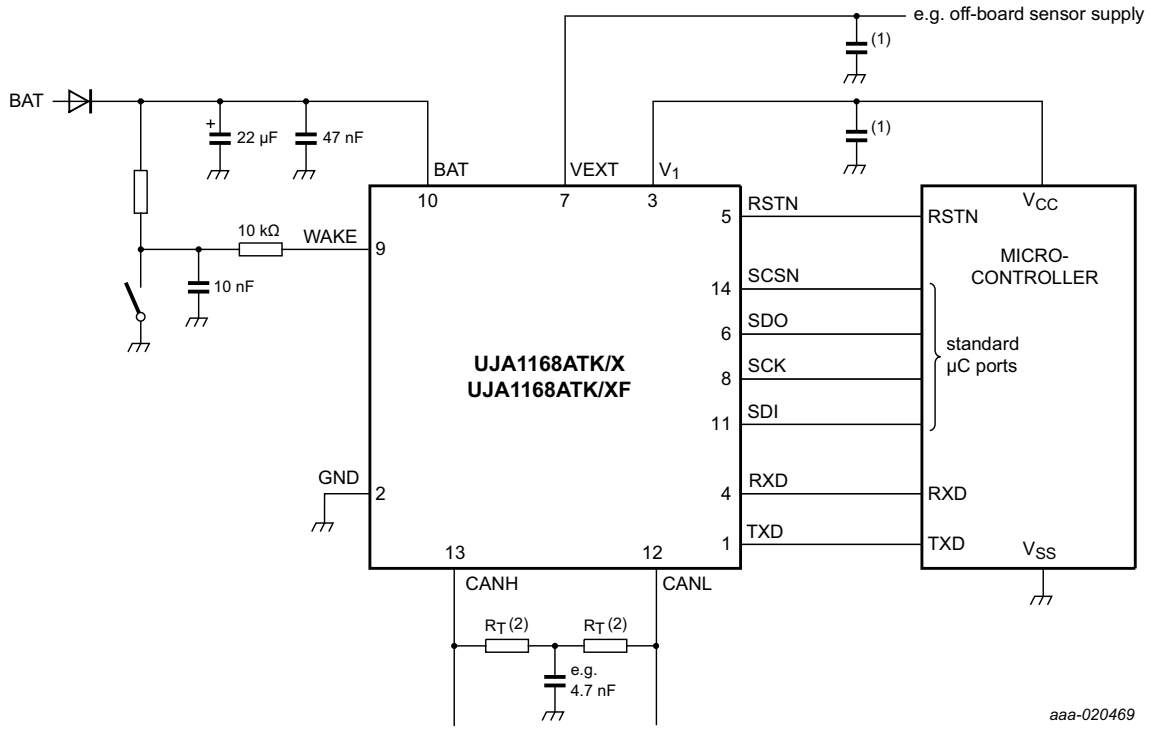
12. Application information

12.1 Application diagram



(1) Actual capacitance value must be a least 1.76 µF with 5 V DC offset (recommended capacitor value is 6.8 µF).

(2) For bus line end nodes, R_T = 60 Ω in order to support the 'split termination concept'. For sub-nodes, an optional 'weak' termination of e.g. R_T = 1.3 kΩ can be used, if required by the OEM.

Fig 17. Typical application using the UJA1168ATK/X or UJA1168ATK/XF

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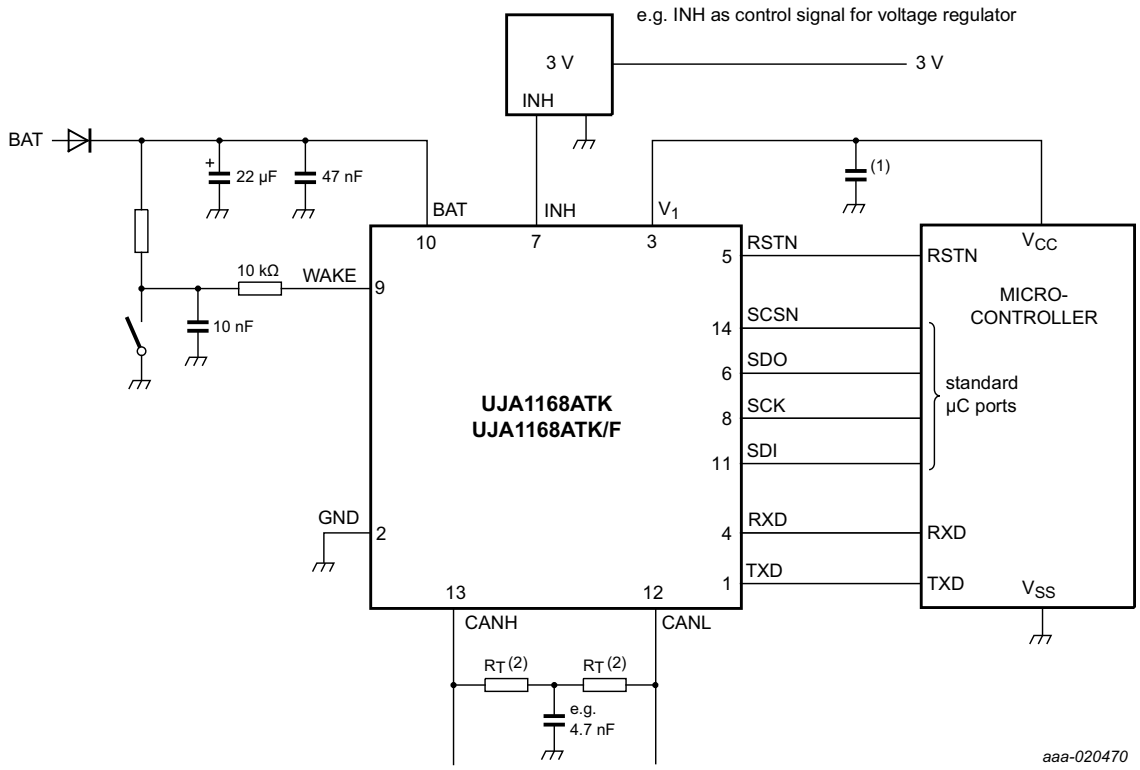

(1) Actual capacitance value must be a least 1.76 µF with 5 V DC offset (recommended capacitor value is 6.8 µF).

(2) For bus line end nodes, R_T = 60 Ω in order to support the 'split termination concept'. For sub-nodes, an optional 'weak' termination of e.g. R_T = 1.3 kΩ can be used, if required by the OEM.

Fig 18. Typical application using the UJA1168ATK or UJA1168ATK/F

12.2 Application hints

Further information on the application of the UJA1168A can be found in the NXP application hints document *AH1902 Application Hints - Mini high speed CAN system basis chips UJA116xA.*

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13. Test information

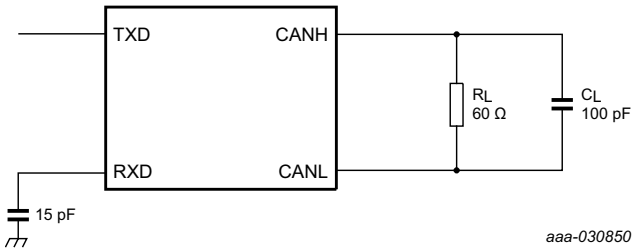

Fig 19. Timing test circuit for CAN transcriber

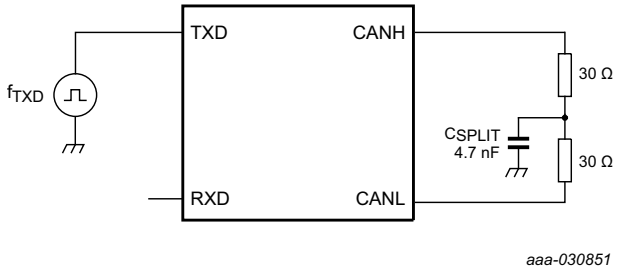

Fig 20. Test circuit for measuring transceiver driver symmetry

13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

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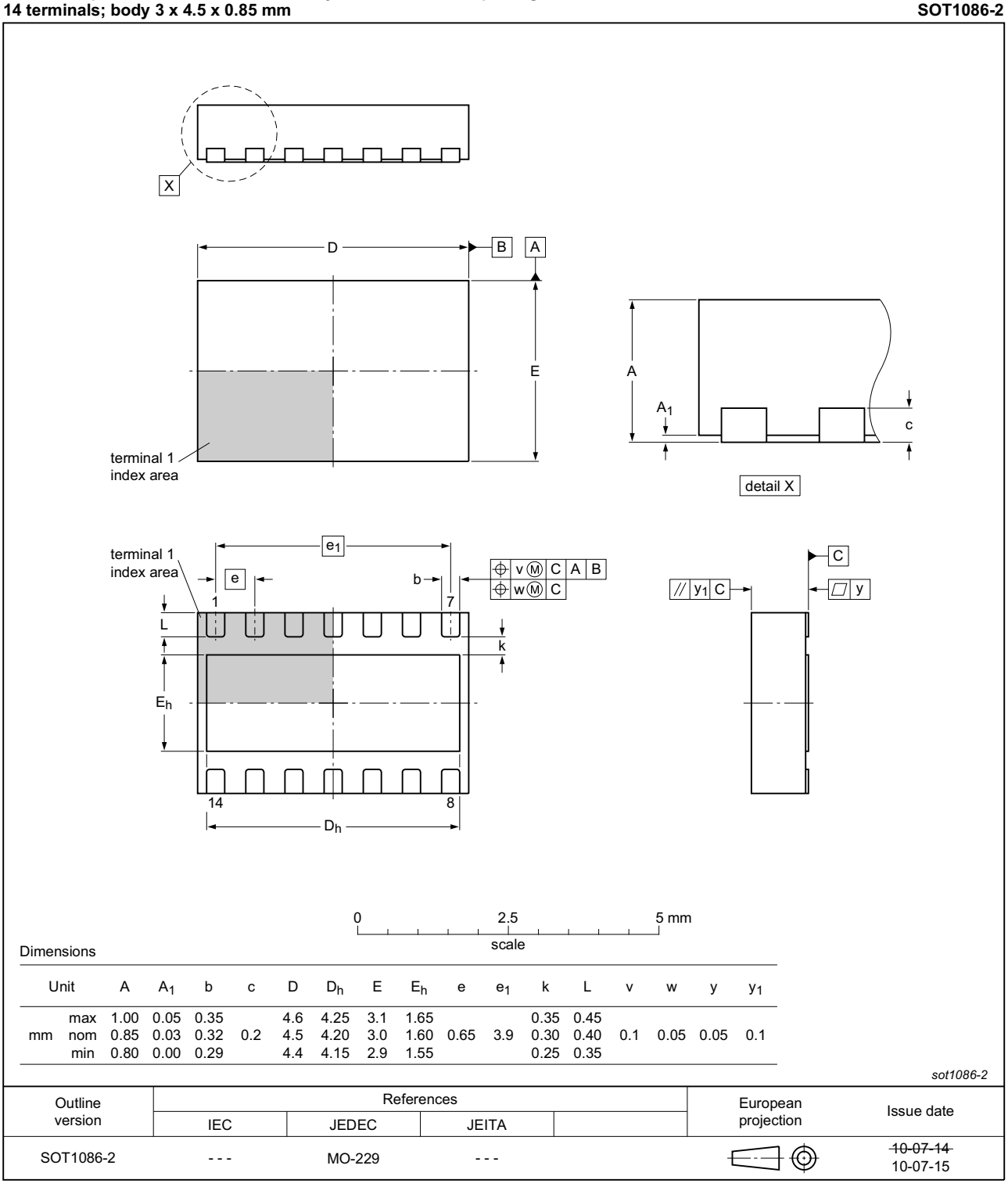
14. Package outline

HVSON14: plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 x 4.5 x 0.85 mm **SOT1086-2**



Dimensions

Unit		A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
mm	max	1.00	0.05	0.35		4.6	4.25	3.1	1.65			0.35	0.45				
	nom	0.85	0.03	0.32	0.2	4.5	4.20	3.0	1.60	0.65	3.9	0.30	0.40	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.29		4.4	4.15	2.9	1.55			0.25	0.35				

sot1086-2

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1086-2	- - -	MO-229	- - -			~~10-07-14~~ 10-07-15

Fig 21. Package outline SOT1086-2 (HVSON14)

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15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

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- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 22) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 61 and 62

Table 61. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 62. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 22.

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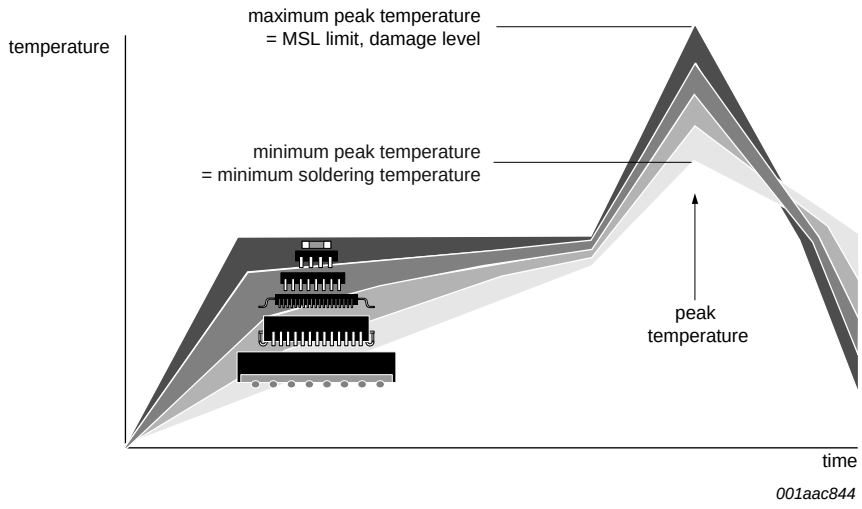

MSL: Moisture Sensitivity Level

Fig 22. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Soldering of HVSON packages

Section 16 contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering HVSON leadless package ICs can be found in the following application notes:

- *AN10365 'Surface mount reflow soldering description"*
- *AN10366 "HVQFN application information"*

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18. Appendix: ISO 11898-2:2016 parameter cross-reference list

Table 63. ISO 11898-2:2016 to NXP data sheet parameter conversion

ISO 11898-2:2016		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(dom)}$	dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff}	$V_{O(dif)}$	differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
HS-PMA driver symmetry			
Driver symmetry	V_{SYM}	V_{TXsym}	transmitter voltage symmetry
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_{O(sc)dom}$	dominant short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(rec)}$	recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{O(dif)}$	differential output voltage
Optional HS-PMA transmit dominant timeout			
Transmit dominant timeout, long	t_{dom}	$t_{to(dom)TXD}$	TXD dominant time-out time
Transmit dominant timeout, short			
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range Dominant state differential input voltage range	V_{Diff}	$V_{th(RX)dif}$	differential receiver threshold voltage
		$V_{rec(RX)}$	receiver recessive voltage
		$V_{dom(RX)}$	receiver dominant voltage
HS-PMA receiver input resistance (matching)			
Differential internal resistance	R_{Diff}	$R_{i(dif)}$	differential input resistance
Single ended internal resistance	R_{CAN_H} R_{CAN_L}	R_i	input resistance
Matching of internal resistance	MR	ΔR_i	input resistance deviation
HS-PMA implementation loop delay requirement			
Loop delay	t_{Loop}	$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH
		$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW
Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s			
Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended	$t_{Bit(Bus)}$	$t_{bit(bus)}$	transmitted recessive bit width
Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{bit(RXD)}$	bit time on pin RXD
Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s	Δt_{Rec}	Δt_{rec}	receiver timing symmetry

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Table 63. ISO 11898-2:2016 to NXP data sheet parameter conversion

ISO 11898-2:2016		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}			
Maximum rating V_{Diff}	V_{Diff}	$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	V_x	voltage on pin x
Optional: Extended maximum rating VCAN_H and VCAN_L			
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered			
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_L	leakage current
Number of recessive bits before next SOF			
Number of recessive bits before a new SOF shall be accepted	n_{Bits_idle}	$N_{bit(idle)}$	number of idle bits
Bitfiter in CAN FD data phase			
CAN FD data phase bitfilter (option 1)	$pBitfilter_{option1}$	$t_{fltr(bit)dom}$	dominant bit filter time
HS-PMA bus biasing control timings			
CAN activity filter time, long	t_{Filter}	$t_{wake(busdom)}$[1]	bus dominant wake-up time
CAN activity filter time, short		$t_{wake(busrec)}$[1]	bus recessive wake-up time
Wake-up timeout, short	t_{Wake}	$t_{to(wake)bus}$	bus wake-up time-out time
Wake-up timeout, long			
Timeout for bus inactivity	$t_{Silence}$	$t_{to(silence)}$	bus silence time-out time
Bus Bias reaction time	t_{Bias}	$t_{d(busact-bias)}$	delay time from bus active to bias

[1] $t_{fltr(wake)bus}$ - bus wake-up filter time, in devices with basic wake-up functionality

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19. Revision history

Table 64. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
UJA1168A v.1	20190823	Product data sheet	-	-

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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