THE DATASHEET OF

AD7719BRUZ-REEL7

Low Voltage, Low Power, Factory-Calibrated 16-/24-Bit Dual Σ-Δ ADC

AD7719

FEATURES

HIGH RESOLUTION Σ-Δ ADCs
2 Independent ADCs (16- and 24-Bit Resolution)
Factory-Calibrated (Field Calibration Not Required)
Output Settles in 1 Conversion Cycle (Single Conversion Mode)
Programmable Gain Front End
Simultaneous Sampling and Conversion of 2 Signal Sources
Separate Reference Inputs for Each Channel
Simultaneous 50 Hz and 60 Hz Rejection at 20 Hz Update Rate
***ISOURCE Select*™**
24-Bit No Missing Codes—Main ADC
13-Bit p-p Resolution @ 20 Hz, 20 mV Range
18-Bit p-p Resolution @ 20 Hz, 2.56 V Range

INTERFACE
3-Wire Serial
SPI®, QSPI™, MICROWIRE™, and DSP Compatible
Schmitt Trigger on SCLK

POWER
Specified for Single 3 V and 5 V Operation
Normal: 1.5 mA Typ @ 3 V
Power-Down: 10 μA (32 kHz Crystal Running)

ON-CHIP FUNCTIONS
Rail-Rail Input Buffer and PGA
4-Bit Digital I/O Port
On-Chip Temperature Sensor
Dual Switchable Excitation Current Sources
Low-Side Power Switches
Reference Detect Circuit

APPLICATIONS

Sensor Measurement
Temperature Measurement
Pressure Measurement
Weigh Scales
Portable Instrumentation
4 to 20 mA Transmitters

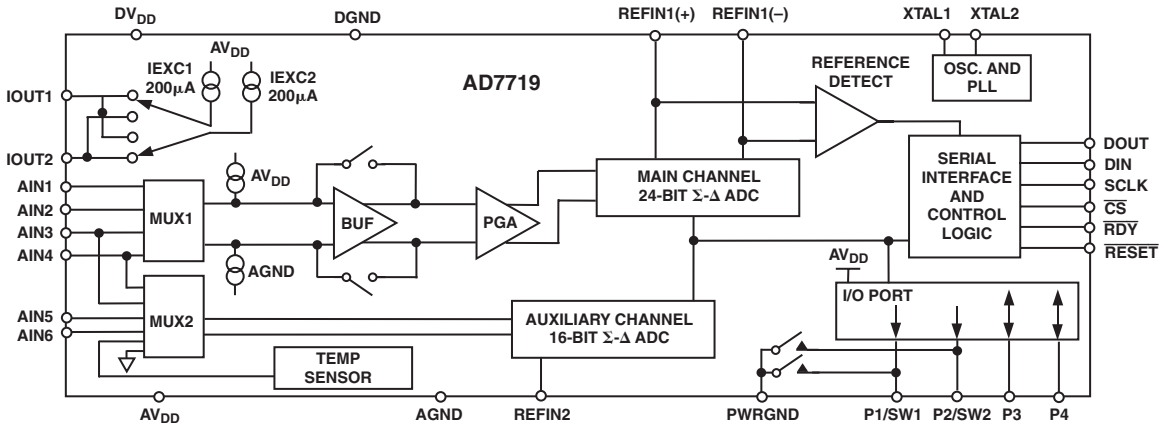
GENERAL DESCRIPTION

The AD7719 is a complete analog front end for low frequency measurement applications. It contains two high resolution Σ-Δ ADCs, switchable matched excitation current sources, low-side power switches, digital I/O port, and temperature sensor. The 24-bit main channel with PGA accepts fully differential, unipolar, and bipolar input signal ranges from 1.024 × REFIN1/128 to 1.024 × REFIN1. Signals can be converted directly from a transducer without the need for signal conditioning. The 16-bit auxiliary channel has an input signal range of REFIN2 or REFIN2/2.

The device operates from a 32 kHz crystal with an on-chip PLL generating the required internal operating frequency. The output data rate from the part is software programmable. The peak-to-peak resolution from the part varies with the programmed gain and output data rate.

The part operates from a single 3 V or 5 V supply. When operating from 3 V supplies, the power dissipation for the part is 4.5 mW with both ADCs enabled and 2.85 mW with only the main ADC enabled in unbuffered mode. The AD7719 is housed in 28-lead SOIC and TSSOP packages.

FUNCTIONAL BLOCK DIAGRAM



REV. A

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AD7719–SPECIFICATIONS[1] (AV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, REFIN(+) = 2.5 V; REFIN(–) = AGND; AGND = DGND = 0 V; XTAL1/XTAL2 = 32.768 kHz Crystal; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	AD7719B	Unit	Test Conditions
ADC CHANNEL SPECIFICATION			
Output Update Rate	5.4	Hz min	Both Channels Synchronized
	105	Hz max	0.732 ms Increments
MAIN CHANNEL			
No Missing Codes[2]	24	Bits min	20 Hz Update Rate
Resolution	13	Bits p-p	±20 mV Range, 20 Hz Update Rate
	18	Bits p-p	±2.56 V Range, 20 Hz Update Rate
Output Noise and Update Rates	See Tables II to V		
Integral Nonlinearity	±10	ppm of FSR max	Typically 2 ppm. $FSR = \frac{2 \times 1.024\ REFIN1}{Gain}$
Offset Error[3]	±3	µV typ	
Offset Error Drift vs. Temperature[4]	±10	nV/°C typ	
Full-Scale Error[5, 6, 7]	±10	µV typ	At the Calibrated Conditions
Gain Drift vs. Temperature[4]	±0.5	ppm/°C typ	
Power Supply Rejection (PSR)	80	dB min	Input Range = ±2.56 V, 100 dB typ. 110 dB typ on ±20 mV Range
ANALOG INPUTS			
Differential Input Voltage Ranges	±1.024 × REFIN1/GAIN	V nom	REFIN1 = REFIN1(+) – REFIN1(–) GAIN = 1 to 128.
ADC Range Matching	±2	µV typ	Input Voltage = 19 mV on All Ranges
Absolute AIN Voltage Limits	AGND + 100 mV	V min	$\overline{BUF}$ = 0; Buffered Mode of Operation
	AV_{DD} – 100 mV	V max	
Analog Input Current[2]			$\overline{BUF}$ = 0
DC Input Current	±1	nA max	
DC Input Current Drift	±5	pA /°C typ	
Absolute AIN Voltage Limits	AGND – 30 mV	V min	$\overline{BUF}$ = 1; Unbuffered mode of operation.
	AV_{DD} + 30 mV	V max	
Analog Input Current			$\overline{BUF}$ = 1. Unbuffered Mode of Operation.
DC Input Current	±125	nA/V typ	Input Current Varies with Input Voltage
DC Input Current Drift	±2	pA/V/°C typ	
Normal-Mode Rejection[2, 8]			
@ 50 Hz	100	dB min	50 Hz ± 1 Hz, 16.65 Hz Update Rate, SF = 82
@ 60 Hz	100	dB min	60 Hz ± 1 Hz, 20 Hz Update Rate, SF = 68
Common-Mode Rejection			
@ DC	90	dB min	Input Range = ±2.56 V, AIN = 1 V. 100 dB typ. 110 dB typ on ±20 mV Range
@ 50 Hz[2]	100	dB min	50 Hz ± 1 Hz, Range = ±2.56 V, AIN = 1 V
@ 60 Hz[2]	100	dB min	60 Hz ± 1 Hz, Range = ±2.56 V, AIN = 1 V
REFERENCE INPUT (REFIN1)			
REFIN1 Voltage	2.5	V nom	REFIN1 = REFIN1(+) – REFIN1(–)
REFIN1 Voltage Range[2]	1	V min	
	AV_{DD}	V max	
REFIN1 Common-Mode Range	AGND – 30 mV	V min	
	AV_{DD} + 30 mV	V max	
Reference DC Input Current	0.5	µA/V typ	
Reference DC Input Current Drift	±0.01	nA/V/°C typ	
Normal-Mode Rejection[2, 8]			
@ 50 Hz	100	dB min	50 Hz ± 1 Hz, SF = 82
@ 60 Hz	100	dB min	60 Hz ± 1 Hz, SF = 68
Common-Mode Rejection			
@ DC	110	dB typ	Input Range = ±2.56 V, AIN = 1 V
@ 50 Hz	110	dB typ	50 Hz ± 1 Hz, Range = 2.56 V, AIN = 1 V
@ 60 Hz	110	dB typ	60 Hz ± 1 Hz, Range = 2.56 V, AIN = 1 V
Reference Detect Levels	0.3	V min	NOXREF Bit Active if VREF < 0.3 V
	0.65	V max	NOXREF Bit Inactive if VREF > 0.65 V
AUXILIARY CHANNEL			
No Missing Codes[2]	16	Bits min	
Resolution	16	Bits p-p	±2.5 V Range, 20 Hz Update Rate
Output Noise and Update Rates	See Tables VI and VIII		
Integral Nonlinearity	±15	ppm of FSR max	

Parameter	AD7719B	Unit	Test Conditions
AUXILIARY CHANNEL (continued)			
Offset Error[3]	±3	µV typ	Selected Channel = AIN5/AIN6
Offset Error Drift vs. Temperature[4]	±10	nV/°C typ	
Full-Scale Error[6, 7]	±0.75	LSB typ	
Gain Drift vs. Temperature[4]	0.5	ppm/°C typ	
Negative Full-Scale Error	±1	LSB typ	
Power Supply Rejection (PSR)	70	dB min	AIN = 1 V Input Range = ±2.5 V, Typically 80 dB
ANALOG INPUTS			
Differential Input Voltage Ranges	±REFIN2	V nom	ARN = 1
	±REFIN2/2	V nom	ARN = 0
Absolute AIN Voltage Limits	AGND – 30 mV	V min	Unbuffered Input
	AV_{DD} + 30 mV	V max	
Analog Input Current			
DC Input Current	±125	nA/V typ	Input Current Varies with Input Voltage
DC Input Current Drift	±2	pA/V/°C typ	
Normal-Mode Rejection[2, 8]			
@ 50 Hz	100	dB min	50 Hz ±1 Hz, SF = 82
@ 60 Hz	100	dB min	60 Hz ±1 Hz, SF = 68
Common-Mode Rejection			
@ DC	85	dB min	Input Range = ±2.5 V, AIN = 1 V
@ 50 Hz[2]	90	dB min	50 Hz ±1 Hz, Range = 2.5 V, AIN = 1 V
@ 60 Hz[2]	90	dB min	60 Hz ±1 Hz, Range = 2.5 V, AIN = 1 V
REFERENCE INPUT (REFIN2)			With Respect to AGND
REFIN2 Voltage	2.5	V nom	
REFIN2 Range[2]	1	V min	
	AV_{DD}	V max	
Reference DC Input Current[2]	0.2	µA/V typ	
Reference DC Input Current Drift	0.003	nA/V/°C typ	
EXCITATION CURRENT SOURCES (IEXC1 and IEXC2)			
Output Current	200	µA nom	
Initial Tolerance at 25°C	±10	% typ	
Drift	200	ppm/°C typ	
Initial Current Matching at 25°C	±1	% typ	Matching between IEXC1 and IEXC2 No Load
Drift Matching	20	ppm/°C typ	
Line Regulation (AV_{DD})	2.1	µA/V max	AV_{DD} = 5 V ± 5%. Typically 1.25 µA/V
Load Regulation	300	nA/V typ	
Output Compliance	AVDD – 0.6	V max	
	AGND – 30 mV	V min	
LOW-SIDE POWER SWITCHES (SW1, SW2)			
R_{ON}	5	Ω max	AV_{DD} = 5 V. Typically 3 Ω
	7	Ω max	AV_{DD} = 3 V. Typically 4.5 Ω
Allowable Current[2]	20	mA max	Continuous Current per Switch
TEMPERATURE SENSOR			
Accuracy	See TPC 5	°C typ	
TRANSDUCER BURNOUT			
AIN(+) Current	–100	nA typ	
AIN(–) Current	100	nA typ	
Initial Tolerance @ 25°C	±15	% typ	
Drift	0.03	%/°C typ	
SYSTEM CALIBRATION[2, 9]			
Full-Scale Calibration Limit	1.05 × FS[10]	V max	
Zero-Scale Calibration Limit	–1.05 × FS	V min	
Input Span	0.8 × FS	V min	
	2.1 × FS	V max	

Parameter	AD7719B	Unit	Test Conditions
LOGIC INPUTS			
All Inputs Except SCLK and XTAL1[2]			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = 5 V
	0.4	V max	DV_{DD} = 3 V
V_{INH}, Input High Voltage	2.0	V min	DV_{DD} = 3 V or 5 V
SCLK Only (Schmitt-Triggered Input)[2]			
$V_{T(+)}$	1.4/2	V min/V max	DV_{DD} = 5 V
$V_{T(-)}$	0.8/1.4	V min/V max	DV_{DD} = 5 V
$V_{T(+)} - V_{T(-)}$	0.3/0.85	V min/V max	DV_{DD} = 5 V
$V_{T(+)}$	0.95/2	V min/V max	DV_{DD} = 3 V
$V_{T(-)}$	0.4/1.1	V min/V max	DV_{DD} = 3 V
$V_{T(+)} - V_{T(-)}$	0.3/0.85	V min/V max	DV_{DD} = 3 V
XTAL1 Only[2]			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = 5 V
V_{INH}, Input High Voltage	3.5	V min	DV_{DD} = 5 V
V_{INL}, Input Low Voltage	0.4	V max	DV_{DD} = 3 V
V_{INH}, Input High Voltage	2.5	V min	DV_{DD} = 3 V
Input Currents	±10	µA max	$V_{IN} = DV_{DD}$
	–70	µA max	V_{IN} = DGND, Typically –40 µA at 5 V and –20 µA at 3 V
Input Capacitance[2]	10	pF typ	All Digital Inputs
LOGIC OUTPUTS (Excluding XTAL2)			
V_{OH}, Output High Voltage[2]	DV_{DD} – 0.6	V min	DV_{DD} = 3 V, I_{SOURCE} = 100 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	DV_{DD} = 3 V, I_{SINK} = 100 µA
V_{OH}, Output High Voltage[2]	4	V min	DV_{DD} = 5 V, I_{SOURCE} = 200 µA
V_{OL}, Output Low Voltage [2]	0.4	V max	DV_{DD} = 5 V, I_{SINK} = 1.6 mA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance	±10	pF typ	
Data Output Coding	Binary		Unipolar Mode
	Offset Binary		Bipolar Mode
I/O PORT[11]			I/O Port Voltages Are with Respect to AV_{DD} and AGND
V_{INL}, Input Low Voltage[2]	0.8	V max	AV_{DD} = 5 V
	0.4	V max	AV_{DD} = 3 V
V_{INH}, Input High Voltage[2]	2.0	V min	AV_{DD} = 3 V or 5 V
Input Currents	±10	µA max	$V_{IN} = AV_{DD}$
	–70	µA max	V_{IN} = AGND, Typically –40 µA at AV_{DD} = 5 V and –20 µA at AV_{DD} = 3 V
Input Capacitance	10	pF typ	All Digital Inputs
V_{OH}, Output High Voltage[2]	AV_{DD} – 0.6	V min	AV_{DD} = 3 V, I_{SOURCE} = 100 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	AV_{DD} = 3 V, I_{SINK} = 100 µA
V_{OH}, Output High Voltage[2]	4	V min	AV_{DD} = 5 V, I_{SOURCE} = 200 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	AV_{DD} = 5 V, I_{SINK} = 1.6 mA
Floating-State Output Leakage Current	±10	µA max	
Floating-State Output Capacitance	±10	pF typ	
START-UP TIME			
From Power-On	300	ms typ	
From Idle Mode	1	ms typ	
From Power-Down Mode	1	ms typ	Osc. Active in Power-Down
	300	ms typ	Osc. Powered Down
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} – AGND	2.7/3.6	V min/max	AV_{DD} = 3 V nom
	4.75/5.25	V min/max	AV_{DD} = 5 V nom
DV_{DD} – DGND	2.7/3.6	V min/max	DV_{DD} = 3 V nom
	4.75/5.25	V min	DV_{DD} = 5 V nom
Power Supply Currents			
DI_{DD} Current (Normal Mode)[12]	0.6	mA max	DV_{DD} = 3 V, 0.5 mA typ
	0.75	mA max	DV_{DD} = 5 V, 0.6 mA typ

Parameter	AD7719B	Unit	Test Conditions
Power Supply Currents (Continued)			
AI_{DD} Current (Main ADC)	1.1	mA max	AV_{DD} = 3 V or 5 V, Buffered Mode, 0.85 mA typ
	0.55	mA max	AV_{DD} = 3 V or 5 V, Unbuffered Mode, 0.45 mA typ
AI_{DD} Current (Aux ADC)	0.3	mA max	AV_{DD} = 3 V or 5 V, 0.25 mA typ
AI_{DD} Current (Main and Aux ADC)	1.25	mA max	AV_{DD} = 3 V or 5 V, Main ADC Buffered, 1 mA typ
DI_{DD} (ADC Disable Mode)[13]	0.35	mA max	DV_{DD} = 3 V, 0.25 mA typ
	0.4	mA max	DV_{DD} = 5 V, 0.3 mA typ
AI_{DD} (ADC Disable Mode)	0.15	mA max	AV_{DD} = 3 V or 5 V
DI_{DD} (Power-Down Mode)	10	μA max	DV_{DD} = 3 V, 32.768 kHz Osc. Running
	2	μA max	DV_{DD} = 3 V, Oscillator Powered Down
	30	μA max	DV_{DD} = 5 V, 32.768 kHz Osc. Running
	8	μA max	DV_{DD} = 5 V, Oscillator Powered Down
AI_{DD} (Power-Down Mode)	1	μA max	AV_{DD} = 3 V or 5 V

NOTES
[1]Temperature range –40°C to +85°C.
[2]Guaranteed by design and/or characterization data on production release.
[3]System zero calibration will remove this error.
[4]A calibration at any temperature will remove this drift error.
[5]The main ADC is factory-calibrated with AV_{DD} = DV_{DD} = 4 V, T_A = 25°C, REFIN1(+) – REFIN1(–) = 2.5 V. If the user power supplies or temperature conditions are significantly different from these, internal full-scale calibration will restore this error to the published specification. System calibration can be used to reduce this error to the order of the noise. Full-scale error applies to both positive and negative full scale.
[6]A system full-scale calibration will remove this error.
[7]A typical gain error of ±10 μV results following a user self-calibration.
[8]Simultaneous 50 Hz and 60 Hz rejection is achieved using 19.8 Hz (SF = 69) update rate. Normal mode rejection in this case is 60 dB min.
[9]After a calibration if the analog input exceeds positive full scale, the converter will output all 1s. If the analog input is less than negative full scale, the device will output all 0s.
[10]FS = Full-Scale Input. FS = 1.024 × REFIN1/Gain on the main ADC, where REFIN1 = REFIN1(+) – REFIN1(–). FS = REFIN2 on the aux ADC when ARN = 1 in the aux ADC control register (AD1CON) and REFIN2/2 on the aux ADC when ARN = 0.
[11]Input and output levels on the I/O Port are with respect to AV_{DD} and AGND.
[12]Normal mode refers to the case where both main and aux ADCs are running.
[13]ADC disable is entered by setting both the AD0EN and AD1EN bits in the main and aux ADC control registers to a 0 and setting the mode bits (MD2, MD1, MD0) in the mode register to non-0.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]
(T_A = 25°C, unless otherwise noted.)

AV_{DD} to AGND ..... –0.3 V to +7 V
AV_{DD} to DGND ..... –0.3 V to +7 V
DV_{DD} to AGND ..... –0.3 V to +7 V
DV_{DD} to DGND ..... –0.3 V to +7 V
AGND to DGND[2]. ..... –20 mV to +20 mV
PWRGND to AGND ..... –20 mV to +20 mV
AV_{DD} to DV_{DD} ..... –5 V to +5 V
Analog Input Voltage to AGND .... –0.3 V to AV_{DD} +0.3 V
Reference Input Voltage to AGND .. –0.3 V to AV_{DD} +0.3 V
Total AIN/REFIN Current (Indefinite) ..... 30 mA
Digital Input Voltage to DGND .... –0.3 V to DV_{DD} +0.3 V
Digital Output Voltage to DGND ... –0.3 V to DV_{DD} +0.3 V
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
SOIC Package
  θ_{JA} Thermal Impedance ..... 71.4°C/W
  θ_{JC} Thermal Impedance ..... 23°C/W
TSSOP Package
  θ_{JA} Thermal Impedance ..... 97.9°C/W
  θ_{JC} Thermal Impedance ..... 14°C/W
Lead Temperature, Soldering
  Vapor Phase (60 sec) ..... 215°C
  Infrared (15 sec) ..... 220°C

NOTES
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] AGND and DGND are connected internally within the AD7719.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7719BR	–40°C to +85°C	SOIC	R-28
AD7719BRU	–40°C to +85°C	TSSOP	RU-28
EVAL-AD7719EB		Evaluation Board	

TIMING CHARACTERISTICS[1, 2] (AV_{DD} = 2.7 V to 3.6 V or AV_{DD} = 4.75 V to 5.25 V; DV_{DD} = 2.7 V to 3.6 V or DV_{DD} = 4.75 V to 5.25 V; AGND = DGND = 0 V; X_{TAL} = 32.768 kHz; Input Logic 0 = 0 V, Logic 1 = DV_{DD}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Unit	Conditions/Comments
t_1	32.768	kHz typ	Crystal Oscillator Frequency
t_2	50	ns min	$\overline{RESET}$ Pulsewidth
Read Operation			
t_3	0	ns min	$\overline{RDY}$ to $\overline{CS}$ Setup Time
t_4	0	ns min	$\overline{CS}$ Falling Edge to SCLK Active Edge Setup Time[3]
t_5[4]	0	ns min	SCLK Active Edge to Data Valid Delay[3]
	60	ns max	DV_{DD} = 4.75 V to 5.25 V
	80	ns max	DV_{DD} = 2.7 V to 3.6 V
t_{5A}[4, 5]	0	ns min	$\overline{CS}$ Falling Edge to Data Valid Delay[3]
	60	ns max	DV_{DD} = 4.75 V to 5.25 V
	80	ns max	DV_{DD} = 2.7 V to 3.6 V
t_6	100	ns min	SCLK High Pulsewidth
t_7	100	ns min	SCLK Low Pulsewidth
t_8	0	ns min	$\overline{CS}$ Rising Edge to SCLK Inactive Edge Hold Time[3]
t_9[6]	10	ns min	Bus Relinquish Time after SCLK Inactive Edge[3]
	80	ns max	
t_{10}	100	ns max	SCLK Active Edge to $\overline{RDY}$ High[3, 7]
Write Operation			
t_{11}	0	ns min	$\overline{CS}$ Falling Edge to SCLK Active Edge Setup Time[3]
t_{12}	30	ns min	Data Valid to SCLK Edge Setup Time
t_{13}	25	ns min	Data Valid to SCLK Edge Hold Time
t_{14}	100	ns min	SCLK High Pulsewidth
t_{15}	100	ns min	SCLK Low Pulsewidth
t_{16}	0	ns min	$\overline{CS}$ Rising Edge to SCLK Edge Hold Time

NOTES

[1]Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.

[2]See Figures 2 and 3.

[3]SCLK active edge is falling edge of SCLK.

[4]These numbers are measured with the load circuit of Figure 1 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

[5]This specification only comes into play if $\overline{CS}$ goes low while SCLK is low. It is required primarily for interfacing to DSP machines.

[6]These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the Timing Characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

[7]$\overline{RDY}$ returns high after a read of both ADCs. The same data can be read again, if required, while $\overline{RDY}$ is high, although care should be taken that subsequent reads do not occur close to the next output update.

Specifications subject to change without notice.

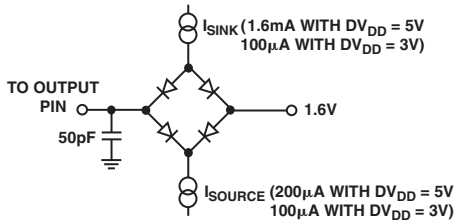


Figure 1. Load Circuit for Timing Characterization

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7719 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DIGITAL INTERFACE

As previously outlined, the AD7719's programmable functions are controlled using a set of on-chip registers. Data is written to these registers via the part's serial interface; read access to the on-chip registers is also provided by this interface. All communications to the part must start with a write operation to the Communications register. After power-on or $\overline{\text{RESET}}$, the device expects a write to its Communications register. The data written to this register determines whether the next operation to the part is a read or a write operation and also determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part starts with a write operation to the Communications register followed by a write to the selected register. A read operation from any other register on the part (including the output data register) starts with a write operation to the Communications register followed by a read operation from the selected register.

The AD7719's serial interface consists of five signals: $\overline{\text{CS}}$, SCLK, DIN, DOUT, and $\overline{\text{RDY}}$. The DIN line is used for transferring data into the on-chip registers while the DOUT line is used for accessing data from the on-chip registers. SCLK is the serial clock input for the device, and all data transfers (either on DIN or DOUT) take place with respect to this SCLK signal. The $\overline{\text{RDY}}$ line is used as a status signal to indicate when data is ready to be read from the AD7719's data register. $\overline{\text{RDY}}$ goes low when a new data-word is available in the output register of either the main or aux ADCs. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the output register to indicate when *not* to read from the device to ensure that a data read is not attempted while the register is being updated. $\overline{\text{CS}}$ is used to select the device. It can be used to decode the AD7719 in systems where a number of parts are connected to the serial bus.

Figures 2 and 3 show timing diagrams for interfacing to the AD7719 with $\overline{\text{CS}}$ used to decode the part. Figure 3 is for a read operation from the AD7719's output shift register while Figure 2 shows a write operation to the input shift register. It is possible to read the same data twice from the output register even though the $\overline{\text{RDY}}$ line returns high after the first read operation. Care must be taken, however, to ensure that the read operations have been completed before the next output update is about to take place.

The AD7719 serial interface can operate in 3-wire mode by tying the $\overline{\text{CS}}$ input low. In this case, the SCLK, DIN, and DOUT lines are used to communicate with the AD7719, and the status of RDY bits (RDY0 and RDY1) can be obtained by interrogating the STATUS register. This scheme is suitable for interfacing to microcontrollers. If $\overline{\text{CS}}$ is required as a decoding signal, it can be generated from a port bit. For microcontroller interfaces, it is recommended that the SCLK idles high between data transfers.

The AD7719 can also be operated with $\overline{\text{CS}}$ used as a frame synchronization signal. This scheme is suitable for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{\text{CS}}$ since $\overline{\text{CS}}$ would normally occur after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers provided the timing numbers are obeyed.

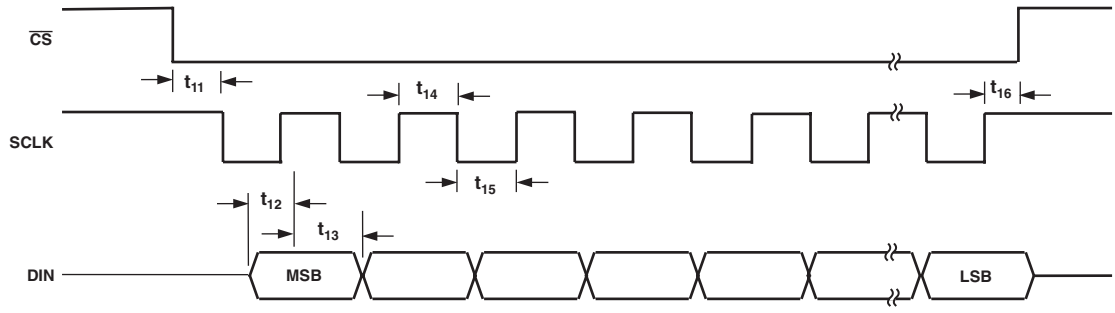


Figure 2. Write Cycle Timing Diagram

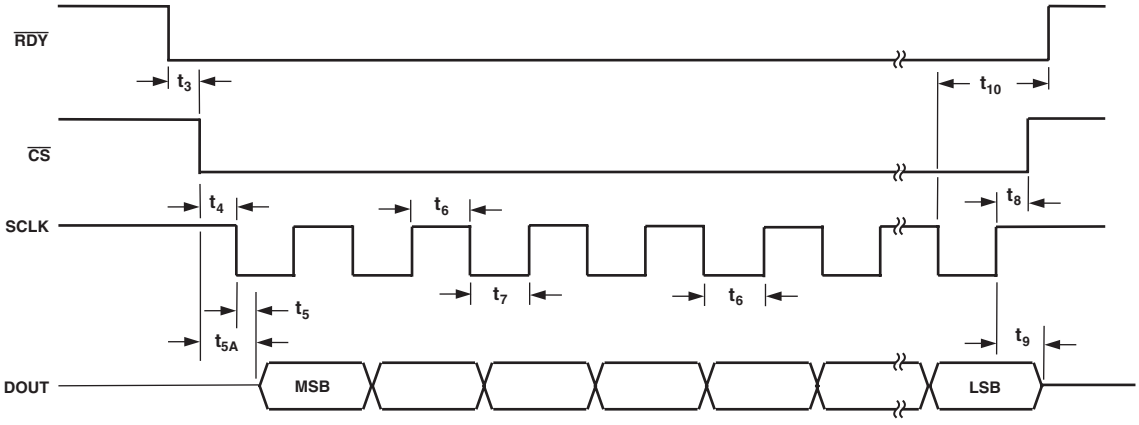
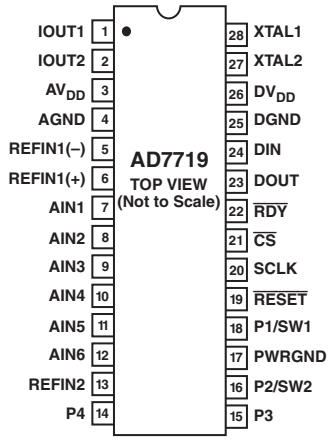


Figure 3. Read Cycle Timing Diagram

The serial interface can be reset by exercising the $\overline{\text{RESET}}$ input on the part. It can also be reset by writing a series of 1s on the DIN input. If a logic 1 is written to the AD7719 DIN line for at least 32 serial clock cycles, the serial interface is reset. This ensures that in 3-wire systems, if the interface gets lost, either via a software error or by some glitch in the system, it can be reset back to a known state. This state returns the interface to where the AD7719 is expecting a write operation to its Communications register. This operation resets the contents of all registers to their power-on reset values.

Some microprocessor or microcontroller serial interfaces have a single serial data line. In this case, it is possible to connect the AD7719's DATA OUT and DATA IN lines together and connect them to the single data line of the processor. A 10 kΩ pull-up resistor should be used on this single data line. In this case, if the interface gets lost, because the read and write operations share the same line, the procedure to reset it to a known state is somewhat different than previously described. It requires a read operation of 24 serial clocks followed by a write operation where a logic 1 is written for at least 32 serial clock cycles to ensure that the serial interface is back in a known state.

PIN CONFIGURATION

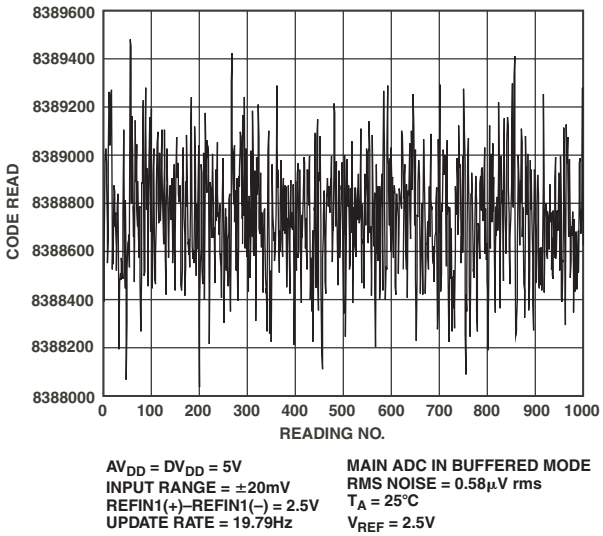


PIN FUNCTION DESCRIPTIONS

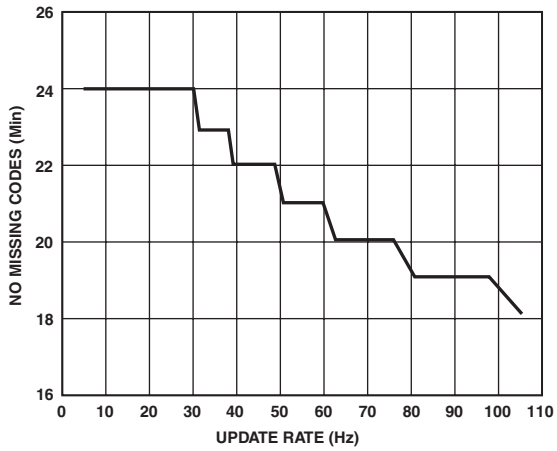
Pin No.	Mnemonic	Function
1	IOUT1	Output for Internal 200 μA Excitation Current Source. Current source IEXC1 and/or IEXC2 can be switched to this output.
2	IOUT2	Output for Internal 200 μA Excitation Current Source. Current source IEXC1 and/or IEXC2 can be switched to this output.
3	AV_{DD}	Analog Supply Voltage.
4	AGND	Analog Ground.
5	REFIN1(–)	Negative Reference Input for Main ADC Channel. This reference input can lie anywhere between AGND and AV_{DD} – 1 V.
6	REFIN1(+)	Positive Reference Input for Main ADC Channel. REFIN1(+) can lie anywhere between AV_{DD} and AGND + 1 V. The nominal reference voltage (REFIN1(+) – REFIN1(–)) is 2.5 V, but the part is functional with a reference range from 1 V to AV_{DD}.
7	AIN1	Analog Input. AIN1 is dedicated to the main channel.
8	AIN2	Analog Input. AIN2 is dedicated to the main channel.
9	AIN3	Analog Input. AIN3 can be multiplexed to either the main or auxiliary channel.
10	AIN4	Analog Input. AIN4 can be multiplexed to either the main or auxiliary channel.
11	AIN5	Analog Input. AIN5 is dedicated to the auxiliary channel and is referenced to AIN6 or AGND.
12	AIN6	Analog Input. AIN6 is dedicated to the auxiliary channel. It forms a differential input pair with AIN5 in fully differential input mode or is referenced to AGND in pseudodifferential mode.
13	REFIN2	Single-Ended Reference Input for Auxiliary Channel. The nominal input reference is 2.5 V. The auxiliary channel will function with an input reference range from 1 V to AV_{DD}.
14	P4	General-Purpose I/O Bit. The input and output voltage levels are referenced to AV_{DD} and AGND.
15	P3	General-Purpose I/O Bit. The input and output voltage levels are referenced to AV_{DD} and AGND.

PIN FUNCTION DESCRIPTIONS (continued)

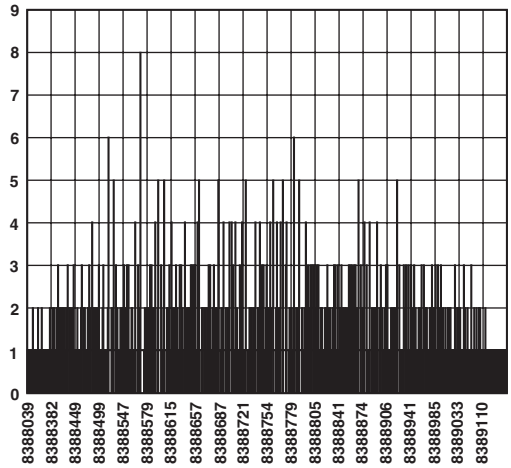
Pin No.	Mnemonic	Function
16	P2/SW2	Dual-Purpose Pin. It can act as a general-purpose output (P2) bit referenced between AV_{DD} and AGND or as a low-side power switch (SW2) to PWRGND.
17	PWRGND	Ground Point for the Low-Side Power Switches SW2 and SW1. PWRGND must be tied to AGND.
18	P1/SW1	Dual-Purpose Pin. It can act as a general-purpose output (P1) bit referenced between AV_{DD} and AGND or as a low-side power switch (SW1) to PWRGND.
19	$\overline{\text{RESET}}$	Digital Input Used to Reset the ADC to Its Power-On Reset Status. This pin has a weak pull-up internally to DV_{DD}.
20	SCLK	Serial Clock Input for Data Transfers to and from the ADC. The SCLK has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the AD7719 in smaller batches of data. A weak pull-up to DV_{DD} is provided on the SCLK input.
21	$\overline{\text{CS}}$	Chip Select Input. This is an active low logic input used to select the AD7719. $\overline{\text{CS}}$ can be used to select the AD7719 in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{\text{CS}}$ can be hardwired low, allowing the AD7719 to be operated in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device. A weak pull-up to DV_{DD} is provided on the CS input.
22	$\overline{\text{RDY}}$	$\overline{\text{RDY}}$ is a logic low status output from the AD7719. $\overline{\text{RDY}}$ is low if either the main ADC or auxiliary ADC channel has valid data in its data register. This output returns high on completion of a read operation from the data register. If data is not read, $\overline{\text{RDY}}$ will return high prior to the next update, indicating to the user that a read operation should not be initiated. The $\overline{\text{RDY}}$ pin also returns low following the completion of a calibration cycle. The $\overline{\text{RDY}}$ pin is effectively the digital NOR function of the RDY0 and RDY1 bits in the Status register. If one of the ADCs is disabled, the $\overline{\text{RDY}}$ pin reflects the active ADC. $\overline{\text{RDY}}$ does not return high after a calibration until the mode bits are written to, enabling a new conversion or calibration. Since the $\overline{\text{RDY}}$ pin provides information on both the main and aux ADCs, when either the main or aux ADC is disabled, it is recommended to immediately read its data register to ensure that its RDY bit goes inactive and releases the $\overline{\text{RDY}}$ pin to indicate output data updates on the remaining active ADC.
23	DOUT	Serial Data Output Accessing the Output Shift Register of the AD7719. The output shift register can contain data from any of the on-chip data, calibration, or control registers.
24	DIN	Serial Data Input Accessing the Input Shift Register on the AD7719. Data in this shift register is transferred to the calibration or control registers within the ADC depending on the selection bits of the Communications register. A weak pull-up to DV_{DD} is provided on the DIN input.
25	DGND	Ground Reference Point for the Digital Circuitry.
26	DV_{DD}	Digital Supply Voltage, 3 V or 5 V Nominal.
27	XTAL2	Output from the 32 kHz Crystal Oscillator Inverter.
28	XTAL1	Input to the 32 kHz Crystal Oscillator Inverter.



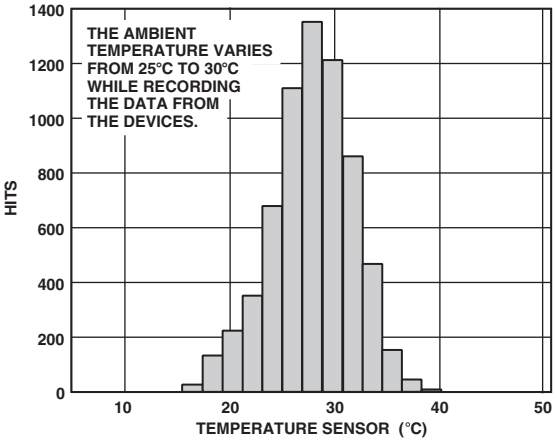
TPC 1. Typical Noise Plot on ±20 mV Input Range with 19.79 Hz Update Rate



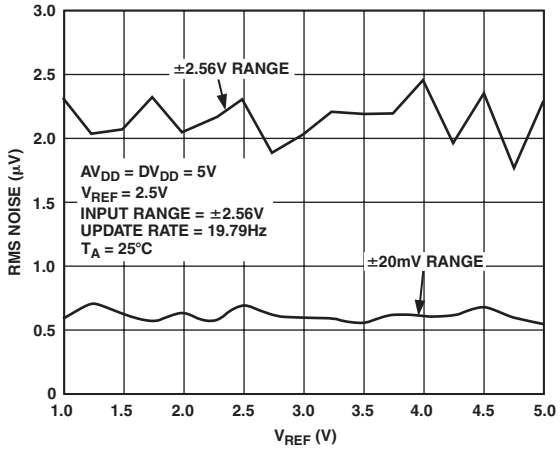
TPC 4. No-Missing-Codes Performance



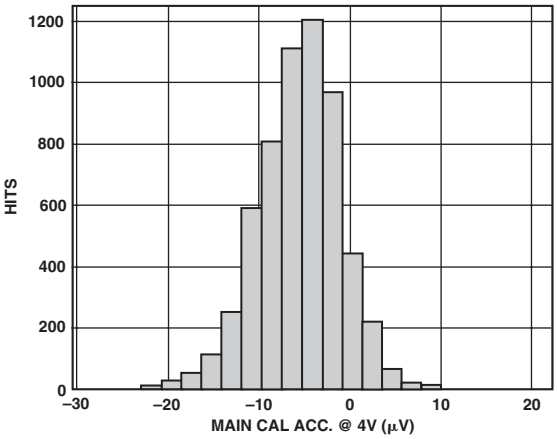
TPC 2. Noise Distribution Histogram



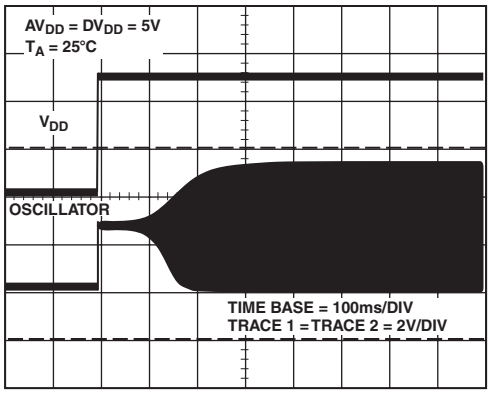
TPC 5. Temperature Sensor Accuracy



TPC 3. RMS Noise vs. Reference Input



TPC 6. Full-Scale Error Distribution



TPC 7. Typical Oscillator Power-Up

DUAL-CHANNEL ADC CIRCUIT INFORMATION

Overview

The AD7719 incorporates two independent Σ-Δ ADC channels (main and auxiliary) with on-chip digital filtering intended for the measurement of wide dynamic range, low frequency signals such as those in weigh-scale, strain gage, pressure transducer, or temperature measurement applications.

Main Channel

This channel is intended to convert the primary sensor input. This channel can be operated in buffered or unbuffered mode, and can be programmed to have one of eight input voltage ranges from ±20 mV to ±2.56 V. This channel can be configured as either two fully differential inputs (AIN1/AIN2 and AIN3/AIN4) or three pseudodifferential input channels (AIN1/AIN4, AIN2/AIN4, and AIN3/AIN4). Buffering the input channel means that the part can accommodate significant source impedances on the analog input and that R, C filtering (for noise rejection or RFI reduction) can be placed on the analog inputs if required. Operating in unbuffered mode leads to lower power consumption in low power applications, but care must be exercised in unbuffered mode because source impedances can introduce gain errors. The main ADC also features sensor burnout currents that can be switched on and off. These currents can be used to check that a transducer is still operational before attempting to take measurements.

The ADC employs a Σ-Δ conversion technique to realize up to 24 bits of no-missing-codes performance. The Σ-Δ modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A Sinc^3 programmable low-pass filter is then employed to decimate the modulator output data stream to give a valid data conversion result at programmable output rates from 5.35 Hz (186.77 ms) to 105.03 Hz (9.52 ms). A chopping scheme is also employed to minimize ADC channel offset errors. A block diagram of the main ADC input channel is shown in Figure 4. The sampling frequency of the modulator loop is many times higher than the bandwidth of the input signal. The integrator in the modulator shapes the quantization noise (which results from the analog-to-digital conversion) so that the noise is pushed toward one-half of the modulator frequency. The output of the Σ-Δ modulator feeds directly into the digital filter. The digital filter then band-limits the response to a frequency significantly lower than one-half of the modulator frequency. In this manner, the 1-bit output of the comparator is translated into a band-limited, low noise output from the AD7719 ADC. The AD7719 filter is a low-pass, Sinc^3, or (SIN(x)/x)^3 filter whose primary function is to remove the quantization noise introduced at the modulator. The cutoff frequency and decimated output data rate of the filter are programmable via the SF word loaded to the filter register.

A chopping scheme is employed where the complete signal chain is chopped, resulting in excellent dc offset and offset drift specifications, and is extremely beneficial in applications where drift, noise rejection, and optimum EMI rejection are important factors. With chopping, the ADC repeatedly reverses its inputs. The decimated digital output words from the Sinc^3 filters therefore have a positive offset and negative offset term included. As a result, a final summing stage is included so that each output word from the filter is summed and averaged with the previous filter output to produce a new valid output result to be written to the ADC data register.

Auxiliary Channel

The Auxiliary (Aux) channel is intended to convert supplementary inputs such as those from a cold junction diode or thermistor. This channel is unbuffered and has an input range of ±REFIN2 or ±REFIN2/2, determined by the ARN bit in the auxiliary ADC control register (AD1CON). AIN3 and AIN4 can be multiplexed into the auxiliary channel as single-ended inputs with respect to AGND, while AIN5 and AIN6 can operate as a differential input pair. With AIN6 tied to AGND, AIN5 can be operated as an additional single-ended input. A block diagram of the auxiliary ADC channel is shown in Figure 5.

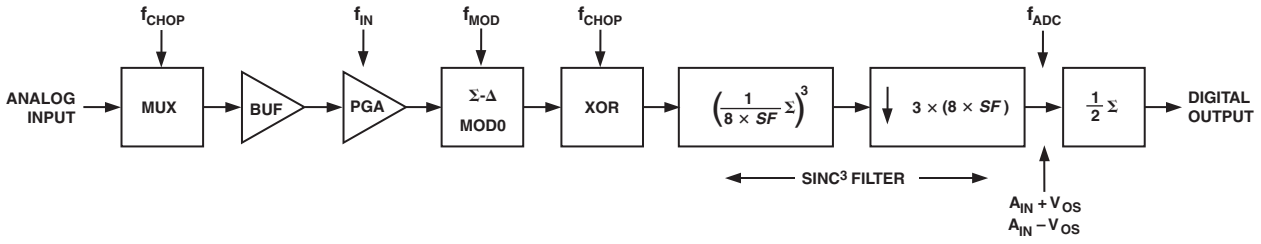


Figure 4. Main ADC Channel Block Diagram

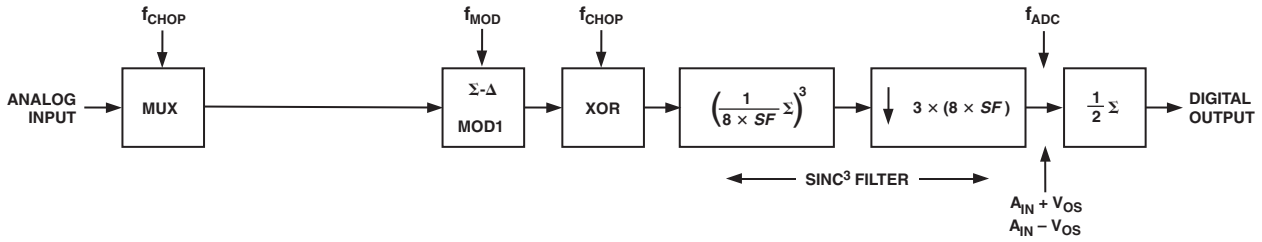


Figure 5. Auxiliary ADC Channel Block Diagram

Both Channels

The operation of the aux channel is identical to the main channel with the exception that there is no PGA on the aux channel. The input chopping is incorporated into the input multiplexer while the output chopping is accomplished by an XOR gate at the output of the modulator. The chopped modulator bit stream is applied to a Sinc^3 filter. The programming of the Sinc^3 decimation factor is restricted to an 8-bit register SF; the actual decimation factor is the register value times 8. The decimated output rate from the Sinc^3 filter (and the ADC conversion rate) will therefore be

$$f_{ADC} = \frac{1}{3} \times \left(\frac{1}{8 \times SF} \right) \times f_{MOD}$$

where:

f_{ADC} is the ADC update rate.

SF is the decimal equivalent of the word loaded to the filter register.

f_{MOD} is the modulator sampling rate of 32.768 kHz.

Programming the filter register determines the update rate for both the main and aux ADC. Both ADCs operate with the same update rate.

The chop rate of the channel is half the output data rate.

The frequency response of the filter H (f) is as follows:

$$\left(\frac{1}{SF \times 8} \times \frac{\sin(SF \times 8 \times \pi \times f/f_{MOD})}{\sin(\pi \times f/f_{MOD})} \right)^3 \times \left(\frac{1}{2} \times \frac{\sin(2 \times \pi \times f/f_{OUT})}{\sin(\pi \times f/f_{OUT})} \right)$$

where:

f_{MOD} = 32,768 Hz

SF = value programmed into SF SFR.

$f_{OUT} = f_{MOD}/(SF \times 8 \times 3)$

The following shows plots of the filter frequency response for the SF words shown in Table I. The overall frequency response is the product of a Sinc^3 and a sinc response. There are Sinc^3 notches at integer multiples of $3 \times f_{ADC}$ and there are sinc notches at odd integer multiples of $f_{ADC}/2$. The 3 dB frequency for all values of SF obeys the following equation:

$$f\left(3\ dB\right) = 0.24 \times f_{ADC}$$

The signal chain is chopped as shown in Figures 4 and 5. The chop frequency is

$$f_{CHOP} = \left(\frac{f_{ADC}}{2} \right)$$

As shown in the block diagram, the Sinc^3 filter outputs alternately contain $+V_{OS}$ and $-V_{OS}$, where V_{OS} is the respective channel offset. This offset is removed by performing a running average of 2. This average by 2 means that the settling time to any change in programming of the ADC will be twice the normal conversion time, while an asynchronous step change on the analog input will not be fully reflected until the third subsequent output.

$$t_{SETTLE} = \left(\frac{2}{f_{ADC}} \right) = 2 \times t_{ADC}$$

The allowable range for SF is 13 to 255, with a default of 69 (0x45). The corresponding conversion rates, conversion times, and settling times are tabulated in Table I. Note that the conversion time increases by 0.732 ms for each increment in SF.

Table I. ADC Conversion and Settling Times for Various SF Words

SF Word	Data Update Rate f_{ADC} (Hz)	Settling Time t_{SETTLE} (ms)
13	105.3	19.04
69 (Default)	19.79	101.07
255	5.35	373.54

Normal mode rejection is the major function of the digital filter on the AD7719. The normal mode 50 Hz ± 1 Hz rejection with an SF word of 82 is typically –100 dB. The 60 Hz ± 1 Hz rejection with SF = 68 is typically –100 dB. Simultaneous 50 Hz and 60 Hz rejection of better than 60 dB is achieved with an SF of 69. Choosing an SF word of 69 places notches at both 50 Hz and 60 Hz. Figures 6 to 9 show the filter rejection for a selection of SF words.

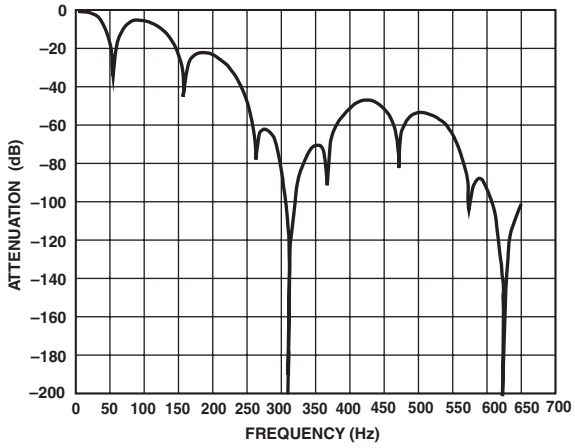


Figure 6. Filter Profile with SF = 13

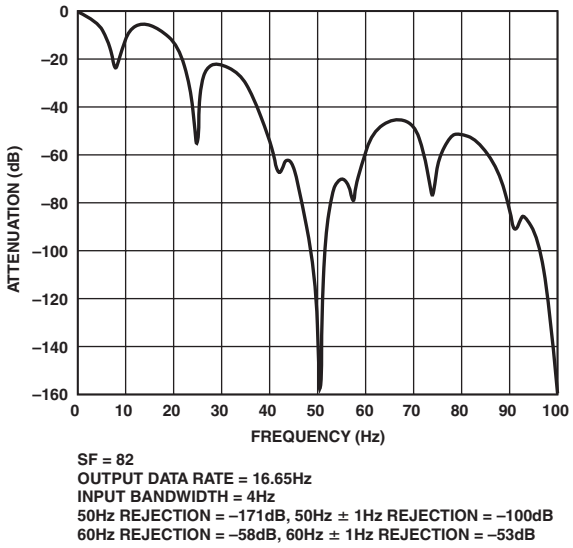


Figure 7. Filter Profile with SF = 82

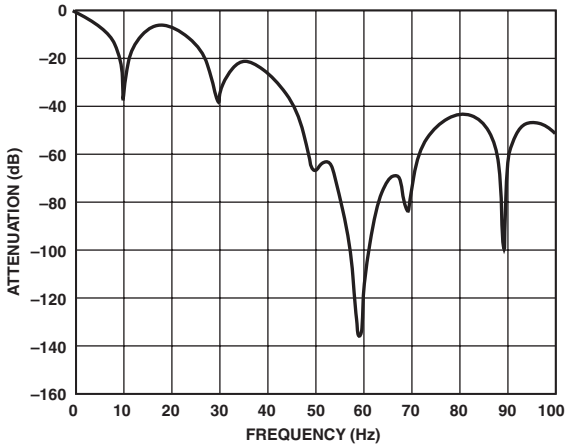


Figure 8. Filter Profile with Default SF = 69 Giving Filter Notches at Both 50 Hz and 60 Hz

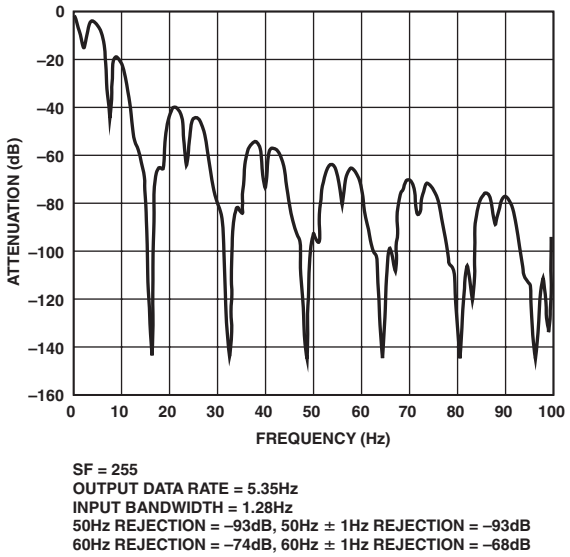


Figure 9. Filter Profile with SF = 255

MAIN AND AUXILIARY ADC NOISE PERFORMANCE

Tables II to VII show the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5 LSB) for a selection of output update rates on both the main and auxiliary ADCs. The numbers are typical and are generated at a differential input voltage of 0 V. The output update rate is selected via the SF7 to SF0 bits in the Filter register. It is important to note that the peak-to-peak resolution figures represent the resolution for which there will be no code flicker within a six-sigma limit. The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. Secondly, when the analog input is converted into the digital domain, quantization noise is added. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. The numbers in the tables are given for the bipolar input ranges. For the unipolar ranges, the rms noise numbers will be the same as the bipolar range, but the peak-to-peak resolution is now based on half the signal range, which effectively means losing one bit of resolution.

Table II. Typical Output RMS Noise vs. Input Range and Update Rate for Main ADC (Buffered Mode) Output RMS Noise in μV

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	1.50	1.50	1.60	1.75	3.50	4.50	6.70	11.75
69	19.79	0.60	0.65	0.65	0.65	0.65	0.95	1.40	2.30
255	5.35	0.35	0.35	0.37	0.37	0.37	0.51	0.82	1.25

Table III. Peak-to-Peak Resolution vs. Input Range and Update Rate for Main ADC (Buffered Mode) Peak-to-Peak Resolution in Bits

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	12	13	14	15	15	15.5	16	16
69	19.79	13	14	15	16	17	17.5	18	18.5
255	5.35	14	15	16	17	18	18.5	18.8	19.2

Table IV. Typical Output RMS Noise vs. Input Range and Update Rate for Main ADC (Unbuffered Mode) Output RMS Noise in μV

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	1.27	1.27	1.35	1.48	2.95	3.82	5.69	10.2
69	19.79	0.52	0.56	0.56	0.56	0.56	0.82	1.21	2.00
255	5.35	0.30	0.30	0.32	0.32	0.32	0.44	0.71	1.10

Table V. Peak-to-Peak Resolution vs. Input Range and Update Rate for Main ADC (Unbuffered Mode) Peak-to-Peak Resolution in Bits

SF Word	Data Update Rate (Hz)	Input Range							
		±20 mV	±40 mV	±80 mV	±160 mV	±320 mV	±640 mV	±1.28 V	±2.56 V
13	105.3	12	13	14	15	15	15.5	16	16
69	19.79	13	14	15	16	17	17.5	18	18.5
255	5.35	14	15	16	17	18	18.5	19	19.5

Table VI. Typical Output RMS Noise vs. Update Rate for Auxiliary ADC (Unbuffered Mode)

SF Word	Data Update Rate (Hz)	Input Range ±2.5 V
13	105.3	10.75 μV
69	19.79	2.00 μV
255	5.35	1.15 μV

Table VII. Peak-to-Peak Resolution vs. Update Rate for Auxiliary ADC (Unbuffered Mode)

SF Word	Data Update Rate (Hz)	Input Range ±2.5 V
13	105.3	16 Bits
69	19.79	16 Bits
255	5.35	16 Bits

ON-CHIP REGISTERS

Both the main and auxiliary ADC channels are controlled and configured via a number of on-chip registers as shown in Figure 10 and described in more detail in the following pages. In the following descriptions, *SET* implies a logic 1 state and *CLEARED* implies a logic 0 state, unless otherwise stated.

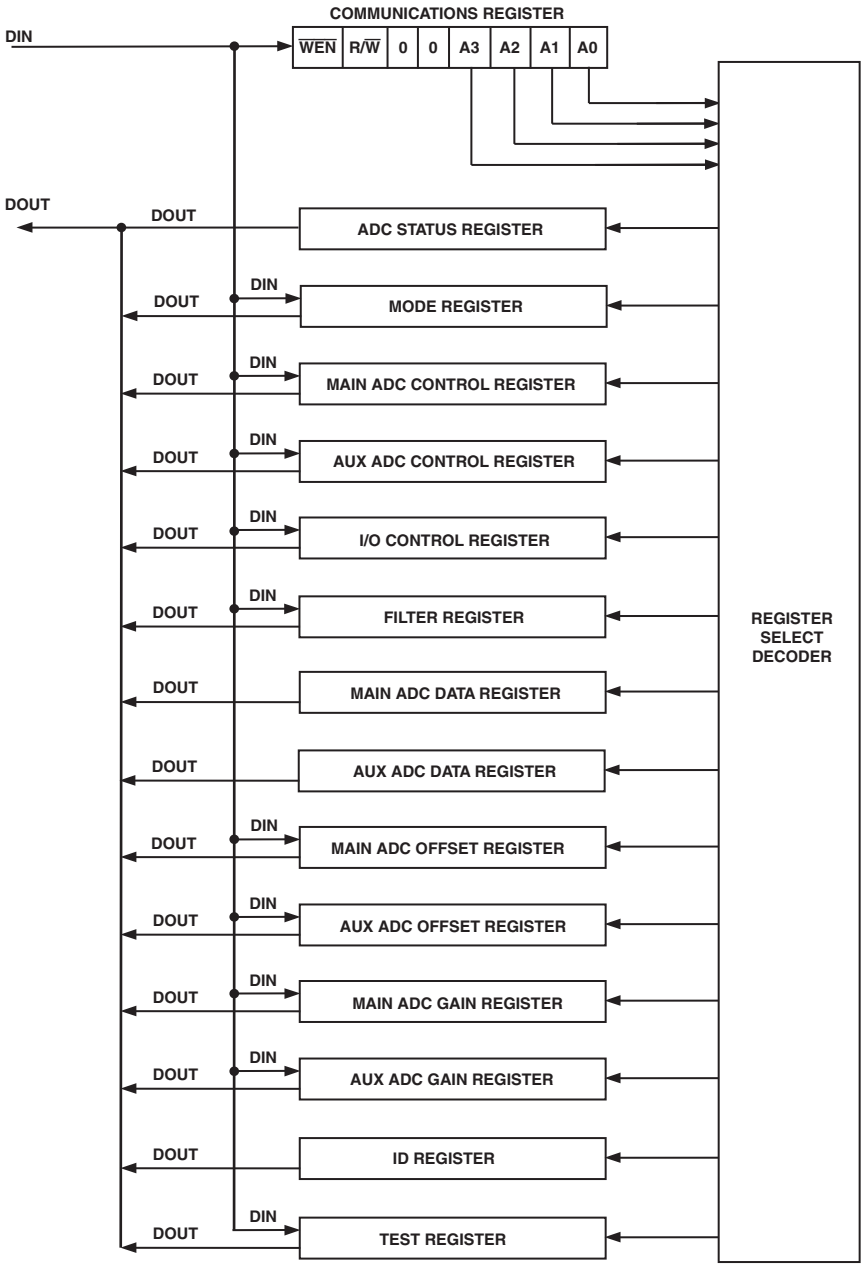


Figure 10. On-Chip Registers

Table VIII. Registers—Quick Reference Guide

Register Name	Type	Size	Power-On/Reset Default Value	Function
Communications	Write Only	8 Bits	Not Applicable	All operations to other registers are initiated through the Communications register. This controls whether subsequent operations are read or write operations and also selects the register for that subsequent operation.

MSB							LSB
$\overline{WEN}$	R/$\overline{W}$	0	0	A3	A2	A1	A0

Register Name	Type	Size	Power-On/Reset Default Value	Function
Status Register	Read Only	8 Bits	0x00	Provides status information on conversions, calibrations, error conditions, and the validity of the reference voltage.

MSB							LSB
RDY0	RDY1	CAL	NOREF	ERR0	ERR1	0	LOCK

Register Name	Type	Size	Power-On/Reset Default Value	Function
Mode Register	Read/Write	8 Bits	0x00	Controls functions such as mode of operation, channel configuration, and oscillator operation in power-down.

MSB							LSB
0	$\overline{BUF}$	0	CHCON	OSCPD	MD2	MD1	MD0

Main ADC (AD0CON)

Register Name	Type	Size	Power-On/Reset Default Value	Function
Control Register	Read/Write	8 Bits	0x07	This register is used to enable the main ADC and to configure the main ADC for range, channel selection, 16-/24-bit operation, and unipolar or bipolar operation.

MSB							LSB
AD0EN	WL	CH1	CH0	U/$\overline{B}$	RN2	RN1	RN0

Aux ADC (AD1CON)

Register Name	Type	Size	Power-On/Reset Default Value	Function
Control Register	Read/Write	8 Bits	0x01	This register is used to enable the aux ADC and to configure the Aux ADC for range, channel selection, unipolar or bipolar operation, and input range.

MSB							LSB
AD1EN	ACH2	ACH1	ACH0	U/$\overline{B}$	0	0	ARN

I/O (IOCON)

Register Name	Type	Size	Power-On/Reset Default Value	Function
Control Register	Read/Write	16 Bits	0x0000	This register is used to control and configure the various excitation and burnout current source options available on-chip along with controlling the I/O port.

MSB							
PSW2	PSW1	0	BO	I2PIN	I1PIN	I2EN	I1EN
							LSB
P4DIR	P3DIR	P2EN	P1EN	P4DAT	P3DAT	P2DAT	P1DAT

Register Name	Type	Size	Power-On/Reset Default Value	Function
Filter Register	Read/Write	8 Bits	0x45	This register determines the amount of averaging performed by the sinc filter and consequently determines the data update rate of the AD7719. The filter register determines the update rate for both the main and aux ADCs.

MSB							LSB
SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0

Register Name	Type	Size	Power-On/Reset Default Value	Function
Main ADC (DATA0)				
Data Register	Read Only	16 Bits or 24 Bits	0x00 0000	Provides the most up-to-date conversion result from the main ADC. Main ADC data register length can be programmed to be 16-bit or 24-bit.
Aux ADC (DATA1)				
Data Register	Read Only	16 Bits	0x0000	Provides the most up-to-date conversion result from the auxiliary ADC. Aux ADC data register length is 16 bits.
Main ADC				
Offset Register	Read/Write	24 Bits	0x80 0000	Contains a 24-bit word that is the offset calibration coefficient for the part. The contents of this register are used to provide offset correction on the output from the digital filter. There are three offset registers on the part and these are associated with input channel pairs as outlined in the AD0CON register.
Main ADC				
Gain Register	Read/Write	24 Bits	0x5X XXX5	Contains a 24-bit word that is the gain calibration coefficient for the part. The contents of this register are used to provide gain correction on the output from the digital filter. There are three Gain registers on the part, which are associated with input channel pairs as outlined in the AD0CON register.
Aux ADC				
Offset Register	Read/Write	16 Bits	0x8000	Contains a 16-bit word that is the offset calibration coefficient for the part. The contents of this register are used to provide offset correction on the output from the digital filter.
Aux ADC				
Gain Register	Read/Write	24 Bits	0x59XX	Contains a 16-bit word that is the gain calibration coefficient for the part. The contents of this register are used to provide gain correction on the output from the digital filter.
ID Register	Read	8 Bits	0x0X	Contains an 8-bit byte that is the identifier for the part.
Test Registers	Read/Write	16 Bits	0x0000	Controls the test modes of the part, which are used when testing the part. **The user is advised not to change the contents of these registers.**

Communications Register (A3, A2, A1, A0 = 0, 0, 2, 0)
The Communications register is an 8-bit write-only register. All communications to the part must start with a write operation to the Communications register. The data written to the Communications register determines whether the next operation is a read or write operation, and to which register this operation takes place. For read or write operations, once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the Communications register. This is the default state of the interface, and on power-up or after a RESET, the AD7719 is in this default state waiting for a write operation to the Communications register. In situations where the interface sequence is lost, a write operation of at least 32 serial clock cycles with DIN high returns the AD7719 to this default state by resetting the part. Table IX outlines the bit designations for the Communications register. CR0 through CR7 indicate the bit location, with CR denoting that the bits are in the Communications register. CR7 denotes the first bit of the data stream.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
$\overline{\text{WEN}}$ (0)	R/$\overline{\text{W}}$ (0)	0 (0)	0 (0)	A3 (0)	A2 (0)	A1 (0)	A0 (0)

Table IX. Communications Register Bit Designations

Bit Location	Bit Name	Description
CR7	$\overline{\text{WEN}}$	Write Enable Bit. A 0 must be written to this bit so the write operation to the Communications register actually takes place. If a 1 is written to this bit, the part will not clock on to subsequent bits in the register. It will stay at this bit location until a 0 is written to this bit. Once a 0 is written to the $\overline{\text{WEN}}$ bit, the next seven bits will be loaded to the Communications register.
CR6	R/$\overline{\text{W}}$	A 0 in this bit location indicates that the next operation will be a write to a specified register. A 1 in this position indicates that the next operation will be a read from the designated register.
CR5	Zero	A 0 must be written to this bit position to ensure correct operation of the AD7719.
CR4	Zero	A 0 must be written to this bit position to ensure correct operation of the AD7719.
CR3–CR0	A3–A0	Register Address Bits. These address bits are used to select which of the AD7719's registers is being accessed during this serial interface communication. A3 is the MSB of the three selection bits.

Table X. Register Selection Table

A3	A2	A1	A0	Register
0	0	0	0	Communications Register during a Write Operation
0	0	0	0	Status Register during a Read Operation
0	0	0	1	Mode Register
0	0	1	0	Main ADC Control Register (AD0CON)
0	0	1	1	Aux ADC Control Register (AD1CON)
0	1	0	0	Filter Register
0	1	0	1	Main ADC Data Register
0	1	1	0	Aux ADC Data Register
0	1	1	1	I/O Control Register
1	0	0	0	Main ADC Offset Calibration Register
1	0	0	1	Aux ADC Offset Calibration Register
1	0	1	0	Main ADC Gain Calibration Register
1	0	1	1	Aux ADC Gain Calibration Register
1	1	0	0	Test 1 Register
1	1	0	1	Test 2 Register
1	1	1	0	Undefined
1	1	1	1	ID Register

Status Register (A3, A2, A1, A0 = 0, 0, 0, 0; Power-On Reset = 0x00)
The ADC Status register is an 8-bit read-only register. To access the ADC Status register, the user must write to the Communications register selecting the next operation to be a read and loading bits A3 to A0 with 0, 0, 0, 0. Table XI outlines the bit designations for the Status register. SR0 through SR7 indicate the bit location, with SR denoting that the bits are in the Status register. SR7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
RDY0 (0)	RDY1 (0)	CAL (0)	NOXREF (0)	ERR0 (0)	ERR1 (0)	(0)	LOCK (0)

Table XI. Status Register Bit Designations

Bit Location	Bit Name	Description
SR7	RDY0	Ready Bit for Main ADC. *Set* when data is written to main ADC data registers or on completion of calibration cycle. The RDY0 bit is *cleared* automatically after the main ADC data register has been read or after a period of time before the data register is updated with a new conversion result. This bit is also cleared by a write to the mode bits to indicate a conversion or calibration.
SR6	RDY1	Ready Bit for Aux ADC. *Set* when data is written to aux ADC data registers or on completion of calibration cycle. The RDY1 bit is *cleared* automatically after the aux ADC data register has been read or a period of time before the data register is updated with a new conversion result. This bit is also cleared by a write to the mode bits to indicate a conversion or calibration.
SR5	CAL	Calibration Status Bit. *Set* to indicate completion of calibration. It is set at the same time that the RDY0 and/or RDY1 bits are set high. *Cleared* by a write to the mode bits to start another ADC conversion or calibration.
SR4	NOXREF	No External Reference Bit. (*Only active if main ADC is active and applies to REFIN1 only.*) *Set* to indicate that one or both of the REFIN1 pins is floating or the applied voltage is below a specified threshold. When *Set*, conversion results are clamped to all 1s. *Cleared* to indicate valid reference applied between REFIN1(+) and REFIN1(–).
SR3	ERR0	Main ADC Error Bit. *Set* to indicate that the result written to the main ADC data registers has been clamped to all 0s or all 1s. After a calibration, this bit also flags error conditions that caused the calibration registers not to be written. Error sources include Overrange, Underrange, and NOXREF. *Cleared* by a write to the mode bits to initiate a conversion or calibration.
SR2	ERR1	Aux ADC Error Bit. *Set* to indicate that the result written to the Aux ADC data registers has been clamped to all 0s or all 1s. After a calibration, this bit also flags error conditions that caused the calibration registers not to be written. Error sources include Overrange, Underrange, and NOXREF. *Cleared* by a write to the mode bits to initiate a conversion or calibration.
SR1	0	Reserved for Future Use.
SR0	LOCK	PLL Lock Status Bit. *Set* if the PLL has locked onto the 32 kHz crystal oscillator clock. If the user is worried about exact sampling frequencies, for example, the LOCK bit should be interrogated and the result discarded if the LOCK bit is 0.

Mode Register (A3, A2, A1, A0 = 0, 0, 0, 1; Power-On Reset = 0x00)

The Mode register is an 8-bit register from which data can be read or to which data can be written. This register configures the operating modes of the AD7719. Table XII outlines the bit designations for the Mode register. MR7 through MR0 indicate the bit location, with MR denoting the bits are in the Mode register. MR7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
0 (0)	$\overline{\text{BUF}}$ (0)	0 (0)	CHCON (0)	OSCPD (0)	MD2 (0)	MD1 (0)	MD0 (0)

Table XII. MODE Register Bit Designations

Bit Location	Bit Name	Description
MR7	0	Reserved for Future Use.
MR6	$\overline{\text{BUF}}$	Configures the main ADC for buffered or unbuffered mode of operation. If *set,* the main ADC operates in unbuffered mode, lowering the power consumption of the AD7719. If *cleared,* the Main ADC operates in buffered mode, allowing the user to place source impedances on the front end without contributing gain errors to the system.
MR5	0	Reserved for Future Use.
MR4	CHCON	Channel Configure Bit. If this bit is *set*, the main ADC operates with three pseudodifferential input channels and the aux ADC does not have AIN3/AIN4 as an input option. If *cleared,* the main ADC operates with two fully differential input channels and the aux channel operates as one fully differential input and two single-ended inputs or as three single-ended inputs.
MR3	OSCPD	Oscillator Power-Down Bit. If this bit is *set*, placing the AD7719 in standby mode will stop the crystal oscillator, reducing the power drawn by the AD7719 to a minimum. The oscillator will require 300 ms to begin oscillating when the ADC is taken out of standby mode. If this bit is *cleared,* the oscillator is not shut off when the ADC is put into standby mode and will not require the 300 ms start-up time when the ADC is taken out of standby.
MR2–MR0	MD2–MD0	Main and Aux ADC Mode Bits.

These bits select the operational mode of the enabled ADC as follows:

MD2	MD1	MD0	Description
0	0	0	Power-Down Mode (Power-On Default). The current sources, power switches, and PLL are shut off in Power-Down mode.
0	0	1	Idle Mode. In Idle mode, the ADC filter and modulator are held in a reset state although the modulator clocks are still provided.
0	1	0	Single Conversion Mode. In Single Conversion mode, a single conversion is performed on the enabled channels. On completion of the conversion, the ADC data registers are updated, the relevant flags in the STATUS register are written, and idle mode is entered with the MD2–MD0 being written accordingly to 001.
0	1	1	Continuous Conversion. In continuous conversion mode, the ADC data registers are regularly updated at the selected update rate (see Filter register).
1	0	0	Internal Zero-Scale Calibration. Internal short automatically connected to the enabled channel(s). Returns to Idle mode (001) when complete.
1	0	1	Internal Full-Scale Calibration. External V_{REF} is connected automatically to the ADC input for this calibration. Returns to idle mode when complete.
1	1	0	System Zero-Scale Calibration. User should connect system zero-scale input to the channel input pins as selected by the CH1/CH0 and ACH1/ACH0 bits in the control registers.
1	1	1	System Full-Scale Calibration. User should connect system full-scale input to the channel input pins as selected by the CH1/CH0 and ACH1/ACH0 bits in the control registers.

Operating Characteristics when Addressing the Mode and Control Registers

1. Any change to the MD bits will immediately reset both ADCs. A write to the MD2–0 bits with no change is also treated as a reset. (See exception to this in Note 3.)
2. If AD0CON is written when AD0EN = 1, or if AD0EN is changed from 0 to 1, both ADCs are also immediately reset. In other words, the main ADC is given priority over the aux ADC and any change requested on main is immediately responded to.
3. On the other hand, if AD1CON is written to, only the aux ADC is reset. For example, if the main ADC is continuously converting when the aux ADC change or enable occurs, the main ADC continues undisturbed. Rather than allow the aux ADC to operate with a phase difference from the main ADC, the aux ADC will fall into step with the outputs of the main ADC. The result is that the first conversion time for the aux channel will be delayed up to three outputs while the aux ADC update rate is synchronized to the main ADC.
4. Once the MODE has been written with a calibration mode, the RDY0/1 bits (STATUS) are immediately reset and the calibration commences. On completion, the appropriate calibration registers are written, the relevant bits in STATUS are written, and the MD2–0 bits are reset to 001 to indicate the ADC is back in Idle mode.
5. Any calibration request of the aux ADC while the temperature sensor is selected will fail to complete.
6. Calibrations are performed with the maximum allowable SF value. SF register is reset to user configuration after calibration.

Main ADC Control Register (AD0CON): (A3, A2, A1, A0 = 0, 0, 1, 0; Power-On Reset = 0x07)

The main ADC control register is an 8-bit register from which data can be read or to which data can be written. This register is used to configure the main ADC for range, channel selection, 16-/24-bit operation, and unipolar or bipolar coding. Table XIII outlines the bit designations for the main ADC control register. AD0CON7 through AD0CON0 indicate the bit location, AD0CON denoting the bits are in the main ADC control register. AD0CON7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

AD0CON7	AD0CON6	AD0CON5	AD0CON4	AD0CON3	AD0CON2	AD0CON1	AD0CON0
AD0EN (0)	WL (0)	CH1 (0)	CH0 (0)	U/$\overline{B}$ (0)	RN2 (1)	RN1 (1)	RN0 (1)

Table XIII. Main ADC Control Register (AD0CON) Bit Designations

Bit Location	Bit Name	Description			
AD0CON7	AD0EN	Main ADC Enable Bit. *Set* by user to enable the main ADC. When set, the main ADC operates according to the MD bits in the mode register. *Cleared* by the user to power down the Main ADC.			
AD0CON6	WL	16-/24-Bit Operating Mode. *Set* by user to enable 16-bit mode. The conversion results from the main ADC will be rounded to 16 bits and the main ADC data register will be 16 bits wide. *Cleared* by user to enable 24-bit mode. The conversion results from the main ADC will be rounded to 24 bits and the main ADC data register will be 24 bits wide.			
AD0CON5 AD0CON4	CH1 CH0	Main ADC Channel Selection Bits. Written by the user to select the differential input pairs used by the main ADC as follows: (Note: The CHCON bit resides in the Mode register.)			
CHCON	**CH1**	**CH0**	**Positive Input**	**Negative Input**	**Calibration Register Pair**
0	0	0	AIN1	AIN2	0
0	0	1	AIN3	AIN4	1
0	1	0	AIN2	AIN2	0
0	1	1	AIN3	AIN2	1
1	0	0	AIN1	AIN4	0
1	0	1	AIN3	AIN4	1
1	1	0	AIN4	AIN4	0
1	1	1	AIN2	AIN4	2
AD0CON3	U/$\overline{B}$	Main ADC Unipolar/Bipolar Bit. *Set* by user to enable unipolar coding, i.e., zero differential input will result in 0x00 0000 output and a full-scale differential input will result in 0xFF FFFF output when operated in 24-bit mode. *Cleared* by user to enable bipolar coding, Negative full-scale differential input will result in an output code of 0x00 0000, zero differential input will result in an output code of 0x80 0000, and a Positive full-scale differential input will result in an output code of 0xFF FFFF.			

Table XIII. Main ADC Control Register (AD0CON) Bit Designations (continued)

Bit Location	Bit Name	Description			
AD0CON2 AD0CON1	RN2 RN1	Main ADC Range Bits. Written by the user to select the main ADC input range as follows.			
AD0CON0	RN0	**RN2**	**RN1**	**RN0**	**Selected Main ADC Input Range (V_{REF} = 2.5 V)**
		0	0	0	±20 mV
		0	0	1	±40 mV
		0	1	0	±80 mV
		0	1	1	±160 mV
		1	0	0	±320 mV
		1	0	1	±640 mV
		1	1	0	±1.28 V
		1	1	1	±2.56 V

Aux ADC Control Registers (AD1CON):
(A3, A2, A1, A0 = 0, 0, 1, 1; Power-On Reset = 0x00)
The aux ADC control register is an 8-bit register from which data can be read or to which data can be written. This register is used to configure the aux ADC for range, channel selection, and unipolar or bipolar coding. Table XIV outlines the bit designations for the aux ADC control register. AD1CON7 through AD1CON0 indicate the bit location, with AD1CON denoting that the bits are in the aux ADC control register. AD1CON7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit.

AD1CON7	AD1CON6	AD1CON5	AD1CON4	AD1CON3	AD1CON2	AD1CON1	AD1CON0
AD1EN (0)	**ACH2 (0)**	**ACH1 (0)**	**ACH0 (0)**	**U/$\overline{B}$ (0)**	**0 (0)**	**0 (0)**	**ARN (1)**

Table XIV. Aux ADC Control Register (AD1CON) Bit Designations

Bit Location	Bit Name	Description			
AD1CON7	AD1EN	Aux ADC Enable Bit. *Set* by user to enable the Aux ADC. When set, the aux ADC operates according to the MD bits in the mode register. *Cleared* by the user to power down the aux ADC.			
AD1CON6 AD1CON5 AD1CON4	ACH2 ACH1 ACH0	Aux ADC Channel Selection Bits. Written by the user to select the active input channels used by the aux ADC as follows:			
CHCON	**ACH2**	**ACH1**	**ACH0**	**Positive Input**	**Negative Input**
0	0	0	0	AIN3	AGND
0	0	0	1	AIN4	AGND
0	0	1	0	AIN5	AIN6
0	0	1	1	Temp Sensor	(Temp Sensor Routed to the ADC Inputs)
0	1	0	0	AGND	AGND (Internal Short)
1	0	0	0	AIN5	AGND
1	0	0	1	AIN6	AGND
1	0	1	0	AIN5	AIN6
1	0	1	1	Temp Sensor	(Temp Sensor Routed to the ADC Inputs)
1	1	0	0	AGND	AGND (Internal Short)
X	1	0	1	Not Defined	
X	1	1	0	Not Defined	
X	1	1	1	Not Defined	
AD1CON3	U/$\overline{B}$	Aux ADC Unipolar/Bipolar Selection Bit. *Set* by user to enable unipolar coding, i.e., zero differential input will result in 0x0000 output. *Cleared* by user to enable bipolar coding, zero differential input will result in 0x8000 output.			
AD1CON2	0	Must be zero for specified operation.			
AD1CON1	0	Must be zero for specified operation.			
AD1CON0	ARN	Auxiliary Channel Input Range Bit. When *set* by the user, the input range is ±REFIN2. When *cleared* by the user, the input range is ±REFIN2/2.			

NOTES
1. When the temperature sensor is selected, the AD7719 automatically selects its internal reference. The temperature sensor is not factory calibrated. Temp sensor is suitable for relative temperature measurements. The temperature sensor yields conversion results where a conversion result of 0x8000 equates to typically 0°C.
2. A 1°C change in temperature will normally result in a 256 LSB change in the AD1 data register (ADC conversion result).

FR7	FR6	FR5	FR4	FR3	FR2	FR1	FR0
SF7 (0)	**SF6 (1)**	**SF5 (0)**	**SF4 (0)**	**SF3 (0)**	**SF2 (1)**	**SF1 (0)**	**SF0 (1)**

Filter Register (A3, A2, A1, A0 = 0, 1, 0, 0; Power-On Reset = 0x45)
The Filter register is an 8-bit register from which data can be read or to which data can be written. This register determines the amount of averaging performed by the sinc filter. Table XV outlines the bit designations for the Filter register. FR7 through FR0 indicate the bit location, with FR denoting that the bits are in the Filter register. FR7 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit. The number in this register is used to set the decimation factor and thus the output update rate for the main and aux ADCs. The filter register cannot be written to by the user while either ADC is active. The update rate is used for both main and aux ADCs and is calculated as follows:

$$f_{ADC} = \frac{1}{3} \times \frac{1}{8 \times SF} \times f_{MOD}$$

where:

f_{ADC} = ADC output update rate
f_{MOD} = Modulator clock frequency = 32.768 kHz (main and aux ADC)
SF = Decimal value written to SF register

The allowable range for SF is 13dec to 255dec. Examples of SF values and corresponding conversion rate (f_{ADC}) and time (t_{ADC}) are shown in Table XV. It should also be noted that both ADC input channels are chopped to minimize offset errors. This means that the time for a single conversion or the time to the first conversion result is $2 \times t_{ADC}$.

Table XV. Update Rate vs. SF WORD

SF (dec)	SF (Hex)	f_{ADC} (Hz)	t_{ADC} (ms)
13	0D	105.3	9.52
69	45	19.79	50.34
255	FF	5.35	186.77

I/O and Current Source Control Register (IOCON): (A3, A2, A1, A0 = 0, 1, 1, 1; Power-On Reset = 0x0000)
The IOCON register is a 16-bit register from which data can be read or to which data can be written. This register is used to control and configure the various excitation and burnout current source options available on-chip along with controlling the I/O port. Table XVI outlines the bit designations for this register. IOCON15 through IOCON0 indicate the bit location, with IOCON denoting that the bits are in the I/O and Current Source control register. IOCON15 denotes the first bit of the data stream. The number in parentheses indicates the power-on/reset default status of that bit. A write to the IOCON register has immediate effect and does not reset the ADCs. Thus if a current source is switched while the ADC is converting, the user will have to wait for the full settling time of the filter before getting a fully settled output. Since the ADC is chopped, this equates to three outputs.

IOCON15	IOCON14	IOCON13	IOCON12	IOCON11	IOCON10	IOCON9	IOCON8
PSW2 (0)	**PSW1 (0)**	**0 (0)**	**BO (0)**	**I2PIN (0)**	**I1PIN (1)**	**I2EN (0)**	**I1EN (0)**

IOCON7	IOCON6	IOCON5	IOCON4	IOCON3	IOCON2	IOCON1	IOCON0
P4DIR (0)	**P3DIR (0)**	**P2EN (0)**	**P1EN (0)**	**P4DAT (0)**	**P3DAT (0)**	**P2DAT (0)**	**P1DAT (0)**

Table XVI. IOCON (I/O and Current Source Control Register) Bit Designations

Bit Location	Bit Name	Description
IOCON15	PSW2	Power Switch 2 Control Bit. *Set* by user to enable power switch P2 to PWRGND. *Cleared* by user to enable use as a standard I/O pin. When the ADC is in standby mode, the power switches are open.
IOCON14	PSW1	Power Switch 1 Control Bit. *Set* by user to enable power switch P1 to PWRGND. *Cleared* by user to enable use as a standard I/O pin. When ADC is in standby mode, the power switches are open.
IOCON13	0	This bit must be zero for correct operation.
IOCON12	BO	Burnout Current Enable Bit. *Set* by user to enable the 100 nA current sources in the main ADC signal path. A 100 nA current source is applied to the positive input leg while a 100 nA sink is applied to the negative input. *Cleared* by user to disable both transducer burnout current sources.
IOCON11	I2PIN	IEXE2, 200 μA Current Source Direction Bit. *Set* by user to enable IEXC2 current source to IOUT1. *Cleared* by user to enable IEXC2 current source to IOUT2.
IOCON10	I1PIN	IEXE1, 200 μA Current Source Direction Bit. *Set* by user to enable IEXC1 current source to IOUT2. *Cleared* by user to enable IEXC1 current source to IOUT1.
IOCON9	I2EN	IEXC2 Current Source Enable Bit. *Set* by user to turn on the IEXC2 excitation current source. *Cleared* by user to turn off the IEXC2 excitation current source.
IOCON8	I1EN	IEXC1 Current Source Enable Bit. *Set* by user to turn on the IEXC1 excitation current source. *Cleared* by user to turn off the IEXC1 excitation current source.
IOCON7	P4DIR	P4, I/O Direction Control Bit. *Set* by user to enable P4 as an output. *Cleared* by user to enable P4 as an input. There are weak active pull-ups internally when enabled as an input.
IOCON6	P3DIR	P3, I/O Direction Control Bit. *Set* by user to enable P3 as an output. *Cleared* by user to enable P3 as an input. There are weak active pull-ups internally when enabled as an input.
IOCON5	P2EN	P2 Digital Output Enable Bit. *Set* by user to enable P2 as a regular digital output pin. *Cleared* by user to three-state P2 output. PSW2 takes precedence over P2EN.
IOCON4	P1EN	P1 Digital Output Enable Bit. *Set* by user to enable P1 as a regular digital output pin. *Cleared* by user to three-state P1 output. PSW1 takes precedence over P1EN.
IOCON3 IOCON2 IOCON1 IOCON0	P4DAT P3DAT P2DAT P1DAT	Digital I/O Port Data Bits. The readback values of these bits indicate the status of their respective pin when the I/O port is active as an input. The values written to these data bits appear at the output port when the I/O bits are enabled as outputs. P2 and P1 are outputs only, so reading P2DAT and P1DAT will return what was last written to these bits.

Main ADC Data Result Registers (DATA0): (A3, A2, A1, A0 = 0, 1, 0, 1; Power-On Reset = 0x00 0000)
The conversion results for the main ADC channel are stored in the main ADC data register (DATA0). This register is either 16 or 24 bits wide, depending on the status of the WL bit in the main ADC control register (AD0CON). This is a read-only register. On completion of a read from this register, the RDY0 bit in the status register is cleared.

Aux ADC Data Result Registers (DATA1): (A3, A2, A1, A0 = 0, 1, 1, 0; Power-On Reset = 0x0000)
The conversion results for the aux ADC channel are stored in the aux ADC data register (DATA1). This register is 16 bits wide and is a read-only register. On completion of a read from this register, the RDY1 bit in the status register is cleared.

Main ADC Offset Calibration Coefficient Registers (OF0): (A3, A2, A1, A0 = 1, 0, 0, 0; Power-On Reset = 0x80 0000)
The offset calibration registers hold the 24-bit data offset calibration coefficient for the main ADC. There are three registers associated with the main ADC channel. In fully differential operating mode, there are two input channels and a register is dedicated to each input. When operating in pseudodifferential mode, the main ADC can be configured for three input channels and there is a dedicated register for each pseudodifferential input. These registers have a power-on reset value of 0x80 0000. The channel bits, in association with the communication register address for the OF0 register, allow access to these registers. These registers are read/write registers. The calibration registers can only be written to if the ADC is inactive (MD bits in the mode register = 000 or 001 or both AD0EN and AD1EN bits in the control registers are cleared). Reading of the calibration registers does not clear the RDY0 bit.

Aux ADC Offset Calibration Coefficient Registers (OF1): (A3, A2, A1, A0 = 1, 0, 0, 1; Power-On Reset = 0x8000)
The offset calibration register OF1 holds the 16-bit data offset calibration coefficient for the aux ADC. This register has a power-on-reset value of 0x8000. The channel bits, in association with the communication register address for the OF1 register, allow access to these registers. These registers are read/write registers. The calibration registers can only be written to if the ADC is inactive (MD bits in the mode register = 000 or 001 or both AD0EN and AD1EN bits in the control registers are cleared). Reading of the calibration registers does not clear the RDY1 bit.

Main ADC Gain Calibration Coefficient Registers (GNO): (A3, A2, A1, A0 = 1, 0, 1, 0; Power-On Reset = 0x5X XXX5)
The gain calibration registers hold the 24-bit data gain calibration coefficient for the main ADC. These registers are configured at power-on with factory calculated internal full-scale calibration coefficients. Every device will have different coefficients. However, these bytes will be automatically overwritten if an internal or system full-scale calibration is initiated by the user via MD2–0 bits in the Mode register. There are three gain calibration registers associated with the main ADC channel. In fully differential operating mode, there are two input channels and a register is dedicated to each input. When operating in pseudodifferential mode, the main ADC can be configured for three input channels and there is a dedicated register for each pseudodifferential input. These registers are read/write registers. The calibration registers can only be written to if the ADC is inactive (MD bits in the mode register = 000 or 001 or both AD0EN and AD1EN bits in the control registers are cleared). Reading of the calibration registers does not clear the RDY1 bit.

Aux ADC Gain Calibration Coefficient Registers (GN1): (A3, A2, A1, A0 = 1, 0, 1, 1; Power-On Reset = 0x59XX)
The gain calibration register GN1 holds the 16-bit data gain calibration coefficient for the aux ADC. This register is configured at power-on with factory calculated internal zero-scale calibration coefficients. Every device will have different coefficients. However, these coefficients will be automatically overwritten if an internal or system zero-scale calibration is initiated by the user via the MD2–0 bits in the Mode register. These registers are read/write registers. The calibration registers can only be written to if the ADC is inactive (MD bits in the mode register = 000 or 001 or both AD0EN and AD1EN bits in the control registers are cleared). Reading of the calibration registers does not clear the RDY1 bit.

ID Register (ID): (A3, A2, A1, A0 = 1, 1, 1, 1; Power-On Reset = 0x0X)
This register is a read-only 8-bit register. The contents are used to determine the die revision of the AD7719. Table XVII indicates the bit locations.

User Nonprogrammable Test Registers
The AD7719 contains two test registers. The bits in this test register control the test modes of the AD7719, which are used for the testing of the device. *The user is advised not to change the contents of these registers.*

Table XVII. ID Register Bit Designations

ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
0	0	0	0	X	X	X	X

CONFIGURING THE AD7719

All user-accessible registers on the AD7719 are accessed via the serial interface. Communication with any of these registers is initiated by first writing to the Communications register. Figure 11 outlines a flow diagram of the sequence used to configure all registers after a power-up or reset on the AD7719. The flowchart shows two methods of determining when it is valid to read the data register or determine when a calibration cycle is complete. The first method is hardware polling of the $\overline{RDY}$ pin and the second method involves software interrogation of bits in the status and mode registers. The flowchart details all the necessary programming steps required to initialize the ADC and read data from the main and aux channel following a power-on or reset. The steps can be broken down as follows:

1. Configure and initialize the microcontroller or microprocessor serial port.
2. Initialize the AD7719 by configuring the following registers:
   a) IOCON to configure the current sources and digital I/O port.
   b) FILTER to configure the update rate for both channels.
   c) AD1CON to enable the aux channel, select the analog input, select unipolar or bipolar operation and input range.
   d) AD0CON to enable the main ADC channel and select 16-/24-bit mode, analog input range, and either unipolar or bipolar operation.
   e) MODE to configure the operating mode. Operating mode consists of calibration or conversion.

   All of these operations consist of a write to the communications register to specify the next operation as a write to a specified register. Data is then written to this register. When each sequence is complete, the ADC defaults to waiting for another write to the Communications register to specify the next operation.
3. When the operating mode is selected, the user needs to determine when it is valid to read the data in conversion mode or when the calibration is complete in calibration mode. This is accomplished either by polling the $\overline{RDY}$ pin (hardware polling) or by interrogating the bits in either the Status or Mode registers (software polling). Both are shown in Figure 11. It is assumed that both the main and aux ADCs are being used and calibration is required. If the AD7719 is operated at the factory-calibrated conditions, a field calibration will not be required and these steps can be bypassed.

MICROCOMPUTER/MICROPROCESSOR INTERFACING

The AD7719's flexible serial interface allows for easy interface to most microcomputers and microprocessors. The flowchart of Figure 11 outlines the sequence that should be followed when interfacing a microcontroller or microprocessor to the AD7719. Figures 12, 13, and 14 show some typical interface circuits.

The serial interface on the AD7719 is capable of operating from just three wires and is compatible with SPI interface protocols. The 3-wire operation makes the part ideal for isolated systems where minimizing the number of interface lines minimizes the number of opto-isolators required in the system. The serial clock input is a Schmitt-triggered input to accommodate slow edges from optocouplers. The rise and fall times of other digital inputs to the AD7719 should be no longer than 1 μs.

Most of the registers on the AD7719 are 8-bit registers, which facilitates easy interfacing to the 8-bit serial ports of microcontrollers. The main channel data register (AD0) on the AD7719 can be either 16 or 24 bits, the aux ADC data register (AD1) is 16 bits wide and the offset and gain registers are 24-bit registers, but data transfers to these registers can consist of multiple 8-bit transfers to the serial port of the microcontroller. DSP processors and microprocessors generally transfer 16 bits of data in a serial data operation. Some of these processors, such as the ADSP-2105, have the facility to program the amount of cycles in a serial transfer. This allows the user to tailor the number of bits in any transfer to match the register length of the required register in the AD7719.

Even though some of the registers on the AD7719 are only eight bits in length, communicating with two of these registers in successive write operations can be handled as a single 16-bit data transfer, if required. For example, if the Filter register is to be updated, the processor must first write to the Communications register (saying that the next operation is a write to the Filter register) and then write eight bits to the Setup register. If required, this can all be done in a single 16-bit transfer because once the eight serial clocks of the write operation to the Communications register have been completed, the part immediately sets itself up for a write operation to the Setup register.

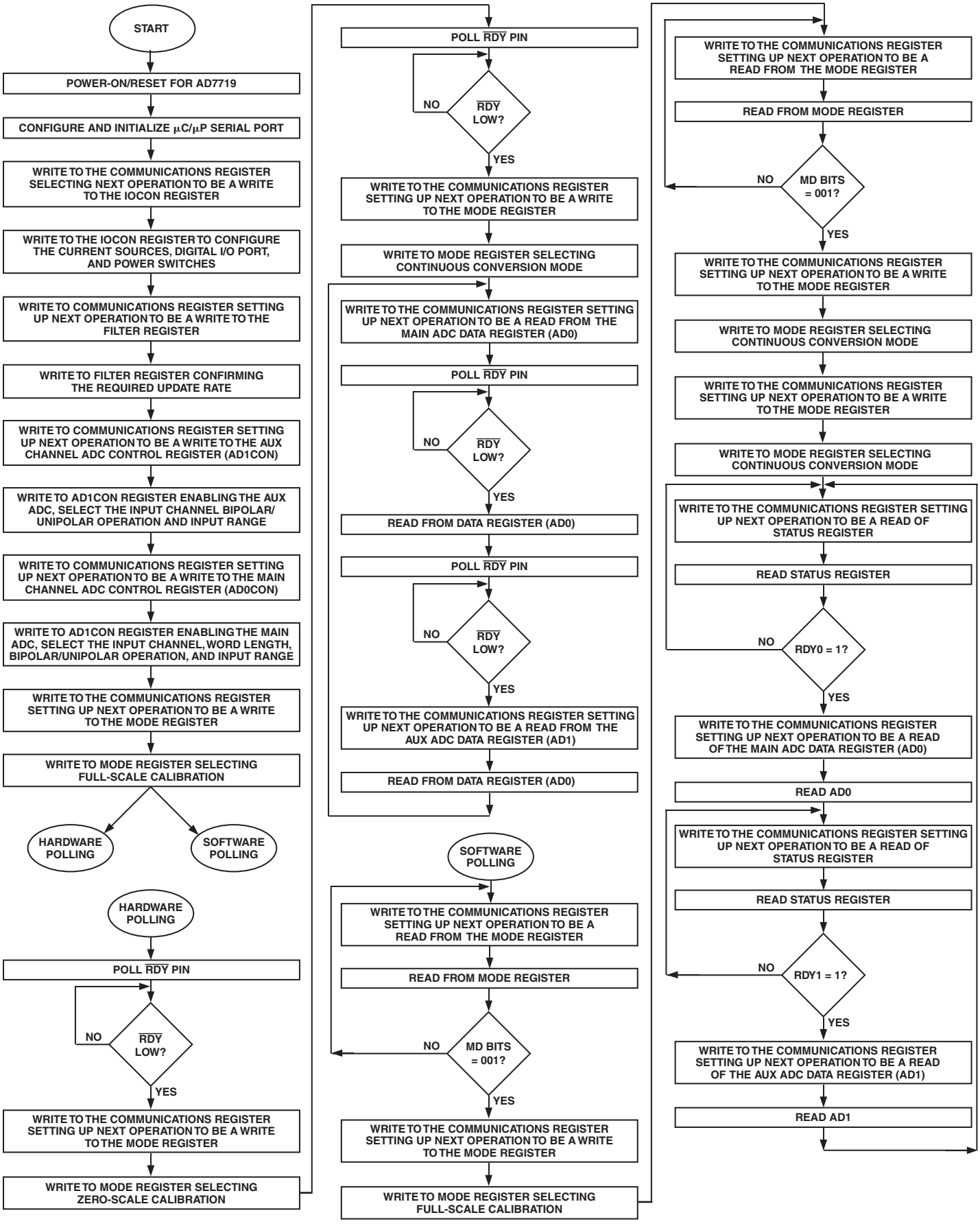


Figure 11. Flowchart for Initializing, Calibrating, and Reading Data from the AD7719 Main and Aux Channels

AD7719-to-68HC11 Interface

Figure 12 shows an interface between the AD7719 and the 68HC11 microcontroller. The diagram shows the minimum (3-wire) interface with $\overline{CS}$ on the AD7719 hardwired low. In this scheme, the RDY bits of the Status register are monitored to determine when the Data register is updated. RDY0 indicates the status of the main ADC channel while RDY1 indicates the status of the aux channel. An alternative scheme, which increases the number of interface lines to four, is to monitor the $\overline{RDY}$ output line from the AD7719. The monitoring of the $\overline{RDY}$ line can be done in two ways. First, $\overline{RDY}$ can be connected to one of the 68HC11's port bits (such as PC0), which is configured as an input. This port bit is then polled to determine the status of $\overline{RDY}$. The second scheme is to use an interrupt driven system, in which case the $\overline{RDY}$ output is connected to the IRQ input of the 68HC11. For interfaces that require control of the $\overline{CS}$ input on the AD7719, one of the port bits of the 68HC11 (such as PC1) that is configured as an output, can be used to drive the $\overline{CS}$ input.

The 68HC11 is configured in the master mode with its CPOL bit set to a logic 1 and its CPHA bit set to a logic 1. When the 68HC11 is configured like this, its SCLK line idles high between data transfers. The AD7719 is not capable of full duplex operation. If the AD7719 is configured for a write operation, no data appears on the DOUT lines even when the SCLK input is active. Similarly, if the AD7719 is configured for a read operation, data presented to the part on the DIN line is ignored even when SCLK is active.

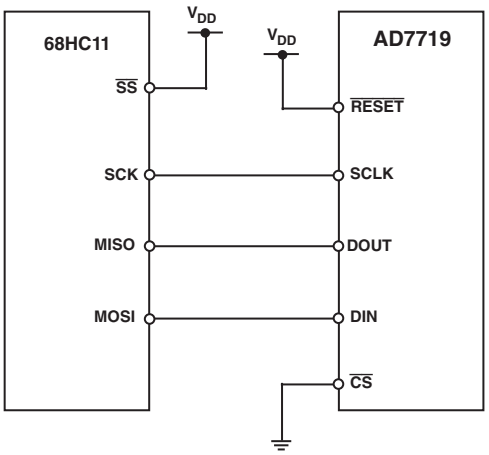


Figure 12. AD7719-to-68HC11 Interface

AD7719-to-8xC51 Interface

An interface circuit between the AD7719 and the 8xC51 microcontroller is shown in Figure 13. The diagram shows the minimum number of interface connections with $\overline{CS}$ on the AD7719 hardwired low. In the case of the 8xC51 interface, the minimum number of interconnects is just two. In this scheme, the RDY bits of the Status register are monitored to determine when the Data register is updated. The alternative scheme, which increases the number of interface lines to three, is to monitor the $\overline{RDY}$ output line from the AD7719. The monitoring of the $\overline{RDY}$ line can be done in two ways. First, $\overline{RDY}$ can be connected to one of the 8xC51's port bits (such as P1.0) that is configured as an input. This port bit is then polled to determine the status of $\overline{RDY}$.

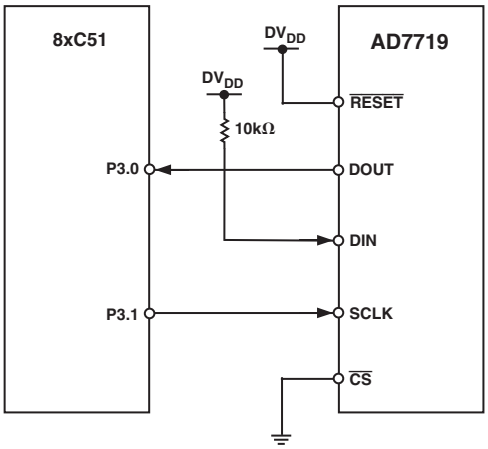


Figure 13. AD7719-to-8XC51 Interface

The second scheme is to use an interrupt-driven system, in which case the $\overline{RDY}$ output is connected to the INT1 input of the 8xC51. For interfaces that require control of the $\overline{CS}$ input on the AD7719, one of the port bits of the 8xC51 (such as P1.1) that is configured as an output can be used to drive the $\overline{CS}$ input. The 8xC51 is configured in its Mode 0 serial interface mode. Its serial interface contains a single data line. As a result, the DOUT and DIN pins of the AD7719 should be connected together with a 10 kΩ pull-up resistor. The serial clock on the 8xC51 idles high between data transfers. The 8xC51 outputs the LSB first in a write operation, while the AD7719 expects the MSB first so the data to be transmitted has to be rearranged before being written to the output serial register. Similarly, the AD7719 outputs the MSB first during a read operation while the 8xC51 expects the LSB first. Therefore, the data read into the serial buffer needs to be rearranged before the correct data word from the AD7719 is available in the accumulator.

AD7719-to-ADSP-2103/ADSP-2105 Interface

Figure 14 shows an interface between the AD7719 and the ADSP-2103/ADSP-2105 DSP processor. In the interface shown, the RDY bits of the Status register are again monitored to determine when the Data register is updated. The alternative scheme is to use an interrupt-driven system, in which case the $\overline{RDY}$ output is connected to the IRQ2 input of the ADSP-2103/ADSP-2105. The serial interface of the ADSP-2103/ADSP-2105 is set up for alternate framing mode. The $\overline{RFS}$ and $\overline{TFS}$ pins of the ADSP-2103/ADSP-2105 are configured as active low outputs and the ADSP-2103/ADSP-2105 serial clock line, SCLK, is also configured as an output. The $\overline{CS}$ for the AD7719 is active when either the $\overline{RFS}$ or $\overline{TFS}$ outputs from the ADSP-2103/ADSP-2105 are active. The serial clock rate on the ADSP-2103/ADSP-2105 should be limited to 3 MHz to ensure correct operation with the AD7719.

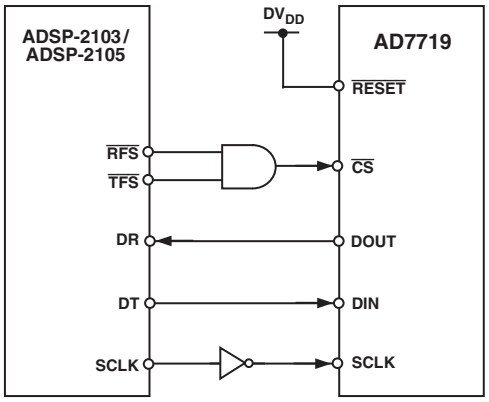


Figure 14. AD7719-to-ADSP-2103/ADSP-2105 Interface

CIRCUIT DESCRIPTION

The AD7719 is a Σ-Δ A/D converter incorporating two independent Σ-Δ A/D converters with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those in weigh scale, pressure, temperature, industrial control, or process control applications.

The main ADC is intended to convert the primary sensor input. The main ADC employs a Σ-Δ conversion technique to realize up to 24 bits of no-missing-codes performance. The Σ-Δ modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A $Sinc^3$ programmable low-pass filter is then employed to decimate the modulator output data stream to give a valid data conversion result at programmable output rates from 5.35 Hz (186.77 ms) to 105.03 Hz (9.52 ms). A Chopping scheme is also employed to minimize ADC offset and offset and gain drift errors. The analog input to the main ADC can be operated in buffered or unbuffered mode and can be programmed for one of eight input ranges from ±20 mV to ±2.56 V. The input channels can be configured for either fully differential inputs or pseudodifferential input channels via the CH1 and CH0 bits in the main ADC control register (AD0CON) and the CHCON bit in the mode register. When configured for buffered mode ($\overline{BUF}$ = 0), the input channels are internally buffered, allowing the part to handle significant source impedances on the analog input, allowing R/C filtering (for noise rejection or RFI reduction) to be placed on the analog inputs if required. When operating in unbuffered mode, care has to be exercised when selecting front end source impedances so as not to introduce gain errors. On-chip burnout currents are available and can be used to check that a transducer on the selected channel is still operational before attempting to take measurements.

The second or auxiliary ADC is intended to convert secondary inputs such as those from a cold junction diode or thermistor. This ADC is unbuffered and has a fixed input range of 0 V to REFIN2 (ARN bit = 1) or 0 to REFIN2/2 (ARN bit = 0). Again, this ADC can be configured for differential or pseudo-differential inputs via the ACH2, ACH1, and ACH0 bits in the auxiliary ADC control register (AD1CON). The auxiliary ADC is specified for 16-bit performance and, since its analog inputs are unbuffered, care must be exercised when placing filtering on the front end to avoid introducing gain errors into the measurement system.

The basic connection diagram for the AD7719 is shown in Figure 15. This shows both the AV_{DD} and DV_{DD} pins of the AD7719 being driven from the analog 5 V supply. Some applications will have AV_{DD} and DV_{DD} driven from separate supplies. AV_{DD} and DV_{DD} can be operated independently of each other, allowing the device to be operated with 5 V analog supply and 3 V digital supply or vice versa. An AD780/REF195 precision 2.5 V reference provides the reference source for the part. A quartz crystal or ceramic resonator provides the 32 kHz master clock source for the part. In some cases, it will be necessary to connect capacitors on the crystal or resonator to ensure that it does not oscillate at overtones of its fundamental operating frequency. The values of capacitors will vary depending on the manufacturer's specifications.

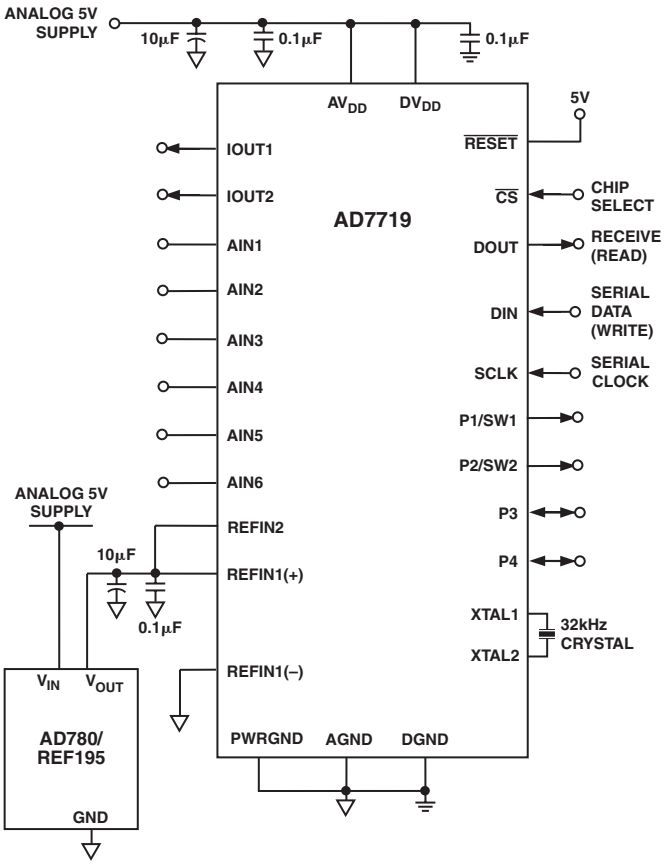


Figure 15. Basic Connection Diagram

Analog Input Channels

The main ADC has four associated analog input pins (labeled AIN1 to AIN4) that can be configured as two fully differential input channels or three pseudodifferential input channels. Channel selection bits CH1 and CH0 in the ADC0CON register, along with the CHCON bit of the mode register, detail the different configurations.

The auxiliary ADC has four external input pins (labeled AIN3 to AIN6) as well as an internal connection to the internal on-chip temperature sensor. Channel selection bits ACH2, ACH1, and ACH0 in the ADC1CON register, along with the CHCON bit in the mode register, detail the various configurations on these input channels.

Two input multiplexers (MUX1 and MUX2) switch the selected input channel to the on-chip buffer amplifier in the case of the main ADC when operated in buffered mode, and directly to the Σ-Δ modulator input in the case of the auxiliary ADC and when the main ADC is operated in unbuffered mode. When the analog input channel is switched, the settling time of the part must elapse before a new valid word is available from the ADC.

Figure 16 shows the analog input channel configurations available to the user when the CHCON bit in the mode register is set to a zero. In this case, the main ADC can be configured as one or two fully differential input channels (AIN1/AIN2 and AIN3/AIN4) and the aux can be configured as two single-ended inputs with respect to AGND (AIN3/AGND and AIN4/AGND) and one fully differential input AIN5/AIN6). The aux can also be configured as three single-ended inputs with respect to AGND (AIN3/AGND, AIN4/AGND, and AIN5/AGND) by tying AIN6 externally to AGND. The temp sensor is available as an internal connection.

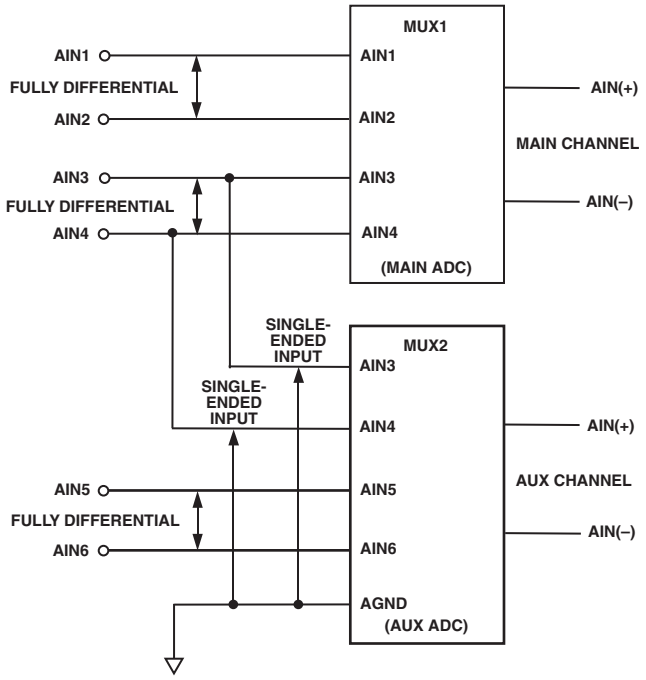


Figure 16. Input Channel Configurations with CHCON = 0

Figure 17 shows the analog input channel configurations available to the user when the CHCON bit in the mode register is set to 1. In this case, the main ADC is configured as three pseudodifferential input channels (AIN1/AIN4, AIN2/AIN4, and AIN3/AIN4) and the aux can be configured as two single-ended inputs with respect to AGND (AIN5/AGND and AIN6/AGND) and one fully differential input (AIN5/AIN6). The temp sensor is available as an internal connection.

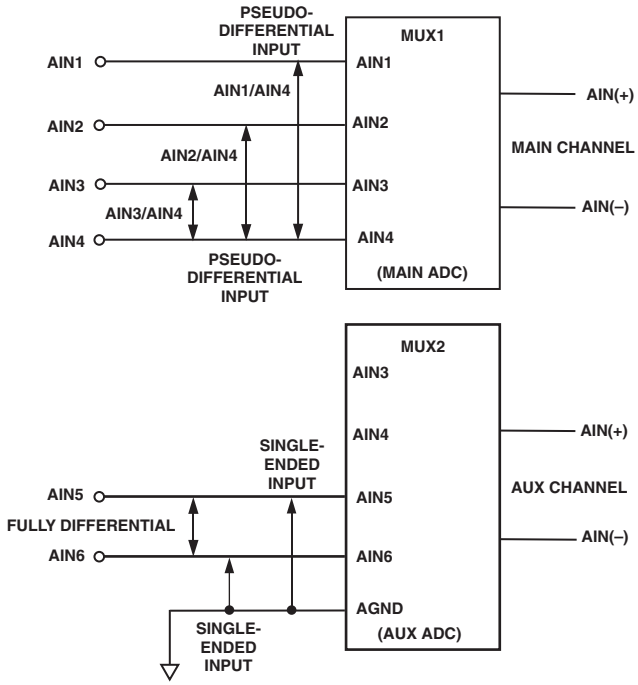


Figure 17. Input Channel Configurations with CHCON = 1

In buffered mode ($\overline{BUF}$ = 0), the output of the main ADC multiplexer feeds into a high impedance input stage of the buffer amplifier. As a result, the main ADC inputs can handle significant source impedances and are tailored for direct connection to external resistive-type sensors like strain gages or resistance temperature detectors (RTDs).

The auxiliary ADC and the main ADC when operated with $\overline{BUF}$ = 1, however, are unbuffered, resulting in higher analog input current. It should be noted that these unbuffered input paths provide a dynamic load to the driving source. Therefore, resistor/capacitor combinations on the input pins can cause dc gain errors, depending on the output impedance of the source that is driving the ADC inputs. Table XVIII and XIX show the allowable external resistance/capacitance values for unbuffered mode such that no gain error at the 16- and 20-bit level, respectively, is introduced.

The absolute input voltage range on the main ADC when operated in buffered mode is restricted to a range between AGND + 100 mV and AV_{DD} – 100 mV. Care must be taken in setting up the common-mode voltage and input voltage range so that these limits are not exceeded; otherwise there will be a degradation in linearity and noise performance.

Table XVIII. Max Resistance for No 16-Bit Gain Error (Unbuffered Mode)

	External Capacitance					
Gain	**0 pF**	**50 pF**	**100 pF**	**500 pF**	**1000 pF**	**5000 pF**
1	111.3K	27.8K	16.7K	4.5K	2.58K	700
2	53.7K	13.5K	8.1K	2.2K	1.26K	360
4	25.4K	6.4K	3.9K	1.0K	600	170
8–128	10.7K	2.9K	1.7K	480	270	75

Table XIX. Max Resistance for No 20-Bit Gain Error (Unbuffered Mode)

	External Capacitance					
Gain	**0 pF**	**50 pF**	**100 pF**	**500 pF**	**1000 pF**	**5000 pF**
1	84.9K	21.1K	12.5K	3.2K	1.77K	440
2	42.0K	10.4K	6.1K	1.6K	880	220
4	20.5K	5.0K	2.9K	790K	430	110
8–128	8.8K	2.3K	1.3K	370	195	50

The absolute input voltage range on the auxiliary ADC and the main ADC in unbuffered mode includes the range between AGND – 30 mV to AV_{DD} + 30 mV as a result of being unbuffered. The negative absolute input voltage limit does allow the possibility of monitoring small true bipolar signals with respect to AGND.

Programmable Gain Amplifier

The output from the buffer on the main ADC is applied to the input of the on-chip programmable gain amplifier (PGA). The PGA can be programmed through eight different unipolar and bipolar ranges. The PGA gain range is programmed via the range bits in the ADC0CON register. With an external 2.5 V reference applied, the unipolar ranges are 0 mV to 20 mV, 0 mV to 40 mV, 0 mV to 80 mV, 0 mV to 160 mV, 0 mV to 320 mV, 0 mV to 640 mV, 0 V to 1.28 V and 0 V to 2.56 V while bipolar ranges are ±20 mV, ±40 mV, ±80 mV, ±160 mV, ±320 mV, ±640 mV, ±1.28 V, and ±2.56 V. These are the ranges that should appear at the input to the on-chip PGA. The ADC range matching specification of 2 μV (typ) across all ranges means that calibration need only be carried out on a single range and does not have to be repeated when the PGA range is changed. This is a significant advantage when compared with similar ADCs available on the market.

Typical matching across ranges is shown in Figure 18. Here, the primary ADC is configured in fully differential, bipolar mode with an external 2.5 V reference, while an analog input voltage of just greater than 19 mV is forced on its analog inputs. The ADC continuously converts the dc voltage at an update rate of 5.35 Hz, i.e., SF = 0xFF. In total, 800 conversion results are gathered. The first 100 results are gathered with the primary ADC operating in the ±20 mV range. The ADC range is then switched to ±40 mV and 100 more results are gathered; this continues until the last 100 samples are gathered with the ADC configured in the ±2.5 V range. From Figure 18, the variation in the sample mean through each range, i.e., the range matching, is seen to be on the order of 2 μV.

The auxiliary ADC does not incorporate an eight range PGA. The aux ADC operates at a gain of 1 or a gain of 2 as determined by the ARN bit in the AD1CON register.

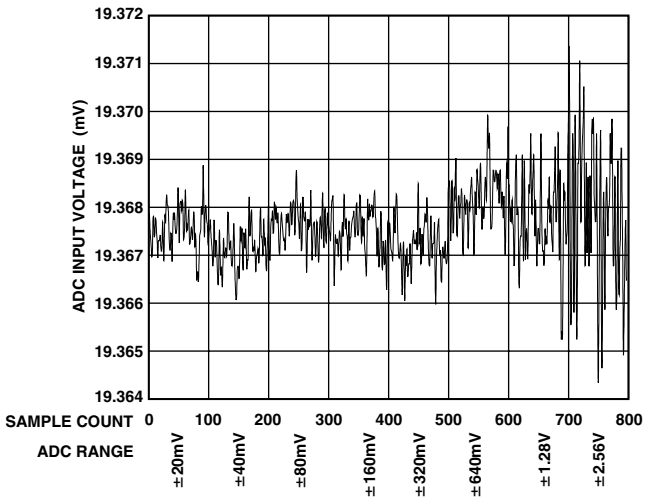


Figure 18. Main ADC Range Matching

Bipolar/Unipolar Configuration

The analog inputs on the AD7719 can accept either unipolar or bipolar input voltage ranges. Bipolar input ranges do not imply that the part can handle negative voltages with respect to system AGND. Unipolar and bipolar signals on the AIN(+) input on the main ADC are referenced to the voltage on the respective AIN(–) input. AIN(+) and AIN(–) refer to the signals seen by the modulator that come from the output of the multiplexer, as shown in Figures 16 and 17.

For example, if AIN(–) is 2.5 V and the main ADC is configured for an analog input range of 0 mV to 20 mV, the input voltage range on the AIN(+) input is 2.5 V to 2.52 V. If AIN(–) is 2.5 V and the AD7719 is configured for an analog input range of ±1.28 V, the analog input range on the AIN(+) input is 1.22 V to 3.78 V (i.e., 2.5 V ± 1.28 V). Bipolar or unipolar options are chosen by programming the main and auxiliary U/$\overline{B}$ bit in the ADC0CON and ADC1CON registers, respectively. This programs the relevant ADC for either unipolar or bipolar operation. Programming for either unipolar or bipolar operation does not change any of the input signal conditioning; it simply changes the data output coding and the points on the transfer function where calibrations occur.

Data Output Coding

When the ADC is configured for unipolar operation, the output coding is natural (straight) binary with a zero differential input voltage resulting in a code of 000 . . . 000, a midscale voltage resulting in a code of 100 . . . 000, and a full-scale input voltage resulting in a code of 111 . . . 111. The output code for any analog input voltage on the main ADC can be represented as follows:

$$Code = \left(AIN \times GAIN \times 2^N\right) \Big/ \left(1.024 \times V_{REF}\right)$$

Where *AIN* is the analog input voltage, *GAIN* is the PGA gain, i.e., 1 on the 2.56 V range and 128 on the 20 mV range, and *N* = 16 in 16-bit mode and *N* = 24 in 24-bit mode of operation.

The output code for any analog input voltage on the aux ADC can be represented as follows:

$$Code = \left(AIN \times GAIN \times 2^N\right) \Big/ V_{REF}$$

Where *AIN* is the analog input voltage, *GAIN* is 1 or 2, determined by the ARN bit in the aux ADC control register, i.e., 1 on the VREF range and 2 on the VREF/2 range, and *N* = 16.

When an ADC is configured for bipolar operation, the coding is offset binary with a negative full-scale voltage resulting in a code of 000 . . . 000, a zero differential voltage resulting in a code of 100 . . . 000, and a positive full-scale voltage resulting in a code of 111 . . . 111. The output code from the main ADC for any analog input voltage can be represented as follows:

$$Code = 2^{N-1} \times \left[\left(AIN \times GAIN \Big/ \left(1.024 \times V_{REF}\right)\right) + 1\right]$$

Where *AIN* is the analog input voltage, *GAIN* is the PGA gain, i.e., 1 on the ±2.56 V range and 128 on the ±20 mV range, *N* = 16 in 16-bit mode, and *N* = 24 in 24-bit mode of operation.

The output code from the aux ADC for any analog input voltage can be represented as follows:

$$Code = 2^{N-1} \times \left[\left(AIN \times GAIN / V_{REF}\right) + 1\right]$$

Where *AIN* is the analog input voltage, *GAIN* is 1 or 2, determined by the ARN bit in the aux ADC control register, i.e., 1 on the ±VREF range, 2 on the ±VREF/2 range, and *N* = 16.

Burnout Currents

The main ADC on the AD7719 contains two 100 nA constant current generators, one sourcing current from AV_{DD} to AIN(+), and one sinking current from AIN(–) to AGND. The currents are switched to the selected analog input pair. Both currents are either on or off, depending on the Burnout Current Enable (BO) bit in the IOCON register. These currents can be used to verify that an external transducer is still operational before attempting to take measurements on that channel. Once the burnout currents are turned on, they will flow in the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken. If the resultant voltage measured is full-scale, the user needs to verify why this is the case. A full-scale reading could mean that the front end sensor is open circuit; it could also mean that the front end sensor is overloaded and is justified in outputting full-scale, or that the reference may be absent and the NOXREF bit is set, thus clamping the data to all 1s.

When reading all 1s from the output, the user needs to check these three cases before making a judgment. If the voltage measured is 0 V, it may indicate that the transducer has short circuited. For normal operation, these burnout currents are turned off by writing a 0 to the BO bit in the IOCON register. The current sources work over the normal absolute input voltage range specifications with buffers on.

Excitation Currents

The AD7719 also contains two matched, software configurable 200 μA constant current sources. Both source current from AV_{DD} that is directed to either the IOUT1 or IOUT2 pins of the device. These current sources are controlled via bits in the IOCON register. The configuration bits enable the current sources and can be configured to source 200 μA individually to both pins or a combination of both currents, i.e., 400 μA to either of the selected output pins. These current sources can be used to excite external resistive bridge or RTD sensors.

Crystal Oscillator

The AD7719 is intended for use with a 32.768 kHz watch crystal. A PLL internally locks onto a multiple of this frequency to provide a stable 4.194304 MHz clock for the ADC. The modulator sample rate is the same as the crystal oscillator frequency.

The start-up time associated with 32 kHz crystals is typically 300 ms. The OSPD bit in the mode register can be used to prevent the oscillator from powering down when the AD7719 is placed in power-down mode. This avoids having to wait 300 ms after exiting power-down to start a conversion at the expense of raising the power-down current.

Reference Input

The AD7719 has a fully differential reference input capability for the main channel while the auxiliary channel accepts only a single-ended reference. On the main channel, the reference inputs REFIN1(+) and REFIN1(–) provide a differential reference input capability. The common-mode range for these differential inputs is from AGND to AV_{DD}. The reference input is unbuffered, and therefore excessive R-C source impedances will introduce gain errors. The nominal reference voltage, VREF, (REFIN1(+) – REFIN1(–), for specified operation is 2.5 V, but the AD7719 is functional with reference voltages from 1 V to AV_{DD}. In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the part, the effect of the low frequency noise in the excitation source will be removed as the application is ratiometric. If the AD7719 is used in a nonratiometric application, a low noise reference should be used. Recommended reference voltage sources for the AD7719 include the AD780, REF43, and REF192. It should also be noted that the reference inputs provide a high impedance, dynamic load. Because the input impedance of each reference input is dynamic, resistor/capacitor combinations on these inputs can cause dc gain errors, depending on the output impedance of the source that is driving the reference inputs. Reference voltage sources like those recommended (e.g., AD780) will typically have low output impedances and are therefore tolerant to having decoupling capacitors on the REFIN1(+) without introducing gain errors in the system. Deriving the reference input voltage across an external resistor, as shown in Figure 19, will mean that the reference input sees a significant external source impedance. External decoupling on the REFIN1(+) and REFIN1(–) pins would not be recommended in this type of circuit configuration.

The auxiliary channel conversion results are based on the voltage applied to REFIN2. This is a single-ended reference input specified for 2.5 V operation but functional with input voltages from 1 V to AV_{DD}.

Reference Detect
The AD7719 includes on-chip circuitry to detect if the part has a valid reference on the main ADC for conversions or calibrations. If the voltage between the external REFIN1(+) and REFIN1(–) pins goes below 0.3 V or either the REFIN1(+) or REFIN1(–) inputs are open circuit, the AD7719 detects that it no longer has a valid reference. In this case, the NOXREF bit of the Status register is set to 1. If the AD7719 is performing normal conversions and the NOXREF bit becomes active, the conversion results revert to all 1s. Therefore, it is not necessary to continuously monitor the status of the NOXREF bit when performing conversions. It is only necessary to verify its status if the conversion result read from the ADC data register is all 1s. If the AD7719 is performing either an offset or gain calibration and the NOXREF bit becomes active, the updating of the respective calibration registers is inhibited to avoid loading incorrect coefficients to these registers, and the ERR0 bit in the Status register is set. If the user is concerned about verifying that a valid reference is in place every time a calibration is performed, the status of the ERR0 bit should be checked at the end of the calibration cycle.

Reset Input
The $\overline{\text{RESET}}$ input on the AD7719 resets all the logic, the digital filter, and the analog modulator while all on-chip registers are reset to their default state. $\overline{\text{RDY}}$ is driven high and the AD7719 ignores all communications to any of its registers while the $\overline{\text{RESET}}$ input is low. When the $\overline{\text{RESET}}$ input returns high, the AD7719 operates with its default setup conditions and it is necessary to set up all registers and carry out a system calibration if required after a $\overline{\text{RESET}}$ command.

Power-Down Mode
Loading 0, 0, 0 to the MD2, MD1, MD0 bits in the ADC mode register places the AD7719 in device power-down mode. Device power-down mode is the default condition for the AD7719 on power-up. Individual ADCs (main or auxiliary) can be put in power-down mode using the AD0EN in the main ADC control register (AD0CON) to power off the main ADC or the AD1EN in the auxiliary ADC control register (AD1CON) to power off the auxiliary ADC. The AD7719 retains the contents of all its on-chip registers (including the data register) while in power-down or ADC disable mode.

The device power-down mode does not affect the digital interface, and it does affect the status of the $\overline{\text{RDY}}$ pin. Putting the AD7719 into power-down or idle mode will reset the $\overline{\text{RDY}}$ line high. Placing the part in power-down mode reduces the total current (AI_{DD} + DI_{DD}) to 31 μA max when the part is operated at 5 V and the oscillator is allowed to run during power-down mode. With the oscillator shuts down, the total I_{DD} is 3 μA max at 3 V and 9 μA max at 5 V.

Idle Mode
The AD7719 also contains an idle mode. The ADC defaults to this mode on completion of a calibration sequence and on the completion of a conversion when operating in single conversion mode. In idle mode, the power consumption of the AD7719 is not reduced below the normal mode dissipation.

ADC Disable Mode
This mode is entered by setting both the AD0EN and AD1EN bits in the main and max ADC control registers to 0 and setting the Mode bits (MD2, MD1, MD0) in the Mode register to non-0. In this mode, the internal PLL is enabled and the user can activate the current sources and power switches, but the power consumption of the ADC is reduced as both ADCs are disabled. In this mode, the AI_{DD} is reduced to 0.15 mA and the DI_{DD} is reduced to 0.35 mA max at 3 V and to 0.4 mA max with DV_{DD} = 5 V.

Calibration
The AD7719 provides four calibration modes that can be programmed via the mode bits in the mode register. One of the major benefits of the AD7719 is that it is factory-calibrated as part of the final test process with the generated coefficients stored within the ADC. At power-on, the factory gain calibration coefficients are automatically loaded to the gain calibration registers on the AD7719. Each ADC (primary and auxiliary) has dedicated calibration register pairs as outlined in the AD0CON and AD1CON register descriptions. Given that the ADC is factory-calibrated and a chopping scheme is employed that gives excellent offset and drift performance, it is envisaged that in the majority of applications the user will not need to perform any field calibrations.

However, the factory calibration values in the ADC calibration registers will be overwritten if any one of the four calibration options are initiated. Even though an internal offset calibration mode is described below, it should be recognized that both ADCs are chopped. This chopping scheme inherently minimizes offset and means that an internal offset calibration should never be required. Also, because factory 25°C gain calibration coefficients are automatically present at power-on, an internal full-scale calibration will only be required if the part is being operated at temperatures significantly different from 25°C or away from the calibration conditions. The AD7719 offers internal or system calibration facilities. For full calibration to occur on the selected ADC, the calibration logic must record the modulator output for two different input conditions. These are zero-scale and full-scale points derived by performing a conversion on the different input voltages provided to the input of the modulator during calibration. The result of the zero-scale calibration conversion is stored in the offset calibration registers for the appropriate ADC. The result of the full-scale calibration conversion is stored in the gain calibration registers for the appropriate ADC. With these readings, the calibration logic can calculate the offset and the gain slope for the input-to-output transfer function of the converter.

During an internal zero-scale or full-scale calibration, the respective zero input and full-scale input are automatically connected to the ADC input pins internally to the device. A system calibration, however, expects the system zero-scale and system full-scale voltages to be applied to the external ADC pins before the calibration mode is initiated. In this way, external ADC errors are taken into account and minimized as a result of system calibration. It should also be noted that to optimize calibration accuracy, all AD7719 ADC calibrations are automatically carried out at the slowest update rate.

Internally in the AD7719, the coefficients are normalized before being used to scale the words coming out of the digital filter. The offset calibration coefficient is subtracted from the result prior to the multiplication by the gain coefficient.

From an operational point of view, a calibration should be treated like another ADC conversion. A zero-scale calibration (if required) should always be carried out before a full-scale calibration. System software should monitor the relevant ADC RDY0/1 bit in the Status register to determine end of calibration via a polling sequence or interrupt driven routine.

Grounding and Layout

Since the analog inputs and reference input on the main ADC are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part will remove common-mode noise on these inputs. The analog and digital supplies to the AD7719 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The AD7719 can be operated with 5 V analog and 3 V digital supplies, or vice versa. The digital filter will provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs provided these noise sources do not saturate the analog modulator. As a result, the AD7719 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7719 is so high, and the noise levels from the AD7719 are so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the AD7719 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes as it gives the best shielding.

Although the AD7719 has separate pins for analog and digital ground, the AGND and DGND pins are tied together within the device via the substrate. The user must not tie these pins external to separate ground planes unless the ground planes are connected together near the AD7719.

In systems where the AGND and DGND are connected somewhere else in the system, i.e., the system power supply, they should not be connected again at the AD7719 as a ground loop will result. In these situations, it is recommended that the AD7719's AGND and DGND pins be tied to the AGND plane. In any layout, it is important that the user keep in mind the flow of currents in the system, ensuring that the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. Avoid forcing digital currents to flow through the AGND sections of the layout.

The PWRGND pin is tied internally to AGND on the AD7719. The PWRGND pad internally has a resistance of less then 50 mΩ to the PWRGND pin, while the resistance back to the AGND pad is >3 Ω. This means that 19.5 mA of the maximum specified current (20 mA) will flow to PWRGND with the remaining 0.5 mA flowing to AGND. PWRGND and AGND should be tied together at the AD7719 and it is important to minimize the resistance on the ground return lines.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7719 to prevent noise coupling. The power supply lines to the AD7719 should use as wide a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. All analog supplies should be decoupled with 10 μF tantalum in parallel with 0.1 μF capacitors to AGND. To achieve the best from these decoupling components, they have to be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 μF ceramic capacitors to DGND. In systems where a common supply voltage is used to drive both the AV_{DD} and DV_{DD} of the AD7719, it is recommended that the system's AV_{DD} supply be used. This supply should have the recommended analog supply decoupling capacitors between the AV_{DD} pin of the AD7719 and AGND, and the recommended digital supply decoupling capacitor between the DV_{DD} pin of the AD7719 and DGND.

APPLICATIONS

The AD7719 provides a low cost, high resolution analog-to-digital function. Because the analog-to-digital function is provided by a Σ-Δ architecture, it makes the part more immune to noisy environments, making it ideal for use in sensor measurement and industrial and process control applications. Given the architecture used in the AD7719, where the signal chain is chopped and the device is factory-calibrated at final test, field calibration can be avoided due to the extremely low offset and gain drifts exhibited by this converter. It also provides a programmable gain amplifier, a digital filter, and system calibration options. Thus, it provides far more system-level functionality than off-the-shelf integrating ADCs without the disadvantage of having to supply a high quality integrating capacitor. In addition, using the AD7719 in a system allows the system designer to achieve a much higher level of resolution because noise performance of the AD7719 is significantly better than that of integrating ADCs.

The on-chip PGA allows the AD7719 to handle an analog input voltage range as low as 10 mV full-scale with V_{REF} = 1.25 V. The differential inputs of the part allow this analog input range to have an absolute value anywhere between AGND + 100 mV and AV_{DD} – 100 mV. It allows the user to connect the transducer directly to the input of the AD7719. The programmable gain front end on the AD7719 allows the part to handle unipolar analog input ranges from 0 mV to 20 mV to 0 V to 2.5 V and bipolar inputs of ±20 mV to ±2.5 V. Because the part operates from a single supply, these bipolar ranges are with respect to a biased-up differential input. Another key advantage of the AD7719 is that it contains two Σ-Δ converters operating in parallel; thus the user does not need to interrupt the main channel when a secondary measurement on a different variable needs to be performed.

Pressure Measurement

One typical application of the AD7719 is pressure measurement. Figure 19 shows the AD7719 used with a pressure transducer, the BP01 from Sensym.

The pressure transducer is arranged in a bridge network and gives a differential output voltage between its OUT(+) and OUT(–) terminals. With rated full-scale pressure (in this case 300 mmHg) on the transducer, the differential output voltage is 3 mV/V of the input voltage (i.e., the voltage between its IN(+) and IN(–) terminals).

Assuming a 5 V excitation voltage, the full-scale output range from the transducer is 15 mV. The excitation voltage for the bridge can be used to directly provide the reference for the ADC as the reference input range includes the supplies. Alternatively, a suitable resistor divider can be implemented that allows the full dynamic range of the input to be utilized in these application. This implementation is fully ratiometric, so variations in the excitation voltage do not introduce errors in the system. Choosing resistor values of 20 kΩ and 12 kΩ as per Figure 19 give a 1.875 V reference voltage for the AD7719 when the excitation voltage is 5 V.

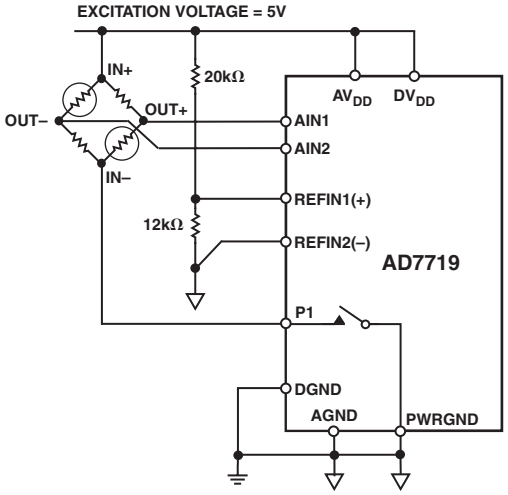


Figure 19. Pressure Measurement Using AD7719

Using the part with a programmed gain of 128 results in the full-scale input span of the AD7719 being 15 mV, which corresponds with the output span from the transducer.

A second key advantage to using the AD7719 in transducer based applications is that the on-chip low-side power switch can be fully utilized in low power applications. The low-side power switch is connected in series with the cold side of the bridge. In normal operation, the switch is closed and measurements can be taken from the bridge. In applications where power is of concern, the AD7719 can be put in low power mode, substantially reducing the power burned in the application. In addition to this, the power switch can be opened while in low power mode thus avoiding the unnecessary burning of power in the front end transducer. When the AD7719 is taken back out of power-down and the power switch is closed, the user should ensure that the front end circuitry is fully settled before attempting a read from the AD7719.

The circuit in Figure 20 shows a method that utilizes all three pseudodifferential input channels on the AD7719 main channel to temperature-compensate a pressure transducer.

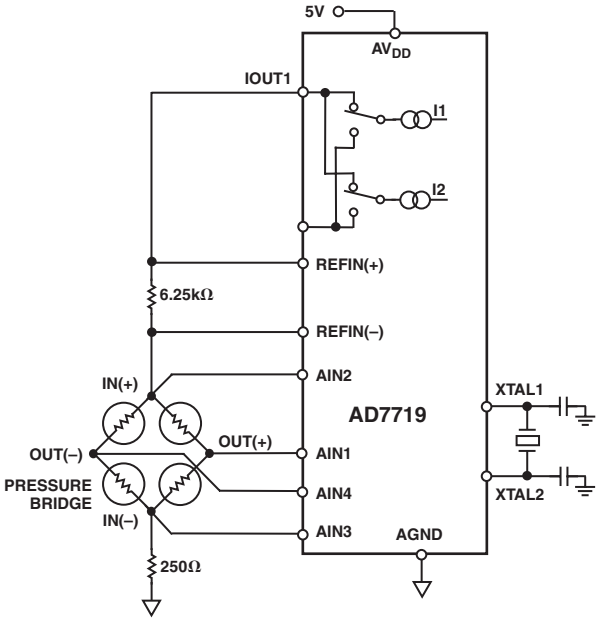


Figure 20. Temperature-Compensating a Pressure Transducer

In this application, pseudodifferential input channel AIN1/AIN4 is used to measure the bridge output while pseudodifferential channels AIN2/AIN4 and AIN3/AIN4 measure the voltage across the bridge. The voltage measured across the bridge will vary proportionally with temperature, and the delta in this voltage can be used to temperature-compensate the output of the pressure bridge.

Temperature Measurement

The AD7719 is also useful in temperature measurement applications; Figure 21 shows an RTD temperature measurement application. In this application, the transducer is an RTD (resistive temperature device), a PT100. The arrangement is a 4-lead RTD configuration. There are voltage drops across the lead resistances RL1 and RL4, but these simply shift the common-mode voltage. There is no voltage drop across lead resistances RL2 and RL3 as the input current to the AD7719 is very low, looking into a high input impedance buffer. R_{CM} is included to shift the analog input voltage to ensure that it lies within the common-mode range (AGND + 100 mV to AV_{DD} – 100 mV) of the ADC. In the application shown, the on-chip 200 μA current source provides the excitation current for the PT100 and also generates the reference voltage for the AD7719 via the 12.5 kΩ resistor. Variations in the excitation current do not affect the circuit as both the input voltage and the reference voltage vary ratiometrically with the excitation current. However, the 12.5 kΩ resistor must have a low temperature coefficient to avoid errors in the reference voltage over temperature.

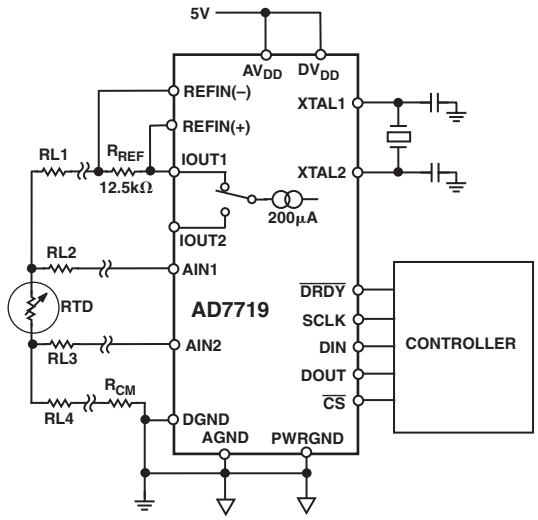


Figure 21. 4-Wire RTD Temperature Measurement Using the AD7719

Figure 22 shows a further enhancement to the circuit shown in Figure 21. Generally, dc excitation has been accepted as the normal method of exciting resistive-based sensors like RTDs (resistance temperature detectors) in temperature measurement applications.

With dc excitation, the excitation current through the sensor must be large enough so that the smallest temperature/resistance change to be measured results in a voltage change that is larger than the system noise, offset, and drift of the system. The purpose of switching the excitation source is to eliminate dc-induced errors. DC errors (EMF1 and EMF2) due to parasitic thermocouples produced by differential metal connections (solder and copper track) within the circuit are also eliminated when using this switching arrangement. This excitation is a form of synchronous detection where the sensor is excited with an alternating excitation source and the ADC only measures information in the same phase as the excitation source.

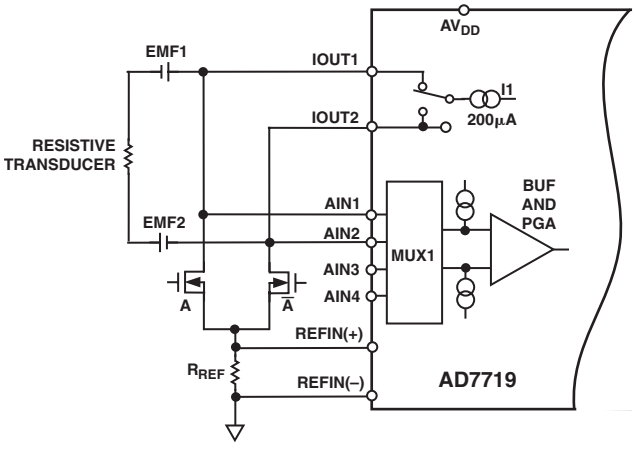


Figure 22. Low Resistance Measurement AD7719

The switched polarity current source is developed using the on-chip current sources and external phase control switches (A and $\overline{A}$) driven from the controller. During the conversion process, the AD7719 takes two conversion results, one on each phase. During Phase 1, the on-chip current source is directed to IOUT1 and flows top to bottom through the sensor and switch controlled by $\overline{A}$. In Phase 2, the current source is directed to IOUT2 and flows in the opposite direction through the sensor and through switch controlled by A. In all cases, the current flows in the same direction through the reference resistor to develop the reference voltage for the ADC. All measurements are ratiometrically derived. The results of both conversions are combined within the microcontroller to produce one output measurement representing the resistance or temperature of the transducer. For example, if the RTD output during Phase 1 is 10 mV, a 1 mV circuit-induced dc error exists due to parasitic thermocouples, and the ADC measures 11 mV. During the second phase, the excitation current is reversed and the ADC measures –10 mV from the RTD and again sees 1 mV dc error, giving an ADC output of –9 mV during this phase. These measurements are processed in the controller (11 mV – (–9 mV)/2 = 10 mV), thus removing the dc-induced errors within the system.

In the circuit shown in Figure 22, the resistance measurement is made using ratiometric techniques. Resistor R_{REF}, which develops the ADC reference, must be stable over temperature to prevent reference-induced errors in the measurement output.

3-Wire RTD Configurations

To fully optimize a 3-wire RTD configuration, two identically matched current sources are required. The AD7719, which contains two well-matched current sources, is ideally suited to these applications. One possible 3-wire configuration using the AD7719 is outlined in Figure 23.

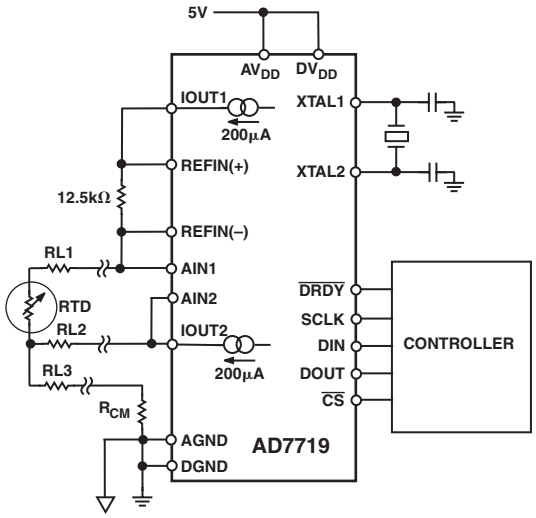


Figure 23. 3-Wire RTD Configuration Using the AD7719

In this 3-wire configuration, the lead resistances will result in errors if only one current source is used because the 200 μA will flow through RL1, developing a voltage error between AIN1 and AIN2. In the scheme outlined below, the second RTD current source is used to compensate for the error introduced by the 200 μA flowing through RL1. The second RTD current flows through RL2. Assuming RL1 and RL2 are equal (the leads would normally be of the same material and of equal length), and IOUT1 and IOUT2 match, the error voltage across RL2 equals the error voltage across RL1, and no error voltage is developed between AIN1 and AIN2. Twice the voltage is developed across RL3, but since this is a common-mode voltage, it will not introduce errors. R_{CM} is included so the current flowing through the combination of RL3 and R_{CM} develops enough voltage that the analog input voltage seen by the AD7719 is within the common-mode range of the ADC. The reference voltage for the AD7719 is also generated using one of these matched current sources. This reference voltage is developed across the 12.5 kΩ resistor as shown, and applied to the differential reference inputs of the AD7719. This scheme ensures that the analog input voltage span remains ratiometric to the reference voltage. Any errors in the analog input voltage due to the temperature drift of the RTD current source is compensated for by the variation in the reference voltage. The typical drift matching between the two RTD current sources is less than 1 ppm/°C. The voltage on either I_{OUT} pin can go to within 0.6 V of the AV_{DD} supply.

Smart Transmitters

Smart transmitters are another key design-in area for the AD7719. The dual Σ-Δ converter, single-supply operation, 3-wire interface capabilities, and small package size are all of benefit in smart transmitters. Here, the entire smart transmitter must operate from the 4 to 20 mA loop. Tolerances in the loop mean that the amount of current available to power the transmitter is as low as 3.5 mA. Figure 24 shows a block diagram of a smart transmitter, which includes the AD7719.

Not shown in Figure 24 is the isolated power source required to power the front end. The advantages of the AD7719 in these applications is the dual-channel operation, meaning that the user does not have to interrupt the main channel when measuring secondary variables, and therefore does not have the latency associated with the settling times of the digital filter. The fact that the AD7719 is factory-calibrated means that in the majority of applications, the user will not have to perform any field calibration given the excellent offset and gain drift performance of the device as a result of the signal chain chopping employed in the signal chain.

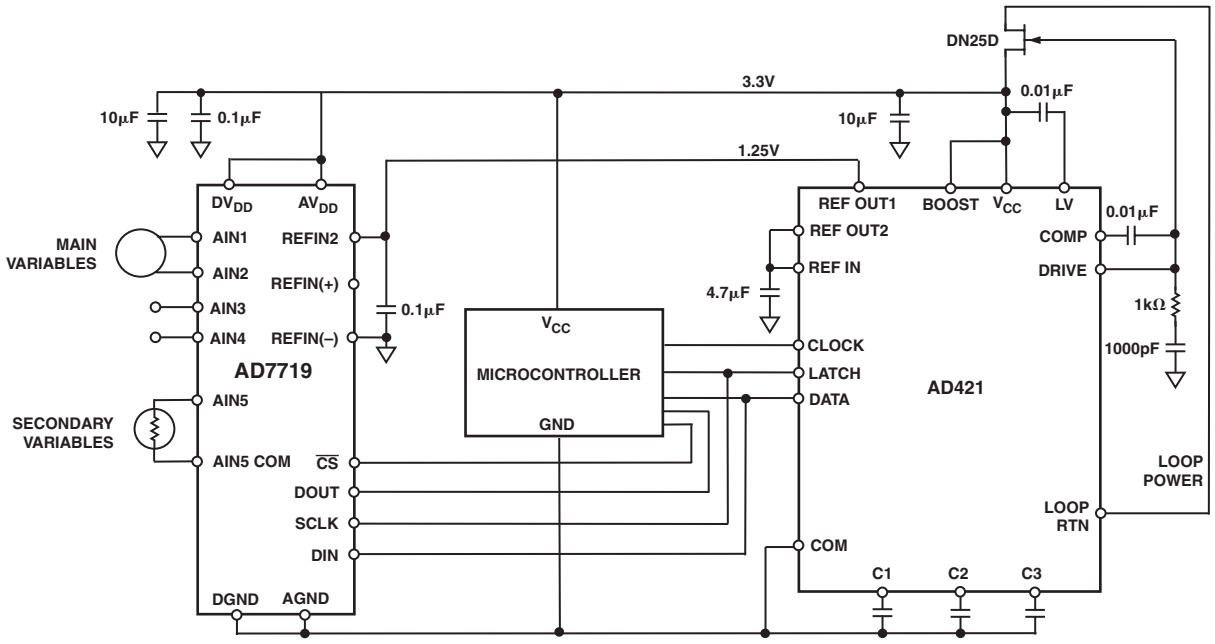
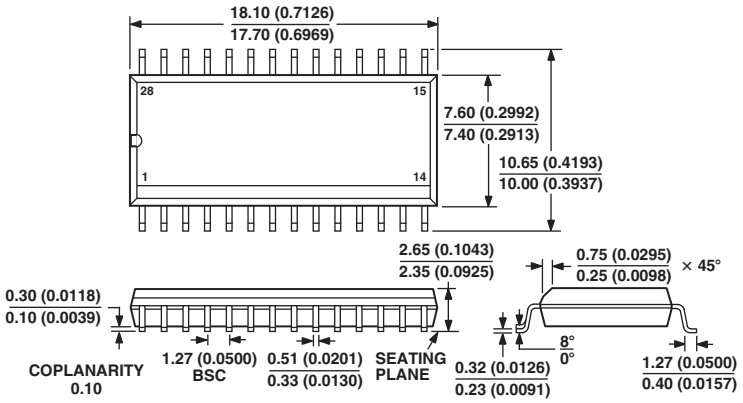


Figure 24. Smart Transmitter Employing the AD7719

OUTLINE DIMENSIONS

28-Lead Standard Small Outline Package [SOIC]
Wide Body
(R-28)

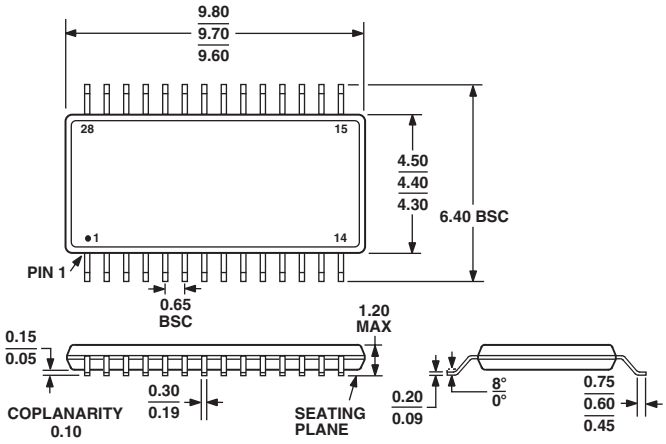
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013AE
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)

Dimensions shown in millimeters



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Revision History

Location	Page
4/03—Data Sheet changed from REV. 0 to REV. A.	
Updated format	Universal
Changes to SPECIFICATIONS	3
Updated OUTLINE DIMENSIONS	39

C02460–0–4/03(A)

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