# THE DATASHEET OF

# AD8228BRMZ-R7

www.win-source.net 0086-755-83957316

# Low Gain Drift Precision Instrumentation Amplifier

# AD8228

## FEATURES

- Easy to use
- Pin strappable gains of 10 and 100
- Wide power supply range: ±2.3 V to ±18 V
- DC specifications (B Grade, G = 10)
  - 2 ppm/°C gain drift
  - 0.02% gain error
  - 50 µV maximum input offset voltage
  - 0.8 µV/°C maximum input offset drift
  - 0.6 nA maximum input bias current
  - 100 dB CMRR
- AC specifications
  - 650 kHz, −3 dB bandwidth (G = 10)
  - 2 V/µs slew rate
- Low noise
  - 8 nV/√Hz, @ 1 kHz (G = 100)
  - 0.3 µV p-p from 0.1 Hz to 10 Hz (G = 100)

## APPLICATIONS

- Weigh scales
- Industrial process controls
- Bridge amplifiers
- Precision data acquisition systems
- Medical instrumentation
- Strain gages
- Transducer interfaces

## CONNECTION DIAGRAM

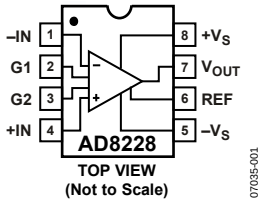


*Figure 1.*

**Table 1. Instrumentation Amplifiers by Category**

| General Purpose | Zero Drift | Military Grade | Low Power | High Speed PGA |
|---|---|---|---|---|
| AD8220[1] | AD8231[1] | AD620 | AD627[1] | AD8250 |
| AD8221 | AD8553[1] | AD621 | AD623[1] | AD8251 |
| AD8222 | AD8555[1] | AD524 | | AD8253 |
| AD8224[1] | AD8556[1] | AD526 | | |
| AD8228 | AD8557[1] | AD624 | | |

[1] Rail-to-rail output.

## GENERAL DESCRIPTION

The AD8228 is a high performance instrumentation amplifier with very high gain accuracy. Because all gain setting resistors are internal and laser trimmed, gain accuracy and gain drift are better than can be achieved with typical instrumentation amplifiers.

Low voltage offset, low offset drift, low gain drift, high gain accuracy, and high CMRR make this part an excellent choice in applications that demand the best dc performance possible, such as bridge signal conditioning.

The AD8228 operates on both single and dual supplies. Because the part can operate on supplies up to ±18 V, it is well suited for applications where high common-mode input voltages are encountered. The AD8228 is available in 8-lead MSOP and SOIC packages.

Performance is specified over the entire industrial temperature range of −40°C to +85°C for all grades. Furthermore, the AD8228 is operational from −40°C to +125°C. For a pin-compatible amplifier with similar specifications, but with a gain range of 1 to 1000, see the AD8221.

**Rev. 0**
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## REVISION HISTORY

**7/08—Revision 0: Initial Version**

# SPECIFICATIONS

## GAIN = 10

$V_S$ = ±15 V, $V_{REF}$ = 0 V, $T_A$ = 25°C, $R_L$ = 2 kΩ, all specifications referred to input, unless otherwise noted.

**Table 2.**

| Parameter | Conditions (Gain = 10) | A Grade Min | A Grade Typ | A Grade Max | B Grade Min | B Grade Typ | B Grade Max | Unit |
|---|---|---|---|---|---|---|---|---|
| COMMON-MODE REJECTION RATIO | | | | | | | | |
| CMRR DC to 60 Hz with 1 kΩ Source Imbalance | $V_{CM}$ = −10 V to +10 V | 94 | | | 100 | | | dB |
| CMRR at 2 kHz | $V_{CM}$ = −10 V to +10 V | 90 | | | 100 | | | dB |
| NOISE | $V_{IN+} = V_{IN-} = V_{REF}$ = 0 V | | | | | | | |
| Voltage Noise | f = 1 kHz | | | 15 | | | 15 | nV/√Hz |
| | f = 0.1 Hz to 10 Hz | | 0.5 | | | 0.5 | | µV p-p |
| Current Noise | f = 1 kHz | | 40 | | | 40 | | fA/√Hz |
| | f = 0.1 Hz to 10 Hz | | 6 | | | 6 | | pA p-p |
| VOLTAGE OFFSET | Referred to input, $V_S$ = ±5 V to ±15 V | | | | | | | |
| Offset | | | | 90 | | | 50 | µV |
| Over Temperature | T = −40°C to +85°C | | | 180 | | | 100 | µV |
| Average TC | T = −40°C to +85°C | | | 1.5 | | | 0.8 | µV/°C |
| Offset vs. Supply (PSR) | | 104 | 120 | | 106 | 120 | | dB |
| INPUT CURRENT | | | | | | | | |
| Input Bias Current | | | 0.5 | 1.5 | | 0.4 | 0.6 | nA |
| Over Temperature | T = −40°C to +85°C | | | 2.0 | | | 1 | nA |
| Average TC | T = −40°C to +85°C | | 1 | | | 1 | | pA/°C |
| Input Offset Current | | | 0.2 | 0.6 | | 0.1 | 0.4 | nA |
| Over Temperature | T = −40°C to +85°C | | | 0.8 | | | 0.6 | nA |
| Average TC | T = −40°C to +85°C | | 1 | | | 1 | | pA/°C |
| REFERENCE INPUT | | | | | | | | |
| $R_{IN}$ | | | 20 | | | 20 | | kΩ |
| $I_{IN}$ | $V_{IN+} = V_{IN-} = V_{REF}$ = 0 V | | 50 | 60 | | 50 | 60 | µA |
| Voltage Range | | $-V_S$ | | $+V_S$ | $-V_S$ | | $+V_S$ | V |
| Gain to Output | | | 1 ± 0.0001 | | | 1 ± 0.0001 | | V/V |
| DYNAMIC RESPONSE | | | | | | | | |
| Small Signal −3 dB Bandwidth | | | 650 | | | 650 | | kHz |
| Settling Time 0.01% | 10 V step | | 6 | | | 6 | | µs |
| Settling Time 0.001% | 10 V step | | 9 | | | 9 | | µs |
| Slew Rate | | 2 | 2.5 | | 2 | 2.5 | | V/µs |
| GAIN | $V_{OUT}$ = −10 V to +10 V | | | | | | | |
| Gain Error | | | | 0.07 | | | 0.02 | % |
| Gain Nonlinearity | | | | | | | | |
| $R_L$ = 10 kΩ | | | 3 | 10 | | 3 | 10 | ppm |
| $R_L$ = 2 kΩ | | | 3 | 10 | | 3 | 10 | ppm |
| Gain vs. Temperature | | | 1 | 10 | | 1 | 2 | ppm/°C |
| INPUT | | | | | | | | |
| Input Impedance | | | | | | | | |
| Differential | | | 100‖2 | | | 100‖2 | | GΩ‖pF |
| Common Mode | | | 100‖2 | | | 100‖2 | | GΩ‖pF |
| Input Operating Voltage Range[1] | $V_S$ = ±2.3 V to ±5 V | $-V_S$ + 1.9 | | $+V_S$ − 1.1 | $-V_S$ + 1.9 | | $+V_S$ − 1.1 | V |
| Over Temperature | T = −40°C to +85°C | $-V_S$ + 2.0 | | $+V_S$ − 1.2 | $-V_S$ + 2.0 | | $+V_S$ − 1.2 | V |
| Input Operating Voltage Range[1] | $V_S$ = ±5 V to ±18 V | $-V_S$ + 1.9 | | $+V_S$ − 1.2 | $-V_S$ + 1.9 | | $+V_S$ − 1.2 | V |
| Over Temperature | T = −40°C to +85°C | $-V_S$ + 2.0 | | $+V_S$ − 1.2 | $-V_S$ + 2.0 | | $+V_S$ − 1.2 | V |

| Parameter | Conditions (Gain = 10) | A Grade Min | A Grade Typ | A Grade Max | B Grade Min | B Grade Typ | B Grade Max | Unit |
|---|---|---|---|---|---|---|---|---|
| OUTPUT | $R_L$ = 10 kΩ | | | | | | | |
| Output Swing | $V_S$ = ±2.3 V to ±5 V | $-V_S$ + 1.1 | | $+V_S$ – 1.2 | $-V_S$ + 1.1 | | $+V_S$ – 1.2 | V |
| Over Temperature | T = –40°C to +85°C | $-V_S$ + 1.4 | | +Vs – 1.3 | $-V_S$ + 1.4 | | $+V_S$ – 1.3 | V |
| Output Swing | $V_S$ = ±5 V to ±18 V | $-V_S$ + 1.2 | | $+V_S$ – 1.4 | $-V_S$ + 1.2 | | $+V_S$ – 1.4 | V |
| Over Temperature | T = –40°C to +85°C | $-V_S$ + 1.6 | | $+V_S$ – 1.5 | $-V_S$ + 1.6 | | $+V_S$ – 1.5 | V |
| Short-Circuit Current | | | 18 | | | 18 | | mA |
| POWER SUPPLY | | | | | | | | |
| Operating Range | $V_S$ = ±2.3 V to ±18 V | ±2.3 | | ±18 | ±2.3 | | ±18 | V |
| Quiescent Current | | | 0.85 | 1 | | 0.85 | 1 | mA |
| Over Temperature | T = –40°C to +85°C | | 1 | 1.2 | | 1 | 1.2 | mA |
| TEMPERATURE RANGE | | | | | | | | |
| Specified Performance | | –40 | | +85 | –40 | | +85 | °C |
| Operating Range[2] | | –40 | | +125 | –40 | | +125 | °C |

[1] Operating near the input voltage range limit may reduce the available output range. See Figure 10 and Figure 11 for the input common-mode range vs. output voltage.
[2] See the Typical Performance Characteristics section for expected operation between 85°C to 125°C.

## GAIN = 100

$V_S$ = ±15 V, $V_{REF}$ = 0 V, $T_A$ = 25°C, $R_L$ = 2 kΩ, all specifications referred to input, unless otherwise noted.

**Table 3.**

| Parameter | Conditions (Gain = 100) | A Grade Min | A Grade Typ | A Grade Max | B Grade Min | B Grade Typ | B Grade Max | Unit |
|---|---|---|---|---|---|---|---|---|
| COMMON-MODE REJECTION RATIO | | | | | | | | |
| CMRR DC to 60 Hz with 1 kΩ Source Imbalance | $V_{CM}$ = −10 V to +10 V | 114 | | | 120 | | | dB |
| CMRR at 2 kHz | $V_{CM}$ = −10 V to +10 V | 100 | | | 105 | | | dB |
| NOISE | $V_{IN+} = V_{IN-} = V_{REF}$ = 0 V | | | | | | | |
| Voltage Noise | f = 1 kHz | | | 8 | | | 8 | nV/√Hz |
| | f = 0.1 Hz to 10 Hz | | 0.3 | | | 0.3 | | µV p-p |
| Current Noise | f = 1 kHz | | 40 | | | 40 | | fA/√Hz |
| | f = 0.1 Hz to 10 Hz | | 6 | | | 6 | | pA p-p |
| VOLTAGE OFFSET | Referred to input, $V_S$ = ±5 V to ±15 V | | | | | | | |
| Offset | | | | 90 | | | 50 | µV |
| Over Temperature | T = −40°C to +85°C | | | 140 | | | 80 | µV |
| Average TC | T = −40°C to +85°C | | | 0.9 | | | 0.5 | µV/°C |
| Offset vs. Supply (PSR) | | 118 | 140 | | 124 | 140 | | dB |
| INPUT CURRENT | | | | | | | | |
| Input Bias Current | | | 0.5 | 1.5 | | 0.4 | 0.6 | nA |
| Over Temperature | T = −40°C to +85°C | | | 2.0 | | | 1 | nA |
| Average TC | T = −40°C to +85°C | | 1 | | | 1 | | pA/°C |
| Input Offset Current | | | 0.2 | 0.6 | | 0.1 | 0.4 | nA |
| Over Temperature | T = −40°C to +85°C | | | 0.8 | | | 0.6 | nA |
| Average TC | T = −40°C to +85°C | | 1 | | | 1 | | pA/°C |
| REFERENCE INPUT | | | | | | | | |
| $R_{IN}$ | | | 20 | | | 20 | | kΩ |
| $I_{IN}$ | $V_{IN+} = V_{IN-} = V_{REF}$ = 0 V | | 50 | 60 | | 50 | 60 | µA |
| Voltage Range | | $-V_S$ | | $+V_S$ | $-V_S$ | | $+V_S$ | V |
| Gain to Output | | | 1 ± 0.0001 | | | 1 ± 0.0001 | | V/V |
| DYNAMIC RESPONSE | | | | | | | | |
| Small Signal −3 dB Bandwidth | | | 110 | | | 110 | | kHz |
| Settling Time 0.01% | 10 V step | | 13 | | | 13 | | µs |
| Settling Time 0.001% | 10 V step | | 15 | | | 15 | | µs |
| Slew Rate | | 2 | 2.5 | | 2 | 2.5 | | V/µs |
| GAIN | $V_{OUT}$ = −10 V to +10 V | | | | | | | |
| Gain Error | | | | 0.1 | | | 0.05 | % |
| Gain Nonlinearity | | | | | | | | |
| $R_L$ = 10 kΩ | | | 5 | 15 | | 5 | 15 | ppm |
| $R_L$ = 2 kΩ | | | 15 | 45 | | 15 | 45 | ppm |
| Gain vs. Temperature | | | 1 | 10 | | 1 | 2 | ppm/°C |
| INPUT | | | | | | | | |
| Input Impedance | | | | | | | | |
| Differential | | | 100\|\|2 | | | 100\|\|2 | | GΩ\|\|pF |
| Common Mode | | | 100\|\|2 | | | 100\|\|2 | | GΩ\|\|pF |
| Input Operating Voltage Range[1] | $V_S$ = ±2.3 V to ±5 V | $-V_S$ + 1.9 | | $+V_S$ − 1.1 | $-V_S$ + 1.9 | | $+V_S$ − 1.1 | V |
| Over Temperature | T = −40°C to +85°C | $-V_S$ + 2.0 | | $+V_S$ − 1.2 | $-V_S$ + 2.0 | | $+V_S$ − 1.2 | V |
| Input Operating Voltage Range[1] | $V_S$ = ±5 V to ±18 V | $-V_S$ + 1.9 | | $+V_S$ − 1.2 | $-V_S$ + 1.9 | | $+V_S$ − 1.2 | V |
| Over Temperature | T =−40°C to +85°C | $-V_S$ + 2.0 | | $+V_S$ − 1.2 | $-V_S$ + 2.0 | | $+V_S$ − 1.2 | V |

| Parameter | Conditions (Gain = 100) | A Grade Min | A Grade Typ | A Grade Max | B Grade Min | B Grade Typ | B Grade Max | Unit |
|---|---|---|---|---|---|---|---|---|
| OUTPUT | $R_L$ = 10 kΩ | | | | | | | |
| Output Swing | $V_S$ = ±2.3 V to ±5 V | $-V_S$ + 1.1 | | $+V_S$ – 1.2 | $-V_S$ + 1.1 | | $+V_S$ – 1.2 | V |
| Over Temperature | T = −40°C to +85°C | $-V_S$ + 1.4 | | +Vs – 1.3 | $-V_S$ + 1.4 | | $+V_S$ – 1.3 | V |
| Output Swing | $V_S$ = ±5 V to ±18 V | $-V_S$ + 1.2 | | $+V_S$ – 1.4 | $-V_S$ + 1.2 | | $+V_S$ – 1.4 | V |
| Over Temperature | T = −40°C to +85°C | $-V_S$ + 1.6 | | $+V_S$ – 1.5 | $-V_S$ + 1.6 | | $+V_S$ – 1.5 | V |
| Short-Circuit Current | | | 18 | | | 18 | | mA |
| POWER SUPPLY | | | | | | | | |
| Operating Range | $V_S$ = ±2.3 V to ±18 V | ±2.3 | | ±18 | ±2.3 | | ±18 | V |
| Quiescent Current | | | 0.85 | 1 | | 0.85 | 1 | mA |
| Over Temperature | T = −40°C to +85°C | | 1 | 1.2 | | 1 | 1.2 | mA |
| TEMPERATURE RANGE | | | | | | | | |
| Specified Performance | | −40 | | +85 | −40 | | +85 | °C |
| Operating Range[2] | | −40 | | +125 | −40 | | +125 | °C |

[1] Operating near the input voltage range limit may reduce the available output range. See Figure 12 and Figure 13 for the input common-mode range vs. output voltage.
[2] See the Typical Performance Characteristics section for expected operation between 85°C to 125°C.

# ABSOLUTE MAXIMUM RATINGS

**Table 4.**

| Parameter | Rating |
|---|---|
| Supply Voltage | ±18 V |
| Output Short-Circuit Current | Indefinite |
| Input Voltage (Common Mode) | $\pm V_S$ |
| Differential Input Voltage | $\pm V_S$ |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range[1] | −40°C to +125°C |
| Maximum Junction Temperature | 140°C |
| ESD | |
| Human Body Model | 2 kV |
| Charge Device Model | 1 kV |

[1] Temperature range for specified performance is −40°C to +85°C. See the Typical Performance Characteristics section for expected operation from 85°C to 125°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for a device in free air.

**Table 5.**

| Package | $\theta_{JA}$ | Unit |
|---|---|---|
| 8-Lead MSOP, 4-Layer JEDEC Board | 135 | °C/W |
| 8-Lead SOIC, 4-Layer JEDEC Board | 121 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

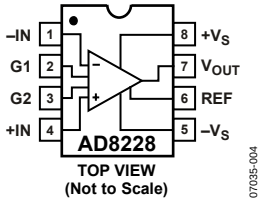



*Figure 2. Pin Configuration*

**Table 6. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | −IN | Negative Input. |
| 2, 3 | G1, G2 | Gain Pins. Short together for a gain of 100. Leave unconnected for a gain of 10. |
| 4 | +IN | Positive Input. |
| 5 | $-V_S$ | Negative Supply. |
| 6 | REF | Reference. |
| 7 | $V_{OUT}$ | Output. |
| 8 | $+V_S$ | Positive Supply. |

# TYPICAL PERFORMANCE CHARACTERISTICS

T = 25°C, $V_S$ = ±15 V, $R_L$ = 10 kΩ, unless otherwise noted.

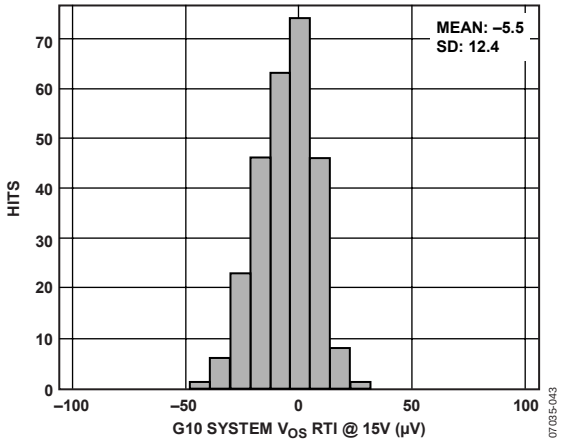



Figure 3. Typical Distribution of Input Offset Voltage (G = 10)

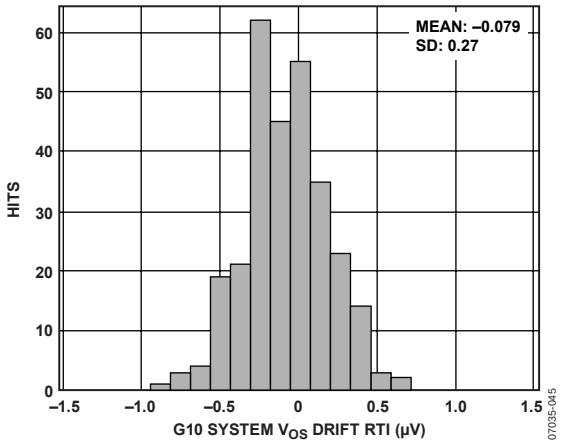



Figure 4. Typical Distribution of Input Offset Voltage Drift (G = 10)

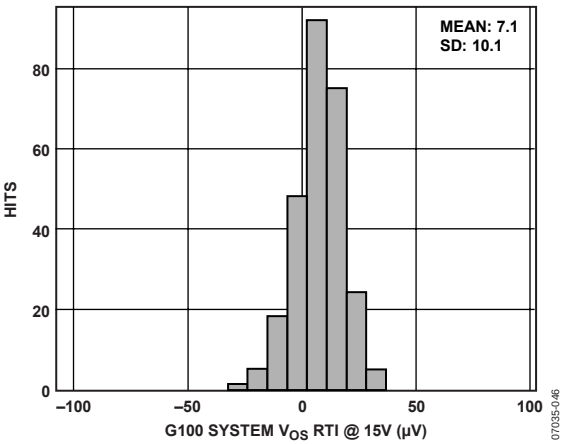



Figure 5. Typical Distribution of Input Offset Voltage (G = 100)

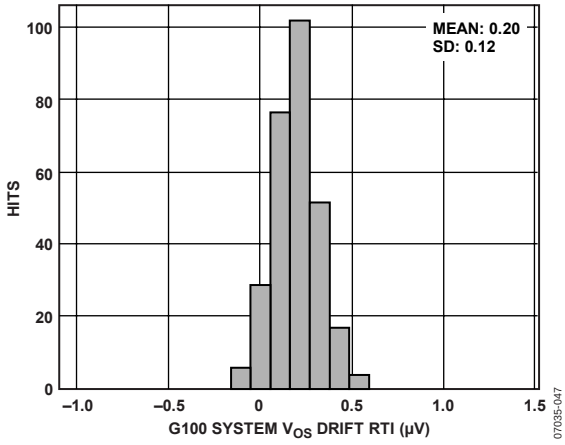



Figure 6. Typical Distribution of Input Offset Voltage Drift (G = 100)

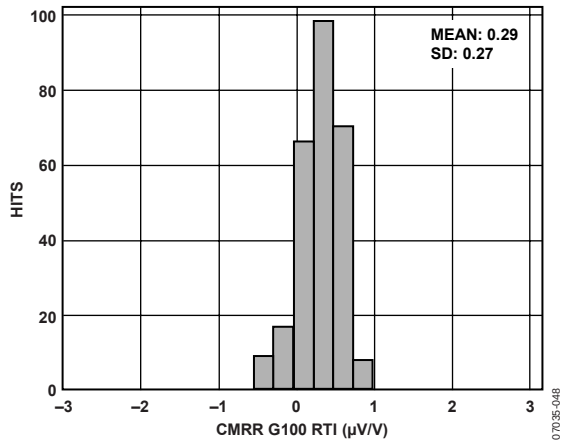



Figure 7. Typical Distribution for CMR (G = 100)

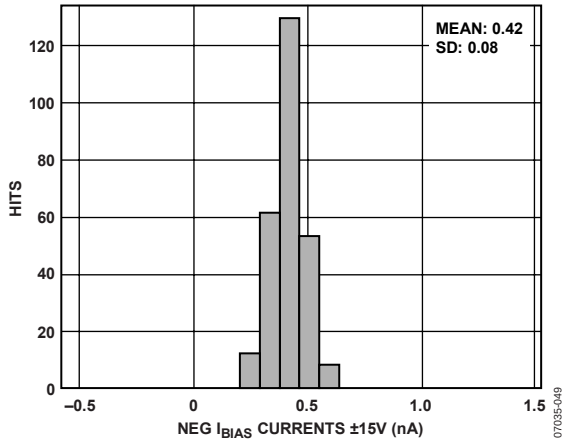



Figure 8. Typical Distribution of Input Bias Current

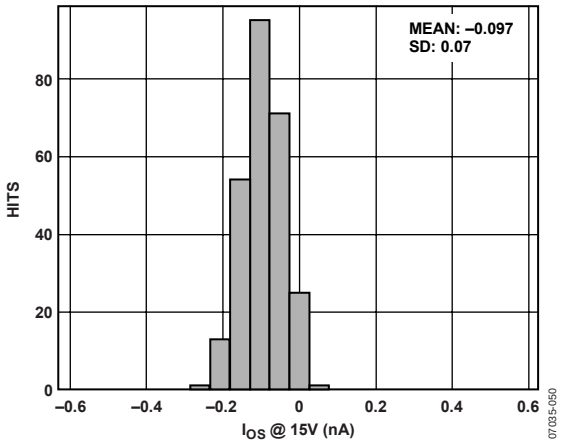



*Figure 9. Typical Distribution of Input Offset Current*

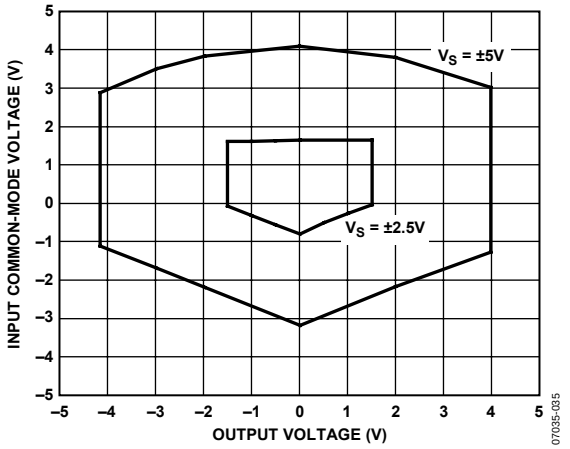



*Figure 12. Input Common-Mode Voltage vs. Output Voltage, $V_S$ = ±2.5 V, ±5 V; G = 100*

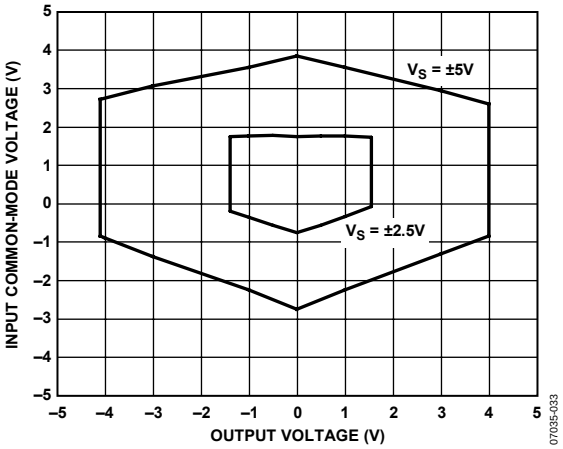



*Figure 10. Input Common-Mode Voltage vs. Output Voltage, $V_S$ = ±2.5 V, ±5 V; G =10*

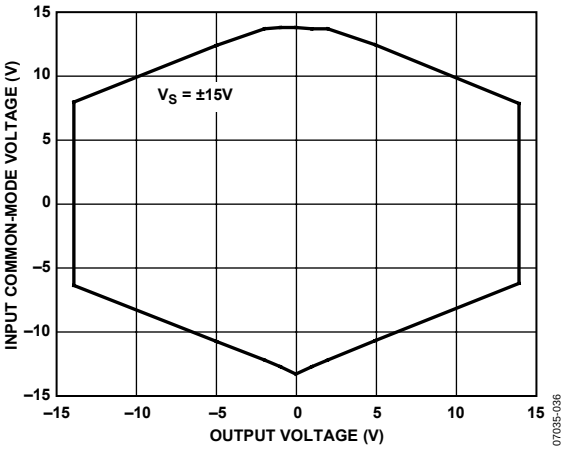



*Figure 13. Input Common-Mode Voltage vs. Output Voltage, $V_S$ = ±15 V, G = 100*

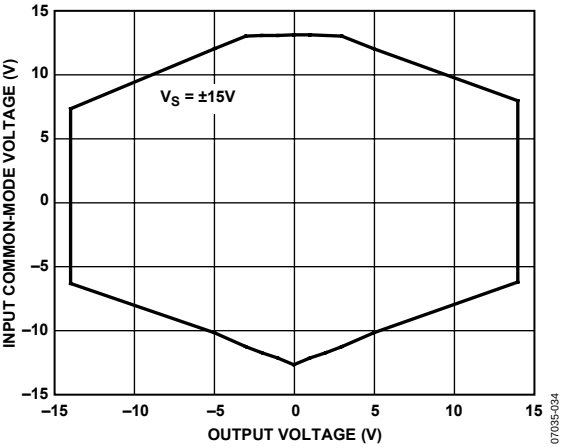



*Figure 11. Input Common-Mode Voltage vs. Output Voltage, $V_S$ = ±15 V, G = 10*

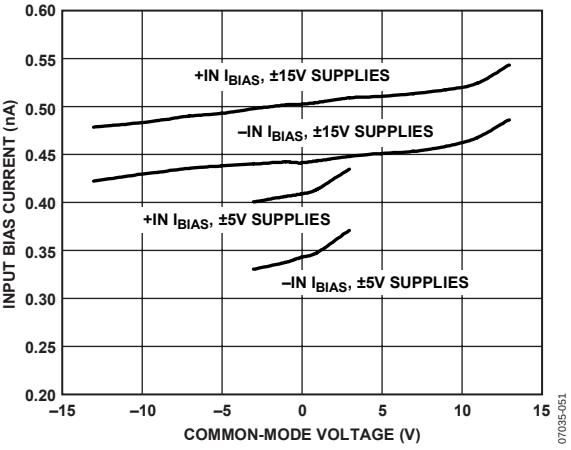



*Figure 14. Input Bias Current vs. Common-Mode Voltage*

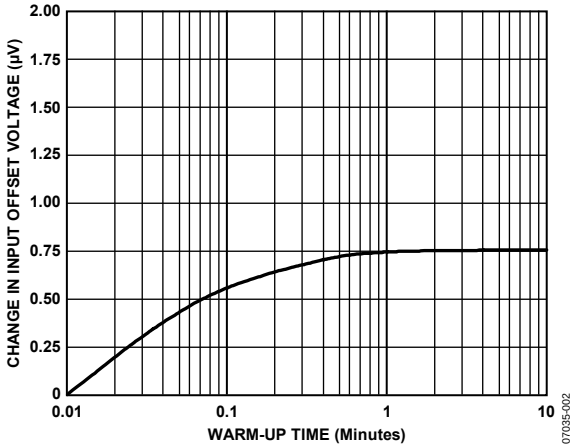



Figure 15. Change in Input Offset Voltage vs. Warm-Up Time

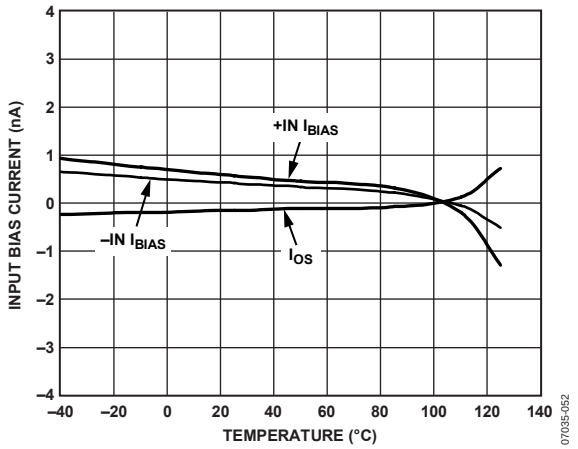



Figure 16. Input Bias Current and Offset Current vs. Temperature

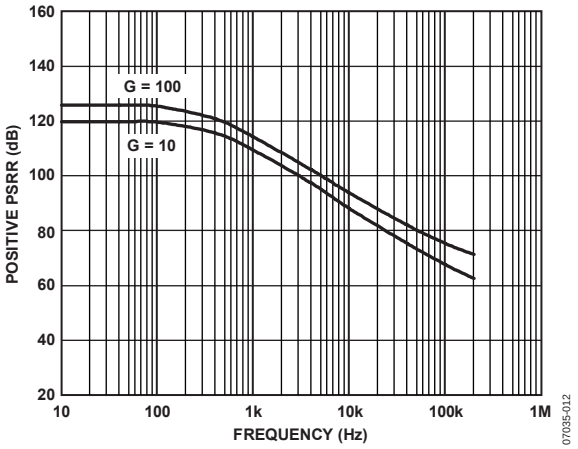



Figure 17. Positive PSRR vs. Frequency, RTI

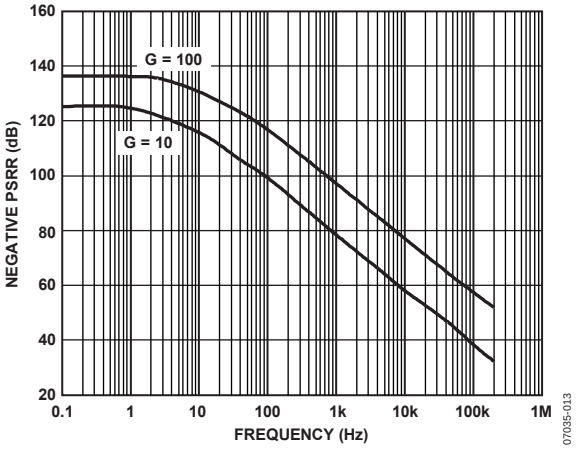



Figure 18. Negative PSRR vs. Frequency

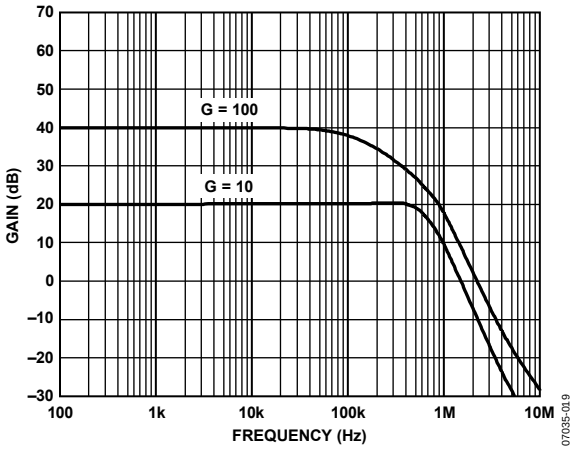



Figure 19. Gain vs. Frequency

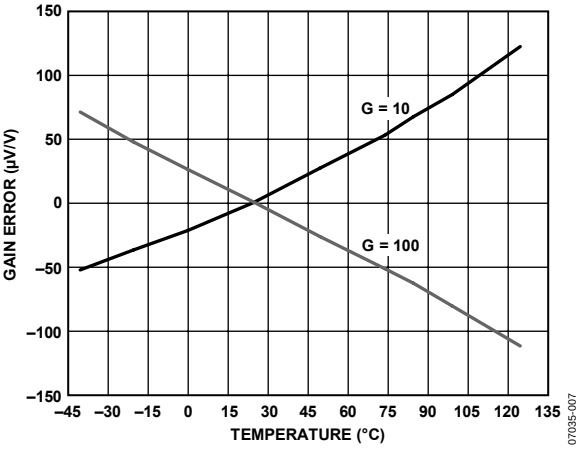



Figure 20. Gain Error vs. Temperature

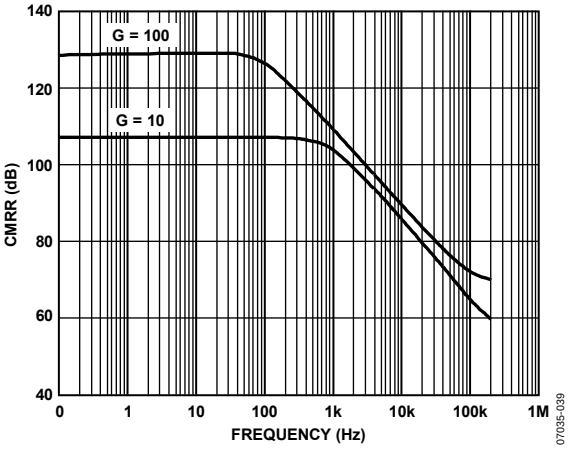



Figure 21. CMRR vs. Frequency, RTI

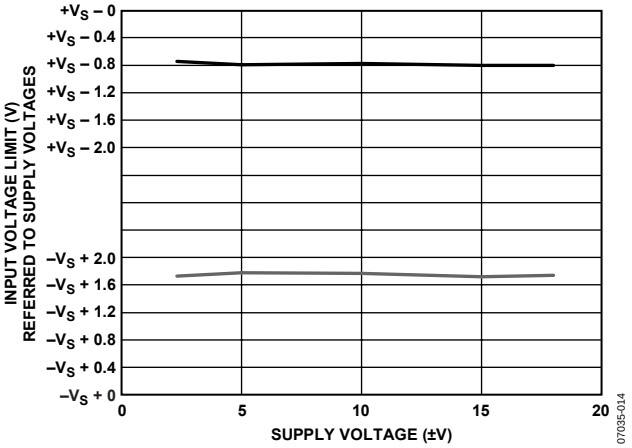



Figure 24. Input Voltage Limit vs. Supply Voltage

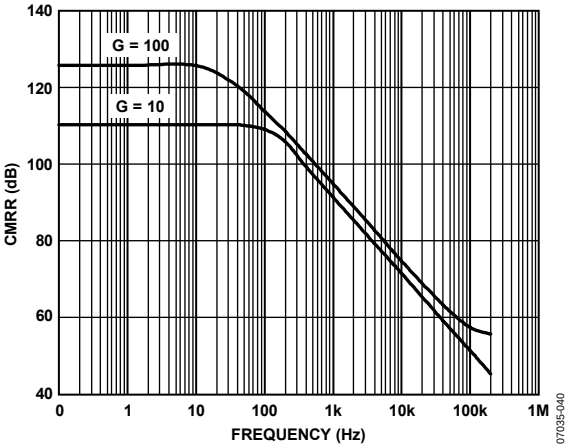



Figure 22. CMRR vs. Frequency, RTI, 1 kΩ Source Imbalance

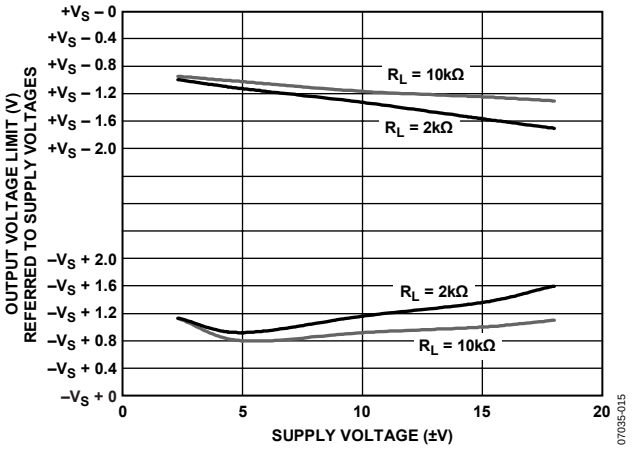



Figure 25. Output Voltage Swing vs. Supply Voltage

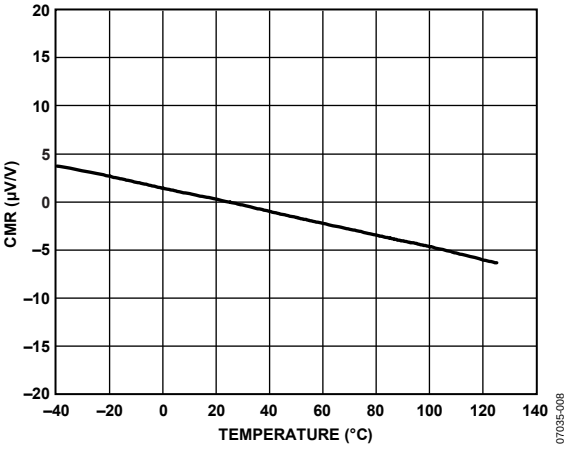



Figure 23. CMR vs. Temperature

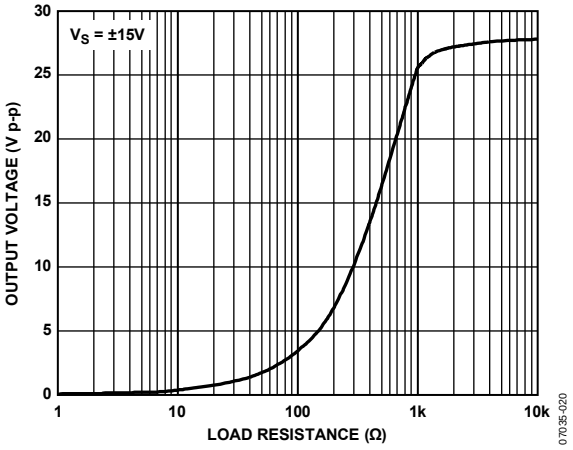



Figure 26. Output Voltage Swing vs. Load Resistance

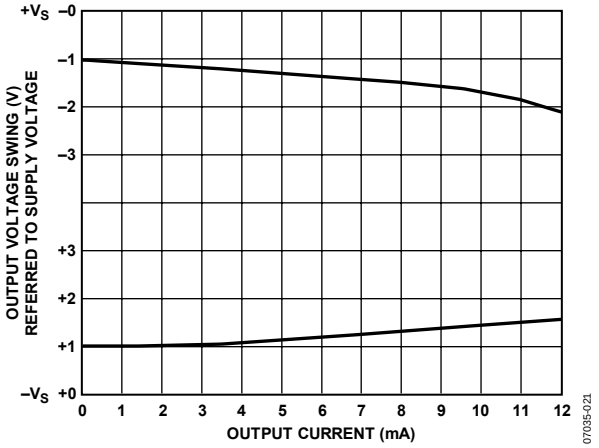



Figure 27. Output Voltage Swing vs. Output Current, G = 1

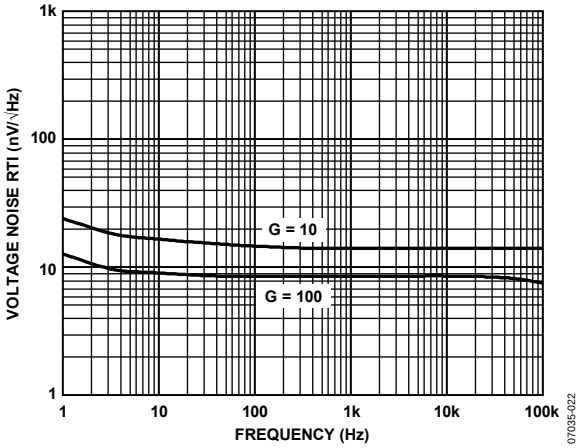



Figure 30. Voltage Noise Spectral Density vs. Frequency

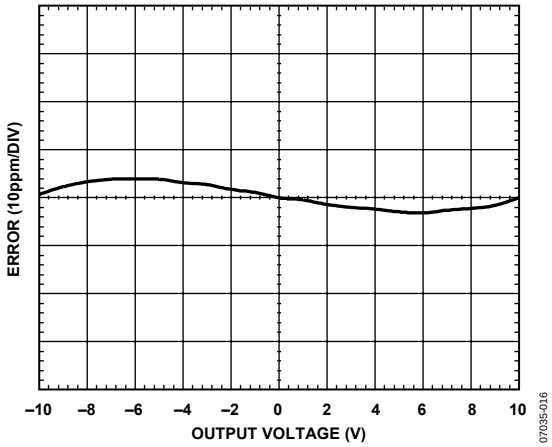



Figure 28. Gain Nonlinearity, G = 10, $R_L$ = 10 kΩ

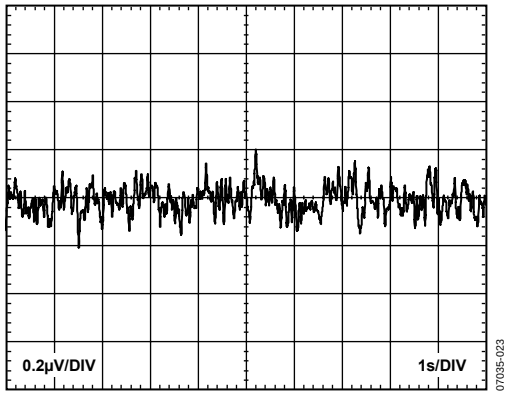



Figure 31. 0.1 Hz to 10 Hz RTI Voltage Noise, G=10

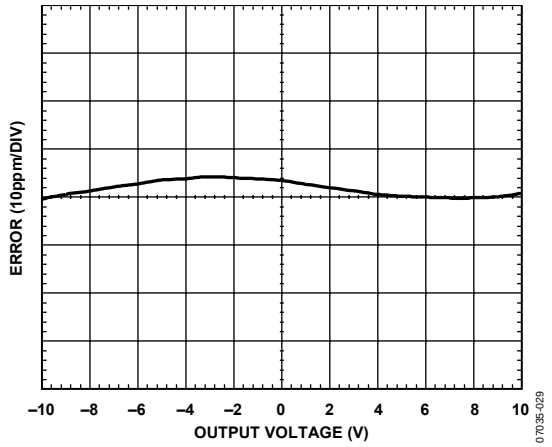



Figure 29. Gain Nonlinearity, G = 100, $R_L$ = 10 kΩ

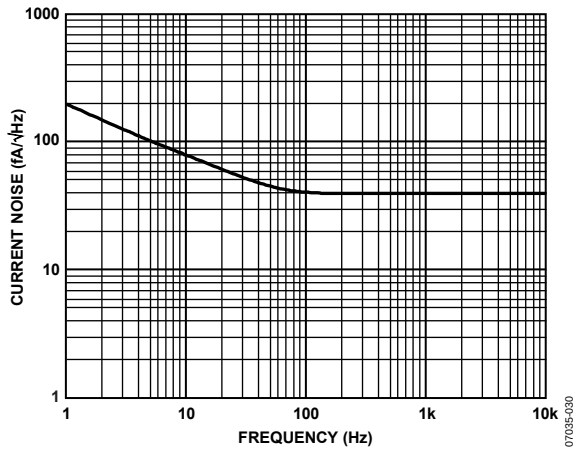



Figure 32. Current Noise Spectral Density vs. Frequency

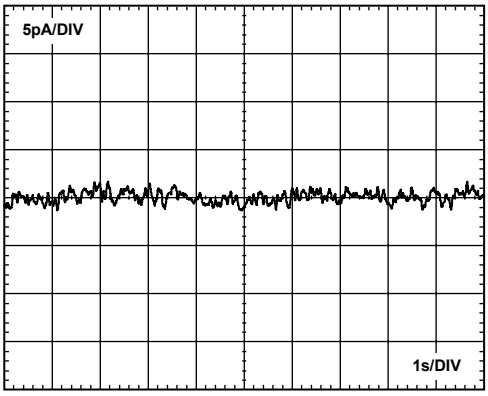



Figure 33. 0.1 Hz to 10 Hz Current Noise

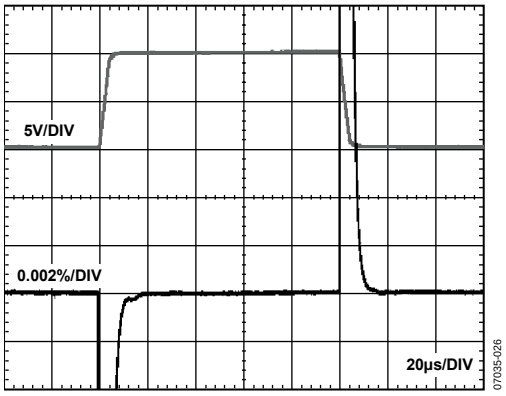



Figure 36. Large Signal Pulse Response and Settling Time (G = 100)

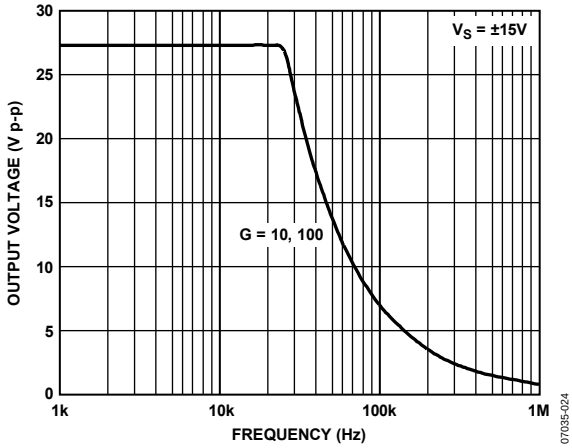



Figure 34. Large Signal Frequency Response

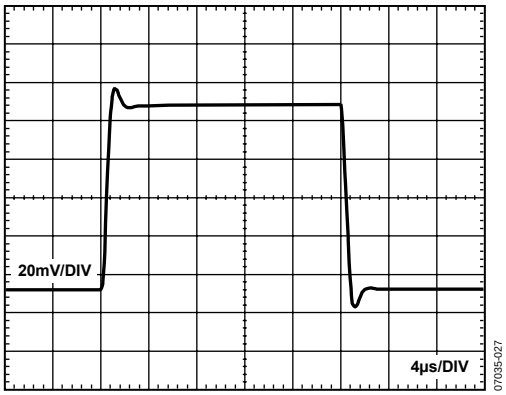



Figure 37. Small Signal Response, G = 10, $R_L$ = 2 kΩ, $C_L$ = 100 pF

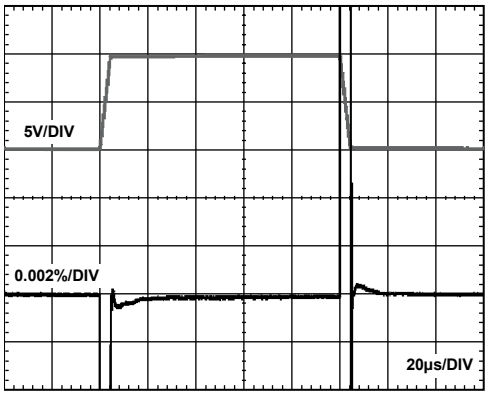



Figure 35. Large Signal Pulse Response and Settling Time (G = 10)

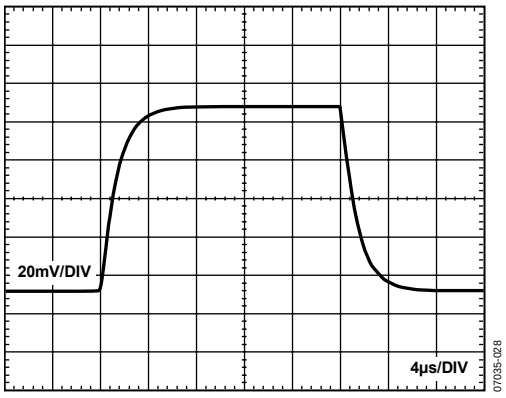



Figure 38. Small Signal Response, G = 100, $R_L$ = 2 kΩ, $C_L$ = 100 pF

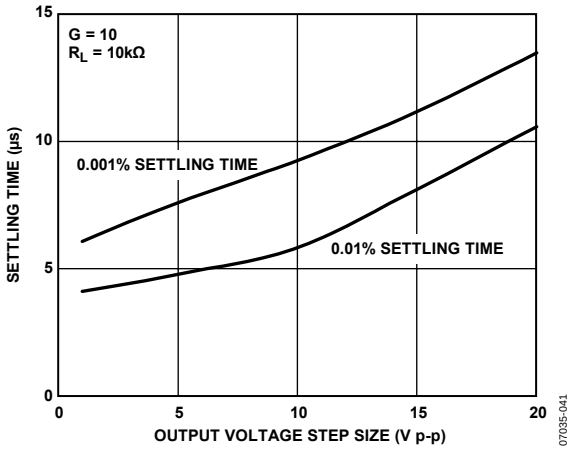



*Figure 39. Settling Time vs. Step Size, G = 10*

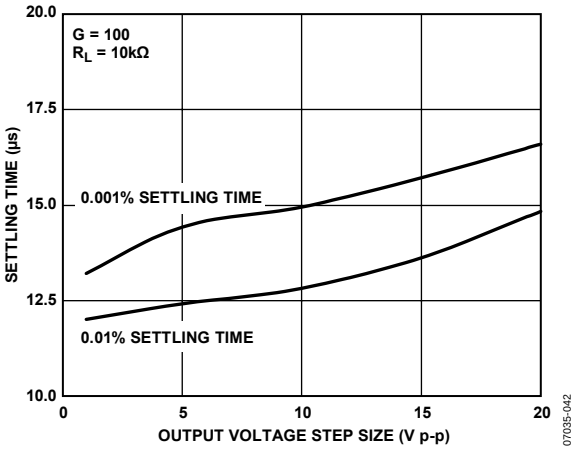



*Figure 40. Settling Time vs. Step Size, G = 100*

# THEORY OF OPERATION

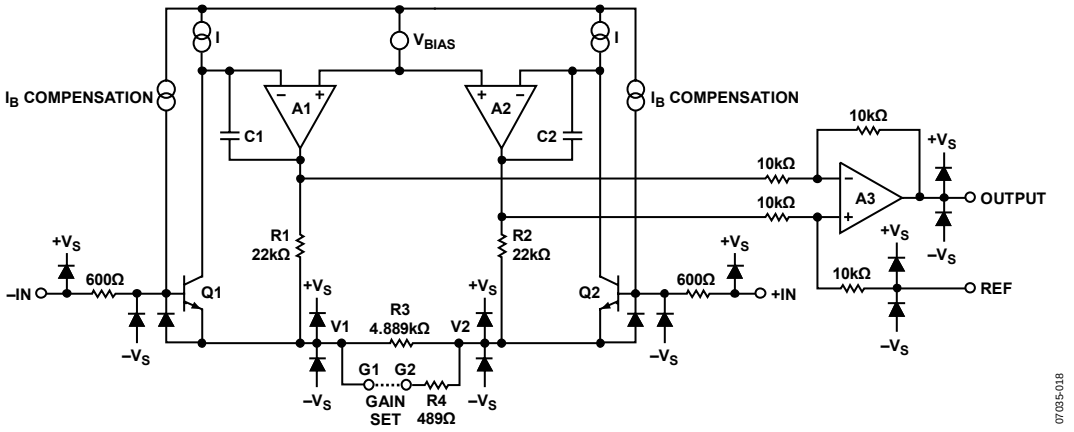



*Figure 41. Simplified Schematic*

## ARCHITECTURE

The AD8228 is based on the classic three op amp topology. This topology has two stages: a preamplifier to provide differential amplification, followed by a difference amplifier to remove the common-mode voltage. Figure 41 shows a simplified schematic of the AD8228.

The first stage is composed of the A1 and A2 amplifiers, the Q1 and Q2 input transistors, and the R1 through R4 resistors. The feedback loop of A1, R1, and Q1 ensures that the V1 voltage is a constant diode drop below in the negative input voltage. Similarly, V2 is kept a constant diode drop below the positive input. Therefore, a replica of the differential input voltage is placed across either R3 (when the gain pins are left open) or R3||R4 (when the gain pins are shorted). The current that flows across this resistance must also flow through the R1 and R2 resistors, creating a gained differential signal between the A2 and A1 outputs. Note that, in addition to a gained differential signal, the original common-mode signal, shifted a diode drop down, is also still present.

The second stage is a difference amplifier, composed of A3 and four 10 kΩ resistors. The purpose of this stage is to remove the common-mode signal from the amplified differential signal.

The AD8228 does not depend on external resistors. Much of the dc performance of precision circuits depends on the accuracy and matching of resistors. The resistors on the AD8228 are laid out to be tightly matched. The resistors of each part are laser trimmed and tested for their matching accuracy. Because of this trimming and testing, the AD8228 can guarantee high accuracy for specifications such as gain drift, common-mode rejection (CMRR), and gain error.

## SETTING THE GAIN

The AD8228 can be configured for a gain of 10 or 100 with no external components. Leave Pin 2 and Pin 3 open for a gain of 10; short Pin 2 and Pin 3 together for a gain of 100 (see Figure 42).

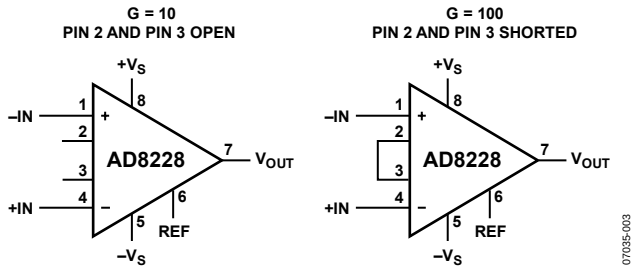



*Figure 42. Setting the Gain*

The transfer function with Pin 2 and Pin 3 open is

$$V_{OUT} = 10 \times (V_{IN+} - V_{IN-}) + V_{REF}$$

The transfer function with Pin 2 and Pin 3 shorted is

$$V_{OUT} = 100 \times (V_{IN+} - V_{IN-}) + V_{REF}$$

## COMMON-MODE INPUT VOLTAGE RANGE

The three op amp architecture of the AD8228 applies gain and then removes the common-mode voltage. Therefore, internal nodes in the AD8228 experience a combination of both the gained signal and the common-mode signal. This combined signal can be limited by the voltage supplies even when the individual input and output signals are not. Figure 10 through Figure 13 show the allowable common-mode input voltage ranges for various output voltages and supply voltages.

## REFERENCE TERMINAL

The output voltage of the AD8228 is developed with respect to the potential on the reference terminal. This is useful when the output signal needs to be offset to a precise midsupply level. For example, a voltage source can be tied to the REF pin to level-shift the output so that the AD8228 can drive a single-supply ADC. The REF pin is protected with ESD diodes and should not exceed either $+V_S$ or $-V_S$ by more than 0.3 V.

For best performance, source impedance to the REF terminal should be kept below 1 Ω. As shown in Figure 41, the reference terminal, REF, is at one end of a 10 kΩ resistor. Additional impedance at the REF terminal adds to this 10 kΩ resistor and results in amplification of the signal connected to the positive input. The amplification from the additional $R_{REF}$ can be computed by

$$\frac{2 \times \left(10\ \text{k}\Omega + R_{REF}\right)}{20\ \text{k}\Omega + R_{REF}}$$

Only the positive signal path is amplified; the negative path is unaffected. This uneven amplification degrades the CMRR of the amplifier.

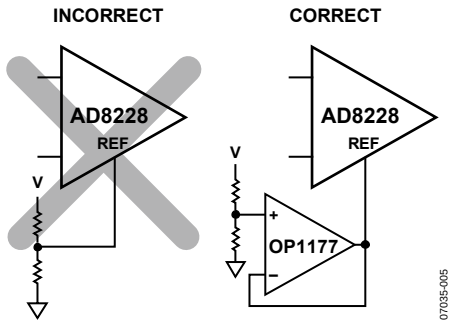



*Figure 43. Driving the Reference*

## LAYOUT

The AD8228 is a high precision device. To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. The AD8228 pins are arranged in a logical manner to aid in this task.

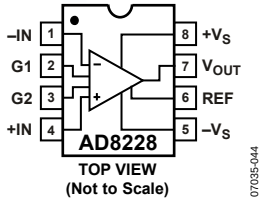



*Figure 44. Pinout Diagram*

### *Common-Mode Rejection Ratio over Frequency*

The AD8228 has a higher CMRR over frequency than typical in-amps, which gives it greater immunity to disturbances such as line noise and its associated harmonics. The AD8228 pinout was designed so that the board designer can take full advantage of this performance with a well-implemented layout.

Poor layout can cause some of the common-mode signal to be converted to a differential signal before it reaches the in-amp. Such conversions occur when one input path has a frequency response that is different from the other. To keep CMRR across frequency high, input source impedance and capacitance of each path should be closely matched. Additional source resistance in the input path (for example, for input protection) should be placed close to the in-amp inputs, which minimizes their interaction with parasitic capacitance from the PCB traces.

Parasitic capacitance at the gain setting pins can also affect CMRR over frequency. If the board design has a component at the gain setting pins (for example, a switch or jumper), the part should be chosen so that the parasitic capacitance is as small as possible.

### *Power Supplies*

A stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. See the PSRR performance curves in Figure 17 and Figure 18 for more information.

A 0.1 µF capacitor should be placed as close as possible to each supply pin. As shown in Figure 45, a 10 µF tantalum capacitor can be used farther away from the part. In most cases, it can be shared by other precision integrated circuits.

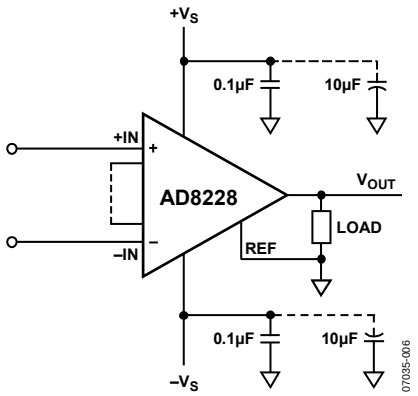



*Figure 45. Supply Decoupling, REF, and Output Referred to Local Ground*

### *References*

The output voltage of the AD8228 is developed with respect to the potential on the reference terminal. Care should be taken to tie REF to the appropriate local ground.

### *Input Bias Current Return Path*

The input bias current of the AD8228 must have a return path to common. When the source, such as a thermocouple, cannot provide a return current path, one should be created, as shown in Figure 46.

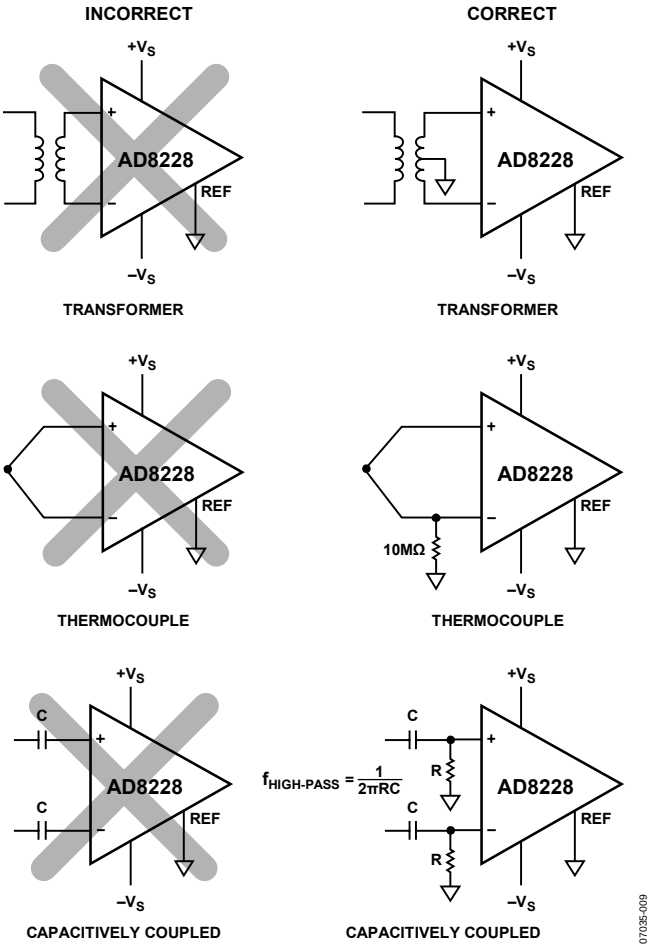



*Figure 46. Creating an $I_{BIAS}$ Path*

## INPUT PROTECTION

All terminals of the AD8228 are protected against ESD (1 kV, human body model). In addition, the input structure allows for dc overload conditions of about 3.5 V beyond the supplies.

### *Input Voltages Beyond the Rails*

For larger input voltages, an external resistor should be used in series with each input to limit current during overload conditions. The AD8228 can safely handle a continuous 6 mA current. The limiting resistor can be computed from

$$R_{LIMIT} \geq \frac{V_{IN} - V_{SUPPLY}}{6\text{ mA}} - 600\ \Omega$$

For applications where the AD8228 encounters extreme overload voltages, such as cardiac defibrillators, external series resistors and low leakage diode clamps such as the BAV199L, the FJH1100s, or the SP720 should be used.

### *Large Differential Voltages When G = 100*

When operating at a gain of 100, large differential input voltages can cause more than 6 mA of current to flow into the inputs. This condition occurs when the voltage between +IN and –IN exceeds 5 V. This is true for differential voltages of either polarity.

The maximum allowed differential voltage can be increased by adding an input protection resistor in series with each input. The value of each protection resistor should be

$$R_{PROTECT} = (V_{DIFF_MAX} - 5\text{ V})/6\text{ mA}$$

## RADIO FREQUENCY INTERFERENCE (RFI)

RF rectification is often a problem when amplifiers are used in applications having strong RF signals. The disturbance can appear as a small dc offset voltage. High frequency signals can be filtered with a low-pass RC network placed at the input of the instrumentation amplifier, as shown in Figure 47. The filter limits the input signal bandwidth, according to the following relationship:

$$FilterFrequency_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFrequency_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10\ C_C$.

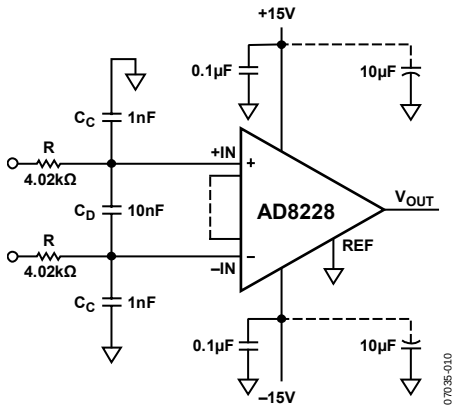



*Figure 47. RFI Suppression*

$C_D$ affects the difference signal, and $C_C$ affects the common-mode signal. Values of R and $C_C$ should be chosen to minimize RFI. Mismatch between the R × $C_C$ at the positive input and the R × $C_C$ at the negative input degrades the CMRR of the AD8228. By using a value of $C_D$ one magnitude larger than $C_C$, the effect of the mismatch is reduced, and performance is improved.

# APPLICATIONS INFORMATION

## DIFFERENTIAL DRIVE

Figure 48 shows how to configure the AD8228 for differential output. The advantage of this circuit is that the dc differential accuracy depends on the AD8228 and not on the op amp or the resistors. This circuit takes advantage of the precise control the AD8228 has of its output voltage relative to the reference voltage. The ideal equation for the differential output is as follows:

$$V_{DIFF_OUT} = V_{OUT+} - V_{OUT-} = Gain \times (V_{IN+} - V_{IN-})$$

Op amp dc performance and resistor matching determine the dc common-mode output accuracy. However, because common-mode errors are likely to be rejected by the next device in the signal chain, these errors typically have little effect on overall system accuracy. The ideal equation for the common-mode output is as follows:

$$V_{CM_OUT} = \frac{V_{OUT+} + V_{OUT-}}{2} = V_{REF}$$

For best ac performance, an op amp with at least 3 MHz gain bandwidth product and 2 V/µs slew rate is recommended.

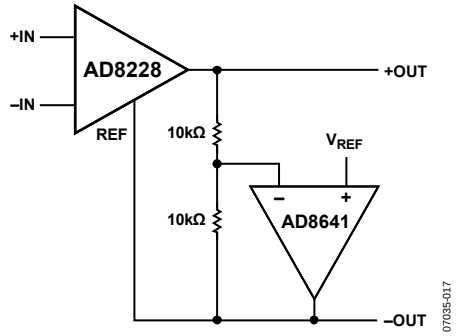



*Figure 48. Differential Output Using an Op Amp*

## PRECISION STRAIN GAGE

The low offset and high CMRR over frequency of the AD8228 make it an excellent candidate for bridge measurements. As shown in Figure 49, the bridge can be connected directly to the inputs of the amplifier.

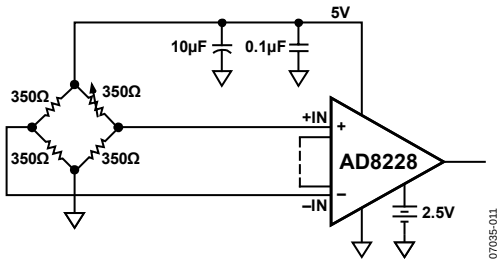



*Figure 49. Precision Strain Gage*

## DRIVING A DIFFERENTIAL ADC

Figure 50 shows how the AD8228 can be used to drive a differential ADC. The AD8228 is configured with an op amp and two resistors for differential drive. The 510 Ω resistors and 2200 pF capacitors isolate the instrumentation amplifier from the switching transients produced by the switched capacitor front end of a typical SAR converter. These components between the ADC and the amplifier also create a filter at 142 kHz, which provides antialiasing and noise filtering. The advantage of this configuration is that it uses less power than a dedicated ADC driver: the AD8641 typically consumes 200 µA, and the current through the two 10 kΩ resistors is 250 µA at full output voltage.

With the AD7688, this configuration gives excellent dc performance and a THD of 71 dB (10 kHz input). For applications that need better distortion performance, a dedicated ADC driver, such as the ADA4941-1 or ADA4922-1, is recommended.

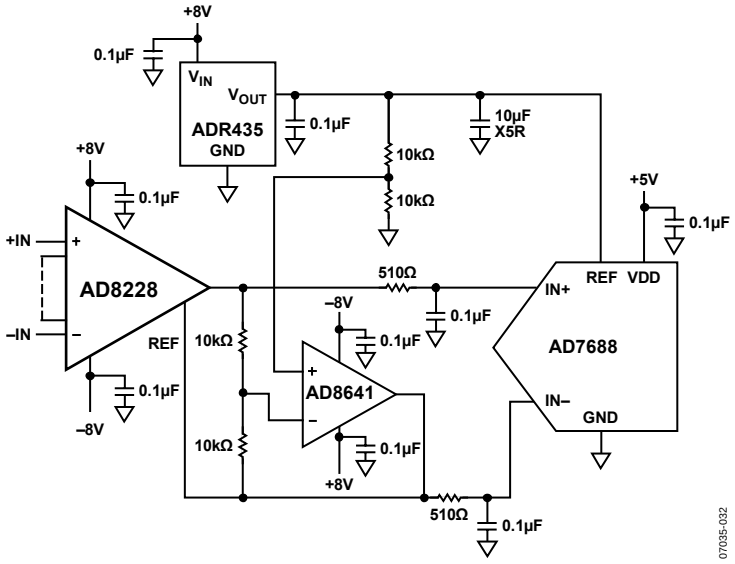
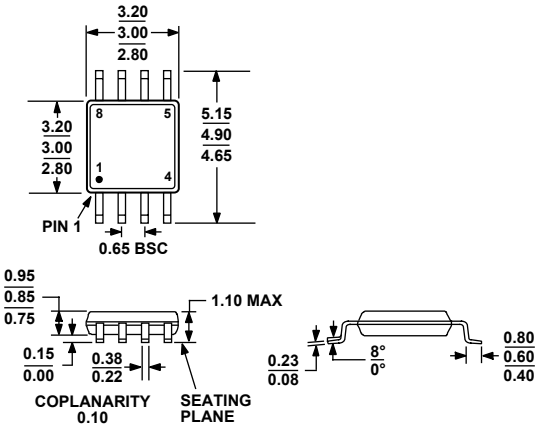


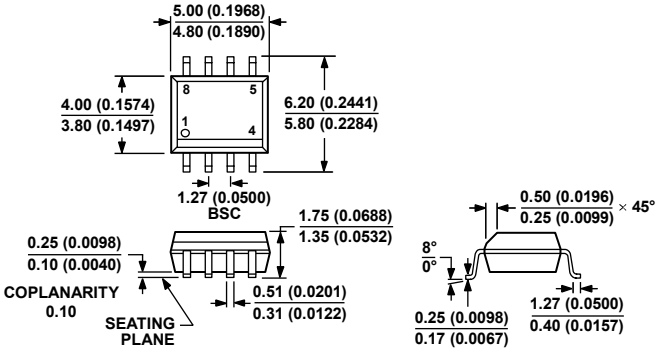

*Figure 50. Driving a Differential ADC*

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-187-AA

*Figure 51. 8-Lead Mini Small Outline Package [MSOP]*
*(RM-8)*
*Dimensions shown in millimeters*




COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

*Figure 52. 8-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body*
*(R-8)*
*Dimensions shown in millimeters and (inches)*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | PackageOption | Branding |
|---|---|---|---|---|
| AD8228ARMZ[1] | –40°C to +85°C | 8-Lead MSOP | RM-8 | Y16 |
| AD8228ARMZ-RL[1] | –40°C to +85°C | 8-Lead MSOP, 13" Tape and Reel | RM-8 | Y16 |
| AD8228ARMZ-R7[1] | –40°C to +85°C | 8-Lead MSOP, 7" Tape and Reel | RM-8 | Y16 |
| AD8228ARZ[1] | –40°C to +85°C | 8-Lead SOIC_N | R-8 | |
| AD8228ARZ-RL[1] | –40°C to +85°C | 8-Lead SOIC_N, 13" Tape and Reel | R-8 | |
| AD8228ARZ-R7[1] | –40°C to +85°C | 8-Lead SOIC_N, 7" Tape and Reel | R-8 | |
| AD8228BRMZ[1] | –40°C to +85°C | 8-Lead MSOP | RM-8 | Y1M |
| AD8228BRMZ-RL[1] | –40°C to +85°C | 8-Lead MSOP, 13" Tape and Reel | RM-8 | Y1M |
| AD8228BRMZ-R7[1] | –40°C to +85°C | 8-Lead MSOP, 7" Tape and Reel | RM-8 | Y1M |
| AD8228BRZ[1] | –40°C to +85°C | 8-Lead SOIC_N | R-8 | |
| AD8228BRZ-RL[1] | –40°C to +85°C | 8-Lead SOIC_N, 13" Tape and Reel | R-8 | |
| AD8228ARZ-R7[1] | –40°C to +85°C | 8-Lead SOIC_N, 7" Tape and Reel | R-8 | |

[1] Z = RoHS Compliant Part.

## NOTES

## NOTES

## NOTES

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Click below to explore more details on WIN SOURCE:

- View AD8228BRMZ-R7 on WIN SOURCE
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- Alternative Solution
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