



**THE DATASHEET OF  
LM9036QMM-3.3/NOPB**



## LM9036Q Ultra-Low Quiescent Current Voltage Regulator

 Check for Samples: [LM9036Q](#)

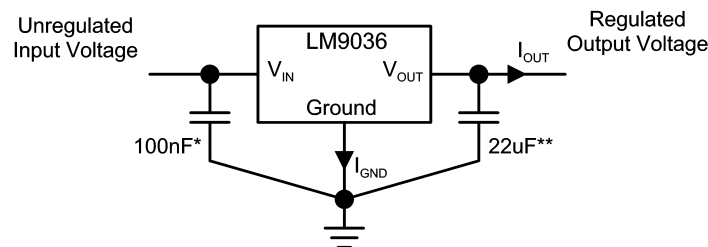
### FEATURES

- AEC-Q100 Grade 1 Qualified (-40°C to 125°C)
- Ultra Low Ground Pin Current ( $I_{GND} \leq 25\mu A$  for  $I_{OUT} = 0.1mA$ )
- Fixed 5V, 3.3V, 50mA Output
- Output Tolerance  $\pm 5\%$  Over Line, Load, and Temperature
- Dropout Voltage Typically 200mV @  $I_{OUT} = 50mA$
- -45V Reverse Transient Protection
- Internal Short Circuit Current Limit
- Internal Thermal Shutdown Protection
- 40V Operating Voltage Limit

### DESCRIPTION

The LM9036Q ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than 25 $\mu A$  Ground Pin current at a 0.1mA load, the LM9036Q is ideally suited for automotive and other battery operated systems. The LM9036Q retains all of the features that are common to low dropout regulators including a low dropout PNP pass device, short circuit protection, reverse battery protection, and thermal shutdown. The LM9036Q has a 40V maximum operating voltage limit, a -40°C to +125°C operating temperature range, and  $\pm 5\%$  output voltage tolerance over the entire output current, input voltage, and temperature range.

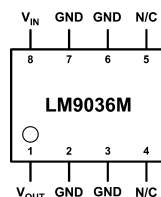
### Typical Application



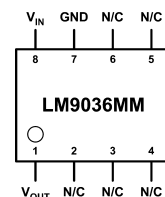
\* Required if regulator is located more than 2" from power supply filter capacitor.

\*\* Required for stability. Must be rated over intended operating temperature range. Effective series resistance (ESR) is critical, see Electrical Characteristics. Locate capacitor as close as possible to the regulator output and ground pins. Capacitance may be increased without bound.

### Connection Diagram



**Figure 1. See Package Number D0008A  
Top View**



**Figure 2. See Package Number DGK0008A  
Top View**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



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### Absolute Maximum Ratings <sup>(1)(2)</sup>

Input Voltage (Survival)	+55V, -45V
ESD Susceptibility <sup>(3)</sup>	±1.9kV
Power Dissipation <sup>(4)</sup>	Internally limited
Junction Temperature ( $T_{Jmax}$ )	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human body model, 100pF discharge through a 1.5kΩ resistor.
- (4) The maximum power dissipation is a function of  $T_{Jmax}$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{Jmax} - T_A)/\theta_{JA}$ . If this dissipation is exceeded, the die temperature will rise above 150°C and the LM9036Q will go into thermal shutdown.

### Operating Ratings

Operating Temperature Range	-40°C to +125°C
Maximum Input Voltage (Operational)	40V
SOIC-8 (D0008A) $\theta_{JA}$ <sup>(1)(2)</sup>	140°C/W
SOIC-8 (D0008A) $\theta_{JC}$	45°C/W
VSSOP-8 (DGK0008A) $\theta_{JA}$ <sup>(1)</sup>	200°C/W

- (1) Typical  $\theta_{JA}$  with 1 square inch of 2 oz. copper pad area directly under the ground tab.
- (2) Worst case (Free Air) per EIA / JESD51-3.

### Electrical Characteristics - LM9036Q-5.0

$V_{IN} = 14V$ ,  $I_{OUT} = 10\text{ mA}$ ,  $T_J = 25^\circ\text{C}$ , unless otherwise specified. **Boldface** limits apply over entire operating temperature range

Parameter	Conditions	Min <sup>(1)</sup>	Typical <sup>(2)</sup>	Max <sup>(1)</sup>	Units
Output Voltage ( $V_{OUT}$ )		4.80	5.00	5.20	V
	$5.5V \leq V_{IN} \leq 26V$ , $0.1mA \leq I_{OUT} \leq 50mA$ <sup>(3)</sup>	<b>4.75</b>	<b>5.00</b>	<b>5.25</b>	
Quiescent Current ( $I_{GND}$ )	$I_{OUT} = 0.1mA$ , $8V \leq V_{IN} \leq 24V$		20	25	$\mu\text{A}$
	$I_{OUT} = 1mA$ , $8V \leq V_{IN} \leq 24V$		50	100	
	$I_{OUT} = 10mA$ , $8V \leq V_{IN} \leq 24V$		0.3	0.5	$\text{mA}$
	$I_{OUT} = 50mA$ , $8V \leq V_{IN} \leq 24V$		2.0	2.5	
Line Regulation ( $\Delta V_{OUT}$ )	$6V \leq V_{IN} \leq 40V$ , $I_{OUT} = 1mA$		10	30	mV
Load Regulation ( $\Delta V_{OUT}$ )	$0.1mA \leq I_{OUT} \leq 5mA$		10	30	mV
	$5mA \leq I_{OUT} \leq 50mA$		10	30	mV
Dropout Voltage ( $\Delta V_{OUT}$ )	$I_{OUT} = 0.1mA$		0.05	0.10	V
	$I_{OUT} = 50mA$		0.20	0.40	V
Short Circuit Current ( $I_{SC}$ )	$V_{OUT} = 0V$	65	120	250	$\text{mA}$
Ripple Rejection (PSRR)	$V_{ripple} = 1V_{rms}$ , $F_{ripple} = 120\text{Hz}$	-40	-60		dB
Output Bypass Capacitance ( $C_{OUT}$ )	$0.3\Omega \leq ESR \leq 8\Omega$ $0.1mA \leq I_{OUT} \leq 50mA$	10	22		$\mu\text{F}$

- (1) Tested limits are specified to AOQL (Average Outgoing Quality Level) and 100% tested.
- (2) Typicals are at 25°C (unless otherwise specified) and represent the most likely parametric norm.
- (3) To ensure constant junction temperature, pulse testing is used.

### Electrical Characteristics - LM9036Q-3.3

$V_{IN} = 14V$ ,  $I_{OUT} = 10\text{ mA}$ ,  $T_J = 25^\circ\text{C}$ , unless otherwise specified. **Boldface** limits apply over entire operating temperature range

Parameter	Conditions	Min (1)	Typical (2)	Max (1)	Units
Output Voltage ( $V_{OUT}$ )		3.168	3.30	3.432	V
	$5.5V \leq V_{IN} \leq 26V$ , $0.1\text{mA} \leq I_{OUT} \leq 50\text{mA}$ (3)	<b>3.135</b>	<b>3.30</b>	<b>3.465</b>	
Quiescent Current ( $I_{GND}$ )	$I_{OUT} = 0.1\text{mA}$ , $8V \leq V_{IN} \leq 24V$		20	25	$\mu\text{A}$
	$I_{OUT} = 1\text{mA}$ , $8V \leq V_{IN} \leq 24V$		50	100	
	$I_{OUT} = 10\text{mA}$ , $8V \leq V_{IN} \leq 24V$		0.3	0.5	mA
	$I_{OUT} = 50\text{mA}$ , $8V \leq V_{IN} \leq 24V$		2.0	2.5	
Line Regulation ( $\Delta V_{OUT}$ )	$6V \leq V_{IN} \leq 40V$ , $I_{OUT} = 1\text{mA}$		10	30	mV
Load Regulation ( $\Delta V_{OUT}$ )	$0.1\text{mA} \leq I_{OUT} \leq 5\text{mA}$		10	30	mV
	$5\text{mA} \leq I_{OUT} \leq 50\text{mA}$		10	30	mV
Dropout Voltage ( $\Delta V_{OUT}$ )	$I_{OUT} = 0.1\text{mA}$		0.05	0.10	V
	$I_{OUT} = 50\text{mA}$		0.20	0.40	V
Short Circuit Current ( $I_{SC}$ )	$V_{OUT} = 0V$	65	120	250	mA
Ripple Rejection (PSRR)	$V_{\text{ripple}} = 1V_{\text{rms}}$ , $F_{\text{ripple}} = 120\text{Hz}$	-40	-60		dB
Output Bypass Capacitance ( $C_{OUT}$ )	$0.3\Omega \leq \text{ESR} \leq 8\Omega$ $0.1\text{mA} \leq I_{OUT} \leq 50\text{mA}$	22	33		$\mu\text{F}$

- (1) Tested limits are specified to AOQL (Average Outgoing Quality Level) and 100% tested.
- (2) Typicals are at  $25^\circ\text{C}$  (unless otherwise specified) and represent the most likely parametric norm.
- (3) To ensure constant junction temperature, pulse testing is used.

Typical Performance Characteristics

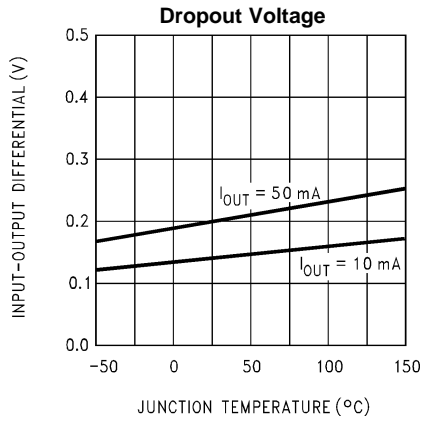


Figure 3.

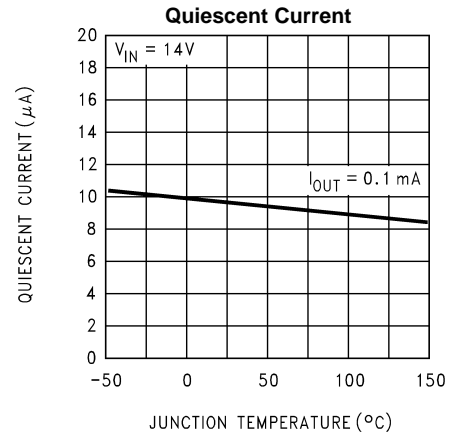


Figure 4.

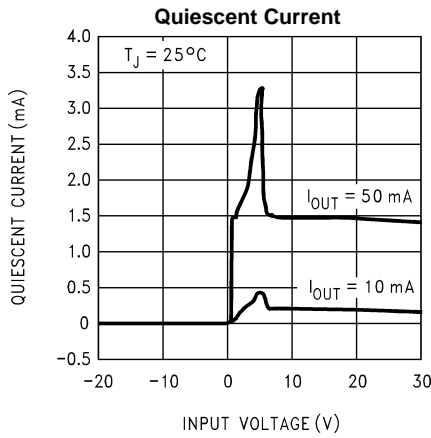


Figure 5.

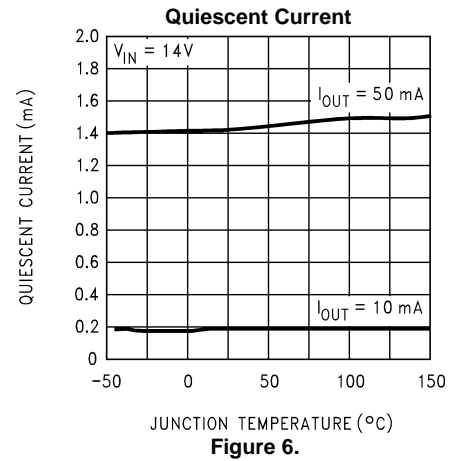


Figure 6.

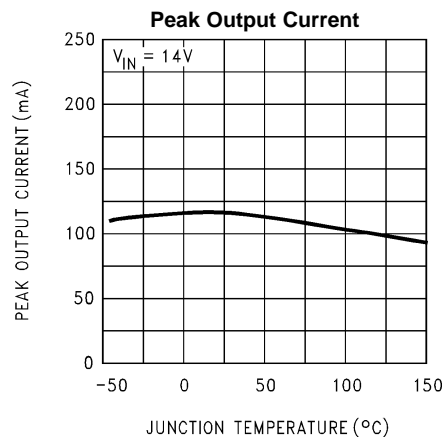


Figure 7.

## APPLICATIONS INFORMATION

Unlike other PNP low dropout regulators, the LM9036Q remains fully operational to 40V. Owing to power dissipation characteristics of the package, full output current cannot be ensured for all combinations of ambient temperature and input voltage.

The junction to ambient thermal resistance  $\theta_{JA}$  rating has two distinct components: the junction to case thermal resistance rating  $\theta_{JC}$ ; and the case to ambient thermal resistance rating  $\theta_{CA}$ . The relationship is defined as:  $\theta_{JA} = \theta_{JC} + \theta_{CA}$ .

While the LM9036Q has an internally set thermal shutdown point of typically 150°C, this is intended as a safety feature only. Continuous operation near the thermal shutdown temperature should be avoided as it may have a negative affect on the life of the device.

The LM9036Q maintains regulation to 55V, it will not withstand a short circuit above 40V because of safe operating area limitations in the internal PNP pass device. Above 55V the LM9036Q will break down with catastrophic effects on the regulator and possibly the load as well. Do not use this device in a design where the input operating voltage may exceed 40V, or where transients are likely to exceed 55V.

## REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format .....	5

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM9036QM-3.3/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM903 6QM-3	<a href="#">Samples</a>
LM9036QM-5.0/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM903 6QM-5	<a href="#">Samples</a>
LM9036QMM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	KDBQ	<a href="#">Samples</a>
LM9036QMM-5.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	KDAQ	<a href="#">Samples</a>
LM9036QMMX-3.3/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	KDBQ	<a href="#">Samples</a>
LM9036QMMX-5.0/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	KDAQ	<a href="#">Samples</a>
LM9036QMX-3.3/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM903 6QM-3	<a href="#">Samples</a>
LM9036QMX-5.0/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM903 6QM-5	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

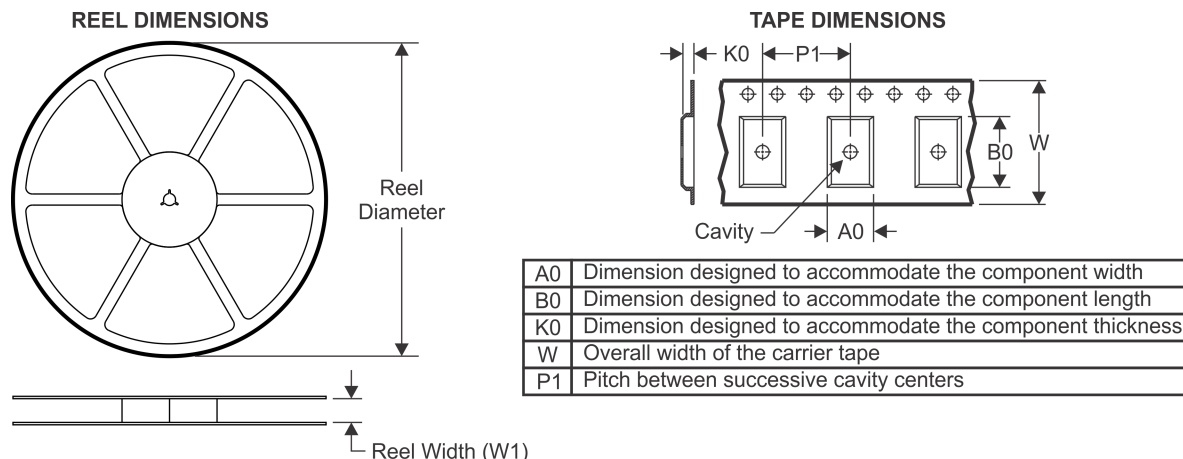
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

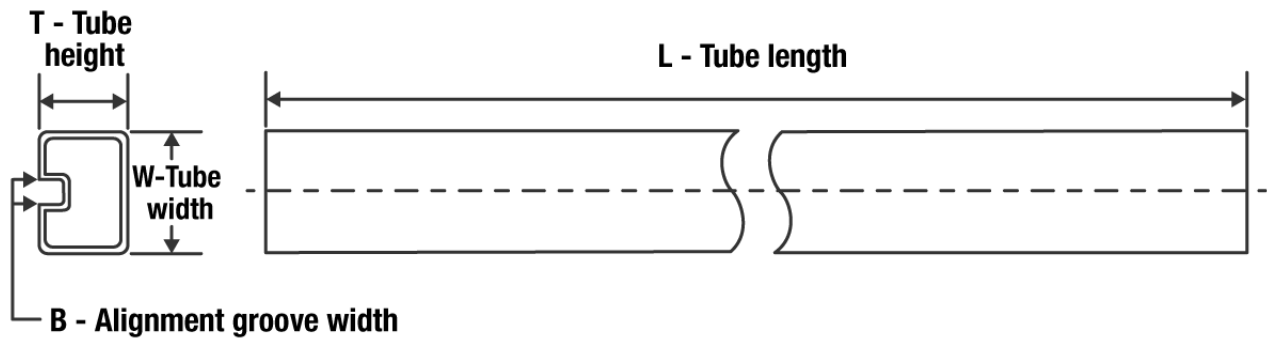

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM9036QMM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036QMM-5.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036QMMX-3.3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036QMMX-5.0/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM9036QMX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM9036QMX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM9036QMM-3.3/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM9036QMM-5.0/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM9036QMMX-3.3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM9036QMMX-5.0/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM9036QMX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM9036QMX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM9036QM-3.3/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM9036QM-5.0/NOPB	D	SOIC	8	95	495	8	4064	3.05



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



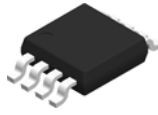
SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

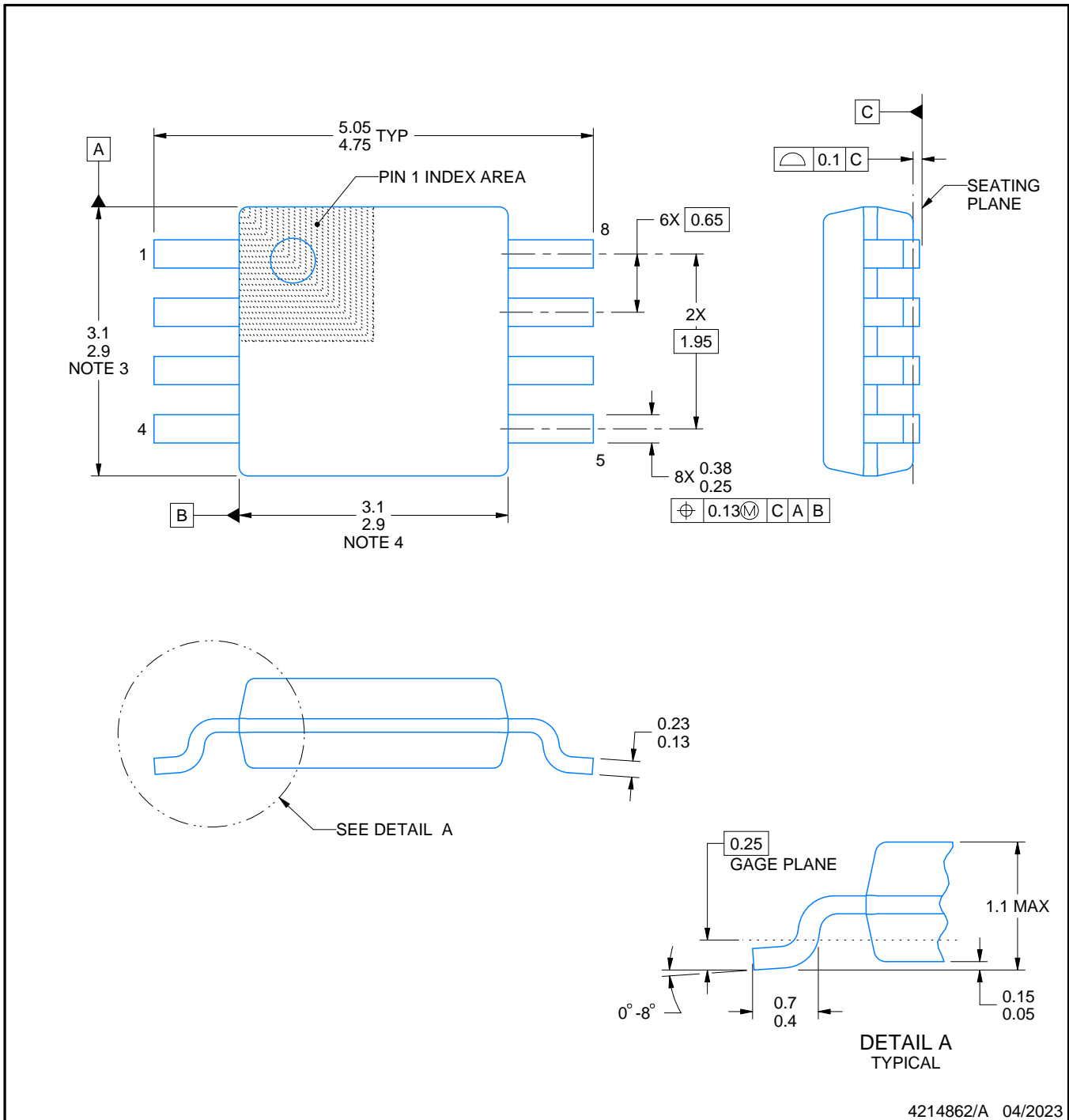
# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**NOTES:**

PowerPAD is a trademark of Texas Instruments.

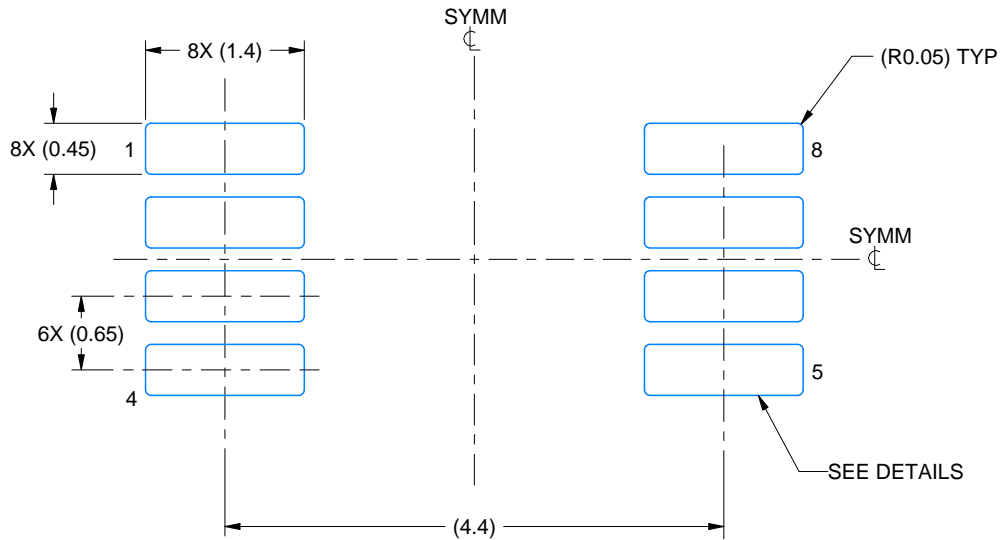
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

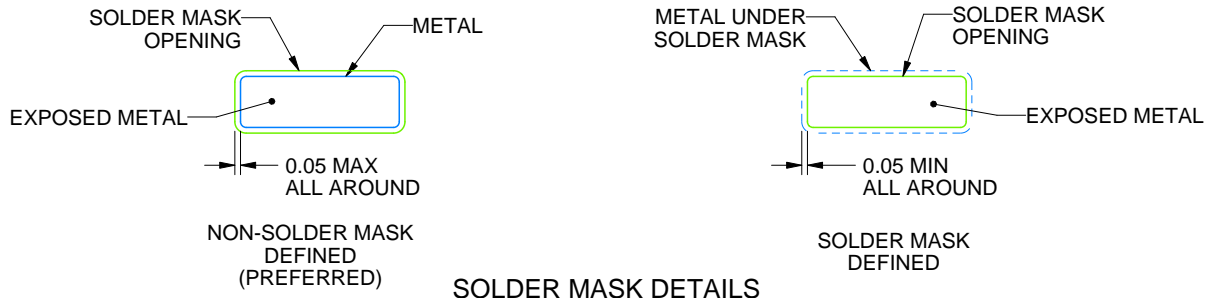
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

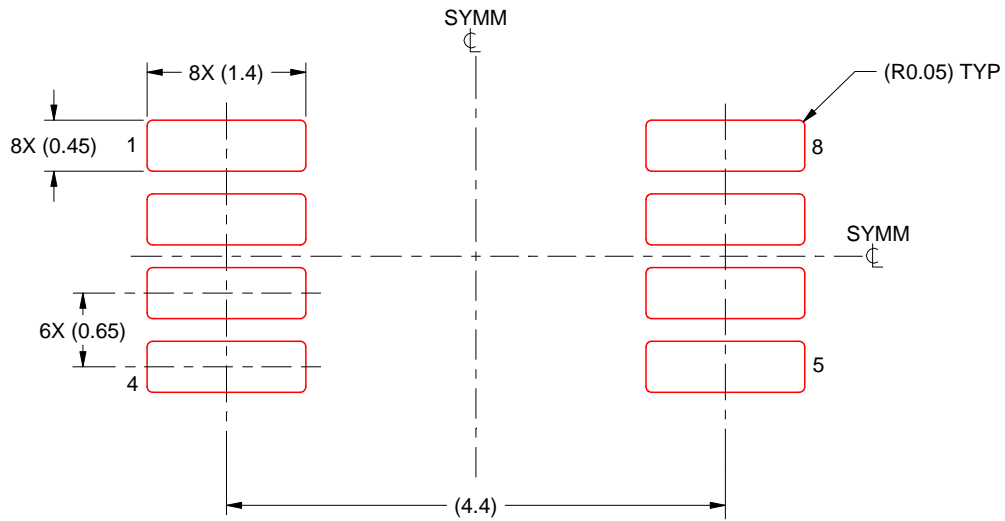
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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