



**THE DATASHEET OF
IXTC13N50**



Power MOSFET ISOPLUS220™

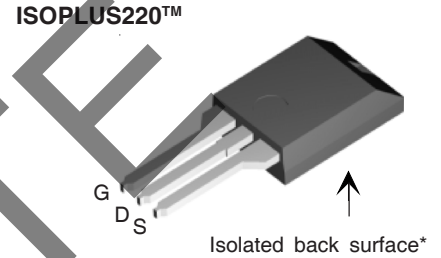
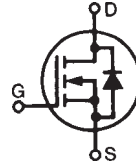
Electrically Isolated Back Surface

N-Channel Enhancement Mode
High dv/dt, Low t_{rr} , HDMOS™ Family

Preliminary Data Sheet

IXTC 13N50

$V_{DSS} = 500 \text{ V}$
 $I_{D25} = 12 \text{ A}$
 $R_{DS(on)} = 0.4 \text{ } \Omega$



Symbol	Test Conditions	Maximum Ratings
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	500 V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1 \text{ M}\Omega$	500 V
V_{GS}	Continuous	± 20 V
V_{GSM}	Transient	± 30 V
I_{D25}	$T_C = 25^\circ\text{C}$	12 A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	48 A
I_{AR}	$T_C = 25^\circ\text{C}$	13 A
E_{AR}	$T_C = 25^\circ\text{C}$	18 mJ
dv/dt	$I_S \leq I_{DM}$, di/dt $\leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$, $R_G = 2 \text{ } \Omega$	5 V/ns
P_D	$T_C = 25^\circ\text{C}$	140 W
T_J		-55 ... +150 $^\circ\text{C}$
T_{JM}		150 $^\circ\text{C}$
T_{stg}		-55 ... +150 $^\circ\text{C}$
T_L	1.6 mm (0.062 in.) from case for 10 s	300 $^\circ\text{C}$
Weight		3 g

G = Gate D = Drain
S = Source

Features

- Silicon chip on Direct-Copper-Bond substrate
 - High power dissipation
 - Isolated mounting surface
 - 2500V electrical isolation
- Low drain to tab capacitance (<35pF)
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated

Applications

- DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control

Advantages

- Easy assembly: no screws or isolation foils required
- Space savings
- High power density
- Low collector capacitance to ground (low EMI)

See IXFH13N50 data sheet for characteristic curves

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
V_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \text{ } \mu\text{A}$	500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 2.5 \text{ mA}$	2		V
I_{GSS}	$V_{GS} = \pm 20 \text{ V}_{DC}$, $V_{DS} = 0$			$\pm 100 \text{ nA}$
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$, $T_J = 25^\circ\text{C}$ $V_{GS} = 0 \text{ V}$, $T_J = 125^\circ\text{C}$			200 μA 1 mA
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = I_T$ Notes 1, 2			0.4 Ω

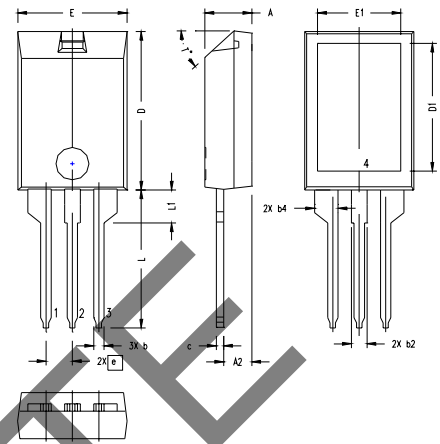
Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)			
		min.	typ.	max.	
g_{fs}	$V_{DS} = 10\text{ V}; I_D = 0; I_T$ Notes 1, 2	7.5	9.0	S	
C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		2800	pF	
C_{oss}		300	pF		
C_{rss}		70	pF		
$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \cdot V_{DSS}; I_D = 0.5 \cdot I_{D25}; R_G = 4.7\ \Omega$ (External)		18	30	ns
t_r			27	40	ns
$t_{d(off)}$			76	100	ns
t_f			32	60	ns
$Q_{g(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 0.5 \cdot V_{DSS}; I_D = I_T$		110	120	nC
Q_{gs}			15	25	nC
Q_{gd}			40	50	nC
R_{thJC}			0.90	K/W	
R_{thCK}			0.30	K/W	

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)			
		min.	typ.	max.	
I_S	$V_{GS} = 0\text{ V}$			13	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			52	A
V_{SD}	$I_F = I_S, V_{GS} = 0\text{ V}$, Note 1			1.5	V
t_{rr}	$I_F = I_S$ $-di/dt = 100\text{ A}/\mu\text{s}$, $V_R = 100\text{ V}$		600		ns

Note: 1. Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$
 2. I_T test current: $I_T = 6.5\text{ A}$

ISOPLUS220 Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.157	.197	4.00	5.00
A2	.098	.118	2.50	3.00
b	.035	.051	0.90	1.30
b2	.049	.065	1.25	1.65
b4	.093	.100	2.35	2.55
c	.028	.039	0.70	1.00
D	.591	.630	15.00	16.00
D1	.472	.512	12.00	13.00
E	.394	.433	10.00	11.00
E1	.295	.335	7.50	8.50
e	.100 BASIC		2.55 BASIC	
L	.512	.571	13.00	14.50
L1	.118	.138	3.00	3.50
T*			42.5*	47.5*

NOTE:

- Bottom heatsink (Pin 4) is electrically isolated from Pin 1, 2, or 3.
- This drawing will meet dimensional requirement of JEDEC SS Product Outline TO-273 except D and D1 dimension.



IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:







4,835,592 4,881,106 5,017,508 5,049,961 5,187,117 5,486,715 6,306,728B1 6,259,123B1 6,306,728B1
 4,850,072 4,931,844 5,034,796 5,063,307 5,237,481 5,381,025 6,404,065B1 6,162,665 6,534,343

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