THE DATASHEET OF

LTC7124IUDD#PBF

17V, Dual 3.5A Synchronous Step-Down Regulator with Ultralow Quiescent Current

FEATURES

- **Wide V_{IN} Range: 3.1V to 17V**
- **Wide V_{OUT} Range: 0.6V to 99% V_{IN}**
- **Dual Step-Down Outputs: 3.5A Per Channel**
- **Integrated 80mΩ/40mΩ N-Channel MOSFETs Provide Up to 95% Efficiency**
- **No-Load I_Q < 8µA with Both Channels Enabled; I_Q < 5.5µA with Only One Channel Enabled**
- **Programmable Frequency (500kHz to 4MHz) with ±25% Frequency Synchronization Range**
- **Configurable for a 2-Phase Single Output at Up to 7A**
- ±1.0% Output Voltage Accuracy
- Current Mode Operation for Excellent Line and Load Transient Response
- Internal or Programmable External Loop Compensation
- Available in a 3mm × 5mm QFN-24 Package

APPLICATIONS

- Battery-Powered Systems
- Point-of-Load Supplies
- Portable Instruments
- Handheld Scanners

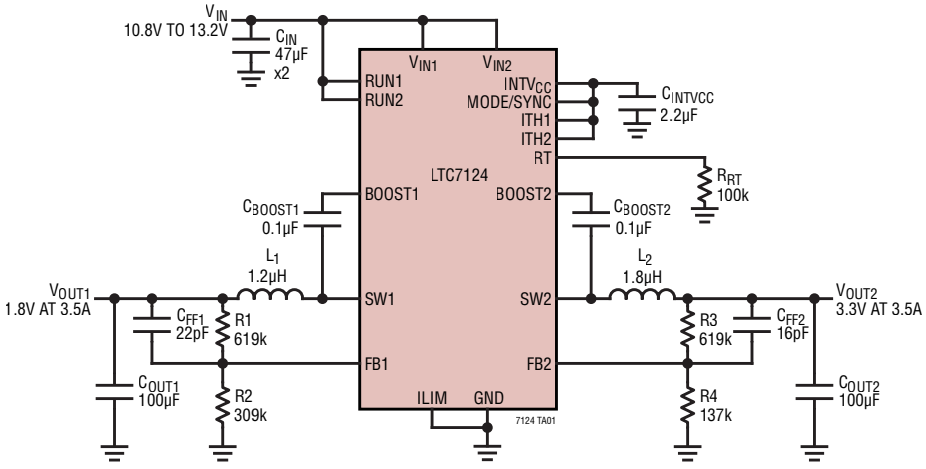
DESCRIPTION

The LTC®7124 is a dual channel, 3.5A per output, high efficiency monolithic step-down regulator capable of operating from input supplies up to 17V. The programmable switching frequency ranges from 500kHz to 4MHz with a ±25% external clock synchronization capability around the programmed frequency. The regulator features ultralow quiescent current for high efficiency over a wide V_{OUT} range.

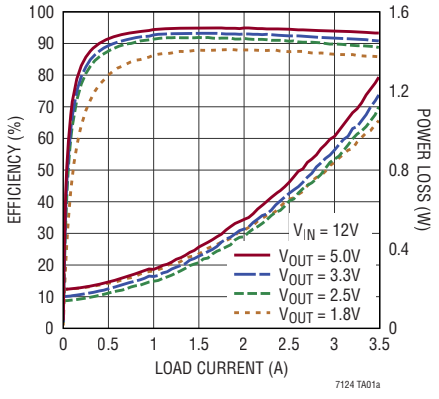
The step-down regulator operates from an input voltage range of 3.1V to 17V and provides an adjustable output range from 0.6V to 99% of V_{IN} while delivering up to 3.5A of output current per channel. A user selectable mode input is provided to allow the user to trade off output ripple for light load efficiency; Burst Mode® operation provides the highest efficiency at light loads, while forced continuous operation provides the lowest output ripple. The LTC7124 includes spread spectrum modulation for low radiated and conductive noise. The LTC7124 is offered in a thermally enhanced, low profile 24-lead 3mm × 5mm QFN package

TYPICAL APPLICATION

1.8V/3.3V 1MHz Step-Down Regulator



Efficiency & Power Loss vs Load Current at 1MHz

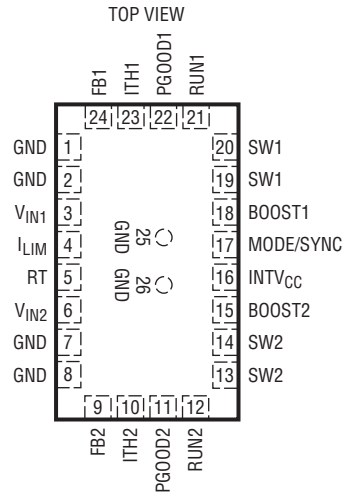


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN1}, V_{IN2} (Note 2) ..... –0.3V to 17V
RUN1, RUN2 ..... –0.3V to 17V
MODE/SYNC .....–0.3V to $INTV_{CC}$+0.3V
I_{LIM}, RT .....–0.3V to $INTV_{CC}$+0.3V
ITH1, ITH2.....–0.3V to $INTV_{CC}$+0.3V
PGOOD1, PGOOD2..... –0.3V to 6V
FB1, FB2..... –0.3V to 6V
Operating Junction Temperature Range
(Note 3).....–40°C to 125°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



UDD PACKAGE
VARIATION: AA
24-LEAD (3mm × 5mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 22°C/W
EXPOSED PAD (PINS 25 & 26) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC7124#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7124EUDD#PBF	LTC7124EUDD#TRPBF	LGVF	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 125°C
LTC7124IUDD#PBF	LTC7124IUDD#TRPBF	LGVF	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN1} = V_{IN2} = 12V, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Voltage			3.1		17	V
V_{OUT}	Output Voltage	(Note 6)		0.6		0.99 • V_{IN}	V
I_Q	Input Quiescent Current	Active Mode, Single Channel (Note 4) Active Mode, Dual Channels (Note 4) Burst Mode, I_{OUT1} = I_{OUT2} = 0A Burst Mode, Single Channel, I_{OUT} = 0A Shutdown Mode; V_{RUN1} = V_{RUN2} = 0V			1.5 2 8 5.5 0.1	2.75 3 16 11 1	mA mA µA µA µA
V_{FB}	Regulated Feedback Voltage	(Note 5)	 ●	0.596 0.594	0.6 0.6	0.604 0.606	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN1} = V_{IN2} = 12V, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\Delta V_{LOAD\&LINE\ REG}$	Output Voltage Load and Line Regulation	V_{IN} = 3.1 to 17V (Note 5) ITH = 0.3V to 0.9V			0.3	0.5	%
I_{FB}	Feedback Pin Input Current					10	nA
$g_{m(EA)}$	Error Amplifier Transconductance	ITH = 0.6V		300	500	700	µS
t_{ON-MIN}	Minimum On Time	(Note 7)			50		ns
I_{SW}	Top NMOS Switch Leakage Bottom NMOS Switch Leakage				0.1 0.1	±1 ±1	µA µA
$R_{DS(ON)}$	Top NMOS On Resistance Bottom NMOS On Resistance				80 40		mΩ mΩ
V_{RUN}	RUN Input High RUN Input Low			1.0		 0.3	V V
	RUN Input Current	V_{RUN} = 12V			0	±100	nA
$V_{MODE/SYNC}$	Pulse Skip Mode Burst Mode Operation Forced Continuous Mode			 $INTV_{CC}$–0.4 1.0		0.3 $INTV_{CC}$–1.2	V V V
V_{ILIM}	I_{LIM} Input Threshold	Input Low Input High		 $INTV_{CC}$–0.3		0.2 	V V
I_{LIM}	Peak Current Limit	I_{LIM} = 0V (Both Channels) I_{LIM} = $INTV_{CC}$ (Both Channels) I_{LIM} = Floating, Channel 1 I_{LIM} = Floating, Channel 2		4.4 2.2 4.4 2.2	5.0 2.6 5.0 2.6	5.6 3.0 5.6 3.0	A A A A
t_{SS}	Internal Soft Start Time				1100		µs
V_{INTVCC}	V_{INTVCC} LDO Output Voltage	V_{IN1} > 4V			3.6		V
	V_{INTVCC} Undervoltage Lockout	V_{IN1} Ramping Up	●	2.75	2.9	3.05	V
	V_{INTVCC} Undervoltage Lockout Hysteresis				300		mV
	V_{IN} Overvoltage Lockout Rising		●	17.9	18.4	18.9	V
	V_{IN} Overvoltage Lockout Hysteresis				500		mV
f_{OSC}	R_T Programmable Oscillator Frequency	R_{RT} = 100k	●	0.92	1	1.08	MHz
f_{SYNC}	SYNC Capture Range	% of Programmed Frequency	●	75		125	%
	Power Good Range			±5	±7.5	±10	%
R_{PGOOD}	Power Good Resistance				650	1000	Ω
t_{PGOOD}	PGOOD Delay	PGOOD Low to High, R_{RT} = 100k PGOOD High to Low, R_{RT} = 100k			25 32		µs µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Transient Absolute Maximum Voltages should not be applied for more than 4% of the switching duty cycle.

Note 3: The LTC7124 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7124E is guaranteed to meet specified performance from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7124I is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

T_J is calculated from the ambient T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D \bullet \theta_{JA})$

Note 4: The Quiescent Current in active mode does not include switching loss of the power FETs.

Note 5: The LTC7124 is tested in a proprietary test mode that connects V_{FB} to the output of error amplifier.

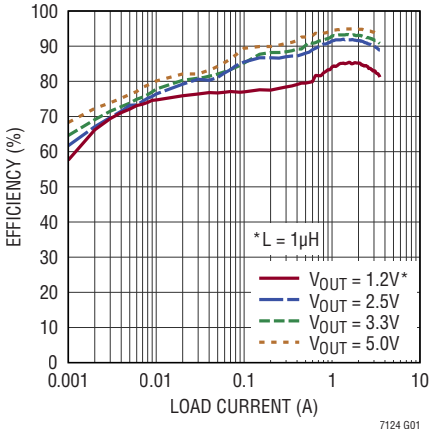
Note 6: The maximum V_{OUT} is limited by the automatic boost refresh that occurs in high duty cycle and dropout cases. The maximum V_{OUT} value listed here is guaranteed by design.

Note 7: The minimum on-time is determined by the speed of the top switch driver and peak current comparator. The typical value listed here is guaranteed by design.

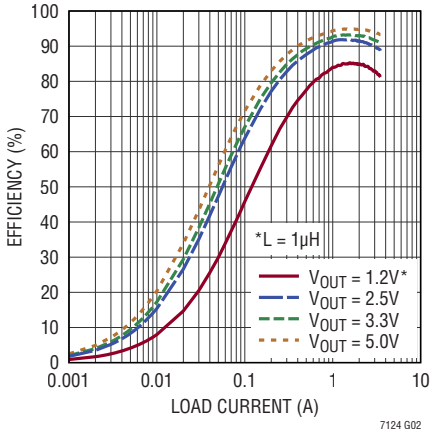
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, L = 2.2µH, f = 1MHz unless otherwise noted.

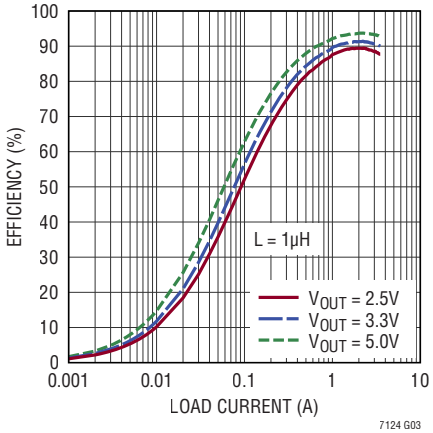
Efficiency vs Load Current in Burst Mode at 1MHz



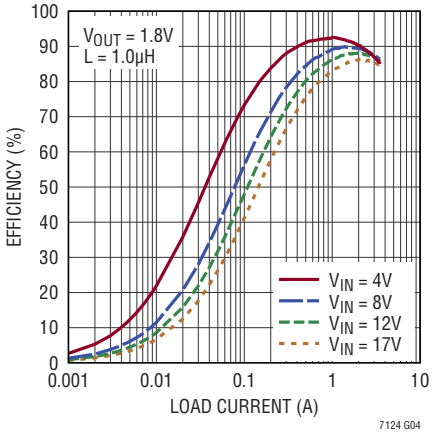
Efficiency vs Load Current in Forced Continuous Mode at 1MHz



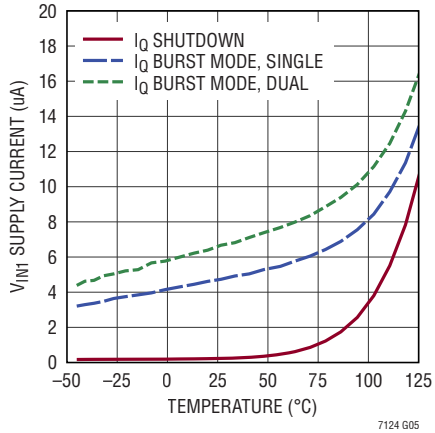
Efficiency vs Load Current in Forced Continuous Mode at 2.25MHz



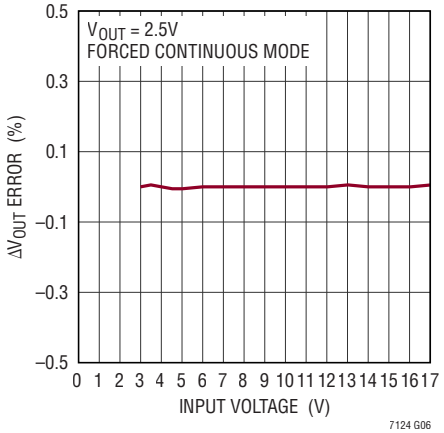
Efficiency vs Load Current for Varying Input Supply



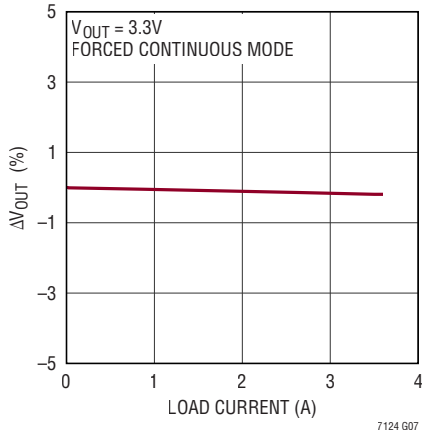
V_{IN1} Supply Current vs Temperature



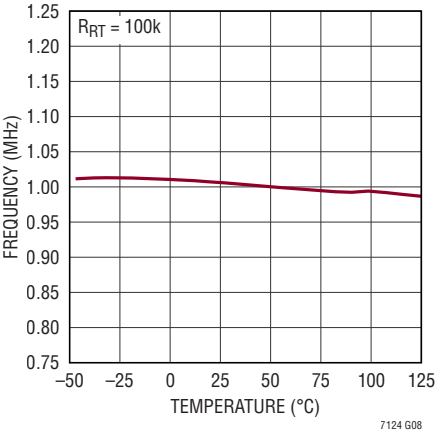
Line Regulation, No Load



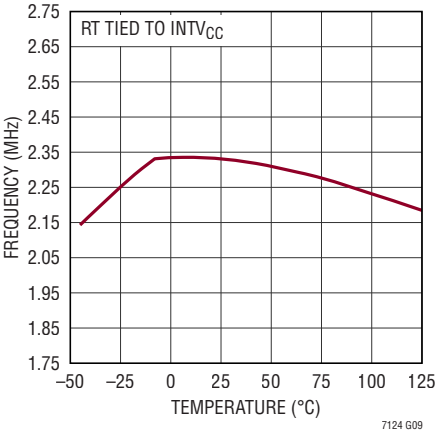
Load Regulation



RT Frequency vs Temperature



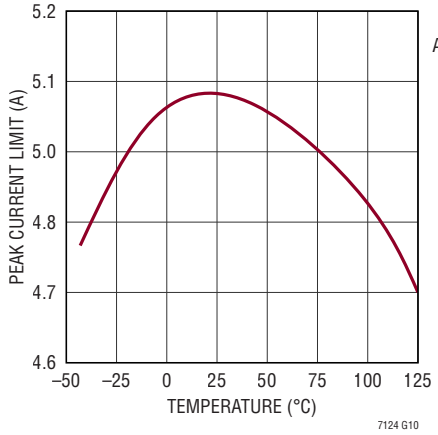
Spread Spectrum Center Frequency vs Temperature



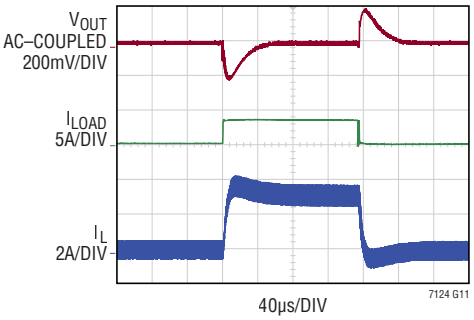
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, L = 2.2µH, f = 1MHz unless otherwise noted.

Peak Current Limit vs Temperature

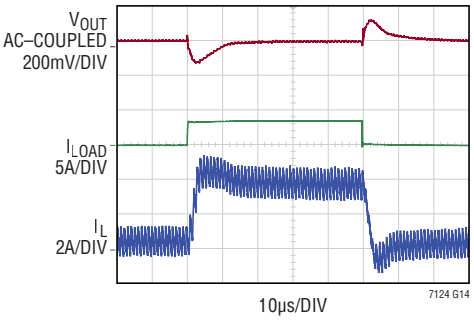


Load Step with Internal Compensation



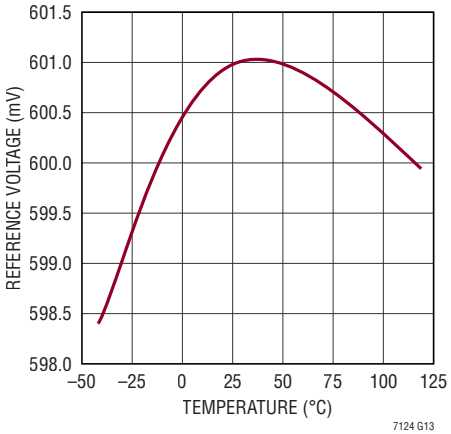
V_{IN} = 12V
V_{OUT} = 2.5V
I_{LOAD} = 100mA to 3.5A
L = 1.8µH
ITH = $INTV_{CC}$
C_{OUT} = 100µF

Load Step with External Compensation

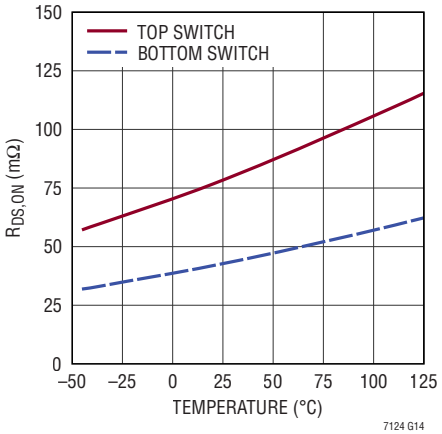


V_{IN} = 12V
V_{OUT} = 2.5V
I_{LOAD} = 150mA to 3.5A
L = 1.2µH
C_{ITH} = 150pF, R_{ITH} = 30kΩ
C_{OUT} = 100µF

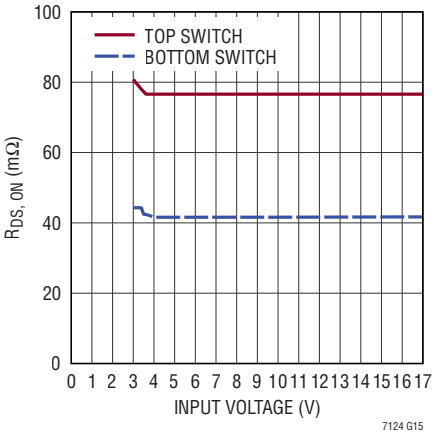
Reference Voltage vs Temperature



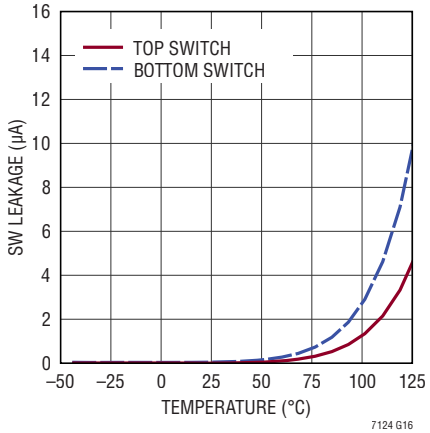
$R_{DS(ON)}$ vs Temperature



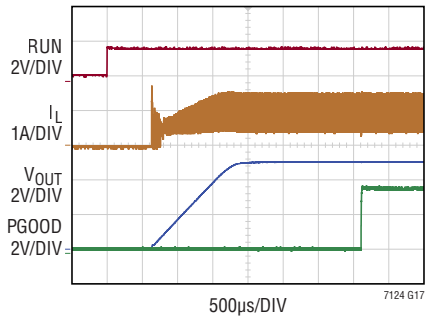
$R_{DS(ON)}$ vs Input Supply Voltage



Switch Leakage Current

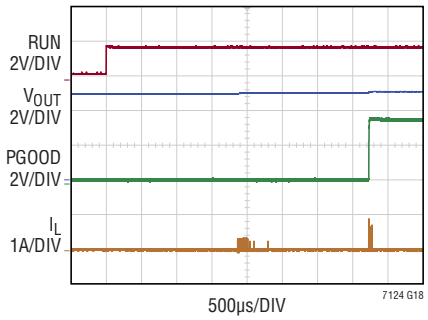


Start–Up With Load in Burst Mode Operation



R_{LOAD} = 5Ω
V_{OUT} = 5V

Start–Up into Pre–Biased Output in Burst Mode Operation

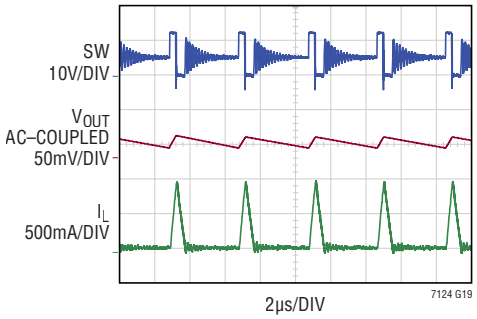


V_{OUT} = 5V

TYPICAL PERFORMANCE CHARACTERISTICS

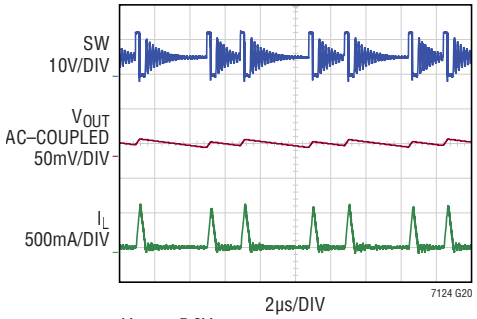
T_A = 25°C, V_{IN} = 12V, L = 2.2µH, f = 1MHz unless otherwise noted.

Burst Mode Operation with Full Current Limit



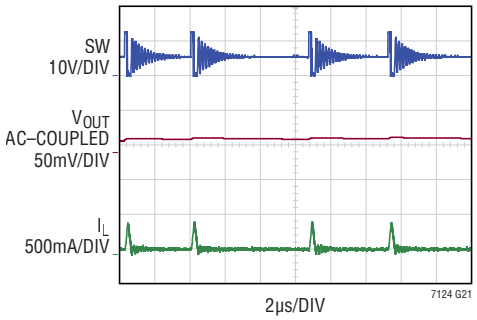
V_{OUT} = 5.0V
I_{OUT} = 100mA
I_{LIM} TIED TO GND

Burst Mode Operation with Half Current Limit



V_{OUT} = 5.0V
I_{OUT} = 50mA
I_{LIM} TIED TO $INTV_{CC}$

Pulse Skip Mode Operation



V_{OUT} = 5.0V
I_{OUT} = 10mA

PIN FUNCTIONS

GND (Pins 1, 2, 7, 8, Exposed Pad 25/26): The exposed pads should be soldered to PCB ground for rated thermal performance. Connect all GND pins together with solid ground plane.

V_{IN1} (Pin 3): Input Voltage of the Channel 1 Step-Down Regulator. This input powers the $INTV_{CC}$ LDO.

I_{LIM} (Pin 4): Current Limit Select Pin. Tying this pin to GND sets full current limit for both channels. Tying this pin to $INTV_{CC}$ drops the current limit by a factor of 2 for both channels. Floating this pin sets full current limit for Channel 1 and half current limit for Channel 2.

RT (Pin 5): Switching Frequency Program Pin. Connect an external resistor (between 208k to 19k) from this pin to GND to program the frequency from 500kHz to 4MHz, respectively. When RT is tied to $INTV_{CC}$, spread spectrum mode of operation will be enabled. In addition, when spread spectrum is enabled, syncing capability on the MODE/SYNC pin is disabled, and the part will operate in forced continuous mode around a center frequency of 2.25MHz.

V_{IN2} (Pin 6): Input Voltage of the Channel 2 Step-Down Regulator. May be a different voltage than V_{IN1}.

FB2 (Pin 9): Feedback Input to the Error Amplifier of the Channel 2 Step-Down Regulator. Connect resistor divider tap to this pin. The output voltage can be adjusted from 0.6V to 0.99 • V_{IN2} by: $V_{OUT2} = 0.6V \times [1 + (R1/R2)]$.

ITH2 (Pin 10): Channel 2 Error Amplifier Output and Switching Regulator Compensation Pin. Connect this pin to appropriate external components to compensate the regulator loop frequency response or to $INTV_{CC}$ to use the default internal compensation.

PGOOD2 (Pin 11): Open Drain Power Good Indicator for Channel 2.

RUN2 (Pin 12): Logic Controlled RUN Input to Channel 2. Do not leave this pin floating. Logic High activates channel 2 of the step-down regulator.

SW2 (Pins 13, 14): Switch Node Connection to the Inductor of the Channel 2 Step-Down Regulator.

BOOST2 (Pin 15): Boosted Floating Driver Supply for Channel 2. The (+) terminal of the bootstrap capacitor connects to this pin while the (–) terminal connects to the SW2 pin. The normal operating voltage swing of this pin ranges from $INTV_{CC}$ to $V_{IN2} + INTV_{CC}$.

$INTV_{CC}$ (Pin 16): Low Dropout Regulator. Bypass with at a low ESR cap of at least 2.2µF to ground.

MODE/SYNC (Pin 17): Burst Mode Select and Oscillator Synchronization of the Step-Down Regulator. This pin can be connected to $INTV_{CC}$ for Burst Mode operation (800mA minimum peak current clamp), GND for pulse skipping mode (200mA minimum peak current clamp), or between 1.0V and $INTV_{CC}$ – 1.2V for forced continuous mode. Furthermore, connecting MODE/SYNC to an external clock will synchronize the internal clock to the external clock and put the part in forced continuous mode. However, syncing capability is disabled when spread spectrum is enabled.

BOOST1 (Pin 18): Boosted Floating Driver Supply for Channel 1. The (+) terminal of the bootstrap capacitor connects to this pin while the (–) terminal connects to the SW1 pin. The normal operating voltage swing of this pin ranges from $INTV_{CC}$ to $V_{IN1} + INTV_{CC}$.

SW1 (Pins 19, 20): Switch Node Connection to the Inductor of the Channel 1 Step-Down Regulator.

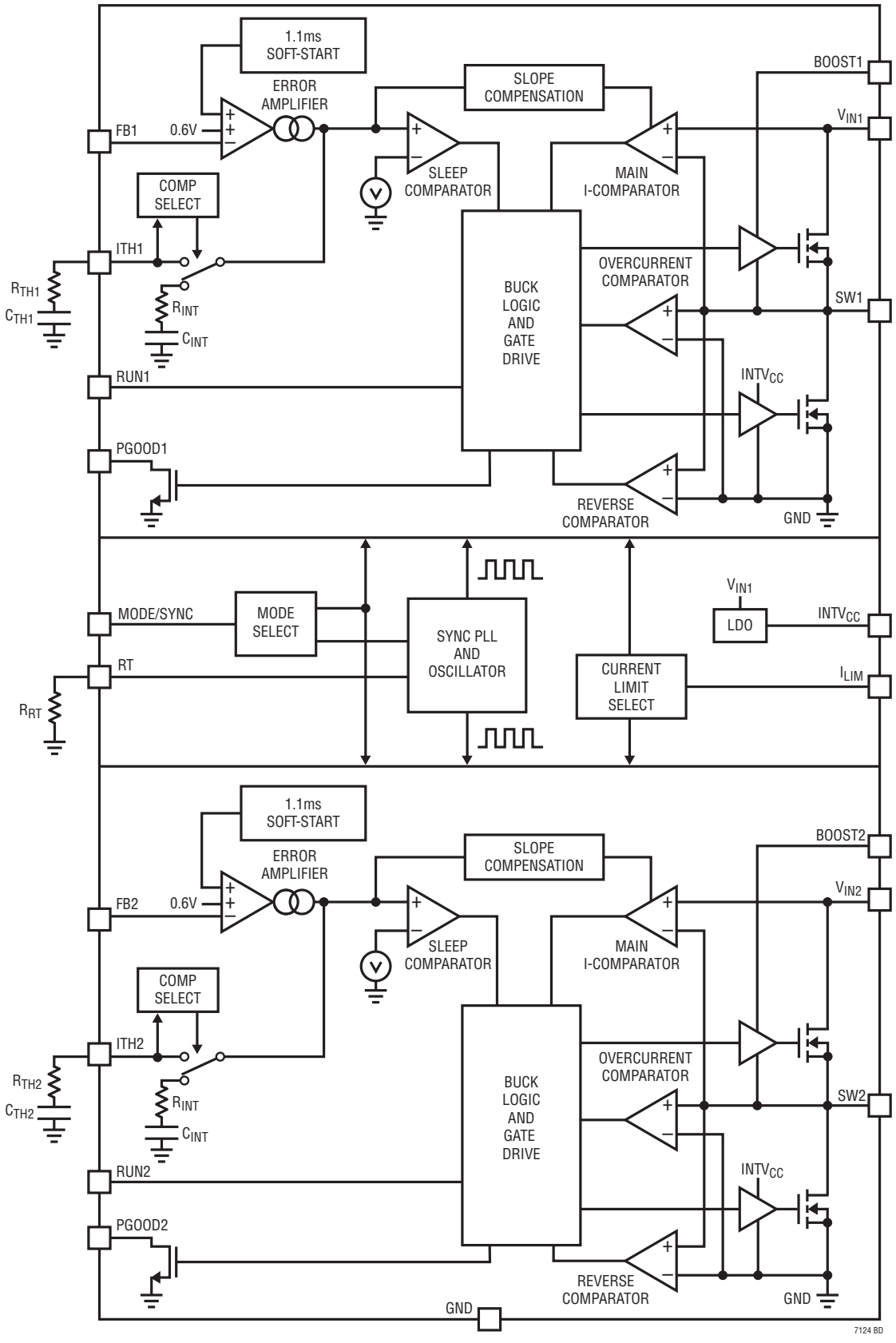
RUN1 (Pin 21): Logic Controlled RUN Input to Channel 1. Do not leave this pin floating. Logic High activates channel 1 of the step-down regulator.

PGOOD1 (Pin 22): Open Drain Power Good Indicator for Channel 1.

ITH1 (Pin 23): Channel 1 Error Amplifier Output and Switching Regulator Compensation Pin. Connect this pin to appropriate external components to compensate the regulator loop frequency response or connect to $INTV_{CC}$ to use the default internal compensation.

FB1 (Pin 24): Feedback Input to the Error Amplifier of the Channel 1 Step-Down Regulator. Connect resistor divider tap to this pin. The output voltage can be adjusted from 0.6V to 0.99 • V_{IN1} by: $V_{OUT1} = 0.6V \times [1 + (R1/R2)]$.

BLOCK DIAGRAM



OPERATION

The LTC7124 is a dual-channel, synchronous step-down regulator featuring a constant frequency, peak current mode architecture. It is capable of providing up to 3.5A of output current across a wide V_{IN} range for each channel, while regulating with ultralow quiescent current when no load is present. Each channel is enabled by raising its respective RUN pin voltage above 1V.

Main Control Loop

In normal operation, the top power switch (N-channel MOSFET) is turned on at the onset of a clock cycle. Once the inductor current has ramped up to a certain peak value, as determined by the I_{TH} voltage, the top power switch turns off, and the bottom switch (N-channel MOSFET) turns on for the remainder of the clock cycle. This I_{TH} voltage is the output of the error amplifier, which compares the FB voltage to an internal 0.6V reference. When the load increases, the FB voltage falls below the reference value, thereby causing the I_{TH} voltage to increase until the average inductor current matches the new load current. Due to a wide range of possible operating frequencies, the error amplifier can be internally or externally compensated based on the I_{TH} pin.

The frequency of operation is programmed by the value of the R_T resistor. If a clock signal is applied to the MODE/SYNC pin, an internal phase-locked loop will synchronize the R_T programmed frequency to the external clock. If the RT pin is tied to $INTV_{CC}$, spread spectrum operation around 2.25MHz (±12%) is enabled, and external clock syncing is not allowed.

Low Current Operation

At light load current levels, the LTC7124 can automatically transition from continuous operation to one of two discontinuous conduction modes (DCMs) of operation, if programmed to do so. In both these modes, Burst Mode and pulse skipping, as long as the I_{TH} voltage is lower than the zero current level, the switcher will halt switching and operate in an ultralow quiescent current sleep state. In this sleep state, the part will draw only 5.5µA of quiescent current from V_{IN1} if only one channel is enabled and 8µA of quiescent current from V_{IN1} if both channels are enabled. When the load increases and pulls the output out of sleep, the part resumes switching in its active state.

To optimize efficiency, Burst Mode can be enabled by tying the MODE/SYNC pin to $INTV_{CC}$. In Burst Mode, the minimum peak current level is set to be 800mA, thereby overriding any I_{TH} voltage that commands a lower peak current.

To minimize V_{OUT} ripple, pulse skipping mode can be enabled by grounding the MODE/SYNC pin. In this case, the minimum peak current level is set to be 200mA, lower than in Burst Mode. As a result, compared to Burst Mode, pulse skipping mode produces a lower output voltage ripple, but at a slightly lower efficiency at light loads.

If a channel is programmed to operate at half peak current with the I_{LIM} pin, the minimum peak current levels likewise scale accordingly by half to 400mA in Burst Mode and 100mA in pulse skipping mode.

Forced Continuous Mode Operation

If operating in DCM is undesirable, the LTC7124 can be put in forced continuous mode by tying the MODE/SYNC pin between 1V and $INTV_{CC}$ –1.2V. In forced continuous mode, the part will switch every clock cycle regardless of the value of the output load current.

"Power Good" Status Output

The PGOOD pin output indicates whether the output voltage is within ±7.5% of the regulation point. Immediately after the output voltage enters this ±7.5% window, the PGOOD output becomes high impedance. Conversely, when the output voltage falls out of regulation, the PGOOD open-drain output is pulled low after a 32 clock cycle delay.

High Duty Cycle/Dropout Operation

As the operating duty cycle of a channel approaches 100%, the part enters dropout operation for that channel. In this very high duty cycle condition, if the bottom power switch has been off for 32 clock cycles, the regulator will automatically turn off the top power switch and turn on the bottom power switch for the last 25% of the next clock cycle to charge the BOOST-SW capacitor.

OPERATION

As the BOOST-SW capacitor depletes charge, the gate drive voltage for the top power switch decreases, which increases the $R_{DS(ON)}$. At heavy loads, this increased $R_{DS(ON)}$ can result in excessive power dissipation. While this scenario is avoided through the forced refresh of the BOOST-SW capacitor, the maximum duty cycle of the regulator is limited to 99%.

If the part is programmed for either Burst Mode or pulse skipping mode, the regulator will transition in and out of the sleep state as needed to keep the output voltage in regulation.

Minimum On-Time Considerations

The minimum on-time is the smallest amount of time that the LTC7124 can turn on the top power MOSFET, trip the peak current comparator and turn off the top power MOSFET. As specified in the Electrical Characteristics Table, this time is typically 50ns. As a result, the minimum duty cycle can be calculated as:

$$DC_{MIN} = f \bullet t_{ON(MIN)}$$

where $t_{ON(MIN)}$ is the minimum on time. As seen in the equation above, decreasing the operating frequency loosens the minimum duty cycle constraint.

For a given V_{IN}, the lowest output voltage for which the switcher can maintain regulation is as follows:

$$V_{OUT(MIN)} = V_{IN} \bullet f \bullet t_{ON(MIN)}$$

In the case where the minimum duty cycle constraint is violated, the output voltage will not be in regulation and generate an overvoltage condition. In both DCMs, the switcher will remain in sleep mode until the output voltage falls out below the desired regulation voltage. In forced continuous mode, an overvoltage condition will halt switching until the output decreases to within 7.5% of the desired regulation voltage.

Input Overvoltage Protection

To protect the power MOSFETs from transient spikes, the input supply voltage of each channel is continually monitored. When the input voltage exceeds 18.4V, the regulator suspends switching and resets the internal soft-start capacitor. Once the input voltage has fallen below 18V, the regulator will resume normal switching operation, if its respective RUN pin is tied high.

Low Supply Operation

To ensure that the regulator will operate properly, the LTC7124 incorporates an undervoltage lockout circuit, which shuts down both channels when V_{IN1} drops below 3.1V. Once V_{IN1} rises above this lower limit, both switchers will resume normal operation if their respective RUN pins are enabled. Nevertheless, the $R_{DS(ON)}$ of the power switches may be slightly higher due to lower gate drive depending on the value of V_{IN1} (see $R_{DS(ON)}$ vs Input Supply Voltage graph).

Soft-Start

The LTC7124 has an internal 1100µs soft start ramp. During this soft-start period, the part will operate in pulse-skipping mode regardless of the mode programmed by the MODE/SYNC pin. Once the soft-start period is complete, the part will transition into the desired mode of operation.

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Output Voltage Programming

For non-fixed output voltage parts, the output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R1}{R2}\right)$$

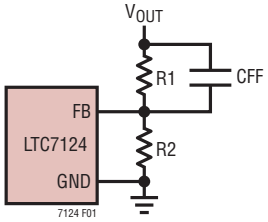

Figure 1. Setting the Output Voltage

Programing Switching Frequency

Connecting a resistor from the RT pin to GND sets the switching frequency between 500kHz and 4MHz based on the graph in Figure 2.

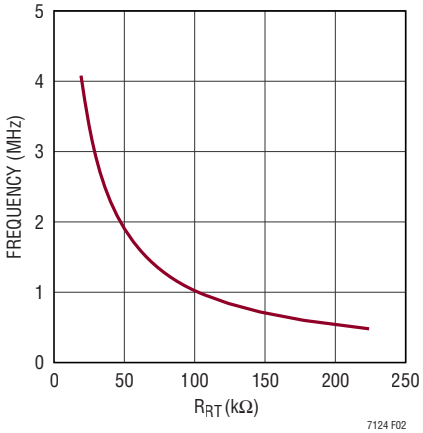

Figure 2. R_{RT} vs Frequency

The LTC7124 also has the capability to sync to an external frequency within ±25% of the RT-programmed frequency when a clock signal is applied to the MODE/SYNC pin. When sync is engaged, the part operates in forced continuous mode.

Table 1. Inductor Selection Table

INDUCTOR	INDUCTANCE (µH)	DCR (mΩ)	MAX CURRENT (A)	DIMENSIONS (mm)	HEIGHT (mm)	MANUFACTURER
IHLP-2020BZ-01 Series	0.22 0.33 0.47 0.68 1	4.9 7.6 8.9 11.2 18.9	15 12 11.5 10 7	5.2 × 5.5 5.2 × 5.5 5.2 × 5.5 5.2 × 5.5 5.2 × 5.5	2 2 2 2 2	Vishay www.vishay.com
XAL4020 Series	0.6 1 1.5 2.2	9.5 13.25 17.75 21.45	8.7 7.9 7.1 5.6	4 × 4 4 × 4 4 × 4 4 × 4	2.1 2.1 2.1 2.1	Coilcraft www.coilcraft.com
XAL4030 Series	3.3	35.2	5.5	4 × 4	3.1	
XAL5030 Series	1 2.2 3.3 4.7 6.8	8.5 13.2 21.2 36 26.75	14 9.2 8.7 6.7 6	5 × 5 5 × 5 5 × 5 5 × 5 5 × 5	3.1 3.1 3.1 3.1 3.1	
RLF7030 Series	1 1.5	7.3 8	6.4 6.1	6.9 × 7.3 6.9 × 7.6	3.2 3.2	TDK www.tdk.com
DFE201610E Series	0.24 0.33	16 21	7 6.1	2 × 1.6 2 × 1.6	1 1	Murata www.murata.com
DFE201512E Series	0.24 0.33 0.47	13 15 20	6 5.7 5	2 × 1.6 2 × 1.6 2 × 1.6	1.2 1.2 1.2	

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Tying the RT pin to $INTV_{CC}$ will enable spread spectrum operation around 2.25MHz (±12%). Doing so will also disable the frequency sync function as well as place the part in the forced continuous mode of operation.

In the LTC7124, the two channels operate 180° out of phase.

Internal/External Loop Compensation

The LTC7124 features both internal and external loop compensation options, allowing the user to optimize the transient response of the regulator based on operating frequency. Tying the ITH pin of a channel to $INTV_{CC}$ will select the internal compensation network, which is designed to be stable at all operating frequencies. For a faster loop transient response, external loop compensation network components can be connected to the ITH pin of a channel to enable external loop compensation. External loop compensation is recommended for switching frequencies at 1MHz or higher.

Inductor Selection

In addition to the desired input and output voltages, the inductor value and operating frequency determine the inductor ripple current.

$$\Delta I_L = \frac{V_{OUT}}{f \bullet L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Based on the equation, a higher inductor value or a higher operating frequency will lower the inductor ripple current. Decreasing the inductor ripple current reduces power loss in the inductor, ESR losses in the output capacitors, and the output voltage ripple, thereby boosting efficiency. Thus, as high efficiency necessitates a large inductor, an inherent tradeoff exists among component size, efficiency, and operating frequency.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on inductance selected. As the inductance or frequency increases, core losses decrease. However, the increased turns of wire required for larger inductances and higher operating frequencies result in higher copper losses.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," meaning that the inductance collapses abruptly when the peak design current is exceeded. When this occurs, the inductor ripple current (and consequently the output voltage ripple) abruptly increases. For this reason, it is key to ensure that the core will not saturate.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. Table 1 gives a sampling of available surface mount inductors.

Checking Transient Response

The loop response can be checked by looking at the transient response to a load step. When external compensation is utilized, the ITH pin allows for optimization of the control loop behavior by providing a DC-coupled and AC filtered closed loop response test point. The DC step, rise time, and settling behavior at this test point reflect the close loop response. Assuming a predominantly second-order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen on the ITH pin.

When the load current is stepped, switching regulators take several cycles to respond. Immediately after the step, V_{OUT} shifts by an amount equal to ΔI_{LOAD} • ESR, where ESR is the effect series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback

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error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The addition of a feedforward capacitor can improve the high frequency response, by providing a phase lead due to the creation of a high frequency zero with R1 in Figure 1.

The stability of the closed-loop system will determine the output voltage settling behavior. LTpowerCAD® and LTspice® can be used to check control loop and transient performance.

In some applications, a more severe transient can be caused by switching in loads with large (>1µF) load capacitors. The discharged load capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection and soft-starting.

Input Capacitor (C_{IN}) Selection

The input capacitance, C_{IN}, filters the square wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current is recommended. The maximum RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \bullet \frac{\sqrt{V_{OUT} \bullet (V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$ where

$$I_{RMS} = \frac{I_{OUT}}{2}$$

This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple ΔV_{OUT} is approximated by:

$$\Delta V_{OUT} < \Delta I_L \bullet \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors are very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints.

When using low-ESR ceramic capacitors, the output capacitor value should be chosen to fulfill a charge storage requirement. During load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle

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does the output drop linearly. The output droop V_{DROOP} is usually about 3 times the linear drop of the first cycle. Thus, a good place to start is the with the output capacitor size of approximately:

$$C_{OUT} = 3 \bullet \frac{\Delta I_{OUT}}{f \bullet V_{DROOP}}$$

Depending on load step requirements and the duty cycle, more capacitance may be required. The actual V_{DROOP} should be verified by applying a load step to the output.

Using Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are available in small case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, due to the self-resonant and high-Q characteristics of some types of ceramic capacitors, care must be taken when these capacitors are used at the input. When a ceramic capacitor is used at the input and the power is supplied by a wall adaptor through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

$INTV_{CC}$ Regulator Bypass Capacitor

An internal low dropout (LDO) regulator produces a 3.6V supply, which powers the internal active circuitry and the gate drive for the internal power MOSFETs. The $INTV_{CC}$ pin connects to the output of the LDO regulator and requires a ceramic decoupling capacitor of at least 2.2µF connected to ground.

Boost Capacitor

In the LTC7124, an internal "bootstrap" circuit generates a voltage rail above the input voltage V_{IN} to create the gate drive for the top power switch. Each time the bottom power MOSFET is turned on, a boost capacitor C_{BOOST}, connected between the BOOST and SW pins, is charged up to $INTV_{CC}$. During the next clock cycle, when the top power MOSFET is turned on, the BOOST pin voltage will then be approximately V_{IN} + $INTV_{CC}$. Due to the low amounts of current drawn from the BOOST rail during operation, a boost capacitance of 0.1µF will be sufficient for most applications.

Efficiency Considerations

The percentage efficiency of a switching regulator is equal to the output power divided by the input power multiplied by 100%. Analyzing individual losses can help identify those that limit efficiency as well as changes that produce most improvement. Percent efficiency can then be expressed as:

$$\% \text{ Efficiency} = 100\% - (\text{Loss1} + \text{Loss2} + \ldots)$$

where Loss1, Loss2, etc. are individual losses as a percentage of input power.

While all lossy elements will contribute to overall power dissipation, the main losses are the result of I^2R losses, switching and biasing losses, and other "hidden" losses.

1. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L but is "chopped" between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $$R_{SW} = R_{DS(ON)TOP} \bullet DC + R_{DS(ON)BOT} \bullet (1 - DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R losses:

   $$I^2R \text{ losses} = I_{OUT}^2(R_{SW} + R_L)$$

2. The switching current is the sum of the MOSFET driver and control currents powered off the $INTV_{CC}$ rail generated by the internal LDO. The power MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting

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*d*Q/*d*t is a current out of $INTV_{CC}$ that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f (Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs, respectively, and f is the switching frequency. The power loss is thus:

$$\text{Switching Loss} = I_{GATECHG} \bullet V_{IN1}$$

The gate charge loss is proportional to V_{IN1} and f, and thus these losses will be more pronounced at higher supply voltages and higher frequencies.

3. Other "hidden" losses such as transition loss and copper trace and internal load resistances can account for additional efficiency degradations in the overall power system. It is very important to include these "system" level losses in the design of the system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The LTC7124 internal power devices switch quickly enough that these losses are not significant compared to other sources. These losses plus other losses, include diode conduction losses during dead-time and inductor core losses, generally account for less than 2% total additional loss.

Thermal Conditions

In most applications, the LTC7124 will not dissipate much heat due to its high efficiency. However, power dissipation can increase significantly when the part is running at high V_{IN}, high ambient temperature, high switching frequency, and/or maximum output load. If enough heat is dissipated such that the maximum junction temperature of 160°C is exceeded, the part will shut down until the temperature falls by at least 15°C. When the part recovers from an overtemperature condition, the switchers will resume normal operation, if enabled, in the soft-start state.

To prevent an overtemperature condition, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$t_{RISE} = P_D \bullet \theta_{JA}$$

As an example, consider the case when the LTC7124 is used in applications where $V_{IN1,2}$ = 12V, $I_{OUT1,2}$ = 3A, f = 1MHz, and $V_{OUT1,2}$ = 1.8V. The equivalent power MOSFET resistance R_{SW} for both channels is:

$$R_{SW} = R_{DS(ON)TOP} \bullet \frac{V_{OUT}}{V_{IN}} + R_{DS(ON)BOT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$= 80m\Omega \bullet \frac{1.8V}{12V} + 40m\Omega \bullet \left(1 - \frac{1.8V}{12V}\right) = 46\ m\Omega$$

The V_{IN1} current during 1MHz forced continuous operation with no load is about 5mA, which includes switching and internal biasing current loss, transition loss, inductor core loss and other losses in the application. The total power dissipated by the part can then be calculated to be:

$$P_D = I_{OUT1}^2 \bullet R_{SW1} + I_{OUT2}^2 \bullet R_{SW2} + V_{IN1} \bullet I_{IN(Q)}$$

$$= 3A^2 \bullet 46m\Omega + 3A^2 \bullet 46m\Omega + 12V \bullet 5mA = 0.888W$$

The QFN 3mm × 5mm package junction to ambient temperature resistance, θ_{JA}, is around 22°C/W. Therefore, the junction temperature of the regulator operating in a 25°C ambient temperature environment is approximately:

$$T_J = 0.888W \bullet 22°C/W + 25°C = 44.5°C$$

Since the above calculation is dependent on the $R_{DS(ON)}$ at 25°C, the junction temperature rise can be recalculated to account for the positive temperature dependence of the $R_{DS(ON)}$. Assuming a 5% rise in the $R_{DS(ON)}$ at 44.5°C results in a slightly higher junction temperature of 45.5°C. If the application calls for a higher ambient temperature and/or higher switching frequency, care should be taken to reduce the temperature rise of the part by using a heat sink or forced air flow.

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC7124. Check the following in your layout:

1. Do the capacitors C_{IN1} and C_{IN2} connect to the V_{IN1} and V_{IN2} pins respectively and GND pins as close as possible? These capacitors provide the AC current to the internal power MOSFETs and their drivers.

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2. Are $C_{OUT1,2}$ and $L_{1,2}$ closely connected? The (–) plate of $C_{OUT1,2}$ returns current to GND.
3. The resistive divider, R1 and R2, of each channel must be connected between the (+) plate of C_{OUT} and a ground line terminated near GND. The feedback signals, V_{FB1} and V_{FB2}, should be routed away from noisy components and traces, such as the SW1 and SW2 lines, and their traces should be minimized. Keep R1 and R2 close to the IC.
4. Solder the exposed pad (Pin 25) on the bottom of the package to the GND plane. Connect this GND plane to the other layers with thermal vias to help dissipate heat from the LTC7124.
5. Keep sensitive components away from the SW1 and SW2 pins. The feedback resistors and $INTV_{CC}$ bypass capacitors should be routed away from the SW1 and SW2 traces and the inductors.
6. A ground plane is preferred.
7. Flood all unused areas of all layers with copper, which will help reduce the temperature rise of power components. The copper areas should be connected to GND. Please refer to Figure 3 for a sample PCB layout.

Design Example

As a design example, consider using the LTC7124 in an application with the following specifications:

$V_{IN1,2}$ = 10.8V to 13.2V

V_{OUT1} = 1.8V

V_{OUT2} = 3.3V

$I_{OUT1,2(MAX)}$ = 3.5A

$I_{OUT1,2(MIN)}$ = 0A

f_{SW} = 2.25MHz

Because efficiency and quiescent current is important at both high and low load currents, Burst Mode operation will be utilized. The I_{LIM} pin is grounded to allow for maximum output current on both channels.

To set a frequency of 2.25MHz, a 40.2k resistor is connected between the RT pin and GND based on Figure 2.

Based on the frequency, the inductor value for Channel 1 for 40% ripple current can be calculated as follows:

$$L_1 = \frac{1.8V}{(2.25MHz \bullet 1.4A)} \bullet \left(1 - \frac{1.8V}{13.2V}\right) = 0.49\mu H$$

A standard value of 0.47µH inductor would work well here. Using the same method for Channel 2 results in an inductor value of 0.75µH, use a standard value of 0.82µH inductor.

C_{OUT} is selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. Allowing for a V_{DROOP} of 5% • V_{OUT}, the output capacitance necessary for Channel 1 can be calculated thusly:

$$C_{OUT1} = \frac{3 \bullet 3.5A}{(2.25MHz \bullet 0.05 \bullet 1.8V)} = 52\mu F$$

A standard capacitance of 68µF or 100µF would work well here. Assuming the same V_{DROOP} for Channel 2 results in a calculated C_{OUT2} of 28µF. A standard capacitance of 33µF or 47µF would be suitable here.

The input capacitances C_{IN1} and C_{IN2} should be sized for a maximum current rating calculated from the I_{RMS} equation given previously. For Channel 1,

$$I_{RMS1} = 3.5A \bullet \frac{1.8V}{13.2V} \bullet \sqrt{\frac{13.2V}{1.8V} - 1} = 1.20A$$

Likewise, for Channel 2, I_{RMS2} is calculated to be 1.5A. Decoupling each V_{IN} pin with a 47µF capacitor is adequate for most applications.

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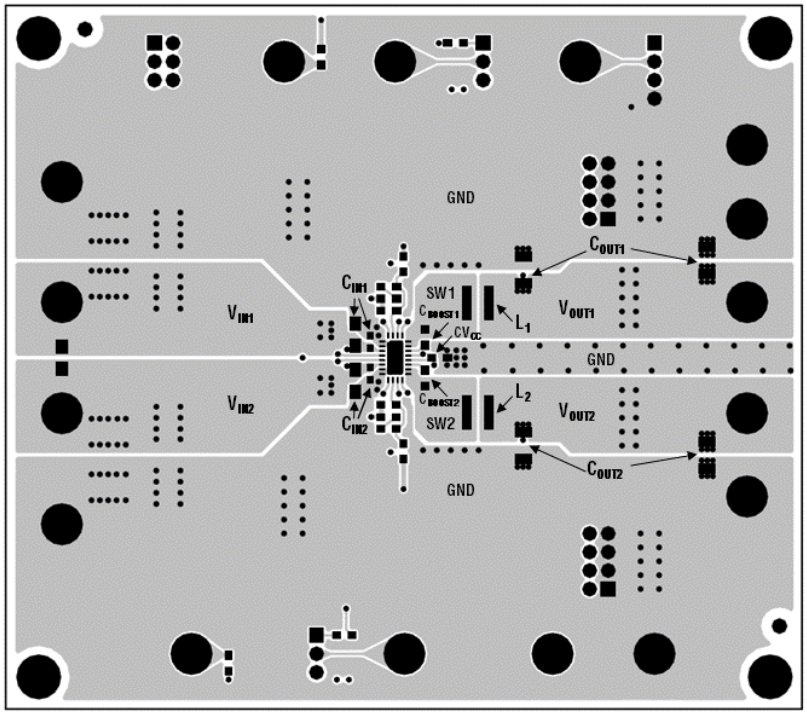
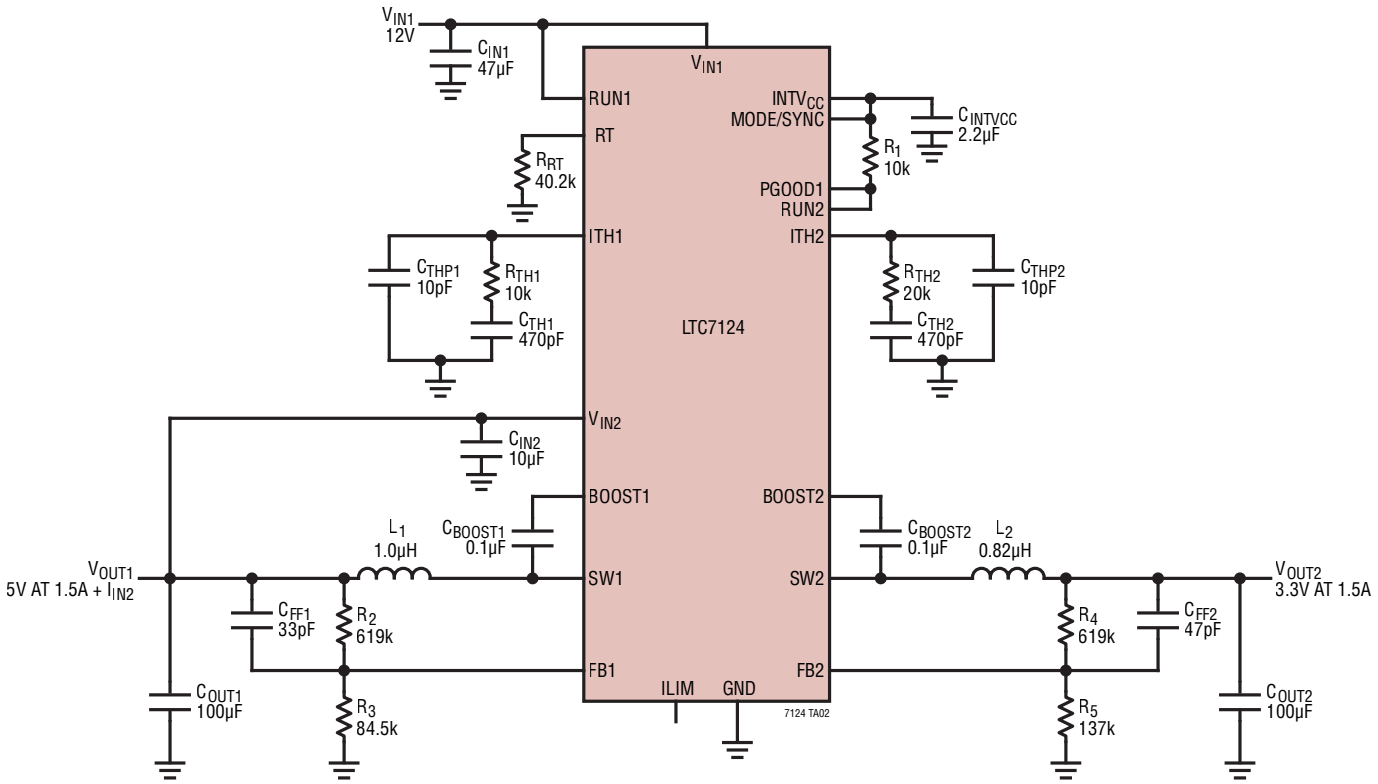


Figure 3. Sample PCB Layout

5V/3.3V Series Output 2.25MHz Step-Down Converter



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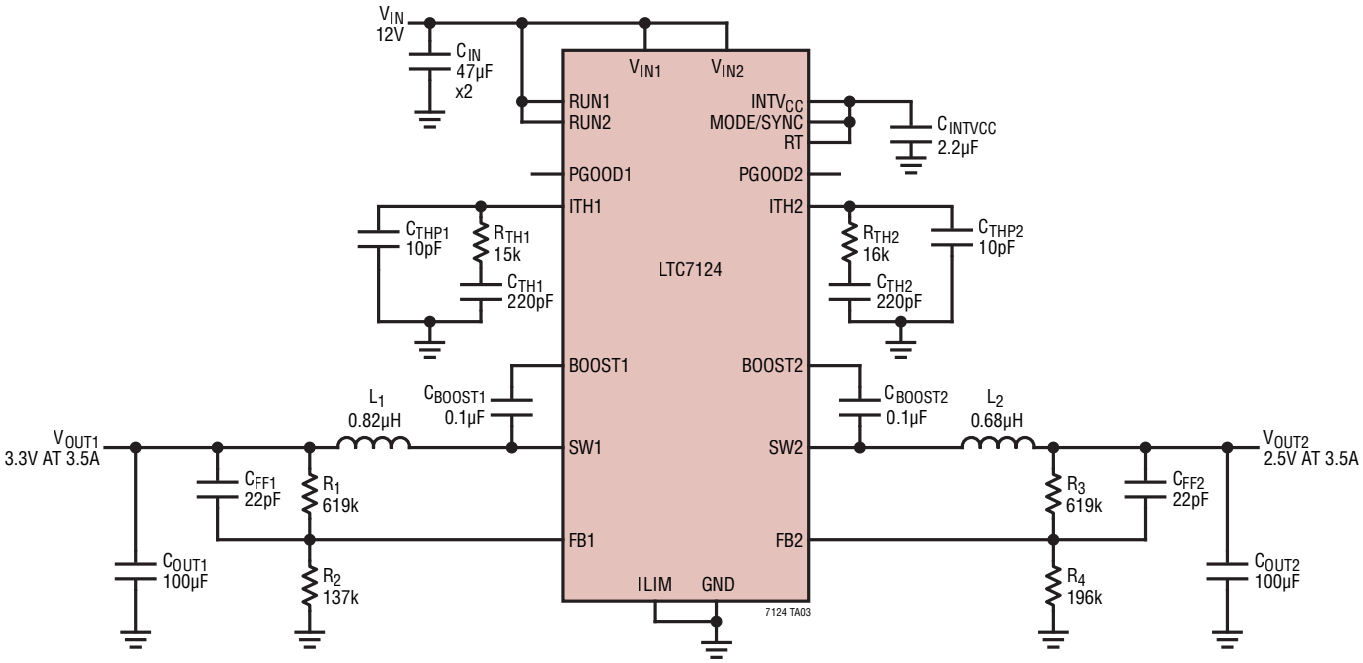
3.3V/2.5V Step-Down Regulator with Spread Spectrum



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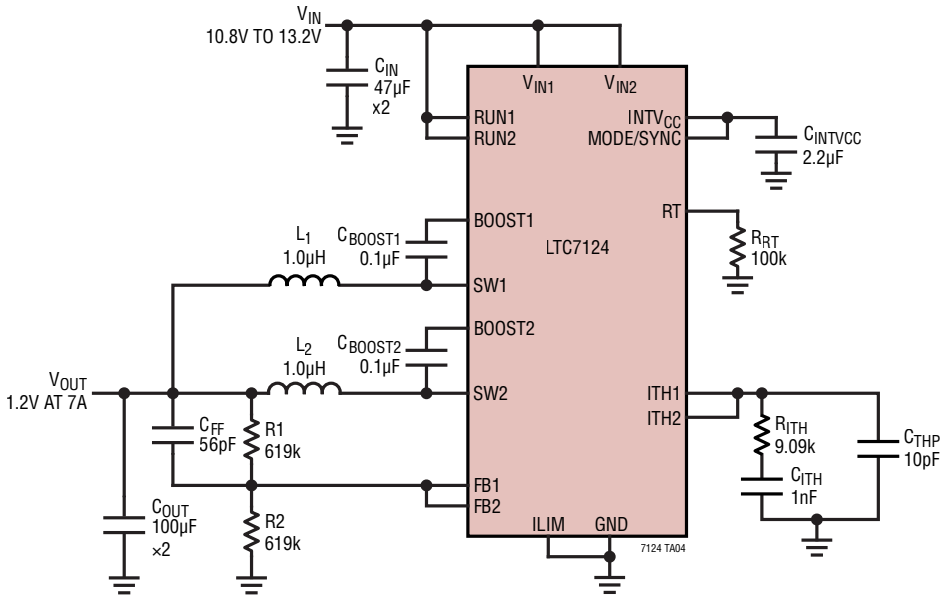
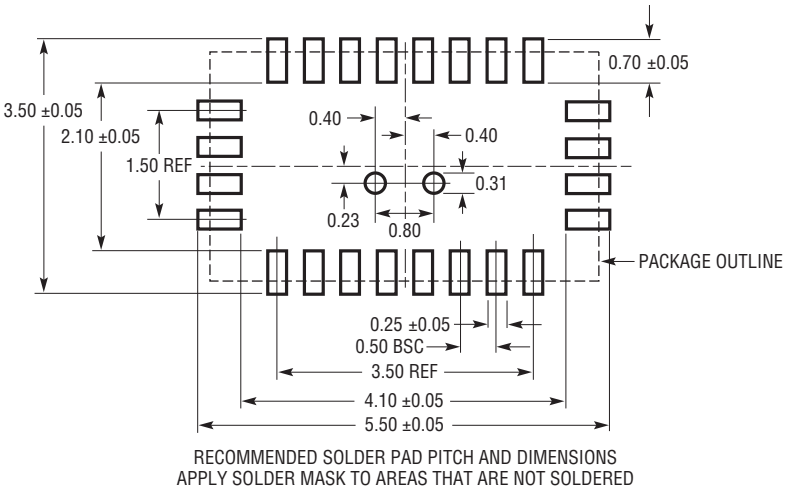
1.2V 1MHz Dual-Phase Single Output Step-Down Regulator



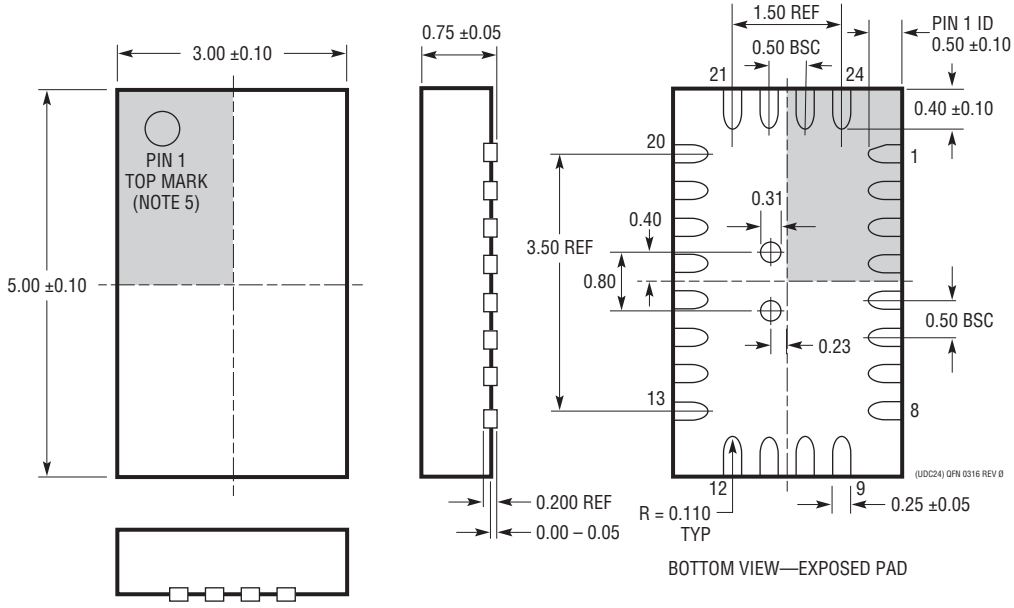
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC7124#packaging for the most recent package drawings.

UDD Package
24-Lead Plastic QFN (3mm × 5mm)
(Reference LTC DWG # 05-08-1537 Rev Ø)
Exposed Pad Variation AA



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

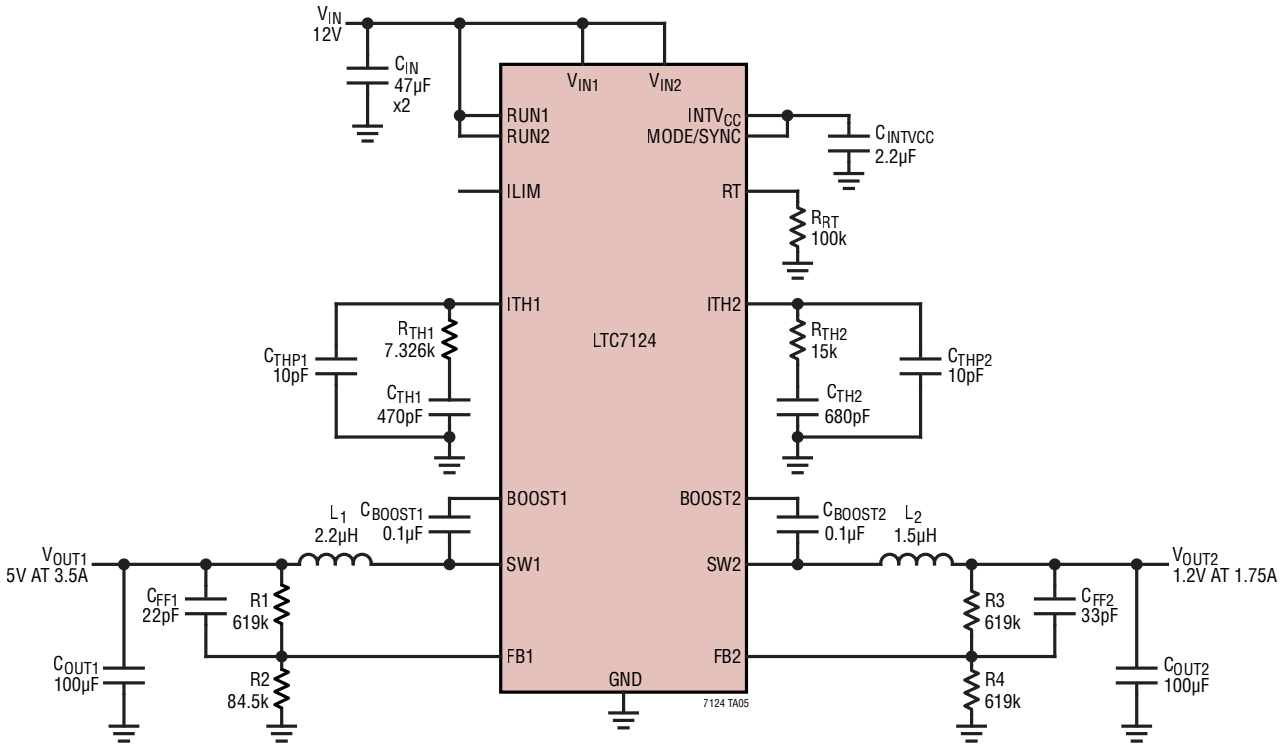
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/17	Electrical Characteristics comments – Changed to Note 3 Modified I_{LIM} Peak Current Limit values Modified Programming Switching Frequency section	3 3 11

TYPICAL APPLICATION

5V/1.2V 1MHz Step-Down Regulator with External Loop Compensation



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3621/ LTC3621-2	1A, 17V, 1/2.25MHz, Synchronous Step-Down Regulator	95% Efficiency, V_{IN}: 2.7V to 17V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 3.5µA, I_{SD} < 1µA, 2mm × 3mm DFN-6, MSOP-8E
LTC3622/ LTC3622-2/ LTC3622-23/5	Dual 1A, 17V 1MHz/2.25MHz Synchronous Step-Down Regulator	95% Efficiency, V_{IN}: 2.7V to 17V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 5µA, I_{SD} ≤ 1µA, 5mm × 4mm DFN-14 and 16-Lead MSOP Package
LTC3624/ LTC3624-2	2A, 17V, 1MHz/2.25MHz Synchronous Step-Down Regulator	95% Efficiency, V_{IN}: 2.7V to 17V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 3.5µA, I_{SD} < 1µA, 3mm × 3mm DFN-8 Package
LTC3636/ LTC3636-1	Dual Channel 6A, 20V Monolithic Synchronous Step-Down Regulator	95% Efficiency, V_{IN}: 3.1V to 20V, $V_{OUT(MIN)}$ = 0.6V (LTC3636), 1.8V (LTC3636-1), I_Q = 1.3mA, I_{SD} < 13µA, 4mm × 5mm QFN-28
LTC3633/ LTC3633A	15V/20V, Dual 3A (I_{OUT}), 4MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 500µA, I_{SD} < 13µA, 4mm × 5mm QFN-28, TSSOP-28E
LTC3616	6A, 4MHz Monolithic Synchronous Step-Down DC/DC Regulator	95% Efficiency, V_{IN}: 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 1.3mA, I_{SD} < 75µA, 3mm × 5mm QFN-24
LTC3605/ LTC3605A	15V/20V, 5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 2mA, I_{SD} < 15µA, 4mm × 4mm QFN-24
LTC3603	15V, 2.5A (I_{OUT}), 3MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 4mm × 4mm QFN-20, MSOP-16E
LTC3604	15V, 2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 15µA, 3mm × 3mm QFN-16, MSOP-16E
LTC3626	20V, 2.5A Synchronous Monolithic Step-Down Regulator with Current and Temperature Monitoring	95% Efficiency, V_{IN}: 3.6V to 20V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 15µA, 3mm × 4mm QFN-20

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