CS4350

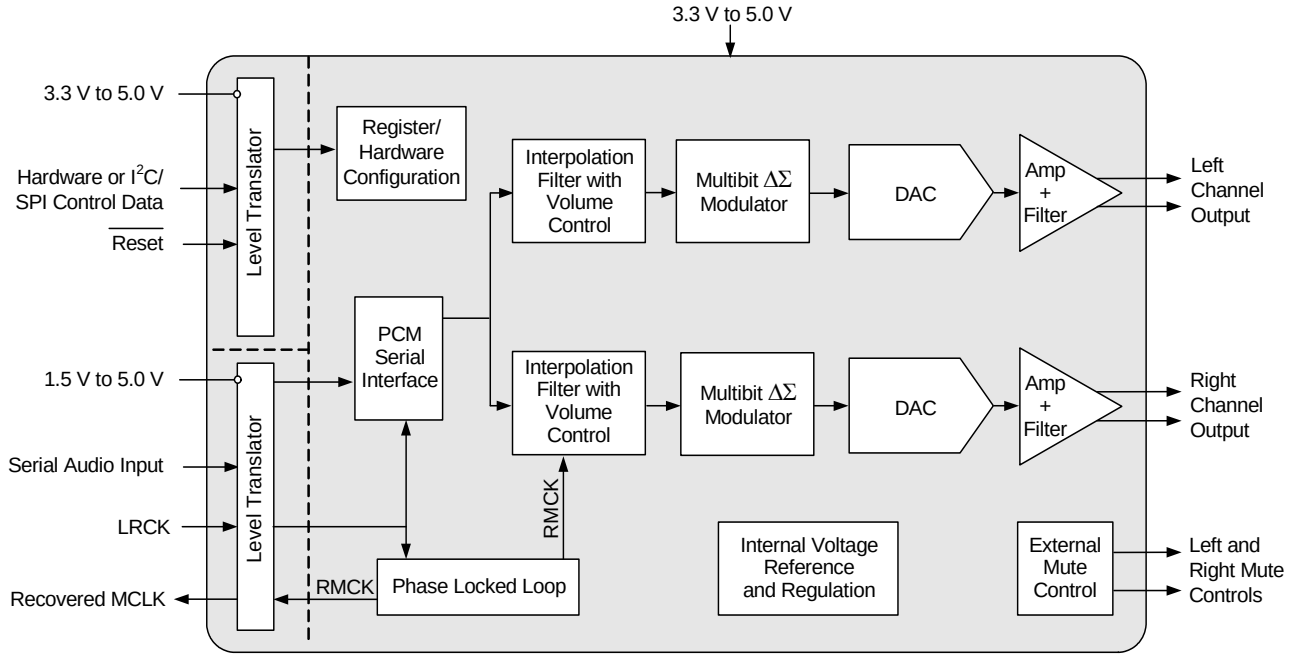
192-kHz Stereo DAC with Integrated PLL

Features

- Advanced multibit delta-sigma architecture
- 109-dB dynamic range
- -91-dB THD+N
- 24-bit conversion
- Supports audio sample rates up to 192 kHz
- Low-latency digital filtering
- Single-ended or differential analog output architecture
- Integrated PLL locks to incoming left-right clock
  - Eliminates the need for external master-clock routing
  - Reduces interference and jitter sensitivity
  - No external loop filter components required
- Automatic sample-rate range detection
- Popguard® technology for control of clicks and pops
- Hardware popguard disable for fast startups
- Supports all standard serial audio formats including time-division multiplexed (TDM)
- +1.5- to 5.0-V logic supplies for serial port
- +3.3- to 5.0-V control port interface

Control Port Mode Features

- SPI™ and I²C Modes
- ATAPI mixing
- Mute control for individual channels
- Digital volume control with soft ramp
  - 127.5-dB attenuation
  - 0.5-dB step size
  - Zero-crossing click-free transitions



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Description

The CS4350 is a complete stereo digital-to-analog system including PLL-based master clock derivation, digital interpolation, 5th-order multibit delta-sigma digital-to-analog conversion, digital de-emphasis, volume control, channel mixing, and analog filtering. The advantages of this architecture include ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature, high tolerance to clock jitter, and a minimal set of external components.

The CS4350 supports all standard digital audio interface formats, including TDM.

The CS4350 is available in a 24-pin QFN package in Commercial grade (-40° to +85°C).

The CS4350 is available in a 24-pin TSSOP package in both Commercial (-40° to +85°C) and Automotive grades (-40° to +105°C).

The CDB4350 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to “Ordering Information” on page 40 for complete ordering information.

These features are ideal for cost-sensitive, two-channel audio systems, including DVD players and recorders, set-top boxes, digital TVs, mini-component systems, mixing consoles and automotive audio systems.

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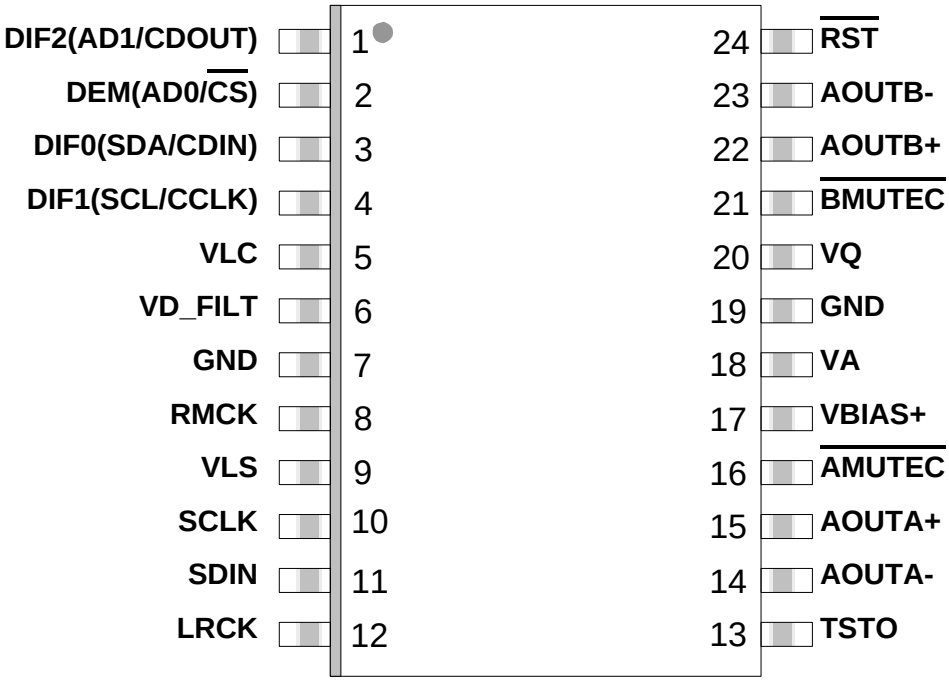
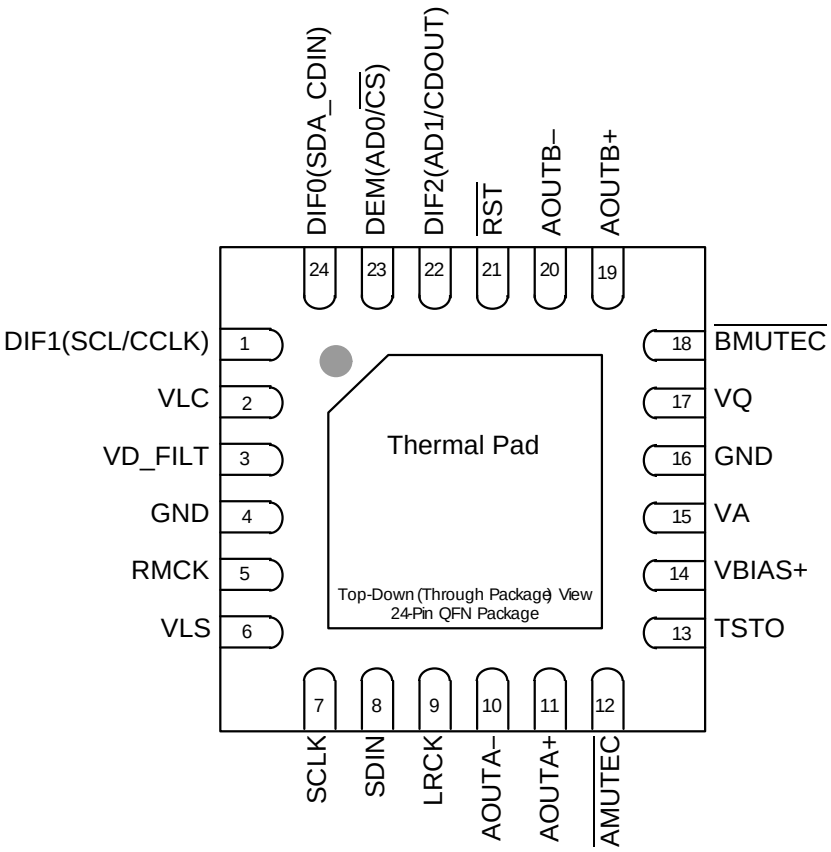
1 PIN DESCRIPTION

1.1 TSSOP Pinout



1.2 QFN Pinout



Pin Name	TSSOP #	QFN #	Pin Description
VLC	5	2	**Control Interface Power** (*Input*) **-** Positive power for the hardware/software control interface
VD_FILT	6	3	**Regulator Voltage** (*Output*) - Filter connection for internal voltage regulator
GND	7, 19	4,16	**Ground** (*Input*) - Ground reference
RMCK	8	5	**Recovered Master Clock** (*Output*) - Outputs a master clock derived from LRCK
VLS	9	6	**Serial Audio Interface Power** (*Input*) **-** Positive power for the serial audio interface
SCLK	10	7	**Serial Clock** (*Input*) - Serial bit-clock for the serial audio interface
SDIN	11	8	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data
LRCK	12	9	**Left/Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line
TSTO	13	13	**Test Output** - These pins need to be floating and not connected to any trace or plane.
AOUTA+,- AOUTB+,-	14, 15, 22, 23	11, 10 19, 20	**Differential Analog Outputs** (*Output*) - The full-scale differential output level is specified in "DAC Analog Characteristics - Commercial (-CZZ,-CNZ)" on page 9.
$\overline{\text{AMUTEC}}$ $\overline{\text{BMUTEC}}$	16, 21	12 18	**Mute Control** (*Output*) - Control signals for optional mute circuit.
VBIAS+	17	14	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal DAC
VA	18	15	**Analog Power** (*Input*) **-** Positive power supply for the analog section
VQ	20	17	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage
$\overline{\text{RST}}$	24	21	**Reset** (*Input*) - When pulled low, device will power down and reset all internal registers to their default settings.
Control Port Definitions			
AD1/CDOUT	1	22	**Address Bit 1/Serial Control Data Out** (*I/O*) - Chip address bit 1 in I²C Mode or data output in SPI Mode
AD0/$\overline{\text{CS}}$	2	23	**Address Bit 0/Chip Select** (*Input*) - Chip address bit 0 in I²C Mode or Chip Select in SPI Mode
SDA/CDIN	3	24	**Serial Control Data In** (*I/O*) - Input/Output for I²C data. Input for SPI data
SCL/CCLK	4	1	**Serial Control Port Clock** (*Input*) - Serial clock for the control port interface
Stand-Alone Definitions			
DIF0 DIF1 DIF2	1 3 4	24 1 22	**Digital Interface Format** (*Input*) - Defines the required relationship between the Left Right Clock, Serial Clock, and Serial Audio Data
DEM	2	23	**De-emphasis** (*Input*) - Selects the standard 15 µs/50 µs digital de-emphasis filter response for 44.1 kHz sample rates
Thermal Pad *(QFN package only)*			
Thermal Pad	n/a	—	Thermal relief pad for optimized heat dissipation. See "QFN Thermal Pad" on page 40 for more information.

2 CHARACTERISTICS AND SPECIFICATIONS

2.1 Recommended Operating Conditions

GND = 0 V; all voltages with respect to ground.

Table 1. Recommended Operating Conditions

Parameters		Symbol	Min	Typ	Max	Units
DC Power Supply	Analog power	VA	4.75	5.0	5.25	V
			3.14	3.3	3.46	V
	Serial Audio Interface power(Note 1)	VLS	1.35	3.3	5.25	V
	Control Interface power	VLC	3.14	3.3	5.25	V
Ambient Operating Temperature (Power Applied)						
	Commercial (-CZZ,-CNZ)	T_A	-40	-	+85	°C
	Automotive (-DZZ)	T_A	-40	-	+105	°C

Notes: 1. RMCK output frequency is dependent on VLS.
See Table 6 for supported RMCK frequencies with respect to VLS.

2.2 Absolute Maximum Ratings

GND = 0 V; all voltages with respect to ground (Note 2).

Table 2. Absolute Maximum Ratings

Parameters		Symbol	Min	Max	Units
DC Power Supply	Analog power	VA	-0.3	6.0	V
	Serial Audio Interface power	VLS	-0.3	6.0	V
	Control Interface power	VLC	-0.3	6.0	V
Input Current	(Note 3)	I_{in}	-	±10	mA
Digital Input Voltage	Serial Audio Interface	V_{IN-LS}	-0.3	VLS+ 0.4	V
Control Interface		V_{IN-LC}	-0.3	VLC+ 0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 2. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

3. Any pin except supplies.

2.3 DAC Analog Characteristics - Commercial (-CZZ,-CNZ)

Test conditions (unless otherwise specified): VLS = VLC = 3.3 V; T_A = 25° C; Input test signal is a 997 Hz sine wave; Valid with the recommended capacitor values on VD_FILT, VQ, VBIAS (as shown in the typical connection diagram in Figure 10) and output circuits as shown in Figure 17 and Figure 18; Fs = 48 kHz, 96 kHz, and 192 kHz; measurement bandwidth 10 Hz to 20 kHz.

Table 3. DAC Analog Characteristics - Commercial (-CZZ,-CNZ)

Parameter			Symbol	Min	Typ	Max	Unit
VA= 5.0 V				**Single-ended/Differential**			
Dynamic Range (Note 4)	24-bit	A-Weighted		98/106	101/109	-	dB
		unweighted		95/103	98/106	-	dB
	16-bit	A-Weighted		-	95/96	-	dB
		unweighted		-	92/93	-	dB
Total Harmonic Distortion + Noise (Note 4)				-			
	24-bit	0 dB		-	-91	-86/-87	dB
		-20 dB		-	-78/-86	-	dB
		-60 dB	THD+N	-	-38/-46	-35/-43	dB
	16-bit	0 dB		-	-90	-	dB
		-20 dB		-	-72/-73	-	dB
		-60 dB		-	-32/-33	-	dB
VA= 3.3 V				**Single-ended/Differential**			
Dynamic Range (Note 4)	24-bit	A-Weighted		98/106	101/109	-	dB
		unweighted		95/103	98/106	-	dB
	16-bit	A-Weighted		-	95/96	-	dB
		unweighted		-	92/93	-	dB
Total Harmonic Distortion + Noise (Note 4)							
	24-bit	0 dB		-	-86	-77	dB
		-2 dB		-	-91/-93	-	dB
		-20 dB	THD+N	-	-78/-86	-	dB
		-60 dB		-	-38/-46	-35/-43	dB
	16-bit	0 dB		-	-83	-	dB
		-20 dB		-	-72/-73	-	dB
		-60 dB		-	-32/-33	-	dB
VA= 3.3 to 5.0 V							
Interchannel Isolation		(1 kHz)		-	100	-	dB
DC Accuracy							
Interchannel Gain Mismatch				-	0.1	0.25	dB
Gain Drift				-	-400	-	ppm/°C
Analog Output							
Full Scale Output Voltage - Single Ended		-CZZ		2.61	2.78	2.96	Vpp
		-CNZ		2.45	2.59	2.91	Vpp
Full Scale Output Voltage - Differential		-CZZ		5.22	5.56	5.92	Vpp
		-CNZ		4.90	5.18	5.82	Vpp
Quiescent Voltage			V_Q	-	0.5•VA	-	VDC
Max DC Current draw from an AOUT pin			I_{OUTmax}	-	10	-	µA
Max Current draw from VQ			I_{Qmax}	-	100	-	µA
Max AC-Load Resistance		(Note 5)	R_L	-	3	-	kΩ
Max Load Capacitance		(Note 5)	C_L	-	100	-	pF
Output Impedance			Z_{OUT}	-	100	-	Ω

Notes: 4. One LSB of triangular PDF dither is added to data

5. R_L and C_L represent the minimum resistance and maximum capacitance required for the CS4350's internal op-amp to remain stable. See Figure 1 and Figure 2 for more details.

2.4 DAC Analog Characteristics - Automotive (-DZZ)

Test conditions (unless otherwise specified): VLS = 1.35 V to 5.25 V, VLC = 3.14 V to 5.25 V, T_A = -40° C to 105° C, input test signal is a 997 Hz sine wave; Valid with the recommended capacitor values on VFILT, VQ, VBIAS (as shown in the typical connection diagram in Figure 10) and output circuits as shown in Figure 17 and Figure 18; Fs = 48 kHz, 96 kHz, and 192 kHz; Measurement bandwidth 10 Hz to 20 kHz.

Table 4. DAC Analog Characteristics - Automotive (-DZZ)

Parameter			Symbol	Min	Typ	Max	Unit
VA= 4.75 V to 5.25 V				**Single-ended/Differential**			
Dynamic Range (Note 4)	24-bit	A-Weighted		95/103	101/109	-	dB
		unweighted		92/100	98/106	-	dB
	16-bit	A-Weighted		-	95/96	-	dB
		unweighted		-	92/93	-	dB
Total Harmonic Distortion + Noise (Note 4)				-			
	24-bit	0 dB		-	-91	-85	dB
		-20 dB		-	-78/-86	-	dB
		-60 dB	THD+N	-	-38/-46	-32/-40	dB
	16-bit	0 dB		-	-90	-	dB
		-20 dB		-	-72/-73	-	dB
		-60 dB		-	-32/-33	-	dB
VA= 3.14 V to 3.46 V				**Single-ended/Differential**			
Dynamic Range (Note 4)	24-bit	A-Weighted		94/103	101/109	-	dB
		unweighted		91/100	98/106	-	dB
	16-bit	A-Weighted		-	95/96	-	dB
		unweighted		-	92/93	-	dB
Total Harmonic Distortion + Noise (Note 6)							
	24-bit	-1 dB		-	-89	-83	dB
		-2 dB		-	-91/-93	-	dB
		-20 dB	THD+N	-	-78/-86	-	dB
		-60 dB		-	-38/-46	-31/-40	dB
	16-bit	0 dB		-	-83	-	dB
		-20 dB		-	-72/-73	-	dB
		-60 dB		-	-32/-33	-	dB
VA= 3.14 to 5.25 V							
Interchannel Isolation		(1 kHz)		-	100	-	dB
DC Accuracy							
Interchannel Gain Mismatch				-	0.1	0.25	dB
Gain Drift				-	-400	-	ppm/°C
Analog Output							
Full Scale Output Voltage - Single Ended				2.55	2.78	3.03	Vpp
Full Scale Output Voltage - Differential				5.10	5.56	6.06	Vpp
Quiescent Voltage			V_Q	-	0.5•VA	-	VDC
Max DC Current draw from an AOUT pin			I_{OUTmax}	-	10	-	µA
Max Current draw from VQ			I_{Qmax}	-	100	-	µA
Max AC-Load Resistance		(Note 5)	R_L	-	3	-	kΩ
Max Load Capacitance		(Note 5)	C_L	-	100	-	pF
Output Impedance			Z_{OUT}	-	100	-	Ω

Note: 6. One-half LSB of triangular PDF dither is added to data. Also, see Figure 3, Figure 4, and Figure 5 for more details on the CS4350-DZZ THD+N performance with 0dB input signal.

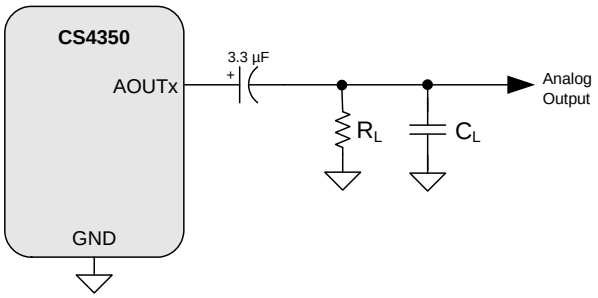


Figure 1. Equivalent Output Load

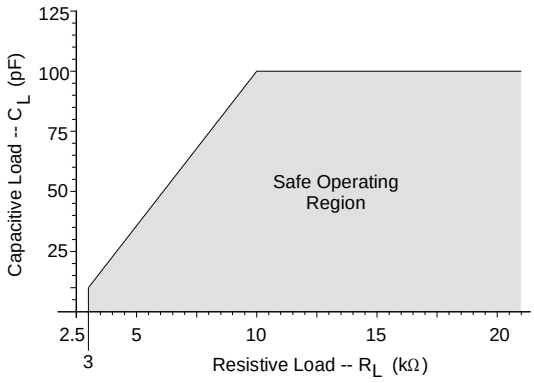


Figure 2. Maximum Loading

Figures 3 through 5 show typical THD+N performance for CS4350 devices that exhibit the maximum full scale output voltages as specified in the DAC Analog Characteristics tables (see page 9 and 10). With decreasing VA, THD+N performance is increasingly affected by the full scale output voltage and temperature, with higher full scale output voltage and lower temperatures corresponding to lower THD+N performance.

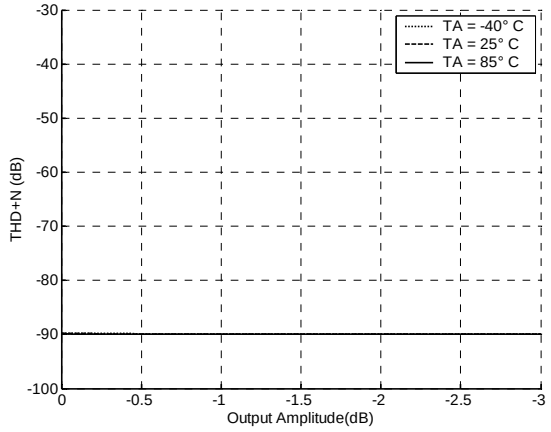


Figure 3. THD+N vs Output Amplitude for VA = 5.0 V

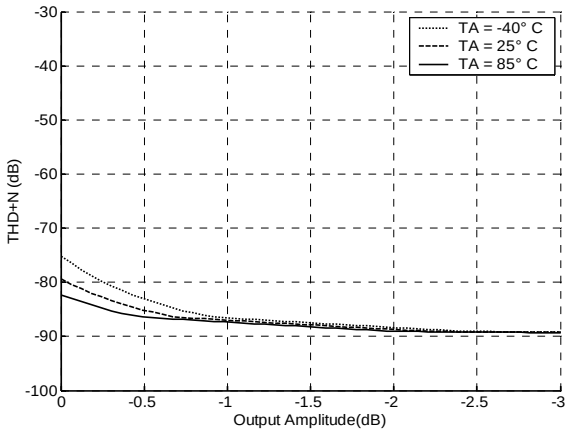


Figure 4. THD+N vs Output Amplitude for VA = 3.3 V

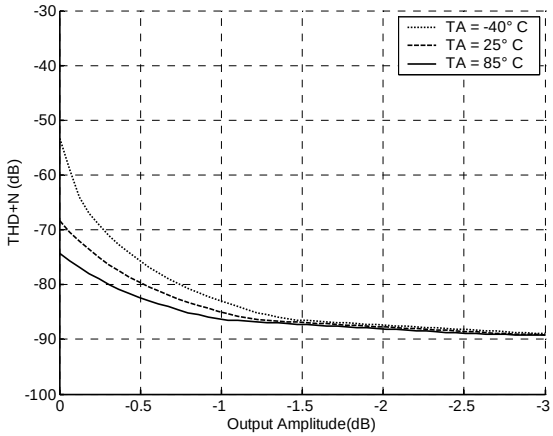


Figure 5. THD+N vs Output Amplitude for VA = 3.14 V

2.5 Combined Interpolation and On-Chip Analog Filter Response

The filter characteristics have been normalized to the sample rate (Fs) and is referenced to the desired sample rate by multiplying the given characteristic by Fs. Amplitude vs. Frequency plots of this data are available in the "Filter Plots" on page 36.

Table 5. Combined Interpolation and On-Chip Analog Filter Response

Parameter		Min	Typ	Max	Unit
Fast Roll-Off					
Passband (Note 7)	-0.01 dB corner (Single Speed)	0	-	.454	Fs
	-0.1 dB corner (Double Speed)	0	-	.42	Fs
	-0.2 dB corner (Quad Speed)	0	-	.27	Fs
	-3 dB corner (All Speed Modes)	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz	Single Speed	-0.01	-	+0.01	dB
	Double Speed, Quad Speed	-0.02	-	+0.02	dB
StopBand		0.547	-	-	Fs
Stop-Band Attenuation (Note 8)		102	-	-	dB
Total Group Delay (Fs - Output Sample Rate)	TDM Slot 0 Channel B	-	8.4/Fs	-	s
	All Other Interface Formats and TDM Slots/Channels	-	9.4/Fs	-	s
Intrachannel Phase Deviation		-	-	±0.56/Fs	s
Interchannel Phase Deviation		-	-	0	s
De-emphasis Error (Note 9)	Fs = 32 kHz	-	-	±0.23	dB
(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	dB
Slow Roll-Off (Note 10)					
Passband (Note 7)	-0.01 dB corner (Single Speed)	0	-	0.417	Fs
	-0.1 dB corner (Double Speed)	0	-	.37	Fs
	-0.2 dB corner (Quad Speed)	0	-	.27	Fs
	-3 dB corner (All Speed Modes)	0	-	.499	Fs
Frequency Response 10 Hz to 20 kHz	Single Speed	-0.01	-	+0.01	dB
	Double Speed, Quad Speed	-0.02	-	+0.02	dB
StopBand		.583	-	-	Fs
Stop-Band Attenuation (Note 8)		64	-	-	dB
Total Group Delay (Fs - Output Sample Rate)	TDM Slot 0 Channel B	-	5.5/Fs	-	s
	All Other Interface Formats and TDM Slots/Channels	-	6.5/Fs	-	s
Intrachannel Phase Deviation		-	-	±0.14/Fs	s
Interchannel Phase Deviation		-	-	0	s
De-emphasis Error (Note 9)	Fs = 32 kHz	-	-	±0.23	dB
(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.14	dB
	Fs = 48 kHz	-	-	±0.09	dB

Notes: 7. Response is clock dependent.

8. The Measurement Bandwidth is from stopband to 3 Fs.
9. De-emphasis is available only in Single-Speed Mode; Only 44.1 kHz De-emphasis is available in Stand-Alone Mode.
10. Slow Roll-off interpolation filter is only available in Control Port Mode.

2.6 Switching Specifications - Serial Audio Interface

Inputs: Logic 0 = GND; Logic 1 = VLS; C_L = 20 pF.

Table 6. Switching Specifications - Serial Audio Interface

Parameters		Symbol	Min	Max	Units
RMCK Output Frequency (Note 11)	VLS=1.5 V nominal		Unsupported		MHz
	VLS=1.62 V or above		7.680	16.896	MHz
	VLS=2.97 V or above		7.680	55.3	MHz
3.14 V ≤ VA ≤ 5.25 V and 1.35 V ≤ VLS ≤ 5.25 V					
RMCK Output Duty Cycle			45	55	%
Input Sample Rate	Single-Speed Mode		30	54	
	Double-Speed Mode	Fs	60	108	kHz
	Quad-Speed Mode		120	216	
LRCK Duty Cycle (Non-TDM Mode)			40	60	%
SDIN Setup Time Before SCLK Rising Edge		t_{ds}	1	-	ns
SDIN Hold Time After SCLK Rising Edge		t_{dh}	8	-	ns
4.75 V ≤ VA ≤ 5.25 V and 3.14 V ≤ VLS ≤ 5.25 V					
SCLK Frequency			-	55.3	MHz
SCLK High Time		t_{sckh}	6	-	ns
SCLK Low Time		t_{sckl}	6	-	ns
Non-TDM Mode (refer to Figure 6)					
LRCK Edge to SCLK Rising Edge		t_{lcks}	11	-	ns
SCLK Rising Edge to LRCK Edge		t_{lckd}	1	-	ns
TDM Mode (refer to Figure 7)					
LRCK High Time		t_{lrckh}	20	-	ns
SCLK Rising to LRCK Falling Edge		t_{fsh}	3	-	ns
LRCK Rising Edge to SCLK Rising Edge		t_{fss}	1	-	ns
3.14 V ≤ VA < 4.75 V or 1.35 V ≤ VLS < 3.14 V					
SCLK Frequency			-	27.7	MHz
SCLK High Time		t_{sckh}	11	-	ns
SCLK Low Time		t_{sckl}	11	-	ns
Non-TDM Mode (refer to Figure 6)					
LRCK Edge to SCLK Rising Edge		t_{lcks}	16	-	ns
SCLK Rising Edge to LRCK Edge		t_{lckd}	1	-	ns
TDM Mode (refer to Figure 7)					
LRCK High Time		t_{lrckh}	25	-	ns
SCLK Rising to LRCK Falling Edge		t_{fsh}	8	-	ns
LRCK Rising Edge to SCLK Rising Edge		t_{fss}	1	-	ns

Note: 11. RMCK output frequency depends on the input LRCK frequency. See Section 4.1 and Section 4.2 for more details.

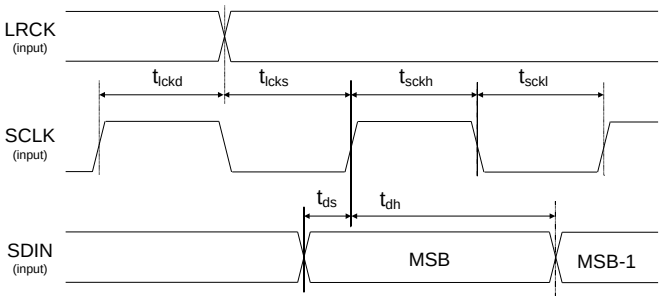


Figure 6. Serial Port Timing, Non-TDM Mode

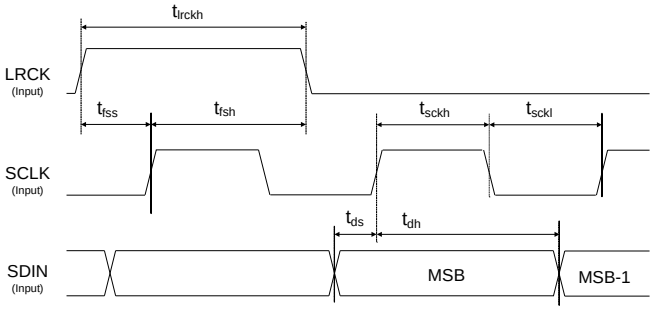


Figure 7. Serial Port Timing, TDM Mode

2.7 Switching Characteristics - Control Port - I²C Format

Inputs: Logic 0 = GND; Logic 1 = VLC; C_L = 20 pF.

Table 7. Switching Characteristics - Control Port - I²C Format

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RST}}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 12)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}, t_{rc}	-	1	µs
Fall Time SCL and SDA	t_{fc}, t_{fc}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

Note: 12. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

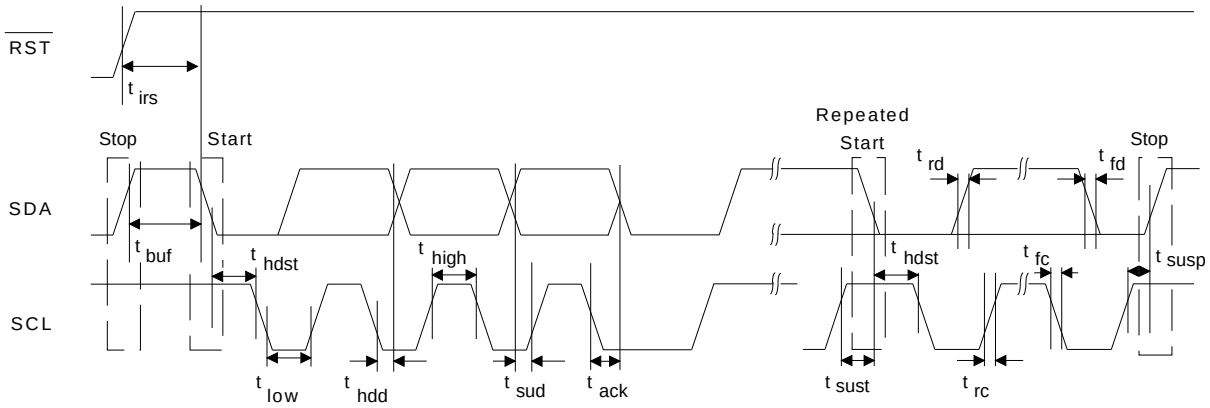


Figure 8. Control Port Timing - I²C Format

2.8 Switching Characteristics - Control Port - SPI Format

Inputs: Logic 0 = GND; Logic 1 = VLC; C_L = 20 pF.

Table 8. Switching Characteristics - Control Port - SPI Format

Parameter	Symbol	Min	Max	Unit
CCLK Clock Frequency	f_{sclk}	-	6	MHz
$\overline{RST}$ Rising Edge to $\overline{CS}$ Falling	t_{srs}	500	-	ns
CCLK Edge to $\overline{CS}$ Falling (Note 13)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions	t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge	t_{css}	20	-	ns
CCLK Low Time	t_{scl}	66	-	ns
CCLK High Time	t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time (Note 14)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN (Note 15)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN (Note 15)	t_{f2}	-	100	ns
Transition Time from CCLK to CDOUT Valid (Note 16)	t_{scdov}	-	100	ns
Time from $\overline{CS}$ rising to CDOUT High-Z	t_{cscdo}	-	100	ns

Notes: 13. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

14. Data must be held for sufficient time to bridge the transition time of CCLK.
15. For F_{SCK} < 1 MHz.
16. CDOUT should *not* be sampled during this time.

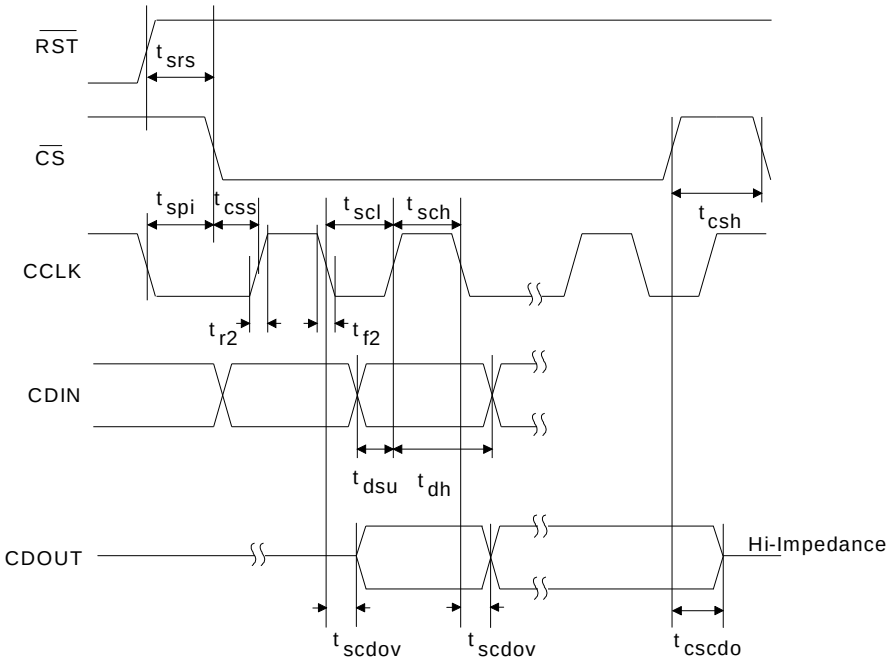


Figure 9. Control Port Timing - SPI Mode

2.9 Digital Characteristics

Table 9. Digital Characteristics

Parameters		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	VLC or VLS = 5.0 V	V_{IH}	0.7•V_L	-	-	V
	VLC or VLS = 3.3 V	V_{IH}	2.0	-	-	V
	VLS = 2.5 V	V_{IH}	1.7	-	-	V
	VLS = 1.5 V	V_{IH}	0.75•V_L	-	-	V
Low-Level Input Voltage	VLC or VLS = 5.0 V	V_{IL}	-	-	0.35•V_L	V
	VLC or VLS = 3.3 V	V_{IL}	-	-	0.8	V
	VLS = 2.5 V	V_{IL}	-	-	0.7	V
	VLS = 1.5 V	V_{IL}	-	-	0.25•V_L	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF
High Level Output Voltage (RMCK) I_O = 2 mA (VLS ≥ 3.0V)		V_{OH}	VLS-1.0	-	-	V
Low Level Output Voltage (RMCK) I_O = -2 mA (VLS ≥ 3.0V)		V_{OL}	-	-	0.4	V
RMCK Output Load Drive			-	-	10	pF
Maximum MUTEC Drive Current			-	2	-	mA
MUTEC High-Level Output Voltage		V_{OH}	-	VA	-	V
MUTEC Low-Level Output Voltage		V_{OL}	-	0	-	V

2.10 Power and Thermal Characteristics

Table 10. Power and Thermal Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Power Supply Current - Normal Operation (Note 17)	VA= 5.0 V	I_A	-	28	34	mA
	VA= 3.3 V	I_A	-	24	29	mA
	VLS = VLC =5.0 V (Note 18)	I_{LS}	-	4	6	mA
	VLS = VLC =3.3 V (Note 18)	I_{LS}	-	2	5	mA
	VLS = VLC = 5.0 V (Note 19)	I_{LC}	-	14	18	mA
	VLS = VLC = 3.3 V (Note 19)	I_{LC}	-	14	18	mA
Power Supply Current - Power-Down State (Note 20)	VA, VLS, VLC	I_{pd}	-	100	-	µA
Power Dissipation - Normal Operation (Note 17)						
	VA = VLC= VLS = 5.0 V		-	230	290	mW
	VA = VLC= VLS = 3.3 V		-	132	171	mW
Power Dissipation - Power-Down State (Note 20)						
	VA = VLC= VLS = 5.0 V		-	0.5	-	mW
	VA = VLC= VLS = 3.3 V		-	0.33	-	mW
Power Supply Rejection Ratio (Note 21)	(1 kHz)	PSRR	-	60	-	dB
	(60 Hz)	PSRR	-	50	-	dB

Notes: 17. Current consumption increases with increasing Fs within the range of a speed mode. Variance between speed modes is small. Typ and Max values are based on Fs = 48 kHz.

18. I_{LS} measured with no external loading on pin 7 (RMCK).

19. I_{LC} measured with no external loading on pin 2 (SDA).

20. Power-down mode is defined as $\overline{RST}$ pin = Low with all clock and data lines held static.

21. Valid with the recommended capacitor values on VFILT, VQ, and VBIAS+ as shown in the typical connection diagram in Figure 10.

3 TYPICAL CONNECTION DIAGRAM

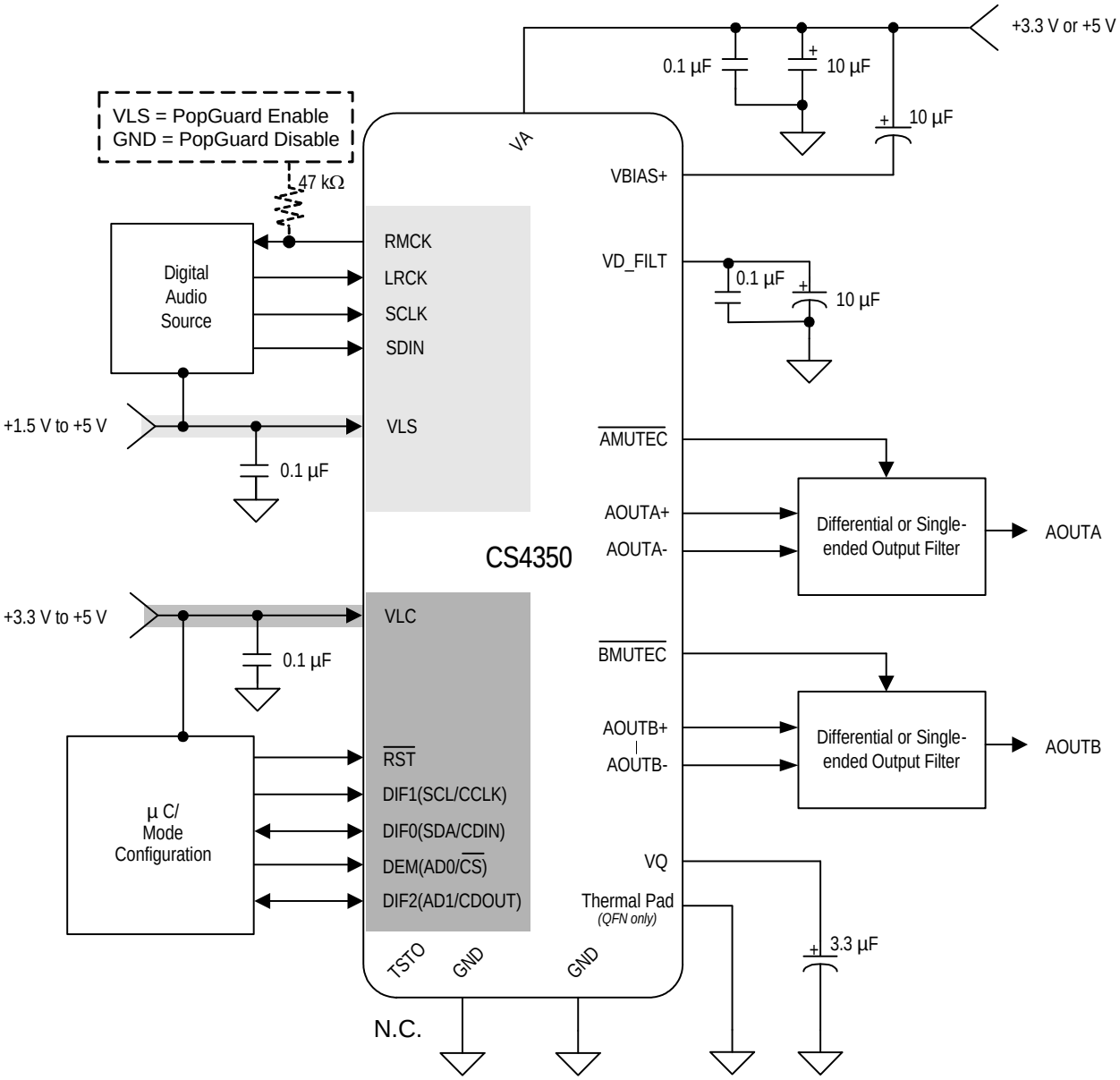


Figure 10. Typical Connection Diagram

4 APPLICATIONS

4.1 Sample Rate Range and Oversampling Mode Detect

The device operates in one of three oversampling modes based on the input sample rate. In Control Port Mode, the allowed sample rate range in each mode will depend on how the FM[1:0] bits are configured. In Stand-Alone Mode, the sample rate range will be according to Table 11.

4.1.1 Sample Rate Auto-Detect

The Auto-Detect feature is enabled by default. In this state, the CS4350 will auto-detect the correct mode when the input sample rate (Fs), defined by the LRCK frequency, falls within one of the ranges shown in Table 11. Sample rates outside the specified range for each mode are not supported when Auto-Detect is enabled.

Table 11. CS4350 Auto-Detect

Input Sample Rate (Fs)	Mode
30 kHz - 54 kHz	Single-Speed Mode
60 kHz - 108 kHz	Double-Speed Mode
120 kHz - 216 kHz	Quad-Speed Mode

In Control Port Mode, the Auto-Detect feature can be disabled by the Functional Mode (FM[1:0]) bits in the control port register 02h. In this state, the CS4350 will not auto-detect the correct mode based on the input sample rate (Fs). The operational mode must then be set manually according to one of the ranges referred to in Section 8.2.3. Sample rates outside the specified range for each mode are not supported. In Stand-Alone Mode it is not possible to disable auto-detect of sample rates.

4.2 System Clocking

The device requires external generation of the left/right (LRCK) and serial (SCLK) clocks. The left/right clock frequency is equal to the input sample rate (Fs).

Refer to Section 4.3 for the required SCLK-to-LRCK timing associated with the selected digital interface format, and “Switching Specifications - Serial Audio Interface” on page 13 for the maximum allowed clock frequencies.

4.2.1 Recovered Master Clock (RMCK)

The CS4350 generates a high-frequency master clock (RMCK) which it derives from the LRCK input, available on the RMCK pin. In Stand-Alone Mode, the frequency of RMCK is equal to 256 x LRCK in Single-Speed and Double-Speed Mode; and 128 x LRCK in Quad-Speed Mode. In Control-Port Mode, the frequency of the RMCK signal can be selected through register 08h (see Section 8.7 on page 34 for more details).

4.3 Digital Interface Format

The device will accept audio samples in 1 of 8 digital interface formats, as shown in Table 12 on page 24 for Stand-Alone Mode and Table 13 on page 29 for Control Port Mode.

The desired serial audio interface format is selected via the DIF[2:0] bits in Control Port Mode (see Section 8.2.1), or the DIF[2:0] pins in Stand-Alone Mode (see Section 5.1). For illustrations of the required relationship between LRCK, SCLK and SDIN, see Figures 11-13. For all formats, SDIN is valid on the rising edge of SCLK.

For more information about serial audio formats, refer to the Cirrus Logic Application Note AN282, *The 2-Channel Serial Audio Interface: A Tutorial*, available at www.cirrus.com.

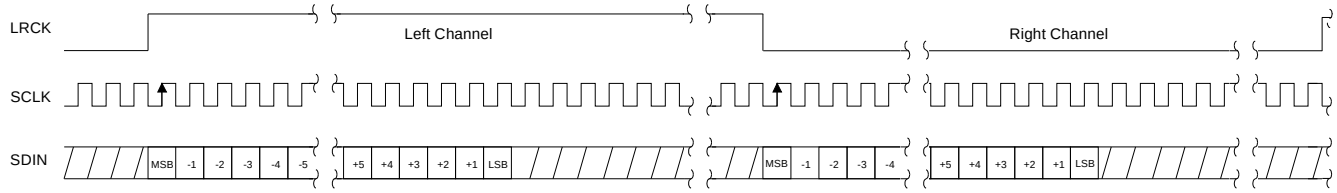


Figure 11. Left-Justified up to 24-Bit Data

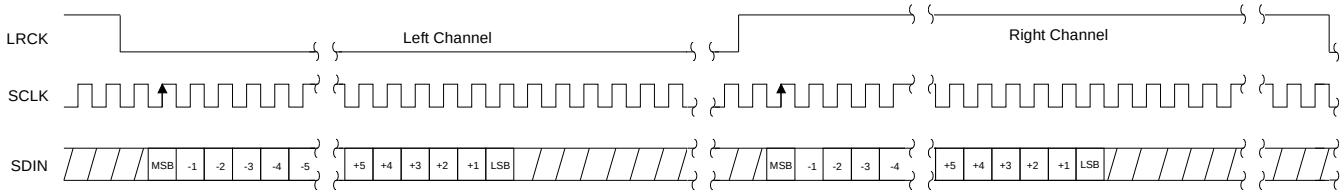


Figure 12. I²S, up to 24-Bit Data

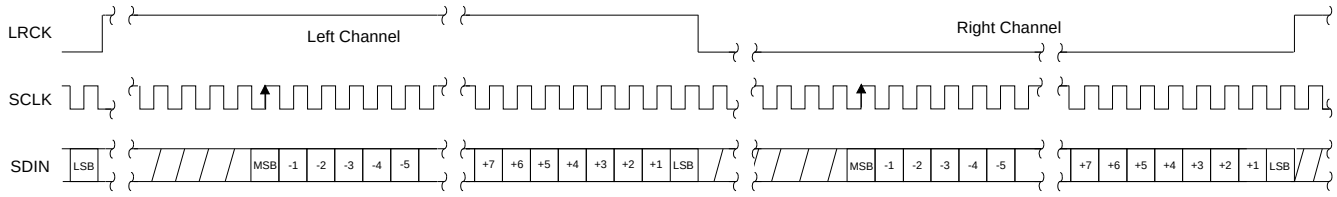


Figure 13. Right-Justified Data

4.3.1 Time-Division Multiplex (TDM) Mode

Four TDM interface modes are available that allow the CS4350 to input stereo PCM data in one of 4 time "slots". Figure 14 shows the serial port connections necessary to input 8-channel TDM data into four CS4350 devices, and the corresponding DIF[2:0] pin or register-bit settings required for each CS4350. Figure 15 shows the TDM data format for each of the four CS4350 devices shown in Figure 14.

Note: The group delay for TDM slot 0 channel B differs from the group delay of all other interface formats and TDM slots/channels by one sample. Refer to the group delay specification in the combined interpolation and on-chip analog filter response specifications table.

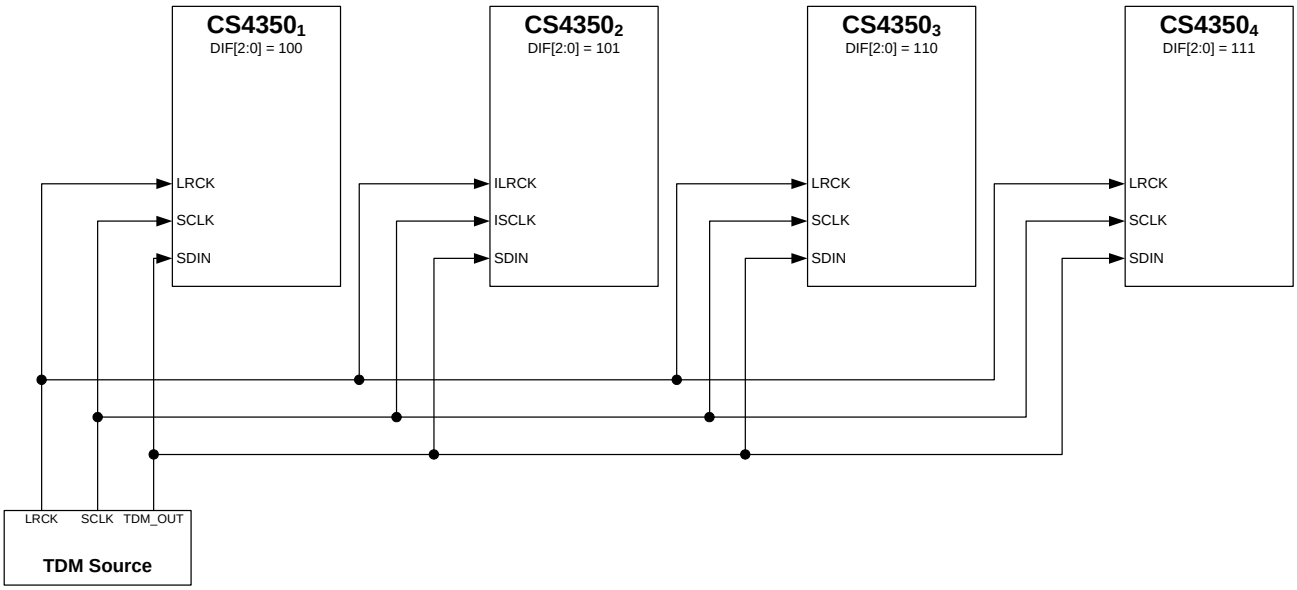


Figure 14. TDM Mode Connection Diagram

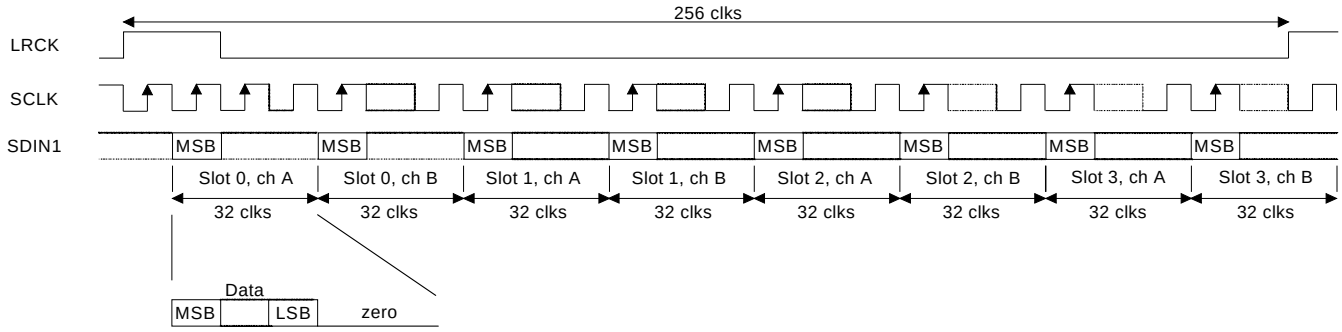


Figure 15. TDM Mode Timing

4.4 De-Emphasis

The device includes on-chip digital de-emphasis. Figure 16 shows the de-emphasis curve for Fs equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs.

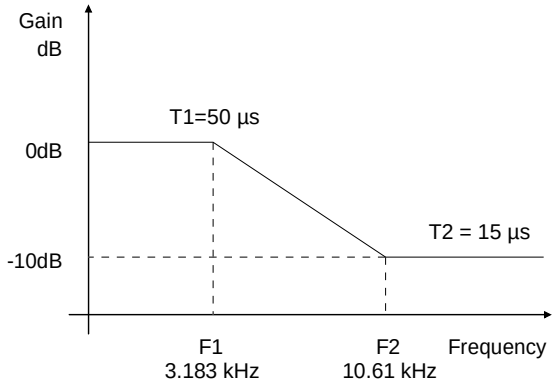


Figure 16. De-Emphasis Curve

Note: De-emphasis is only available in Single-Speed Mode.

4.5 Mute Control

The mute control pins ($\overline{\text{AMUTEC}}$ and $\overline{\text{BMUTEC}}$) go active during power-up initialization, reset, muting (see Section 8.4.3), and loss of LRCK. These pins are intended to be used as control for external mute circuits to prevent the clicks and pops that can occur in any single-ended single-supply system.

Use of the mute control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle-channel noise and signal-to-noise ratios which are only limited by the external mute circuit.

4.6 Recommended Power-Up Sequence

4.6.1 Stand-Alone Mode

1. Hold $\overline{\text{RST}}$ low until the power supplies and configuration pins are stable and the left/right clock is fixed to the appropriate frequencies, as discussed in Section 4.2. In this state, the control port registers are reset to their default settings, VQ will remain low, and VBIAS will be connected to VA.
2. Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with VQ low for approximately 192 LRCK cycles in Single-Speed Mode (384 LRCK cycles in Double-Speed Mode, and 768 LRCK cycles in Quad-Speed Mode).
3. The device will then initiate the power up sequence which lasts approximately 130 ms when the Popguard is disabled. If the Popguard is enabled, see Section 4.7 for a complete description of power-up timing.

4.6.2 Control Port Mode

1. Hold $\overline{\text{RST}}$ low until the power supply is stable and the left/right clock is fixed to the appropriate frequency, as discussed in Section 4.2. In this state, the control port is reset to its default settings, VQ will remain low, and VBIAS will be connected to VA.
2. Bring $\overline{\text{RST}}$ high. The device will remain in a low-power state with VQ low.
3. Perform a control port write to a valid register prior to the completion of approximately 192 LRCK cycles in Single-Speed Mode (384 LRCK cycles in Double-Speed Mode, and 768 LRCK cycles in Quad-Speed Mode). The desired register settings can be loaded while keeping the PDN bit set to 1.
4. Set the PDN bit to 0. This will initiate the power-up sequence, which lasts approximately 130 ms when the Popguard is disabled. If the Popguard is enabled, see Section 4.7 for a complete description of power-up timing.

4.7 Popguard Transient Control

The CS4350 uses a novel technique to minimize the effects of output transients during power-up and power-down. This technology, when used with external DC-blocking capacitors in series with the audio outputs, minimizes the audio transients commonly produced by single-ended single-supply converters. It is activated inside the DAC when the $\overline{\text{RST}}$ pin is toggled and requires no other external control, aside from choosing the appropriate DC-blocking capacitors.

4.7.1 Power-Up

When the device is initially powered-up, the audio outputs, AOUTA and AOUTB, are clamped to GND. Following a delay of approximately 192 sample periods, each output begins to ramp toward the quiescent voltage. The amount of time it takes the outputs to ramp is related to the value of the DC-blocking capacitance and the output load. Using the example output circuit from Figure 18, the ramp up time will be approximately 0.25 seconds. When the ramp is complete, the outputs reach V_Q and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitors to charge to the quiescent voltage, minimizing audible power-up transients.

Note the ramp up time will vary due to internal factors such as variance across device process, supply voltage, and die temperature corners as well as external output circuit component tolerances.

4.7.2 Power-Down

To prevent audible transients at power-down, the device must first enter its power-down state. When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTA and AOUTB. In their place, a soft-start current sink is substituted which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off, and the system is ready for the next power-on.

4.7.3 Discharge Time

To prevent an audio transient at the next power-on, the DC-blocking capacitors must fully discharge before turning on the power or exiting the power-down state. If full discharge does not occur, a transient will occur when the audio outputs are initially clamped to GND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance and the output load. For example, with a 3.3 µF capacitor, the minimum power-down time will be approximately 0.2 seconds.

4.8 Analog Output and Filtering

The Cirrus Application Note titled *Design Notes for a 2-Pole Filter with Differential Input*, available as AN48 at www.cirrus.com, discusses the second-order Butterworth filter and differential-to-single-ended converter that was implemented on the CS4350 evaluation board, CDB4350. Figure 17 illustrates this implementation. If only single-ended outputs from the CS4350 are required, the passive output filter shown in Figure 18 can be used.

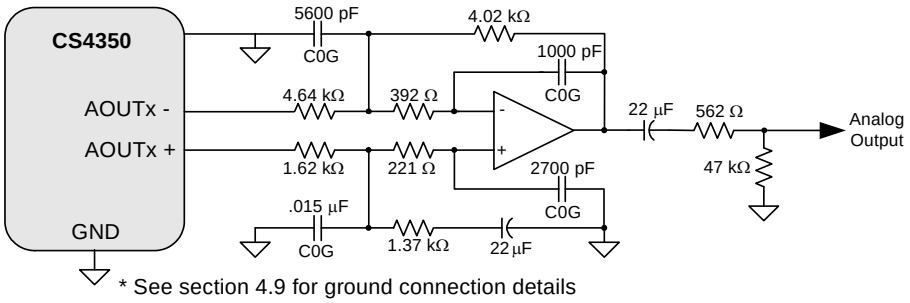


Figure 17. Differential to Single-Ended Output Filter

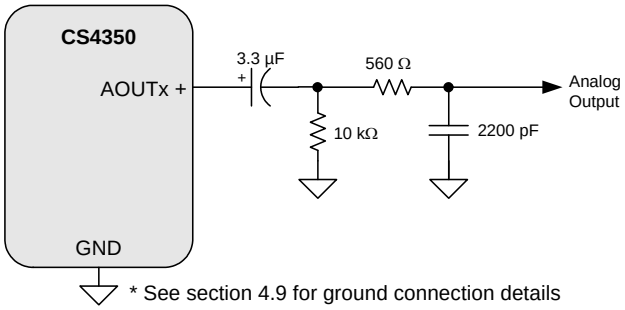


Figure 18. Passive Single-Ended Output Filter

4.9 Grounding and Power Supply Arrangements

As with any high-resolution converter, the CS4350 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 10 shows the recommended power arrangements, with VA, VLC, and VLS connected to clean supplies. The use of split analog and digital ground planes is not recommended. However, if planes are split between digital ground and analog ground the GND pins of the CS4350 should be connected to the analog ground plane.

All signals, especially clocks, should be kept away from the VBIAS, VFILT, and VQ pins in order to avoid unwanted coupling into the DAC.

4.9.1 Capacitor Placement

Decoupling capacitors should be placed as close to the DAC as possible, with the low value ceramic capacitor being the closest. To further minimize impedance, these capacitors should be located on the same layer as the DAC. If desired, all supply pins may be connected to the same supply, but a decoupling capacitor should still be placed on each supply pin.

Note: All decoupling capacitors should be referenced to GND.

The CDB4350 evaluation board demonstrates the optimum layout and power supply arrangements.

5 STAND-ALONE OPERATION

5.1 Serial Port Format Selection

The desired serial audio format is selected with the DIF2, DIF1 and DIF0 pins. For an explanation of the required relationship between the LRCK, SCLK and SDIN, see Figures 11-13. For all formats, SDIN is valid on the rising edge of SCLK. TDM Mode requires the selection of which stereo pair time “slot” is used to output data as shown in Table 12 and Figure 15.

Note: The group delay for TDM slot 0 channel B differs from the group delay of all other interface formats and TDM slots/channels by one sample. Refer to the group delay specification in the combined interpolation and on-chip analog filter response specifications table.

DIF2	DIF1	DIF0	DESCRIPTION	FORMAT	FIGURE
0	0	0	Left-Justified, up to 24-bit data	0	12
0	0	1	I²S, up to 24-bit data	1	11
0	1	0	Right-Justified, 16-bit data	2	13
0	1	1	Right-Justified, 24-bit data	3	13
1	0	0	TDM slot 0	4	15
1	0	1	TDM slot 1	5	15
1	1	0	TDM slot 2	6	15
1	1	1	TDM slot 3	7	15

Table 12. Digital Interface Format - Stand-Alone Mode

5.2 De-Emphasis Control

When pulled to VLC, the DEM pin activates the 44.1 kHz de-emphasis filter. When pulled to GND, the DEM pin turns off the de-emphasis filter.

5.3 Popguard Transient Control

In Stand-Alone Mode, Popguard is selected by placing a 47 kΩ resistor between RMCK and VLS. Popguard is defeated in Stand-Alone Mode by placing a 47 kΩ resistor between RMCK and ground.

6 CONTROL PORT OPERATION

The control port is used to load all the internal register settings (see ”Register Description” on page 29). The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port can operate in I²C or SPI mode.

6.1 MAP Auto Increment

The device has a MAP (memory address pointer) auto-increment capability enabled by the INCR bit (also the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for consecutive writes or reads. If INCR is set to 1, MAP will auto increment after each byte is read or written, allowing block reads or writes of consecutive registers.

6.2 I²C Mode

In the I²C Mode, data is clocked into and out of the bi-directional serial control data line, SDA, by the serial control port clock, SCL (see Figure 19 for the clock to data relationship). There is no $\overline{CS}$ pin. AD1 and AD0

enable the user to alter the chip address (10010[AD1][AD0][R/$\overline{W}$]) and should be tied to VLC or GND as required before powering up the device. SPI Mode will be selected if the device ever detects a high to low transition on the AD0/$\overline{CS}$ pin after power-up.

6.2.1 I²C Write

To write to the device, follow the procedure below while adhering to the control port Switching Specifications in "Switching Characteristics - Control Port - I²C Format" on page 14.

1. Initiate a START condition to the I²C bus followed by the address byte. The upper 5 bits must be 10010. The sixth and seventh bit must match the settings of the AD1 and AD0 pins respectively, and the eighth must be 0 (the eighth bit of the address byte is the R/$\overline{W}$ bit).
2. Wait for an acknowledge (ACK) from the part, then write to the memory address pointer, MAP. This byte points to the register to be written.
3. Wait for an acknowledge (ACK) from the part, then write the desired data to the register pointed to by the MAP.
4. If the INCR bit (see Section 6.1) is set to 1, repeat the previous step until all the desired registers are written, then initiate a STOP condition to the bus.
5. If the INCR bit is set to 0 and further I²C writes to other registers are desired, it is necessary to initiate a repeated START condition and follow the procedure detailed from step 1. If no further writes to other registers are desired, initiate a STOP condition to the bus.

6.2.2 I²C Read

To read from the device, follow the procedure below while adhering to the control port switching specifications in "Switching Characteristics - Control Port - I²C Format" on page 14.

1. Initiate a START condition to the I²C bus followed by the address byte. The upper 5 bits must be 10010. The sixth and seventh bits must match the setting of the AD1 and AD0 pins, respectively, and the eighth must be 1. The eighth bit of the address byte is the R/$\overline{W}$ bit.
2. After transmitting an acknowledge (ACK), the device will then transmit the contents of the register pointed to by the MAP. The MAP register will contain the address of the last register written to the MAP or the default address (see Section 6.4.2) if an I²C read is the first operation performed on the device.
3. Once the device has transmitted the contents of the register pointed to by the MAP, issue an ACK.
4. If the INCR bit is set to 1, the device will continue to transmit the contents of successive registers. Continue providing a clock and issue an ACK after each byte until all the desired registers are read; then initiate a STOP condition to the bus.
5. If the INCR bit is set to 0 and further I²C reads from other registers are desired, it is necessary to initiate a repeated START condition and follow the procedure detailed from steps 1 and 2 from the I²C Write instructions, followed by step 1 of the I²C Read section. If no further reads from other registers are desired, initiate a STOP condition to the bus.

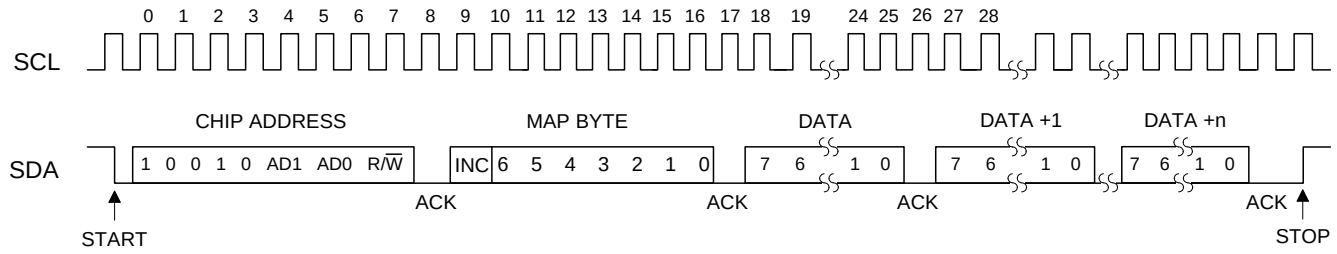


Figure 19. Control Port Timing, I²C Mode

6.3 SPI Mode

In SPI Mode, data is clocked into the serial control data line, CDIN, by the serial control port clock, CCLK (see Figure 20 for the clock to data relationship). There are no AD0 or AD1 pins. Pin $\overline{CS}$ is the chip select signal and is used to control SPI writes to the control port. When the device detects a high-to-low transition on the AD0/$\overline{CS}$ pin after power-up, SPI Mode will be selected. All signals are inputs and data is clocked in on the rising edge of CCLK.

6.3.1 SPI Write

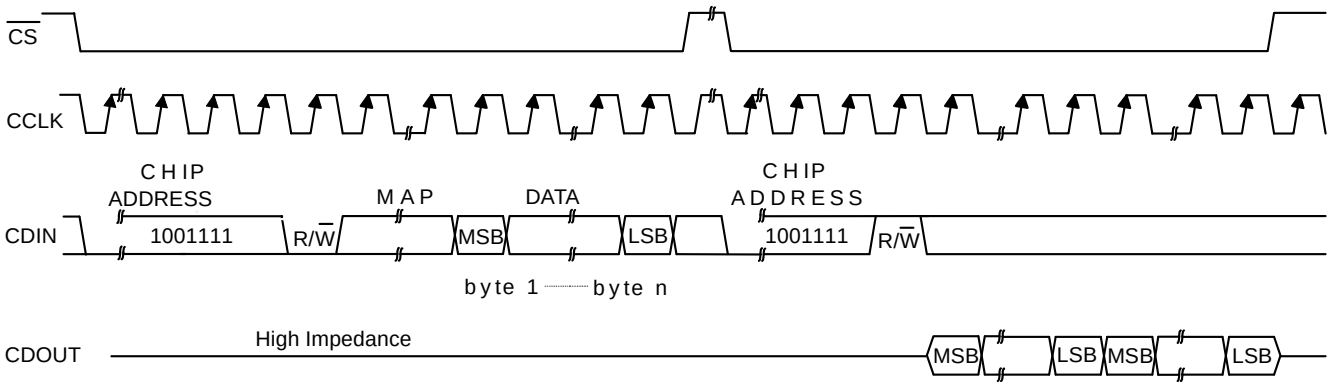
To write to the device, follow the procedure below while adhering to the control port switching specifications in "Switching Characteristics - Control Port - SPI Format" on page 15.

1. Bring $\overline{CS}$ low.
2. The address byte on the CDIN pin must then be 10011110 (R/$\overline{W}$ = 0).
3. Write to the memory address pointer, MAP. This byte points to the register to be written.
4. Write the desired data to the register pointed to by the MAP.
5. If the INCR bit (see Section 6.1) is set to 1, repeat the previous step until all the desired registers are written, then bring $\overline{CS}$ high.
6. If the INCR bit is set to 0 and further SPI writes to other registers are desired, it is necessary to bring $\overline{CS}$ high, and follow the procedure detailed from step 1. If no further writes to other registers are desired, bring $\overline{CS}$ high

6.3.2 SPI Read

To read from the device, follow the procedure below while adhering to the values specified in "Switching Characteristics - Control Port - SPI Format" on page 15.

1. Bring $\overline{CS}$ low.
2. The address byte on the CDIN pin must then be 10011111 (R/$\overline{W}$ = 1).
3. CDOUT pin will then output the data from the register pointed to by the MAP, which is set during the SPI write operation.
4. If the INCR bit (see Section 6.1) is set to 1, keep $\overline{CS}$ low and continue providing clocks on CCLK to read from multiple consecutive registers. Bring $\overline{CS}$ high when reading is complete.
5. If the INCR bit is set to 0 and further SPI reads from other registers are desired, it is necessary to bring $\overline{CS}$ high, and follow the procedure detailed from step 1. If no further reads from other registers are desired, bring $\overline{CS}$ high.



MAP = Memory Address Pointer, 8 bits, MSB first

Figure 20. Control Port Timing, SPI Mode

6.4 Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	MAP3	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

6.4.1 INCR (Auto Map Increment Enable)

Default = '0'
0 - Disabled
1 - Enabled

6.4.2 MAP (Memory Address Pointer)

Default = '0000'

7 REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
1h	Device and RevID	DeviceID4	DeviceID3	DeviceID2	DeviceID1	DeviceID0	RevID2	RevID1	RevID0
	default	1	1	1	1	-	-	-	-
2h	Mode Control	Reserved	DIF2	DIF1	DIF0	DEM1	DEM0	FM1	FM0
	default	0	0	0	0	0	0	0	0
3h	Volume, Mixing, and Inversion Control	VOLB=A	INVERTA	INVERTB	Reserved	ATAPI3	ATAPI2	ATAPI1	ATAPI0
	default	0	0	0	0	1	0	0	1
4h	Mute Control	AMUTE	Reserved	MUTEC A=B	MUTE_A	MUTE_B	Reserved	Reserved	Reserved
	default	1	0	0	0	0	0	0	1
5h	Channel A Volume Control	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
	default	0	0	0	0	0	0	0	0
6h	Channel B Volume Control	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
	default	0	0	0	0	0	0	0	0
7h	Ramp and Filter Control	SZC1	SZC0	RMP_UP	RMP_DN	Reserved	FILT_SEL	Reserved	Reserved
	default	1	0	1	1	0	0	0	1
8h	Misc. Control	PDN	Reserved	FREEZE	POPG_EN	RMCK_ CTRL1	RMCK_ CTRL0	R_ SELECT1	R_ SELECT0
	default	0	0	0	1	0	0	0	0

8 REGISTER DESCRIPTION

Note: All register access is Read/Write unless specified otherwise

8.1 Device and Revision ID - Register 01h

7	6	5	4	3	2	1	0
Device4	Device3	Device2	Device1	Device0	Rev2	Rev1	Rev0
1	1	1	1	-	-	-	-

Function:

This register is Read-Only. It is decoded as follows:

Rev	Register 01h contents
A	1111,0000
B	1111,0001
C2	1111,1111

8.2 Mode Control - Register 02h

7	6	5	4	3	2	1	0
Reserved	DIF2	DIF1	DIF0	DEM1	DEM0	FM1	FM0
0	0	0	0	0	0	0	0

8.2.1 Digital Interface Format (DIF[2:0]) Bits 6-4

Function:

These bits select the interface format for the serial audio input.

The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Figures 11-13.

Note: The group delay for TDM slot 0 channel B differs from the group delay of all other interface formats and TDM slots/channels by one sample. Refer to the group delay specification in the combined interpolation and on-chip analog filter response specifications table.

Table 13. Digital Interface Formats

DIF2	DIF1	DIF0	Description	Format	Figure
0	0	0	Left-Justified, up to 24-bit data	0 (Default)	11
0	0	1	I²S, up to 24-bit data	1	12
0	1	0	Right-Justified, 16-bit data	2	13
0	1	1	Right-Justified, 24-bit data	3	13
1	0	0	TDM slot 0	4	15
1	0	1	TDM slot 1	5	15
1	1	0	TDM slot 2	6	15
1	1	1	TDM slot 3	7	15

8.2.2 De-Emphasis Control (DEM[1:0]) Bits 3-2

Default = 0
00 - No De-emphasis
01 - 44.1 kHz De-emphasis
10 - 48 kHz De-emphasis
11 - 32 kHz De-emphasis

Function:

Selects the appropriate digital filter to maintain the standard 15 µs/50 µs digital de-emphasis filter response at 32, 44.1 or 48 kHz sample rates. (See Figure 21)

Note: De-emphasis is only available in Single-Speed Mode

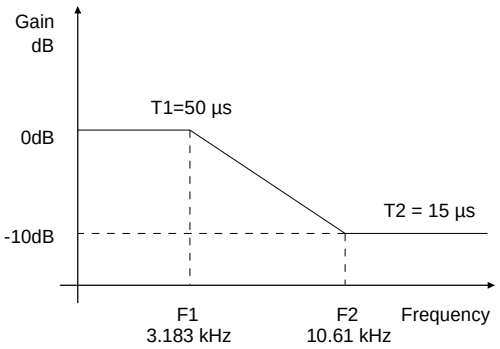


Figure 21. De-Emphasis Curve

8.2.3 Functional Mode (FM[1:0]) Bits 1-0

Default = 00
00 - Auto speed mode detect
01 - Single-Speed Mode (30 to 54 kHz sample rates)
10 - Double-Speed Mode (50 to 108 kHz sample rates)
11 - Quad-Speed Mode (100 to 216 kHz sample rates)

Function:

Selects the required range of input sample rates or auto speed mode.

8.3 Volume Mixing and Inversion Control - Register 03h

7	6	5	4	3	2	1	0
VOLB=A	INVERT_A	INVERT_B	Reserved	ATAPI3	ATAPI2	ATAPI1	ATAPI0
0	0	0	0	1	0	0	1

8.3.1 Channel A Volume = Channel B Volume (VOLB=A) Bit 7

Function:

When set to 0 (default), the AOUTA and AOUTB volume levels are independently controlled by the A and the B Channel Volume Control Bytes.

When set to 1, the volume on both AOUTA and AOUTB are determined by the A Channel Attenuation and Volume Control Bytes, and the B Channel Bytes are ignored.

8.3.2 Invert Signal Polarity (INVERT_A) Bit 6

Function:

When set to 1, this bit inverts the signal polarity of channel A.

When set to 0 (default), this function is disabled.

This function is only available for Left Justified, Right Justified 16, and Right Justified 24 data formats.

8.3.3 Invert Signal Polarity (INVERT_B) Bit 5

Function:

When set to 1, this bit inverts the signal polarity of channel B.

When set to 0 (default), this function is disabled.

This function is only available for Left Justified, Right Justified 16, and Right Justified 24 data formats.

8.3.4 ATAPI Channel Mixing and Muting (ATAPI[3:0]) Bits 3-0

Default = 1001 - AOUTA=aL, AOUTB=bR (Stereo)

Function:

The CS4350 implements the channel mixing functions of the ATAPI CD-ROM specification. Refer to Table 14 and Figure 22 for additional information.

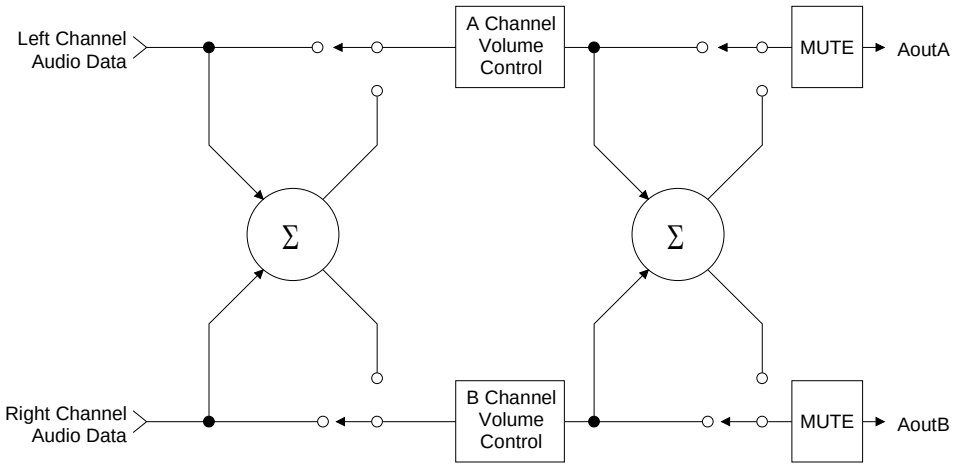


Figure 22. ATAPI Block Diagram

Table 14. ATAPI Decode

ATAPI_A1	ATAPI_A0	ATAPI_B1	ATAPI_B0	AOUTA	AOUTB
0	0	0	0	MUTE	MUTE
0	0	0	1	MUTE	bR
0	0	1	0	MUTE	bL
0	0	1	1	MUTE	b[(L+R)/2]
0	1	0	0	aR	MUTE
0	1	0	1	aR	bR
0	1	1	0	aR	bL
0	1	1	1	aR	b[(L+R)/2]

Table 14. ATAPI Decode (Continued)

ATAPI_A1	ATAPI_A0	ATAPI_B1	ATAPI_B0	AOUTA	AOUTB
1	0	0	0	aL	MUTE
1	0	0	1	aL	bR
1	0	1	0	aL	bL
1	0	1	1	aL	b[(L+R)/2]
1	1	0	0	a[(L+R)/2]	MUTE
1	1	0	1	a[(L+R)/2]	bR
1	1	1	0	a[(L+R)/2]	bL
1	1	1	1	a[(L+R)/2]	b[(L+R)/2]

8.4 Mute Control - Register 04h

7	6	5	4	3	2	1	0
AMUTE	Reserved	MUTEC A=B	MUTE_A	MUTE_B	Reserved	Reserved	Reserved
1	0	0	0	0	0	0	0

8.4.1 Auto-Mute (AMUTE) Bit 7

Function:

When set to 1 (default), the Digital-to-Analog converter output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained and the Mute Control pin will go active during the mute period.

When set to 0, this function is disabled

8.4.2 AMUTEC = BMUTEC (MUTEC A=B) Bit 5

Function:

When set to 0 (default), the $\overline{\text{AMUTEC}}$ and $\overline{\text{BMUTEC}}$ pins operate independently.

When set to 1, the individual controls for $\overline{\text{AMUTEC}}$ and $\overline{\text{BMUTEC}}$ are internally connected through an AND gate prior to the output pins. Therefore, the external $\overline{\text{AMUTEC}}$ and $\overline{\text{BMUTEC}}$ pins go active only when the requirements for both $\overline{\text{AMUTEC}}$ and $\overline{\text{BMUTEC}}$ are valid.

8.4.3 Channel A Mute (MUTE_A) Bit 4 & Channel B Mute (MUTE_B) Bit 3

Function:

When set to 1, the Digital-to-Analog converter output will mute. The quiescent voltage on the output will be retained. The muting function is affected, similar to attenuation changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register. The corresponding MUTEC pin will go active following any ramping due to the soft and zero cross function.

When set to 0 (default), this function is disabled.

8.5 Channel A & B Volume Control - Register 05h & 06h

7	6	5	4	3	2	1	0
VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
0	0	0	0	0	0	0	0

Digital Volume Control (VOL[7:0]) Bits 7-0

Default = 00h (0 dB)

Function:

The Digital Volume Control registers allow independent control of the signal levels in 1/2 dB increments from 0 to -127.5 dB. Volume settings are decoded as shown in Table 15. The volume changes are implemented as dictated by the Soft and Zero Cross bits in the Power and Muting Control register. The actual attenuation is determined by taking the decimal value of the volume register and multiplying by 6.02/12.

Table 15. Example Digital Volume Settings

Binary Code	Decimal Value	Volume Setting
00000000	0	0 dB
00000001	1	-0.5 dB
00000110	6	-3.0 dB
11111111	255	-127.5 dB

8.6 Ramp and Filter Control - Register 07h

7	6	5	4	3	2	1	0
SZC1	SZC0	RMP_UP	RMP_DN	Reserved	FILT_SEL	Reserved	Reserved
1	0	1	1	0	0	0	1

8.6.1 Soft Ramp and Zero Cross Control (SZC[1:0]) Bits 7-6

Default = 10

SZC1	SZC0	Description
0	0	Immediate Change
0	1	Zero Cross
1	0	Soft Ramp
1	1	Soft Ramp on Zero Crossings

Function:

Immediate Change

When Immediate Change is selected, all level changes will take effect immediately in one step.

Zero Cross

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp PCM

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

Soft Ramp and Zero Cross

Soft Ramp and Zero Cross Enable dictate that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

8.6.2 Soft Volume Ramp-Up after Error (RMP_UP) Bit 5

Function:

When set to 1 (default), an un-mute will be performed after executing a filter mode change, after LRCK is lost, and after changing the Functional Mode. This un-mute is affected, similar to attenuation changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register.

When set to 0, an immediate un-mute is performed in these instances.

Note: For best results, it is recommended that this feature be used in conjunction with the RMP_DN bit.

8.6.3 Soft Ramp-Down before Filter Mode Change (RMP_DN) Bit 4

Function:

When set to 1 (default), a mute will be performed prior to executing a filter mode change. This mute is affected, similar to attenuation changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register.

When set to 0, an immediate mute is performed prior to executing a filter mode change.

Note: For best results, it is recommended that this feature be used in conjunction with the RMP_UP bit.

8.6.4 Interpolation Filter Select (FILT_SEL) Bit 2

Function:

When set to 0 (default), the Interpolation Filter has a fast roll off.

When set to 1, the Interpolation Filter has a slow roll off.

The specifications for each filter can be found in the ”Combined Interpolation and On-Chip Analog Filter Response” on page 12, and response plots can be found in Figures 25 through 30.

8.7 Misc. Control - Register 08h

7	6	5	4	3	2	1	0
PDN	Reserved	FREEZE	POPG_EN	RMCK_CTRL1	RMCK_CTRL0	R_SELECT1	R_SELECT0
0	0	0	1	0	0	0	0

8.7.1 Power Down (PDN) Bit 7

Function:

When set to 1 the entire device will enter a low-power state and the contents of the control registers will be retained. The power-down bit defaults to ‘0’ on power-up.

8.7.2 Freeze Controls (FREEZE) Bit 5

Function:

When set to 1, this function allows modifications to be made to the registers without the changes taking effect until FREEZE is set back to 0. To make multiple changes in the Control Port registers take effect simultaneously, enable the FREEZE bit, make all register changes, then disable the FREEZE bit.

When set to 0 (default), register changes take effect immediately.

8.7.3 Popguard Enable (POPG_EN) Bit 4

Function:

When set to 1, (default) the Device will initiate a ramping function as outlined in Section 4.7 on page 22. When set to 0, the outputs will step to VQ upon release of PDN.

8.7.4 RMCK control (RMCK_CTRL[1:0]) Bits 3:2

Default = 00

RMCK_CTRL1	RMCK_CTRL0	Mode
0	0	256x LRCK for 48 kHz and 96 kHz, 128x @ 192kHz
0	1	512x @ 48kHz, 256x @ 96 kHz, 128x @ 192kHz
1	0	Manual control (see RMCK Ratio Select)
1	1	RMCK pin driven low

Function: These bits set the function of the RMCK pin with respect to the LRCK.

8.7.5 RMCK Ratio Select (R_SELECT[1:0]) Bits 2:1

Default = 00

Function: To select the RMCK-to-LRCK ratio.

R_SELECT1	R_SELECT0	RMCK/LRCK Ratio
0	0	512
0	1	256
1	0	128
1	1	64

Note: RMCK_CTRL must be set to 10 to enable this function. Please note the maximum RMCK output frequency as specified in the ”Switching Specifications - Serial Audio Interface” on page 13.

9 FILTER PLOTS

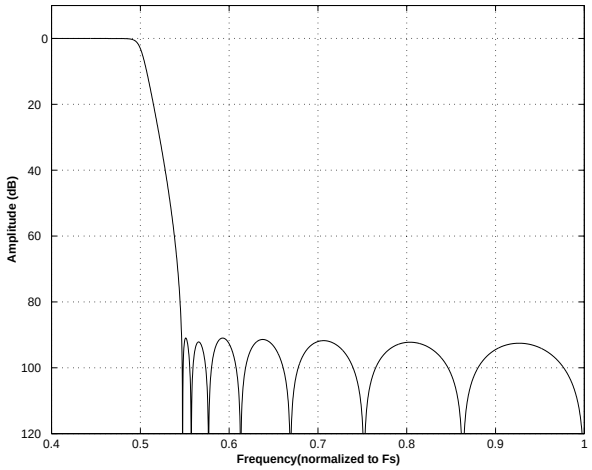


Figure 23. Stopband Rejection (fast), all Modes

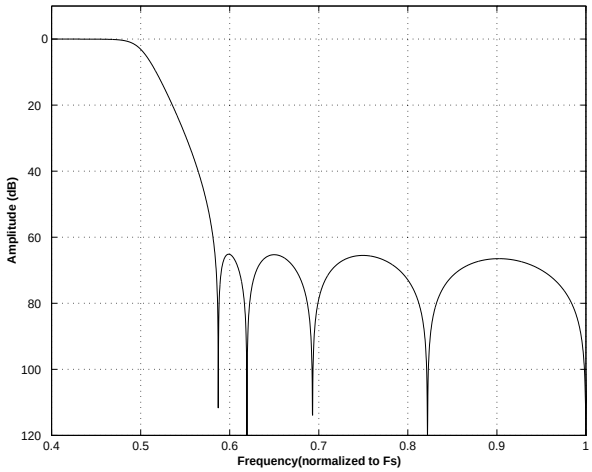


Figure 24. Stopband Rejection (slow), all Modes

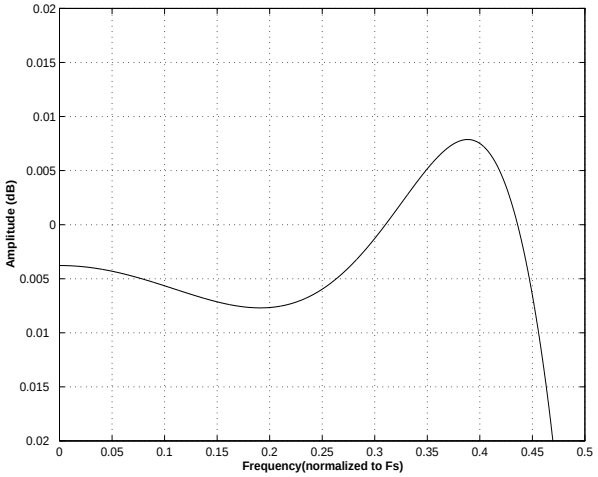


Figure 25. Single-Speed (fast) Passband Detail

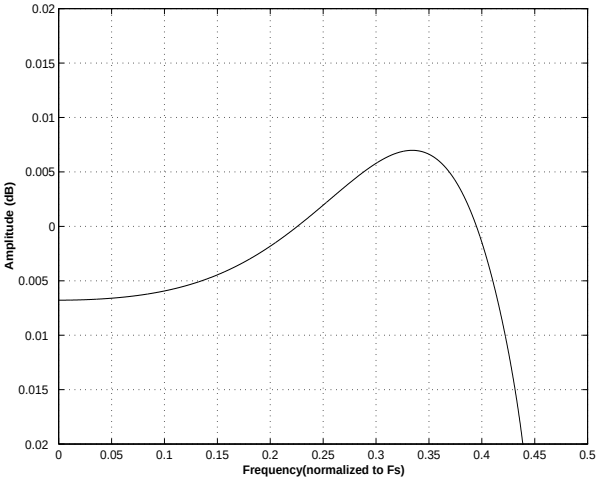


Figure 26. Single-Speed (slow) Passband Detail

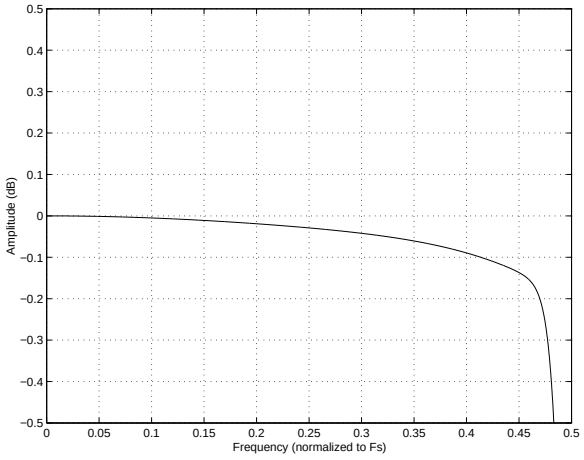


Figure 27. Double-Speed (fast) Passband Detail

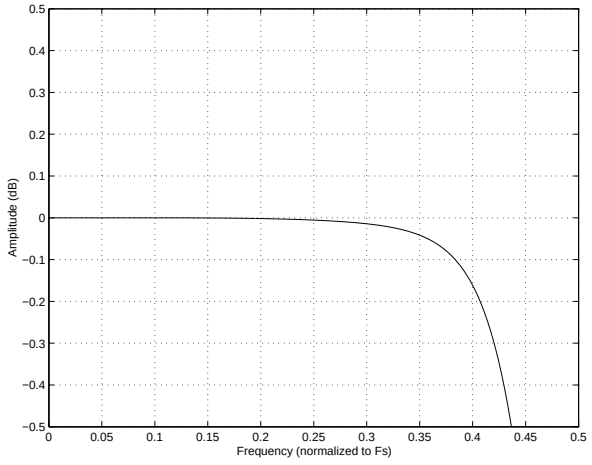


Figure 28. Double-Speed (slow) Passband Detail

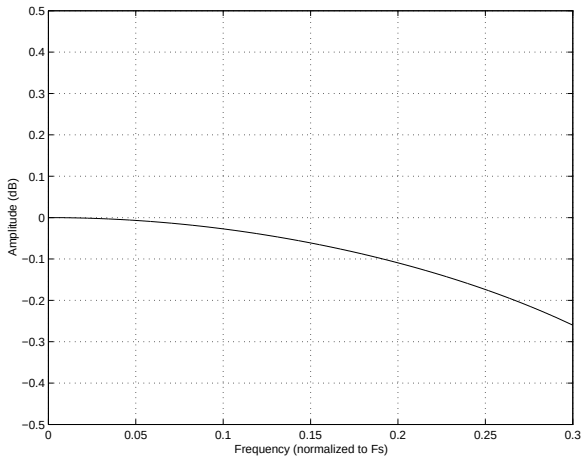


Figure 29. Quad-Speed (fast) Passband Detail

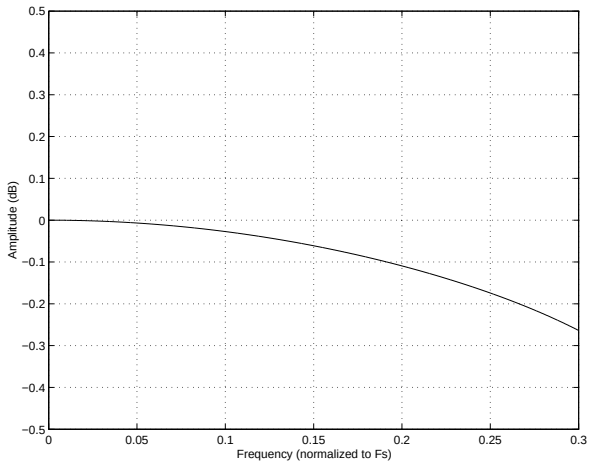


Figure 30. Quad-Speed (slow) Passband Detail

10 PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full-scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. Then, 60 dB is added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Intrachannel Phase Deviation

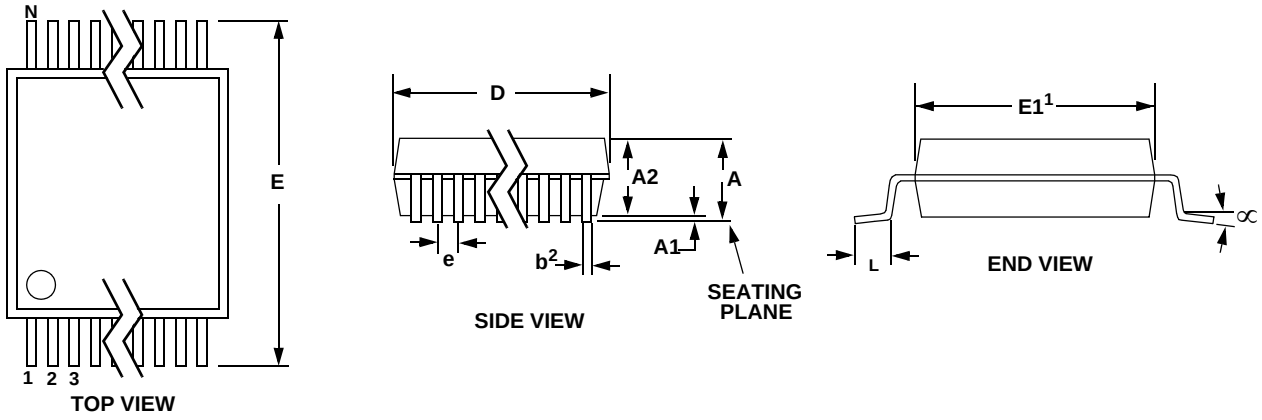
The deviation from linear phase within a given channel.

Interchannel Phase Deviation

The difference in phase between channels.

11 PACKAGE DIMENSIONS

11.1 24L TSSOP (4.4 mm BODY) PACKAGE DRAWING

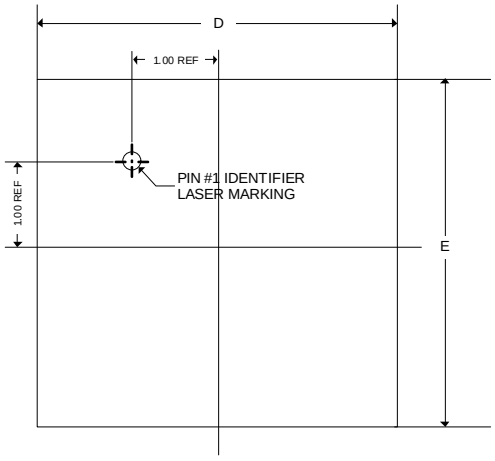


	INCHES			MILLIMETERS			NOTE
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.303	0.307	0.311	7.70	7.80	7.90	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.65 BSC	--	
L	0.020	0.024	0.028	0.50	0.60	0.70	
µ	0°	4°	8°	0°	4°	8°	

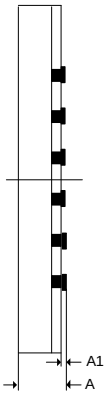
JEDEC #: MO-153
Controlling Dimension is Millimeters.

1. D" and "E1" are reference datums and do not include mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

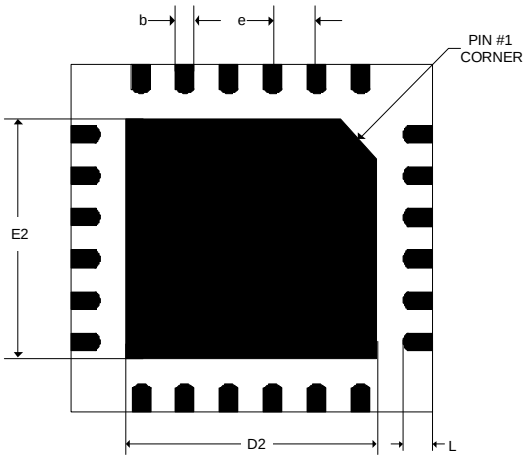
11.2 24L QFN (4.00 mm BODY) PACKAGE DRAWING



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Dimension	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.031	0.033	0.035	0.80	0.85	0.90
A1	0.000	0.001	0.002	0.00	0.035	0.05
b	0.008	0.010	0.012	0.20	0.25	0.30
D		0.157 BSC			4.00 BSC	
D2	0.102	0.106	0.110	2.6	2.7	2.8
e		0.020 BSC			0.50 BSC	
E		0.157 BSC			4.00 BSC	
E2	0.102	0.106	0.110	2.6	2.7	2.8
L	0.014	0.016	0.018	0.35	0.40	0.45

1. Controlling dimensions are in millimeters.
2. Compliant to JEDEC MO-220 VGGD.
3. Recommended reflow profile is per JEDEC/IPC J-STD-020.

12 THERMAL CHARACTERISTICS

Table 16. Thermal Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Package Thermal Resistance—TSSOP	Single-Layer PCB Multiple-Layer PCB	θ_{JA}	-	70 105	-	°C/Watt
Package Thermal Resistance—QFN	Two-Layer PCB Multiple-Layer PCB	θ_{JA}	-	130 53	-	°C/Watt

12.1 QFN Thermal Pad

The QFN package version of this device is designed to have the metal pad on the bottom of the device soldered directly to a metal plane on the PCB. To enhance the thermal dissipation capabilities of the system, this metal plane should be coupled with vias to a large metal plane on the backside (and inner ground layer, if applicable) of the PCB.

In either case, it is beneficial to use copper fill in any unused regions inside the PCB layout, especially those immediately surrounding the CS4350. In addition to improving in electrical performance, this practice also aids in heat dissipation.

The heat dissipation capability required of the metal plane for a given output power can be calculated as follows:

$$\theta_{CA} = [(T_{J(MAX)} - T_A) / P_D] - \theta_{JC}$$

where,
θ_{CA} = Thermal resistance of the metal plane in °C/Watt
$T_{J(MAX)}$ = Maximum rated operating junction temperature in °C, equal to 150 °C
T_A = Ambient temperature in °C
P_D = RMS power dissipation of the device, equal to $0.176*P_{RMS\text{-}OUT}$ (assuming 85% efficiency)
θ_{JC} = Junction-to-case thermal resistance of the device in °C/Watt

13 ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order#
CS4350	192 kHz Stereo DAC with Integrated PLL	24-TSSOP	Yes	Commercial	-40° to +85°C	Rail	CS4350-CZZ
						Tape and Reel	CS4350-CZZR
				Automotive	-40° to +105°C	Rail	CS4350-DZZ
						Tape and Reel	CS4350-DZZR
		24-QFN	Yes	Commercial	-40° to +85°C	Rail	CS4350-CNZ
						Tape and Reel	CS4350-CNZR
CDB4350	Evaluation Board for CS4350		-	-	-	-	CDB4350

14 REVISION HISTORY

Release	Changes
F2 APR ‘13	• Updated Total Group Delay typical values in the Combined Interpolation and On-Chip Analog Filter Response table in Section 2.5. • Updated RMCK connection in typical connection drawing, Figure 10. • Updated Figure 15 to show slot numbering from 0–3 rather than 1–4. • Removed reference to master clock in Step 1 in Section 4.6.1. • Updated timings in the recommended power-up sequences in Section 4.6.1 and Section 4.6.2. • Updated sample periods and latency in Section 4.7.1, Power-Up.” • Updated minimum power-down time in Section 4.7.3, Discharge Time.” • Updated description in Section 5.3 of how Popguard is selected/defeated in Stand-Alone Mode. • Added a note regarding differences in group delay for TDM slot 0 channel B to Section 4.3.1, Section 5.1, Section 8.2.1.
F3 SEPT ‘15	• Added text describing QFN package availability to Description section on page 2. • Added QFN pinout to Section 1.2. • Noted presence of QFN thermal pad in QFN figure in Section 1.2. • Updated full-scale output voltage in Table 3. • Updated RMCK output frequency, SDIN hold time, and LRCK high time in Table 6. • Corrected parameter definition in Table 9. • Added QFN thermal pad detail to Figure 10. • Added QFN package to Section 11.2. • Added QFN thermal resistances to Section 12. • Added QFN thermal pad Section 12.1. • Added ordering information for QFN package to Section 13.
F4 FEB ‘17	• Updated full-scale output voltage in Table 3.

Contacting Cirrus Logic Support

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