THE DATASHEET OF

CS5231-3GDPR5

CS5231-3

500 mA, 3.3 V Linear Regulator with Auxiliary Control

The CS5231−3 combines a three−terminal linear regulator with circuitry controlling an external PFET transistor thus managing two input supplies. The part provides a 3.3 V regulated output either from the main 5.0 V supply or a 3.3 V auxiliary that switches on when the 5.0 V supply is not present. This delivers constant, uninterrupted power to the load. The CS5231−3 meets Intel's "Instantly Available" power requirements which follows from the "Advanced Configuration and Power Interface" (ACPI) standards developed by Intel, Microsoft and Toshiba.

The CS5231−3 linear regulator provides a fixed 3.3 V output at 500 mA with an overall accuracy of ± 2.0%. The internal NPN−PNP composite pass transistor provides a low dropout voltage and requires less supply current than a straight PNP design. Full protection with both current limit and thermal shutdown is provided.

Designed for low reverse current, the IC prevents excessive current from flowing from V_{OUT} to either V_{IN} or ground when the regulator input voltage is lower than the output voltage.

The CS5231−3 can be used to provide power to an ASIC on a PCI Network Interface Card (NIC). When the system enters a Sleep State and the 5.0 V input drops below 4.4 V, the AuxDrv control signal on the CS5231−3 is activated turning on the external PFET. This switches the supply source from the 5.0 V input to the 3.3 V input through the PFET, guaranteeing a constant 3.3 V output to the ASIC that is "glitch free."

The CS5231−3 is available in two package types: the D^2PAK−5 (TO263) package and the SOIC−8 4−Lead−fused (DF) package. Other applications include desktop computers, power supplies with multiple input sources and PCMCIA/PCI interface cards.

Features

- Linear Regulator
  - 3.3 V ± 2.0% Output Voltage
  - 3.0 mA Quiescent Current @ 500 mA
  - Fast Transient Response
  - Current Limit Protection
  - Thermal Shutdown with Hysteresis
  - 450 µA Reverse Output Current
- System Power Management
  - Auxiliary Supply Control
  - "Glitch Free" Transition Between Two Supplies
- Internally Fused Leads in SOIC−8 Package

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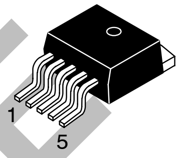
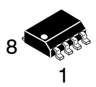
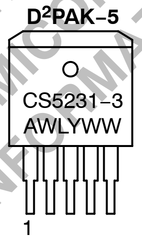


D^2PAK−5
DP SUFFIX
CASE 936AC



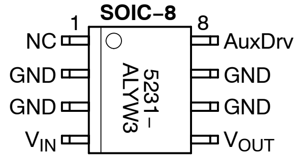
SOIC−8
DF SUFFIX
CASE 751

PIN CONNECTIONS AND MARKING DIAGRAMS



Pin
1. No Connect
2. V_{IN}
3. GND
4. V_{OUT}
5. AuxDrv

Tab = GND



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
CS5231−3GDP5	D^2PAK−5	50 Units/Rail
CS5231−3GDPR5	D^2PAK−5	750 Tape & Reel
CS5231−3GDF8	SOIC−8	95 Units/Rail
CS5231−3GDFR8	SOIC−8	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

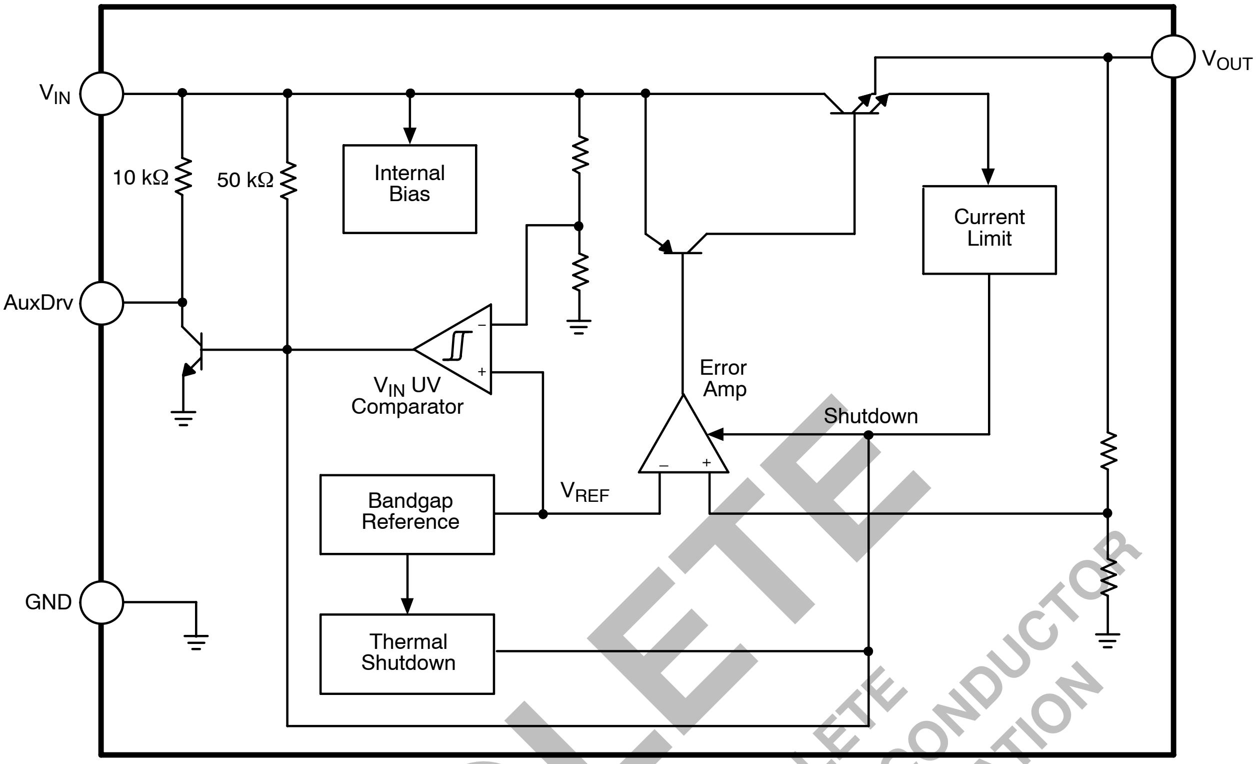


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS*

Rating		Value	Unit
Maximum Operating Junction Temperature		150	°C
Storage Temperature Range		−65 to +150	°C
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1)	230 peak	°C
ESD Damage Threshold (Human Body Model)		2.0	kV

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ABSOLUTE MAXIMUM RATINGS

Pin Name	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
IC Power Input	V_{IN}	14 V	−0.3 V	100 mA	Internally Limited
Output Voltage	V_{OUT}	6.0 V	−0.3 V	Internally Limited	100 mA
Auxiliary Drive Output	AuxDrv	14 V	−0.3 V	10 mA	50 mA
IC Ground	GND	N/A	N/A	N/A	N/A

ELECTRICAL CHARACTERISTICS ($0°C < T_A < 70°C$; $0°C < T_J < 125°C$; $4.75\ V \le V_{CC} < 6.0\ V$; $C_{OUT} \ge 10\ \mu F$ with ESR < 1.0 Ω, $I_{OUT} = 10\ mA$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Linear Regulator					
Output Voltage	10 mA < I_{OUT} < 500 mA.	3.234 (− 2%)	3.3	3.366 (+ 2%)	V
Line Regulation	I_{OUT} = 10mA; V_{IN} = 4.75 V to 6.0 V	–	1.0	5.0	mV
Load Regulation	V_{IN} = 5.0 V; I_{OUT} = 10 mA to 500 mA	–	5.0	15	mV
Ground Current	I_{OUT} = 10 mA I_{OUT} = 500 mA	– –	2.0 3.0	3.0 6.0	mA mA
Reverse Current	V_{IN} = 0 V, V_{OUT} = 3.3 V	–	0.45	1.0	mA
Current Limit	0 V < V_{OUT} < 3.2 V	0.55	0.85	1.2	A
Thermal Shutdown	Note 2	150	180	210	°C
Thermal Shutdown Hysteresis	Note 2	–	25	–	°C
Auxiliary Drive					
Upper V_{IN} Threshold	Increase V_{IN} until regulator turns on and AuxDrv drives high	4.35	4.5	4.65	V
Lower V_{IN} Threshold	Decrease V_{IN} until regulator turns off and AuxDrv drives low	4.25	4.4	4.55	V
V_{IN} Threshold Hysteresis	–	75	100	125	mV
Output Low Voltage	I_{AuxDrv} = 100 μA, 1.0 V < V_{IN} < 4.5 V	–	0.1	0.4	V
Output Low Peak Voltage	Increase V_{IN} from 0V to 1.0 V. Record peak AuxDrv output voltage	–	0.65	0.9	V
AuxDrv Current Limit	V_{AuxDrv} = 1.0 V; V_{IN} = 4.0 V	0.5	6.0	25	mA
Response Time	Step V_{IN} from 5.0 V to 4.0 V, measure time for V_{AuxDrv} to drive low. Note 2	–	1.0	10	μs
Pull−Up/Down Resistance	V_{IN} = 0 V and V_{IN} > 4.7 V.	5.0	10	25	kΩ

2. Guaranteed by design, not 100% production tested. Thermal shutdown is 100% functionally tested at wafer probe.

PACKAGE PIN DESCRIPTION

Package Lead #			
D^2PAK−5	SOIC−8	Lead Symbol	Function
1	1	NC	No connection.
2	4	V_{IN}	Input voltage.
3, Tab	2, 3, 6, 7	GND	Ground and IC substrate connection.
4	5	V_{OUT}	Regulated output voltage.
5	8	AuxDrv	Output used to control an auxiliary supply voltage. This lead is driven low if V_{IN} is less than 4.5 V, and is otherwise pulled up to V_{IN} through an internal 10 kΩ resistor.

TYPICAL PERFORMANCE CHARACTERISTICS

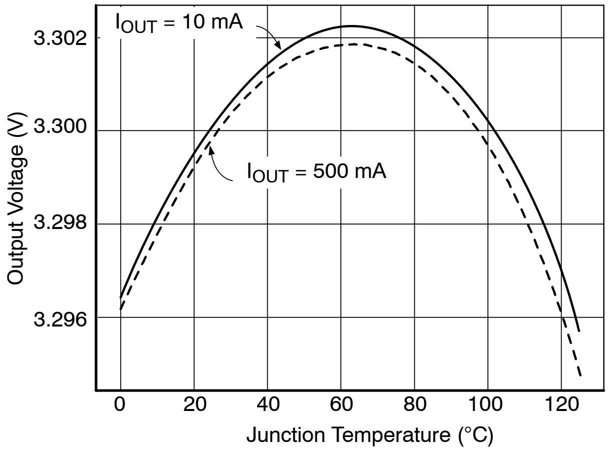


Figure 2. Output Voltage vs. Junction Temperature

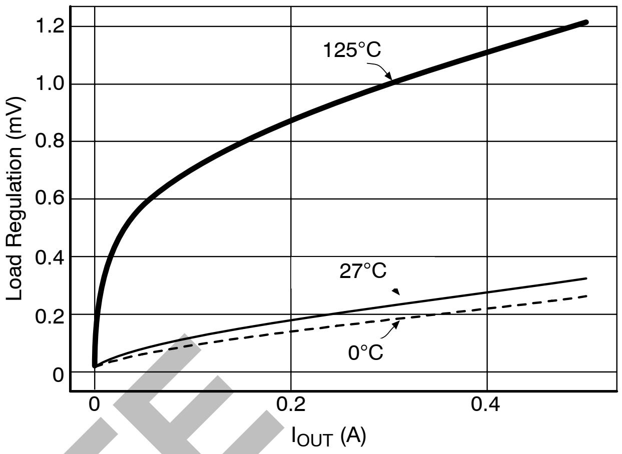


Figure 3. Line Regulation vs. I_{OUT} Over Temperature

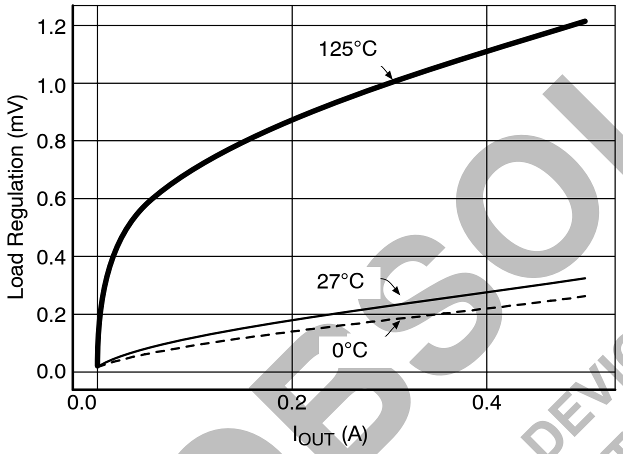


Figure 4. Load Regulation vs. I_{OUT} Over Temperature

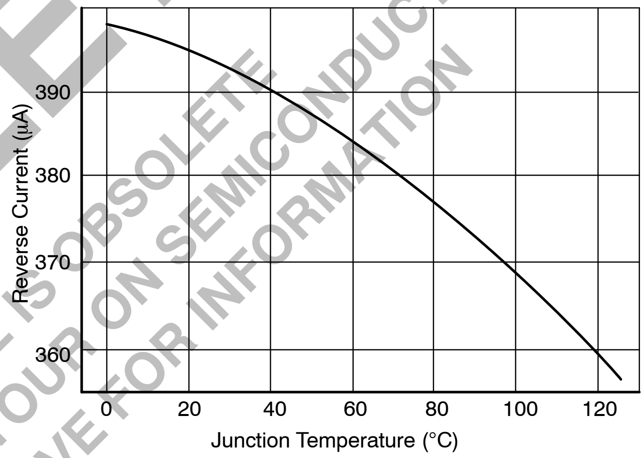


Figure 5. Reverse Current vs. Junction Temperature

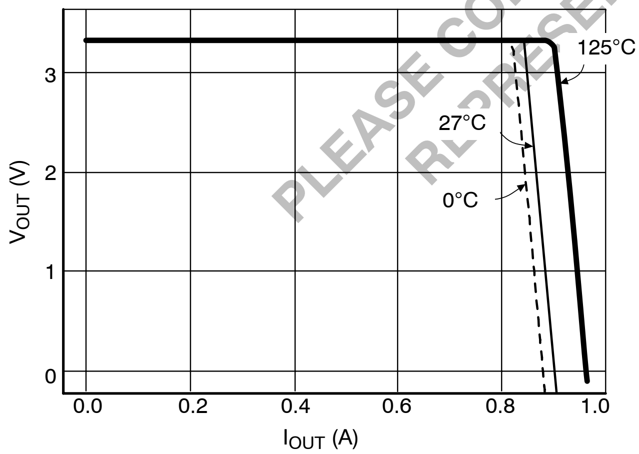


Figure 6. V_{OUT} vs. I_{OUT} Over Junction Temperature

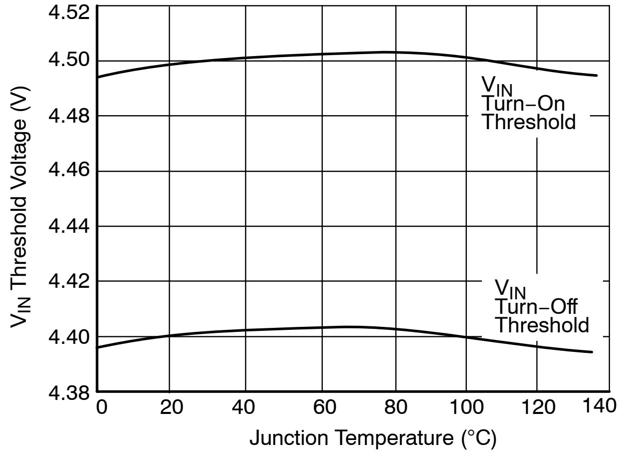


Figure 7. V_{IN} Thresholds vs. Junction Temperature

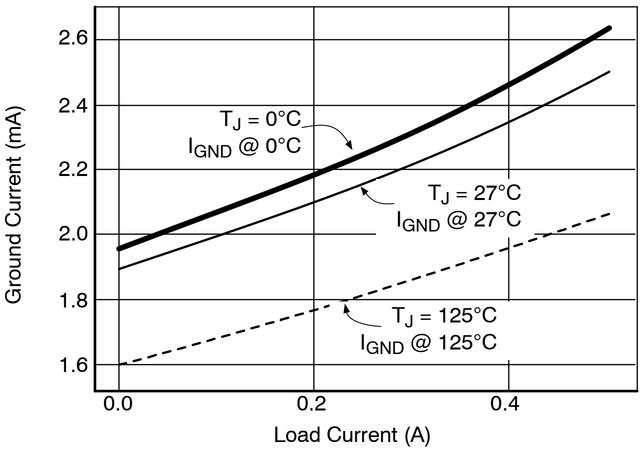


Figure 8. Ground Current vs. Load Current

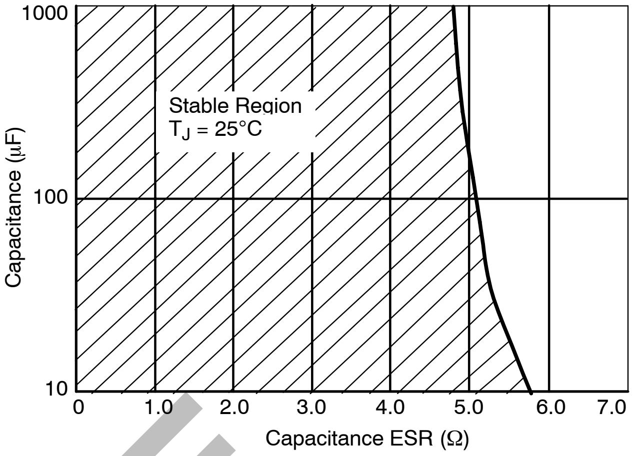


Figure 9. Region of Stable Operation

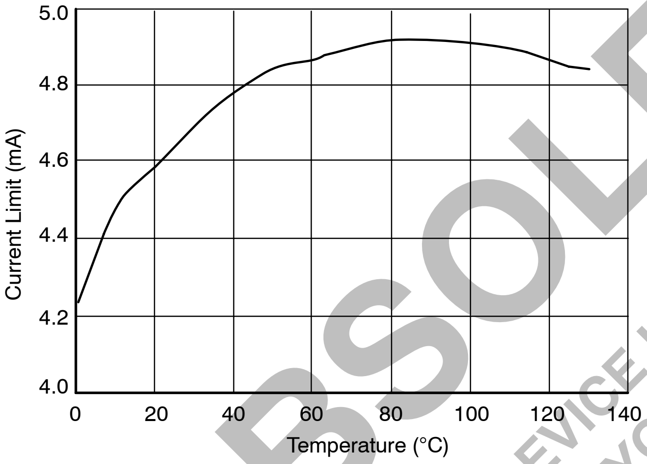


Figure 10. AuxDrv Current Limit vs. Junction Temperature

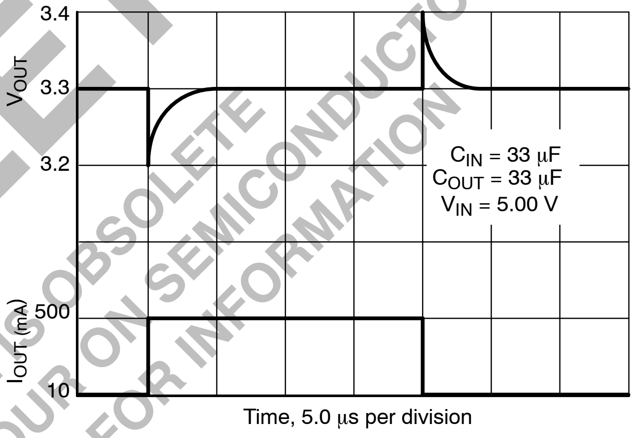
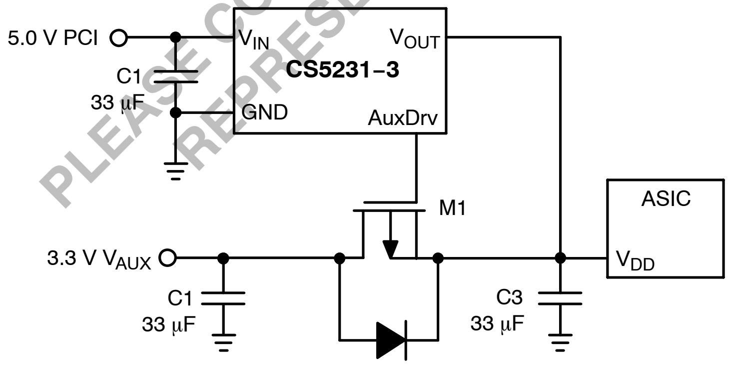


Figure 11. Transient Response



* indicates PFET body diode

Figure 12. Application Circuit

APPLICATION INFORMATION

THEORY OF OPERATION

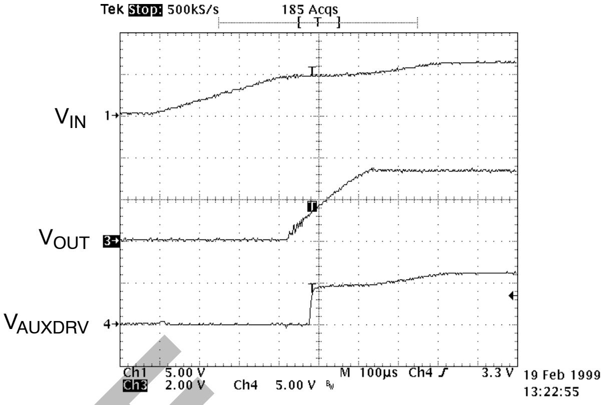
The CS5231−3 is a fixed 3.3 V linear regulator that contains an auxiliary drive control feature. When V_{IN} is greater than the typical 4.5 V threshold, the IC functions as a linear regulator. It provides up to 500 mA of current to a load through a composite PNP−NPN pass transistor. An output capacitor greater than 10 μF with equivalent series resistance less than 1.0 Ω is required for compensation. More information is provided in the Stability Considerations section.

The CS5231−3 provides an auxiliary drive feature that allows a load to remain powered even if the V_{IN} supply for the IC is absent. An external p−channel FET is the only additional component required to implement this function if an auxiliary power supply is available. The PFET gate is connected to the AuxDrv lead. The PFET drain is connected to the auxiliary power supply, and the PFET source is connected to the load. The polarity of this connection is very important, since the PFET body diode will be connected between the load and the auxiliary supply. If the PFET is connected with its drain to the load and its source to the supply, the body diode will be forward−biased if the auxiliary supply is turned off. This will result in the linear regulator providing current to everything on the auxiliary supply rail.

The AuxDrv lead is internally connected to a 10 kΩ resistor and to a saturating NPN transistor that acts as a switch. If the V_{IN} supply is off, the AuxDrv output will connect the PFET gate to ground through the 10 kΩ resistor, and the PFET will conduct current to the load.

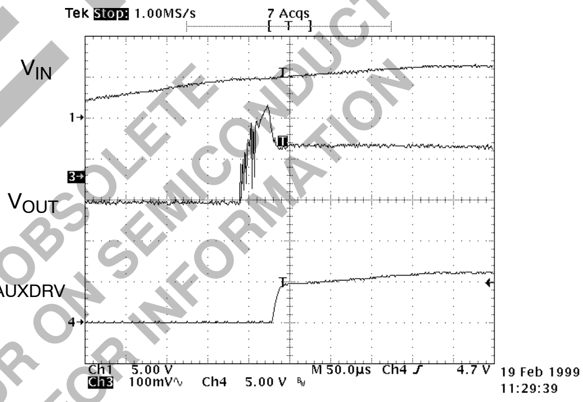
As the V_{IN} supply begins to rise, the AuxDrv lead will also rise until it reaches a typical voltage of about 650 mV. The NPN transistor connected to the AuxDrv lead will saturate at this point, and the gate of the PFET will be pulled down to a typical voltage of about 100 mV. The PFET will continue to conduct current to the load.

The V_{IN} supply voltage will continue to rise, but the linear regulator output is disabled until V_{IN} reaches a typical threshold of 4.5 V. During this time, the load continues to be powered by the auxiliary driver. Once the 4.5 V V_{IN} threshold is reached, the saturating NPN connected to the AuxDrv lead turns off. The on−chip 10 kΩ pull−up resistor will pull the PFET gate up to V_{IN}, thus turning the PFET off. The linear regulator turns on at the same time. An external compensation capacitor is required for the linear regulator to be stable, and this capacitance also serves as a charge reservoir to minimize any “glitching” that might result during the supply changeover. Hysteresis is present in the AuxDrv circuitry, requiring V_{IN} to drop by 100 mV (typical) after the linear regulator is providing power to the load before the AuxDrv circuitry can be re−enabled.



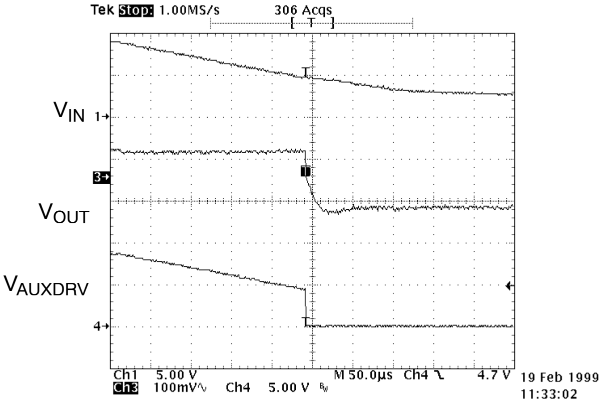
I_{OUT} = STARTUP 375 mA

Figure 13. Initial Power−Up, V_{AUX} Not Present R_{OUT} = 8.8 Ω



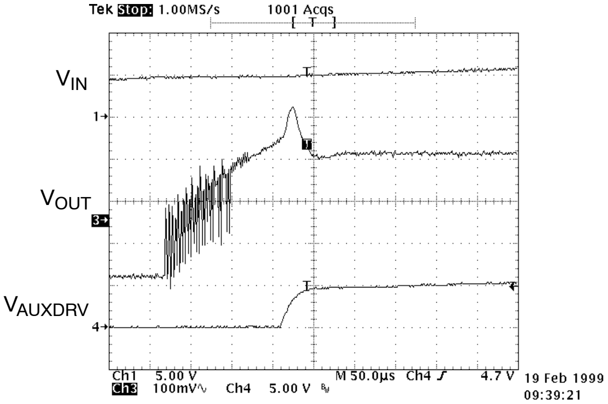
I_{OUT} = 375 mA V_{AUX} = 3.30 V

Figure 14. Power−Up, V_{AUX} = 3.3 V. Note the “Oscillatory Performance” as the Linear Regulator Changes the V_{OUT} Node. $I_{OUT} \times R_{DS(ON)} \approx$ 130 mV



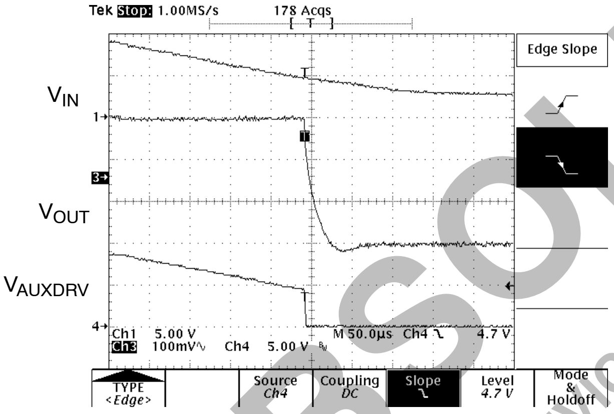
I_{OUT} = 375 mA V_{AUX} = 3.30

Figure 15. Power−Down, V_{AUX} = 3.3 V. Again, Note $\Delta V = I\ R_{DS(ON)} \approx$ 130 mV



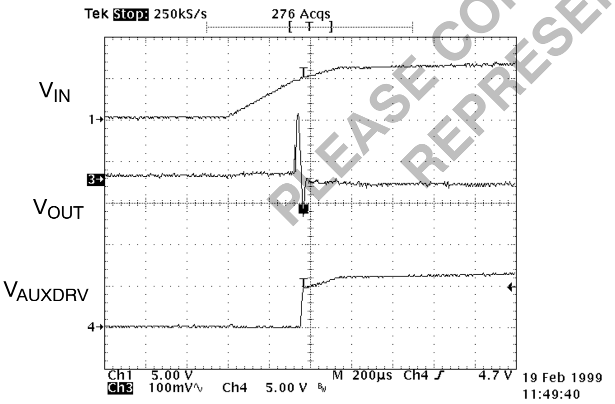
I_{OUT} = 375 mA V_{AUX} = 3.135 V

Figure 16. Power−Up, V_{AUX} = 3.135 V. The “Oscillatory Performance” Mode Lasts Longer Because the Difference Between V_{AUX} and 3.3 is Greater



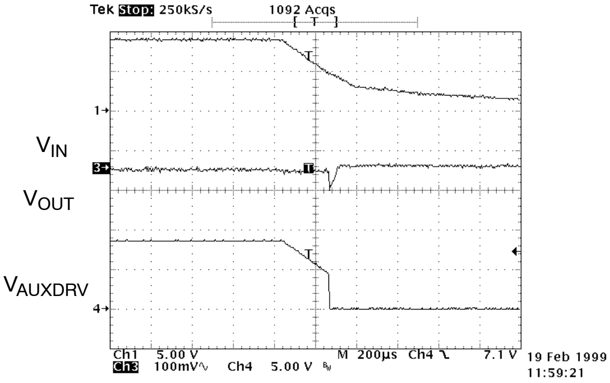
I_{OUT} = 375 mA V_{AUX} = 3.135

Figure 17. Power−Down, V_{AUX} = 3.135 V. The Difference in Voltage is Now $I_{OUT} \times R_{DS(ON)}$ Plus the Difference in Supply Voltages (3.3 − V_{AUX})



I_{OUT} = 375 mA V_{AUX} = 3.465

Figure 18. Power−Up, V_{AUX} = 3.465 V. $I_{OUT} \times R_{DS(ON)}$ is Compensated By Higher Value of V_{AUX}



I_{OUT} = 375 mA V_{AUX} = 3.465

Figure 19. Power−Down, V_{AUX} = 3.465 V

STABILITY CONSIDERATIONS

The output capacitor helps determine three main characteristics of a linear regulator: startup, transient response and stability.

Startup is affected because the output capacitor must be charged. At initial startup, the V_{IN} supply may not be present, and the output capacitor will be charged through the PFET. The PFET will initially provide current to the load through its body diode. The diode will act as a voltage follower until sufficient voltage is present to turn the FET on. Since most commercial power supplies have a fairly low ramp rate, charging through the body diode should effectively limit in−rush current to the capacitor.

During normal operation, transient load current requirements will be satisfied from the charge stored in the output capacitor until either the linear regulator or the auxiliary supply can respond. Larger values of capacitance will improve transient response, but will also cost more. A linear regulator will respond within microseconds, where an external power supply may take milliseconds to react. The output capacitance will provide the difference in current until this occurs. The result will be an instantaneous voltage change at the output. This change is the product of the current change and the capacitor ESR:

$$\Delta V_{OUT} = \Delta I_{LOAD} \times ESR$$

This limitation directly affects load regulation. Capacitor ESR must be minimized if output voltage must be maintained within tight tolerances. In such a case, it is often advisable to use a parallel network of different types of capacitors. For example, electrolytic capacitors provide high charge storage capacity in a small size, while tantalum capacitors have low ESR. The parallel combination will result in a high capacity, low ESR network. It is also important to physically locate the capacitance network close to the load, and to connect the network to the load with wide PC board traces to minimize the metal resistance.

The CS5231−3 has been carefully designed to be stable for output capacitances greater than 10 μF with equivalent series resistance less than 1.0 Ω. While careful board layout is important, the user should have a stable system if these constraints are met. A graph showing the region of stability for the CS5231−3 is included in the “Typical Performance Characteristics” section of this datasheet.

INPUT CAPACITORS AND THE V_{IN} THRESHOLDS

A capacitor placed on the V_{IN} pin will help to improve transient response. During a load transient, the input capacitor serves as a charge “reservoir,” providing the needed extra current until the external power supply can respond. One of the consequences of providing this current is an instantaneous voltage drop at V_{IN} due to capacitor ESR. The magnitude of the voltage change is again the product of the current change and the capacitor ESR.

It is very important to consider the maximum current step that can exist in the system. If the change in current is large enough, it is possible that the instantaneous voltage drop on V_{IN} will exceed the V_{IN} threshold hysteresis, and the IC will enter a mode of operation resembling an oscillation. As the part turns on, the output current I_{OUT} will increase, reaching current limit during initial charging. Increasing I_{OUT} results in a drop at V_{IN} such that the shutdown threshold is reached. The part will turn off, and the load current will decrease. As I_{OUT} decreases, V_{IN} will rise and the part will turn on, starting the cycle all over again. This oscillatory operation is most likely at initial start−up when the output capacitance is not charged, and in cases where the ramp−up of the V_{IN} supply is slow. It may also occur during the power transition when the regulator turns on and the PFET turns off. A 15 μs delay exists between turn−on of the regulator and the AuxDrv pin pulling the gate of the PFET high. This delay prevents “chatter” during the power transitions. During this interval, the linear regulator will attempt to regulate the output voltage as 3.3 V. If the output voltage is significantly below 3.3 V, the IC will go into current limit while trying to raise V_{OUT}. It is a short−lived phenomenon and is mentioned here to alert the user that the condition can exist. It is typically not a problem in applications. Careful choice of the PFET switch with respect to $R_{DS(ON)}$ will minimize the voltage drop which the output must charge through to return to a regulated state. More information is provided in the section on choosing the PFET switch.

If required, using a few capacitors in parallel to increase the bulk charge storage and reduce the ESR should give better performance than using a single input capacitor. Short, straight connections between the power supply and V_{IN} lead along with careful layout of the PC board ground plane will reduce parasitic inductance effects. Wide V_{IN} and V_{OUT} traces will reduce resistive voltage drops.

CHOOSING THE PFET SWITCH

The choice of the external PFET switch is based on two main considerations. First, the PFET should have a very low turn−on threshold. Choosing a switch transistor with $V_{GS(ON)} \approx 1.0$ V will ensure the PFET will be fully enhanced with only 3.3 V of gate drive voltage. Second, the switch transistor should be chosen to have a low $R_{DS(ON)}$ to minimize the voltage drop due to current flow in the switch. The formula for calculating the maximum allowable on−resistance is

$$R_{DS(ON)MAX} = \frac{V_{AUX(MIN)} - V_{OUT(MIN)}}{1.5 \times I_{OUT(MAX)}}$$

where $V_{AUX(MIN)}$ is the minimum value of the auxiliary supply voltage, $V_{OUT(MIN)}$ is the minimum allowable output voltage, $I_{OUT(MAX)}$ is the maximum output current and 1.5 is a “fudge factor” to account for increases in $R_{DS(ON)}$ due to temperature.

OUTPUT VOLTAGE SENSING

It is not possible to remotely sense the output voltage of the CS5231−3 since the feedback path to the error amplifier is not externally available. It is important to minimize voltage drops due to metal resistance of high current PC board traces. Such voltage drops can occur in both the supply traces and the return traces.

The following board layout practices will help to minimize output voltage errors:

- Always place the linear regulator as close to both load and output capacitors as possible.
- Always use the widest possible traces to connect the linear regulator to the capacitor network and to the load.
- Connect the load to ground through the widest possible traces.
- Connect the IC ground to the load ground trace at the point where it connects to the load.

CURRENT LIMIT

The CS5231−3 has internal current limit protection. Output current is limited to a typical value of 850 mA, even under output short circuit conditions. If the load current drain exceeds the current limit value, the output voltage will be pulled down and will result in an out of regulation condition. The IC does not contain circuitry to report this fault.

THERMAL SHUTDOWN

The CS5231−3 has internal temperature monitoring circuitry. The output is disabled if junction temperature of the IC reaches 180°C. Thermal hysteresis is typically 25°C and allows the IC to recover from a thermal fault without the need for an external reset signal. The monitoring circuitry is located near the composite PNP−NPN output transistor, since this transistor is responsible for most of the on−chip power dissipation. The combination of current limit and thermal shutdown will protect the IC from nearly any fault condition.

REVERSE CURRENT PROTECTION

During normal system operation, the auxiliary drive circuitry will maintain voltage on the V_{OUT} pin when V_{IN} is absent. IC reliability and system efficiency are improved by limiting the amount of reverse current that flows from V_{OUT} to ground and from V_{OUT} to V_{IN}. Current flows from V_{OUT} to ground through the feedback resistor divider that sets up the output voltage This resistor can range in value from 6.0 kΩ to about 10 kΩ, and roughly 500 μA will flow in the typical case. Current flow from V_{OUT} to V_{IN} will be limited to leakage current after the IC shuts down. On−chip RC time constants are such that the output transistor should be turned off well before V_{IN} drops below the V_{OUT} voltage.

CALCULATING POWER DISSIPATION AND HEATSINK REQUIREMENTS

Most linear regulators operate under conditions that result in high on−chip power dissipation. This results in high junction temperatures. Since the IC has a thermal shutdown feature, ensuring the regulator will operate correctly under normal conditions is an important design consideration. Some heatsinking will usually be required.

Thermal characteristics of an IC depend on four parameters: ambient temperature (T_A in °C), power dissipation (P_D in watts), thermal resistance from the die to the ambient air (θ_{JA} in °C per watt) and junction temperature (T_J in °C). The maximum junction temperature is calculated from the formula below:

$$T_{J(MAX)} = T_{A(MAX)} + (\theta_{JA} \times P_{D(MAX)})$$

Maximum ambient temperature and power dissipation are determined by the design, while θ_{JA} is dependent on the package manufacturer. The maximum junction temperature for operation of the CS5231−3 within specification is 150°C. The maximum power dissipation of a linear regulator is given as

$$\begin{aligned} P_{D(MAX)} = {} & (V_{IN(MAX)} - V_{OUT(MIN)}) \\ & \times (I_{LOAD(MAX)} + V_{IN(MAX)}) \\ & \times I_{GND(MAX)} \end{aligned}$$

where $I_{GND(MAX)}$ is the IC bias current.

It is possible to change the effective value of θ_{JA} by adding a heatsink to the design. A heatsink serves in some manner to raise the effective area of the package, thus improving the flow of heat from the package into the surrounding air. Each material in the path of heat flow has its own characteristic thermal resistance, all measured in °C per watt. The thermal resistances are summed to determine the total thermal resistance between the die junction and air. There are three components of interest: junction−to−case thermal resistance (θ_{JC}), case−to−heatsink thermal resistance (θ_{CS}) and heatsink−to−air thermal resistance (θ_{SA}). The resulting equation for junction−to−air thermal resistance is

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

The value of θ_{JC} both packages of the CS5231−3 are provided in the Packaging Information section of this data sheet. The value of θ_{CS} can be considered zero, since heat is conducted out of the D^2PAK package by the IC leads and the tab, and out of the SOIC−8 package by its IC leads that are soldered directly to the PC board.

Modification of θ_{SA} is the primary means of thermal management. For surface mount components, this means modifying the amount of trace metal that connects to the IC.

The thermal capacity of PC board traces is dependent on how much copper area is used, whether or not the IC is in direct contact with the metal, whether or not the metal surface is coated with some type of sealant, and whether or not there is airflow across the PC board. The chart provided below shows heatsinking capability of a square, single sided copper PC board trace. The area is given in square millimeters, and it is assumed there is no airflow across the PC board.

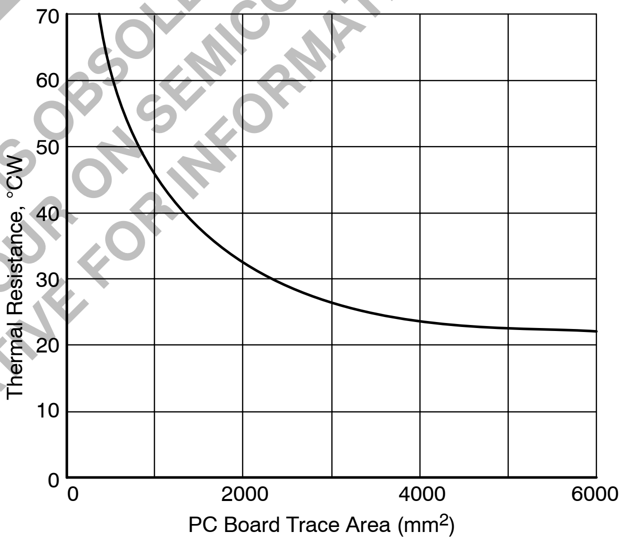


Figure 20. Thermal Resistance Capability of Copper PC Board Metal Traces

TYPICAL D²PAK PC BOARD HEATSINK DESIGN

A typical design of the PC board surface area needed for the D^2PAK package is shown on page 11. Calculations were made assuming $V_{IN(MAX)} = 5.25$ V, $V_{OUT(MIN)} = 3.266$ V, $I_{OUT(MAX)} = 500$ mA, $I_{GND(MAX)} = 5.0$ mA and $T_A = 70°C$.

$$\begin{aligned} P_D = {} & (5.25\text{ V} - 3.266\text{ V}) \times 0.5\text{ A} \\ & + (5.25\text{ V})(0.005\text{ A}) = 1018\text{ mW} \end{aligned}$$

Maximum temperature rise

$$\Delta T = T_{J(MAX)} - T_A = 150^\circ C - 70^\circ C = 80^\circ C$$

$$\theta_{JA}(\text{worst case}) = \Delta T / P_D = 80^\circ C / 1.018\text{ W} = 78.56^\circ C/W$$

First, we determine the need for heatsinking. If we assume the maximum θ_{JA} = 50 °C/W for the D^2PAK, the maximum temperature rise is found to be

$$\Delta T = P_D \times \theta_{JA} = 1.018\ W \times 50^\circ C/W = 50.9^\circ C$$

This is less than the maximum specified operating junction temperature of 125°C, and no heatsinking is required. Since the D^2PAK has a large tab, mounting this part to the PC board by soldering both tab and leads will provide superior performance with no PC board area penalty.

TYPICAL FUSED SOIC−8 DESIGN

We first determine the need for a heat sink for the SOIC−8 package at a load of 500 mA. Using the dissipation from the D^2PAK example of 1018 mW and the θ_{JA} of the SOIC−8 package of 110°C/W gives a temperature rise of 112°C. Adding this to an ambient temperature of 70°C gives 182°C junction temperature. This is an excessive temperature rise but it can be reduced by adding additional cooling in the form of added surface area of copper on the PCB. Using the relationship of maximum temperature rise of

$$\Delta T_{JA} = T_{J(MAX)} - T_A = 150^\circ C - 70^\circ C = 80^\circ C$$

We calculate the thermal resistance allowed from junction to air:

$$\theta_{JA}(\text{worst case}) = \Delta T_{JA}/P_D = 80^\circ C/1.018\ W = 79.6^\circ C/W$$

The thermal resistance from the die to the leads (case) is 25°C/W. Subtracting these two numbers gives the allowable thermal resistance from case to ambient:

$$\theta_{CA} = \theta_{JA} - \theta_{JC} = 79.6^\circ C/W - 25^\circ C/W = 54.6^\circ C/W$$

The thermal resistance of this copper area will be 54.6°C/W. We now look at Figure 20 and find the PCB trace area that will be less than 54.5°C/W. Examination shows that 750 mm^2 of copper will provide cooling for this part. This would be the SOIC−8 part with the center 4 ground leads soldered to pads in the center of a copper area about 27 mm × 27 mm. A lower dissipation or the addition of air−flow could result in a smaller required surface area.

DESCRIPTION

The CS5231−3 application circuit has been implemented as shown in the following pages. The schematic, bill of materials and printed circuit board artwork can be used to build the circuit. The design is very simple and consists of two capacitors, a p−channel FET and the CS5231−3. Five turret pins are provided for connection of supplies, meters, oscilloscope probes and loads. The CS5231−3 power supply management solution is implemented in an area less than 1.5 square inches. Due to the simplicity of the design, output current must be derated if the CS5231−3 is operated at V_{IN} voltages greater than 7.0 V. Figure 21 provides the derating curve on a maximum power dissipation if heatsink is added. Operating at higher power dissipation without CS5231−3 heatsink may result in a thermal shutdown condition.

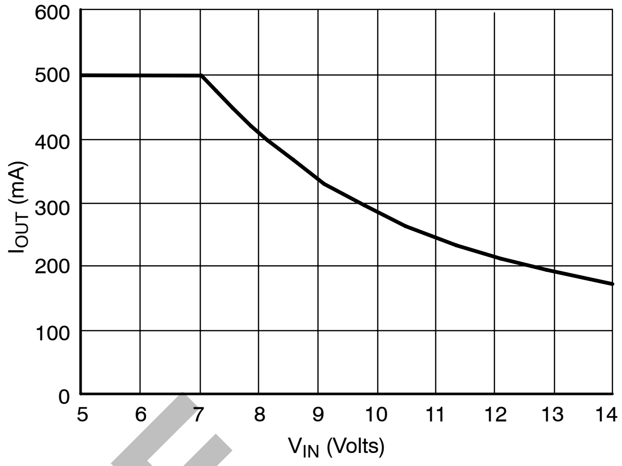


Figure 21. Demo Board Output Current Derating vs. V_{IN}

The V_{IN} Connection

The V_{IN} connection is denoted as such on the PC board. The maximum input voltage to the IC is 14 V before damage to the IC is possible. However, the specification range for the IC is 4.75 V < V_{IN} < 6.0 V.

The GND Connection

The GND connection ties the IC power return to two turret pins. The extra turret pin provides for connection of multiple instrument grounds to the demonstration board.

The AuxDrv Connection

The AuxDrv lead of the CS5231−3 is connected to the gate of the external PFET. This connection is also brought to a turret pin to allow easy connection of an oscilloscope probe for viewing the AuxDrv waveforms.

The V_{AUX} Connection

The V_{AUX} turret pin provides a connection point between an external 3.3 V supply and the PFET drain.

The V_{OUT} Connection

The V_{OUT} connection is tied to the V_{OUT} lead of the CS5231−3 and the PFET source. This point provides a convenient point at which some type of lead may be applied.

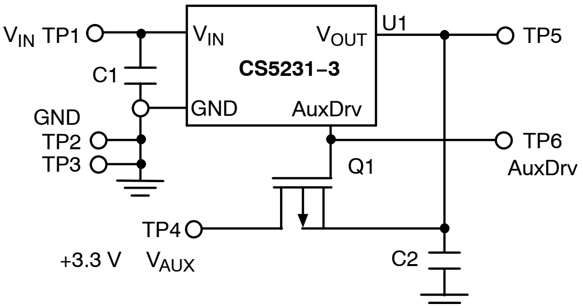


Figure 22. Application Circuit Schematic

PC Board Layout Artwork

The PC Board is a single layer copper design. The layout artwork is reproduced at actual size below.

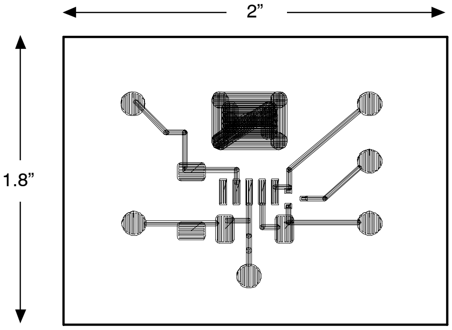


Figure 23. Top Copper Layer

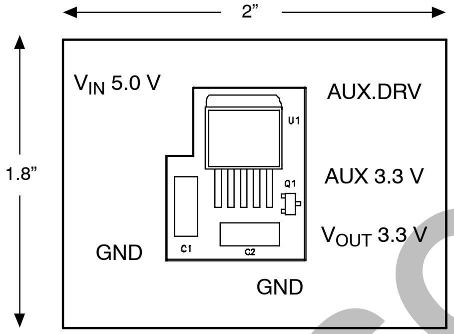


Figure 24. Top Silk Screen Layer

Test Description

The startup and supply transition waveforms shown in Figures 13 through 19 were obtained using the application circuit board with a resistive load of 8.8 Ω. This provides a DC load of 375 mA when the regulated output voltage is 3.3 V. A standard 2.0 A bench supply was used to provide power to the application circuit. The transient response waveforms shown in the Typical Performance Characteristics section were obtained by switching a 6.3 Ω resistor across the output.

Temperature Performance

The graph below shows thermal performance for the CS5231−3 across the normal operating output current range.

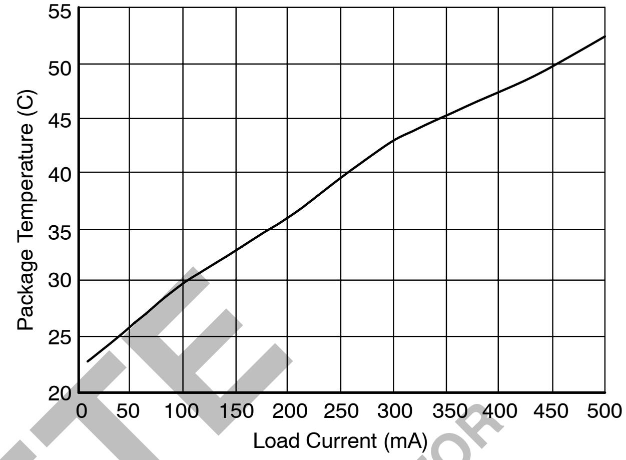


Figure 25. Package Temperature vs. Load Current (V_{IN} = 5.0 V, T_A = 23°C)

PFET $R_{DS(ON)}$ Performance

The graph provided below show typical $R_{DS(ON)}$ performance for the PFET. The data is provided as V_{DS} vs I_{OUT} for different values of V_{AUX}.

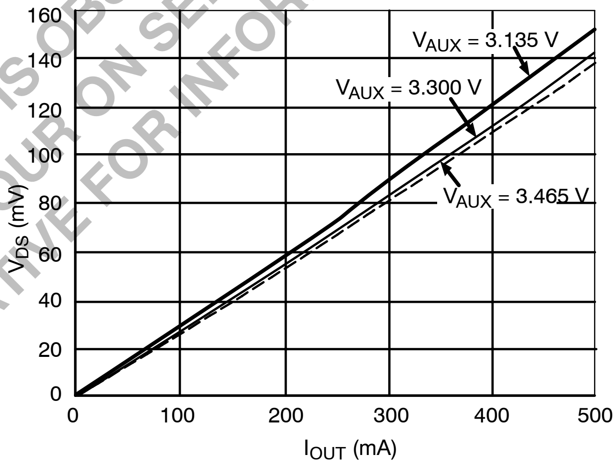


Figure 26. PFET V_{DS} vs. I_{OUT}

APPLICATIONS CIRCUIT BILL OF MATERIALS

Ref des	Description	Part Number	Manufacturer	Contact Information
C1, C2	33 μF, 16 V tantalum capacitors	TAJD336K016	AVX Corp	www.avxcorp.com 1−843−448−9411
Q1	p−channel FET transistor	MGSF1P02ELT1	ON Semiconductor	http://onsemi.com
U1	Linear regulator with auxiliary	CS5231−3DPS	ON Semiconductor	http://onsemi.com
T1−T6	Turret pins	40F6023	Newark Electronics	www.newark.com 1−800−463−9275

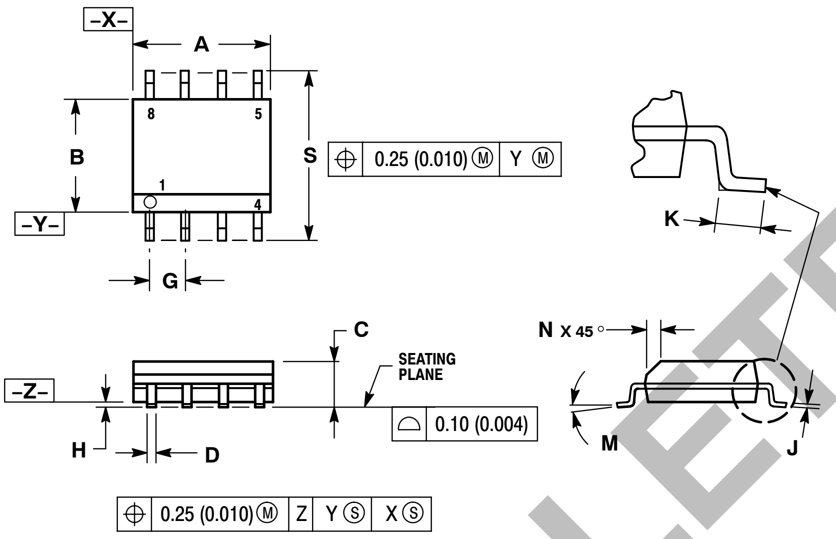
PACKAGE DIMENSIONS

D^{2}PAK−5
DP SUFFIX
CASE 936AC−01
ISSUE O

For D^{2}PAK Outline and Dimensions − Contact Factory

PACKAGE DIMENSIONS

SOIC−8
DF SUFFIX
CASE 751−07
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT

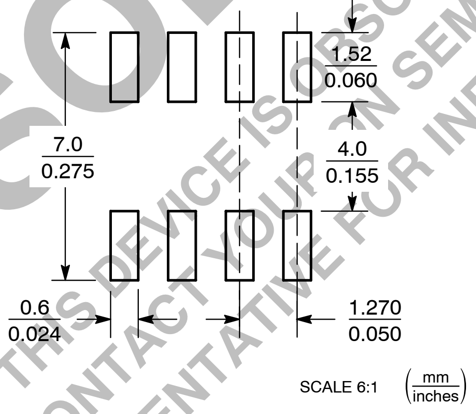


Figure 27. SOIC−8

PACKAGE THERMAL DATA

Parameter		D^2PAK−5	SOIC−8	Unit
$R_{\theta JC}$	Typical	2.5	25	°C/W
$R_{\theta JA}$	Typical	10−50*	110	°C/W

*Depending on thermal properties of substrate. $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$.

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