



**THE DATASHEET OF  
NVMFS5C673NLT1G**



# MOSFET – Power, Single N-Channel, DFN5/DFNW5

## 60 V, 9.2 mΩ, 50 A

### NVMFS5C673NL

#### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- NVMFS5C673NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	$V_{DSS}$	60	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	50	A
		$T_C = 100^\circ\text{C}$	35	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	46	W
		$T_C = 100^\circ\text{C}$	23	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	14	A
		$T_A = 100^\circ\text{C}$	10	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	Steady State	$T_A = 25^\circ\text{C}$	3.6	W
		$T_A = 100^\circ\text{C}$	1.8	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	290	A
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	52	A	
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 2.3 \text{ A}$ )	$E_{AS}$	88	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	

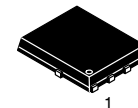
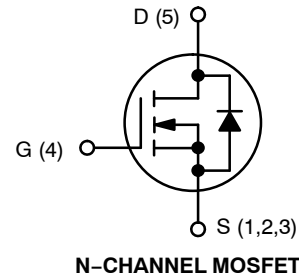
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE MAXIMUM RATINGS

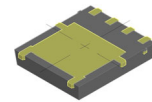
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	3.2	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	42	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
60 V	9.2 mΩ @ 10 V	50 A
	13 mΩ @ 4.5 V	

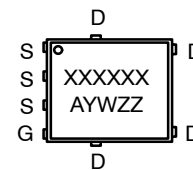


DFN5 (SO-8FL)  
CASE 488AA



DFNW5  
(FULL-CUT SO8FL WF)  
CASE 507BA

#### MARKING DIAGRAM



XXXXXX = 5C673L  
(NVMFS5C673NL) or  
673LWF  
(NVMFS5C673NLWF)

A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

#### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NVMFS5C673NL

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			28		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$		10	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		250	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

## ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 35\ \mu\text{A}$	1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-4.5		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 25\text{ A}$		7.7	9.2	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 25\text{ A}$		11	13	
Forward Transconductance	$g_{FS}$	$V_{DS} = 15\text{ V}, I_D = 25\text{ A}$		37		S

## CHARGES AND CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 25\text{ V}$		880		$\text{pF}$
Output Capacitance	$C_{OSS}$			450		
Reverse Transfer Capacitance	$C_{RSS}$			11		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V}, I_D = 25\text{ A}$		4.5		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}, I_D = 25\text{ A}$		9.5		nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}, I_D = 25\text{ A}$		1.0		nC
Gate-to-Source Charge	$Q_{GS}$			2.0		
Gate-to-Drain Charge	$Q_{GD}$			0.8		
Plateau Voltage	$V_{GP}$			2.9		

## SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}, I_D = 25\text{ A}, R_G = 2.5\ \Omega$		6.0		ns
Rise Time	$t_r$			25		
Turn-Off Delay Time	$t_{d(OFF)}$			16		
Fall Time	$t_f$			2.0		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 25\text{ A}$	$T_J = 25^\circ\text{C}$		0.9	1.2	V
			$T_J = 125^\circ\text{C}$		0.8		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, di/dt = 100\text{ A}/\mu\text{s}, I_S = 25\text{ A}$		28		ns	
Charge Time	$t_a$			14			
Discharge Time	$t_b$			14			
Reverse Recovery Charge	$Q_{RR}$			18			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

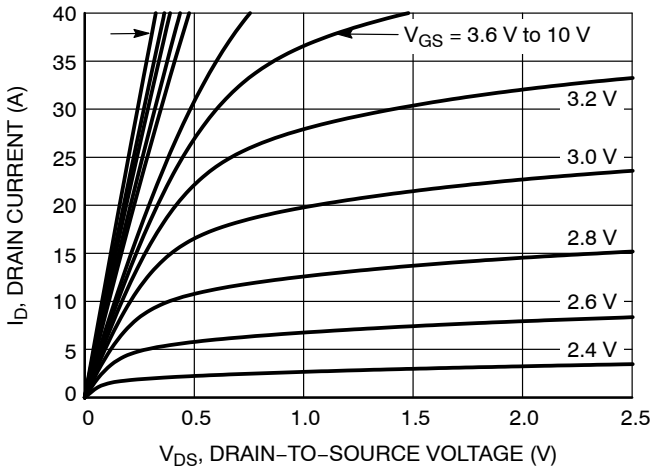


Figure 1. On-Region Characteristics

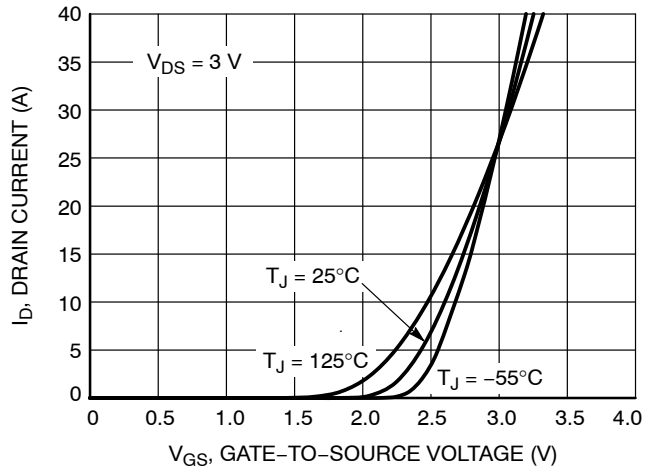


Figure 2. Transfer Characteristics

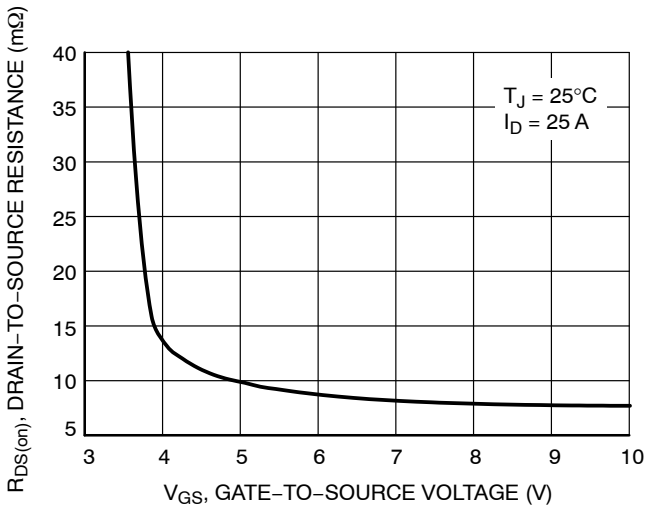


Figure 3. On-Resistance vs. Gate-to-Source Voltage

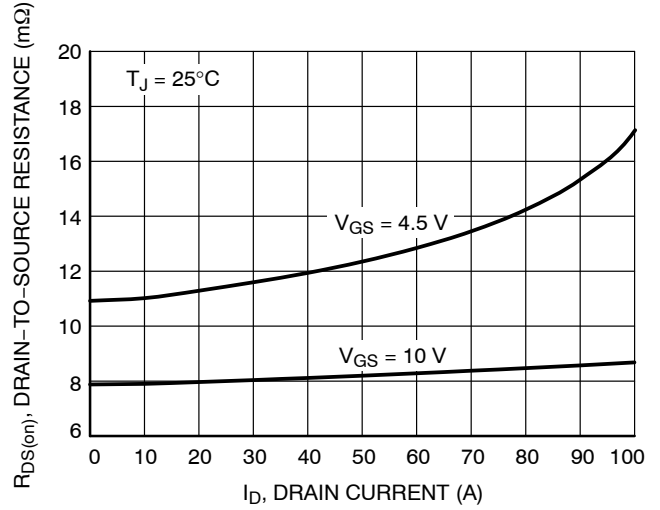


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

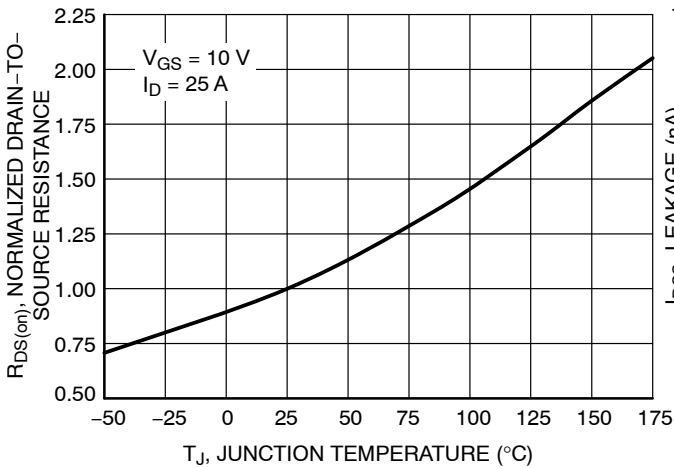


Figure 5. On-Resistance Variation with Temperature

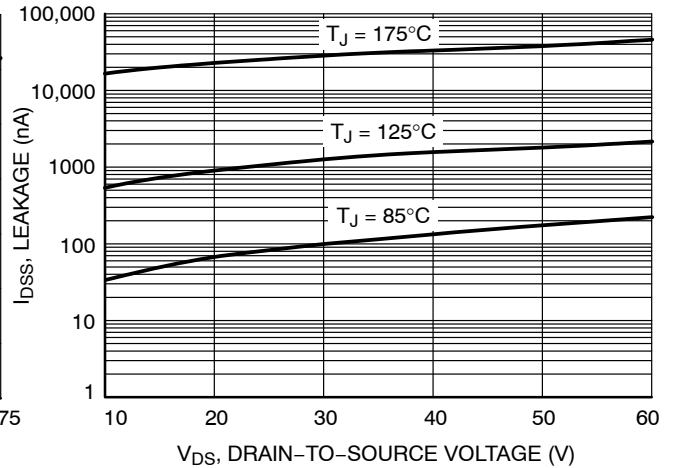


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NVMFS5C673NL

## TYPICAL CHARACTERISTICS

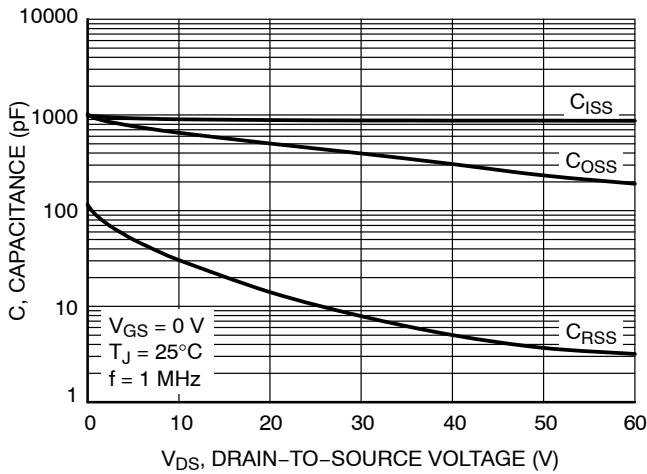


Figure 7. Capacitance Variation

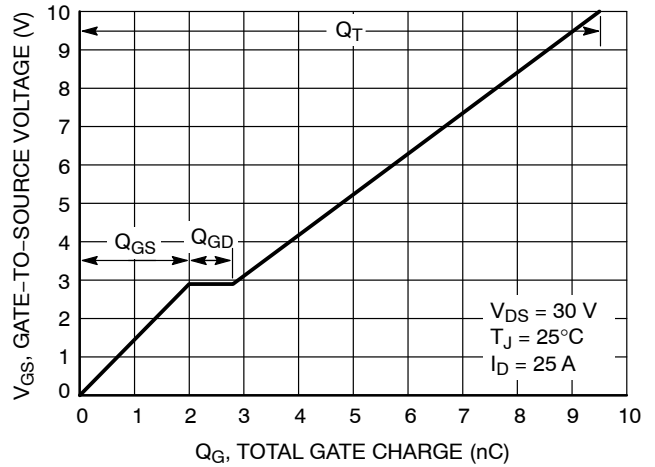


Figure 8. Gate-to-Source vs. Total Charge

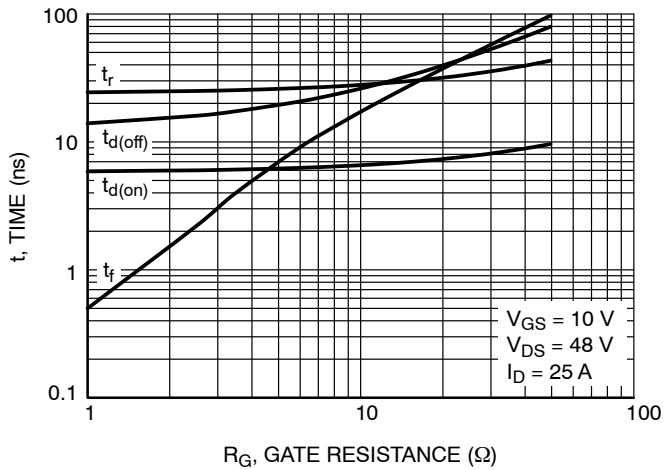


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

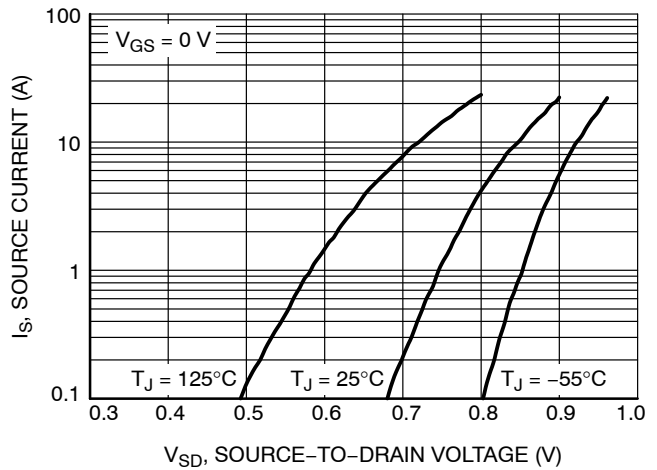


Figure 10. Diode Forward Voltage vs. Current

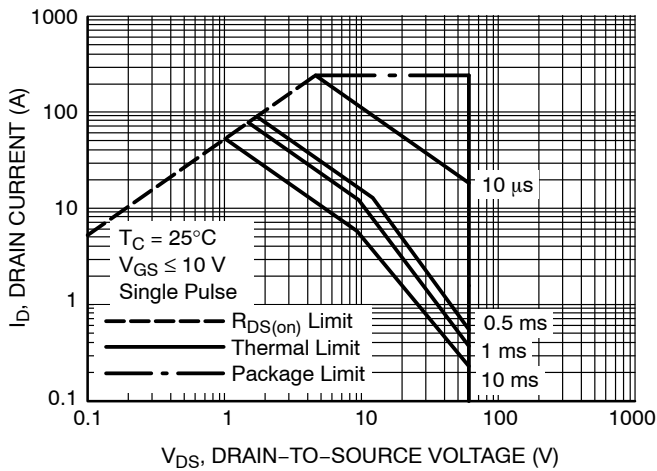


Figure 11. Maximum Rated Forward Biased Safe Operating Area

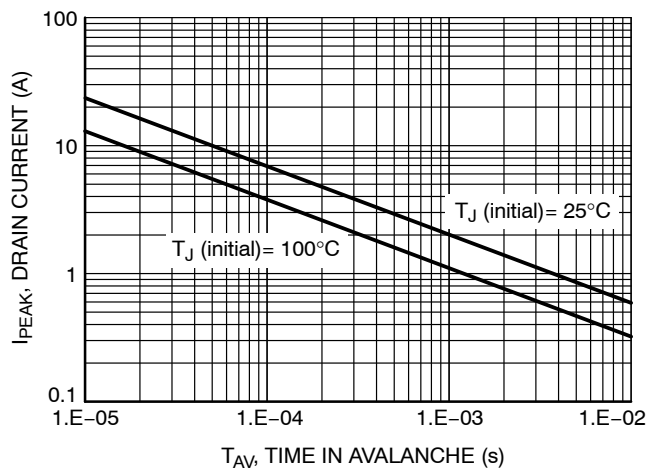


Figure 12. Maximum Drain Current vs. Time in Avalanche

# NVMFS5C673NL

## TYPICAL CHARACTERISTICS

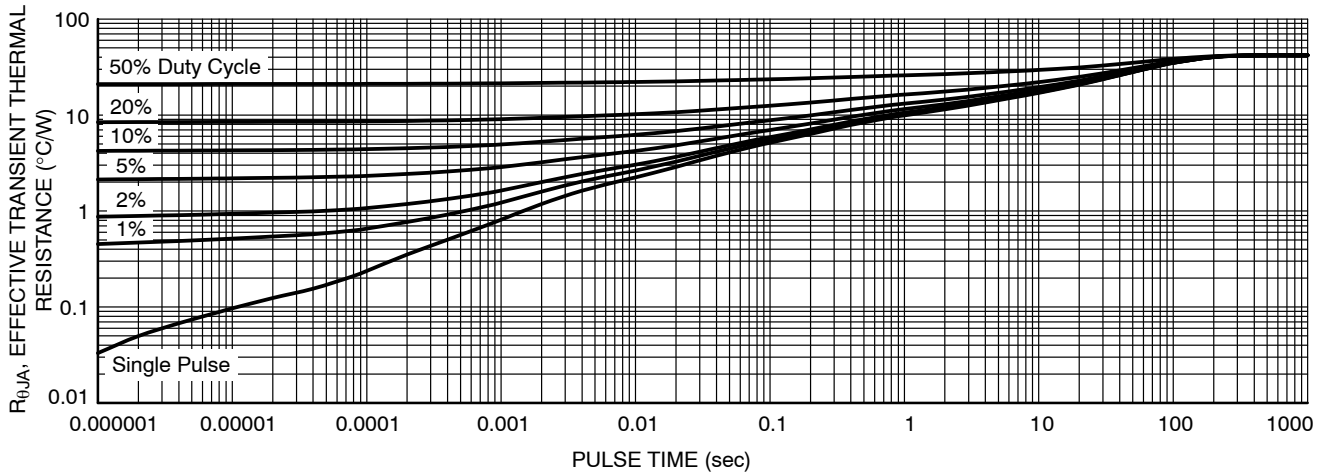


Figure 13. Thermal Characteristics

### DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
NVMFS5C673NLT1G	5C673L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C673NLWFT1G	673LWF	DFNW5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C673NLT3G	5C673L	DFN5 (Pb-Free)	5000 / Tape & Reel
NVMFS5C673NLWFT3G	673LWF	DFNW5 (Pb-Free, Wettable Flanks)	5000 / Tape & Reel
NVMFS5C673NLAFT1G	5C673L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C673NLAFT1G-YE	5C673L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C673NLWFAFT1G	673LWF	DFNW5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS



1  
SCALE 2:1

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE N

DATE 25 JUN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

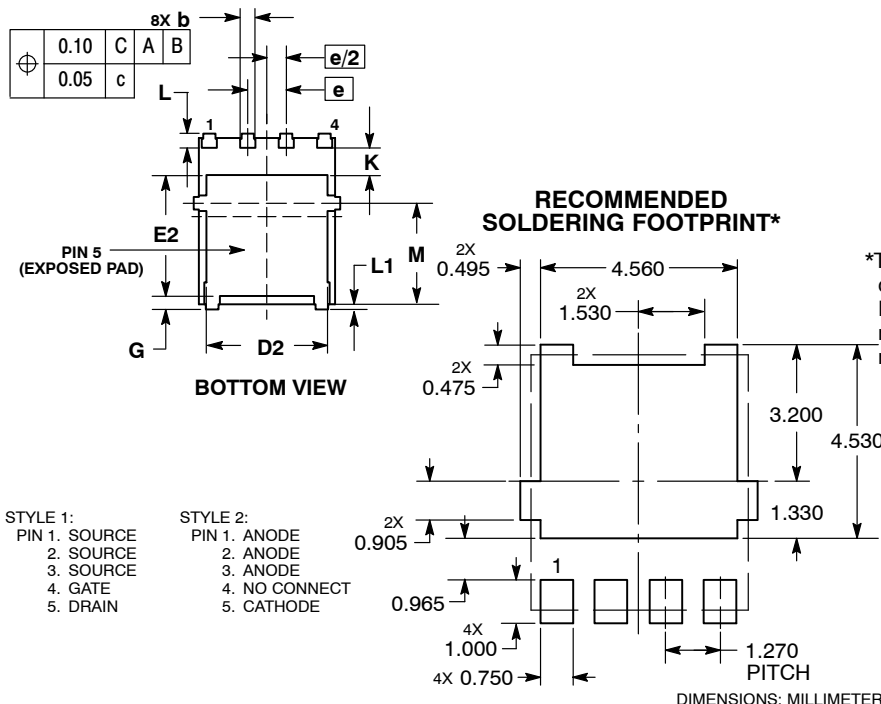
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



- STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN
- STYLE 2:  
PIN 1. ANODE  
2. ANODE  
3. ANODE  
4. NO CONNECT  
5. CATHODE

DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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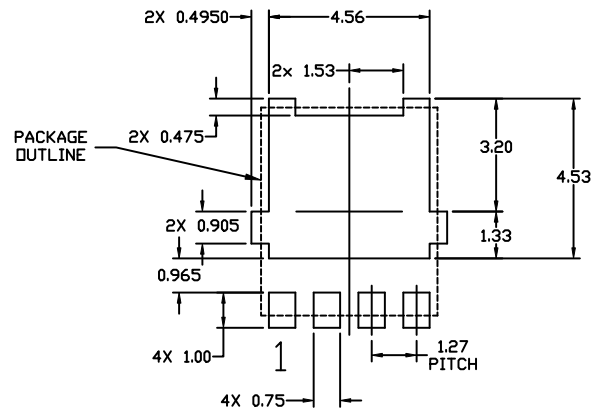
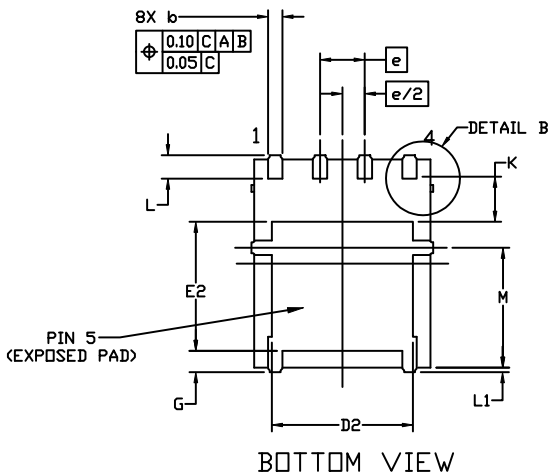
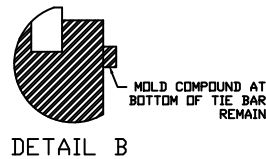
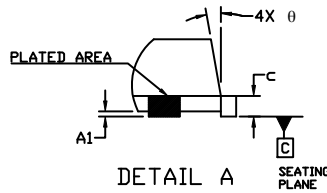
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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



## DFNW5 5x6 (FULL-CUT SO8FL WF) CASE 507BA ISSUE A

DATE 03 FEB 2021



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
  2. CONTROLLING DIMENSION: MILLIMETERS
  3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
  4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.150 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 W = Work Week  
 ZZ = Lot Traceability
- \*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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-  Alternative Solution
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