WINSOURCE ELECTRONICS

# THE DATASHEET OF

# BSC670N25NSFDATMA1

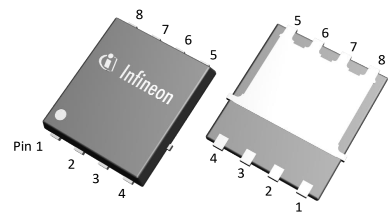
# MOSFET

**OptiMOS™3 Power-Transistor, 250 V**

## Features

- N-channel, normal level
- 175 °C rated
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[1] for target application
- Halogen-free according to IEC61249-2-21
- Ideal for high-frequency switching and synchronous rectification

PG-TDSON-8



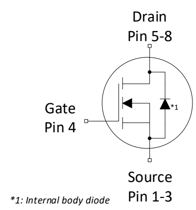




**Table 1 Key Performance Parameters**

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS}$ | 250 | V |
| $R_{DS(on),max}$ | 67 | mΩ |
| $I_D$ | 24 | A |

| Type / Ordering Code | Package | Marking | Related Links |
|---|---|---|---|
| BSC670N25NSFD | PG-TDSON-8 | 670N25NF | - |

[1] J-STD20 and JESD22

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# 1 Maximum ratings

at $T_A$=25 °C, unless otherwise specified

## Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current | $I_D$ | -<br>- | -<br>- | 24<br>19 | A | $T_C$=25 °C<br>$T_C$=100 °C |
| Pulsed drain current[1)] | $I_{D,pulse}$ | - | - | 96 | A | $T_C$=25 °C |
| Avalanche energy, single pulse | $E_{AS}$ | - | - | 69 | mJ | $I_D$=16 A, $R_{GS}$=25 Ω |
| Reverse diode d$v$/d$t$ | d$v$/d$t$ | - | - | 60 | kV/µs | $I_D$=46 A, $V_{DS}$=125 V,<br>d$i$/d$t$=1500 A/µs, $T_{j,max}$=175 °C |
| Gate source voltage | $V_{GS}$ | -20 | - | 20 | V | - |
| Power dissipation | $P_{tot}$ | - | - | 150 | W | $T_C$=25 °C |
| Operating and storage temperature | $T_j$, $T_{stg}$ | -55 | - | 175 | °C | - |

# 2 Thermal characteristics

## Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | $R_{thJC}$ | - | 0.6 | 1 | K/W | - |
| Thermal resistance, junction - ambient, minimal footprint | $R_{thJA}$ | - | - | 75 | K/W | - |
| Thermal resistance, junction - ambient, 6 cm$^2$ cooling area[2)] | $R_{thJA}$ | - | - | 50 | K/W | - |

# 3 Electrical characteristics

## Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 250 | - | - | V | $V_{GS}$=0 V, $I_D$=1 mA |
| Gate threshold voltage | $V_{GS(th)}$ | 2 | 3 | 4 | V | $V_{DS}$=$V_{GS}$, $I_D$=90 µA |
| Zero gate voltage drain current | $I_{DSS}$ | -<br>- | 0.1<br>10 | 1<br>100 | µA | $V_{DS}$=200 V, $V_{GS}$=0 V, $T_j$=25 °C<br>$V_{DS}$=200 V, $V_{GS}$=0 V, $T_j$=125 °C |
| Gate-source leakage current | $I_{GSS}$ | - | 1 | 100 | nA | $V_{GS}$=20 V, $V_{DS}$=0 V |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 59 | 67 | mΩ | $V_{GS}$=10 V, $I_D$=24 A |
| Gate resistance | $R_G$ | - | 3.3 | 5 | Ω | - |
| Transconductance | $g_{fs}$ | 24 | 47 | - | S | $\lvert V_{DS}\rvert>2\lvert I_D\rvert R_{DS(on)max}$, $I_D$=24 A |

[1)] See Diagram 3
[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm$^2$ (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

## Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | $C_{iss}$ | - | 1810 | 2410 | pF | $V_{GS}$=0 V, $V_{DS}$=125 V, $f$=1 MHz |
| Output capacitance[1] | $C_{oss}$ | - | 103 | 137 | pF | $V_{GS}$=0 V, $V_{DS}$=125 V, $f$=1 MHz |
| Reverse transfer capacitance | $C_{rss}$ | - | 5.4 | - | pF | $V_{GS}$=0 V, $V_{DS}$=125 V, $f$=1 MHz |
| Turn-on delay time | $t_{d(on)}$ | - | 8.0 | - | ns | $V_{DD}$=125 V, $V_{GS}$=10 V, $I_D$=12 A, $R_{G,ext}$=1.6 Ω |
| Rise time | $t_r$ | - | 3.6 | - | ns | $V_{DD}$=125 V, $V_{GS}$=10 V, $I_D$=12 A, $R_{G,ext}$=1.6 Ω |
| Turn-off delay time | $t_{d(off)}$ | - | 19 | - | ns | $V_{DD}$=125 V, $V_{GS}$=10 V, $I_D$=12 A, $R_{G,ext}$=1.6 Ω |
| Fall time | $t_f$ | - | 4.0 | - | ns | $V_{DD}$=125 V, $V_{GS}$=10 V, $I_D$=12 A, $R_{G,ext}$=1.6 Ω |

## Table 6 Gate charge characteristics[2]

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | $Q_{gs}$ | - | 8.2 | - | nC | $V_{DD}$=125 V, $I_D$=24 A, $V_{GS}$=0 to 10 V |
| Gate to drain charge | $Q_{gd}$ | - | 2.9 | - | nC | $V_{DD}$=125 V, $I_D$=24 A, $V_{GS}$=0 to 10 V |
| Switching charge | $Q_{sw}$ | - | 5.6 | - | nC | $V_{DD}$=125 V, $I_D$=24 A, $V_{GS}$=0 to 10 V |
| Gate charge total[1] | $Q_g$ | - | 22 | 30 | nC | $V_{DD}$=125 V, $I_D$=24 A, $V_{GS}$=0 to 10 V |
| Gate plateau voltage | $V_{plateau}$ | - | 4.5 | - | V | $V_{DD}$=125 V, $I_D$=24 A, $V_{GS}$=0 to 10 V |
| Output charge | $Q_{oss}$ | - | 48 | - | nC | $V_{DD}$=125 V, $V_{GS}$=0 V |

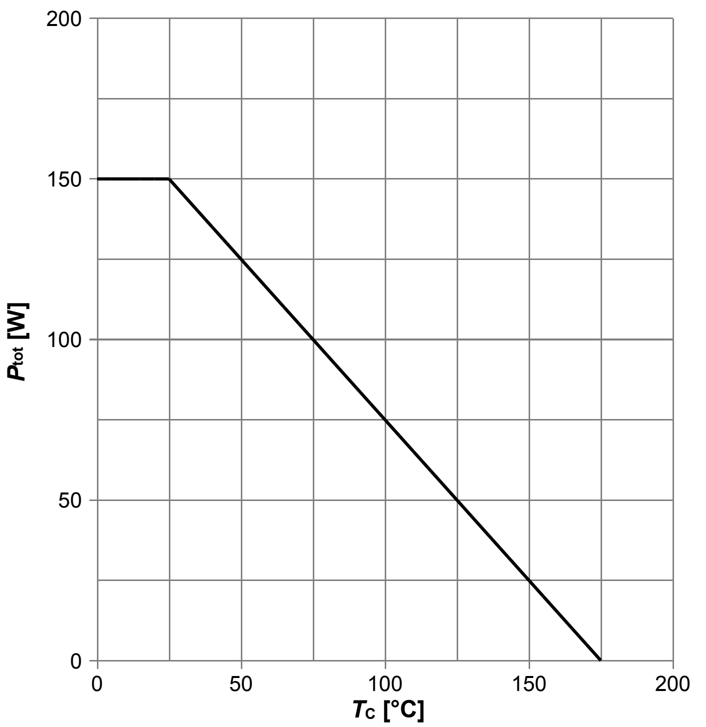
## Table 7 Reverse diode

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Diode continous forward current | $I_S$ | - | - | 24 | A | $T_C$=25 °C |
| Diode pulse current[3] | $I_{S,pulse}$ | - | - | 96 | A | $T_C$=25 °C |
| Diode hard commutation current[4] | $I_{S,hard}$ | - | - | 46 | A | $T_C$=25 °C, d$i_F$/d$t$=1500 A/µs |
| Diode forward voltage | $V_{SD}$ | - | 0.9 | 1.2 | V | $V_{GS}$=0 V, $I_F$=24 A, $T_j$=25 °C |
| Reverse recovery time[1] | $t_{rr}$ | - | 69 | 138 | ns | $V_R$=125 V, $I_F$=16.1A, d$i_F$/d$t$=100 A/µs |
| Reverse recovery charge[1] | $Q_{rr}$ | - | 153 | 306 | nC | $V_R$=125 V, $I_F$=16.1A, d$i_F$/d$t$=100 A/µs |

[1] Defined by design. Not subject to production test.
[2] See "Gate charge waveforms" for parameter definition
[3] Diode pulse current is defined by thermal and/or package limits
[4] Maximum allowed hard-commutated current through diode at di/dt=1500 A/µs

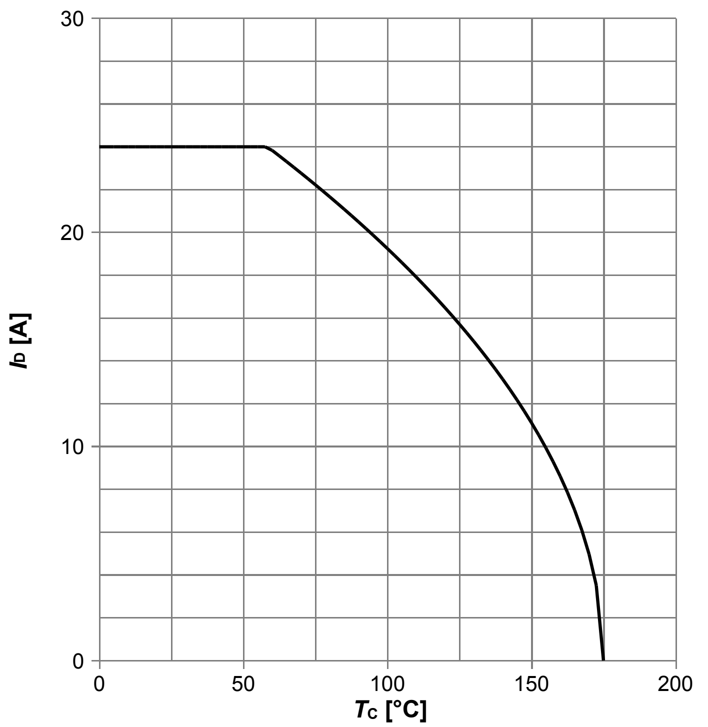
## 4 Electrical characteristics diagrams

**Diagram 1: Power dissipation**



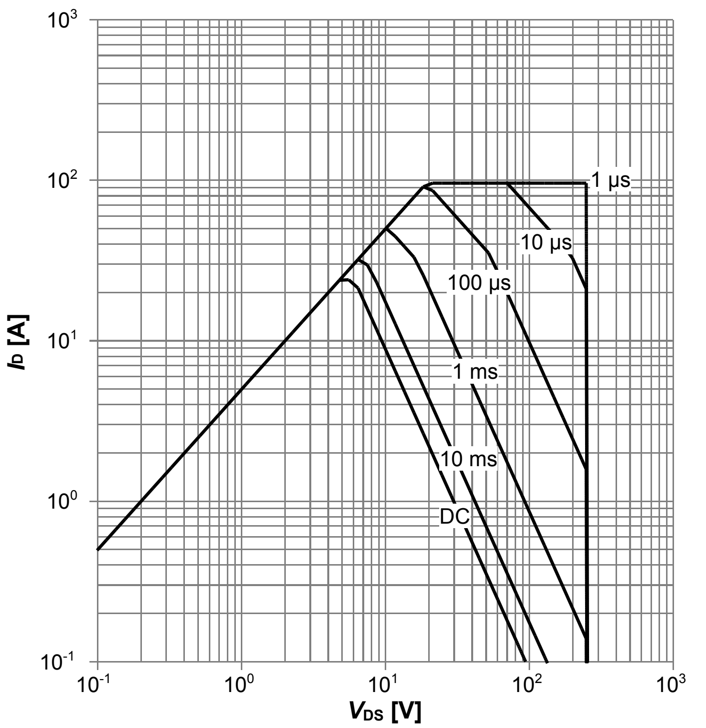

$P_{tot}$=f($T_C$)

**Diagram 2: Drain current**



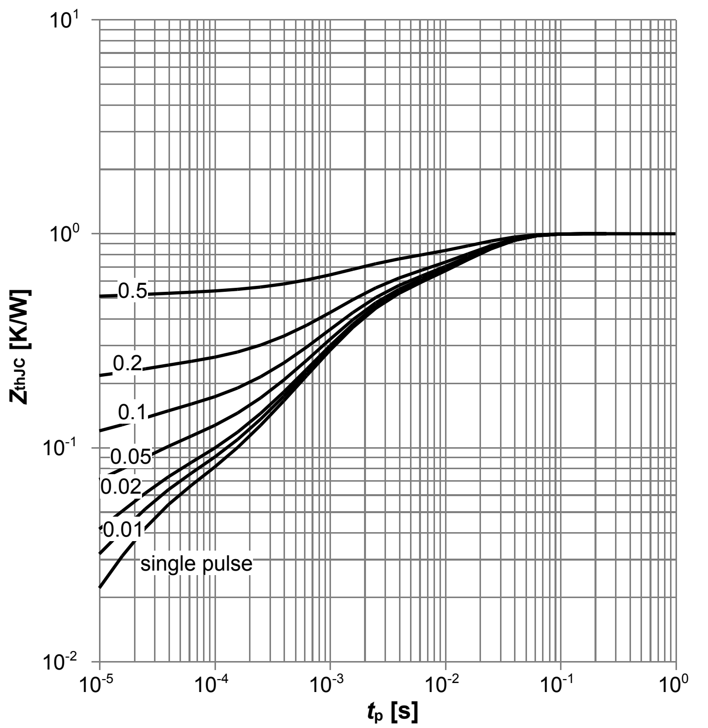

$I_D$=f($T_C$); $V_{GS}$>=10 V

**Diagram 3: Safe operating area**



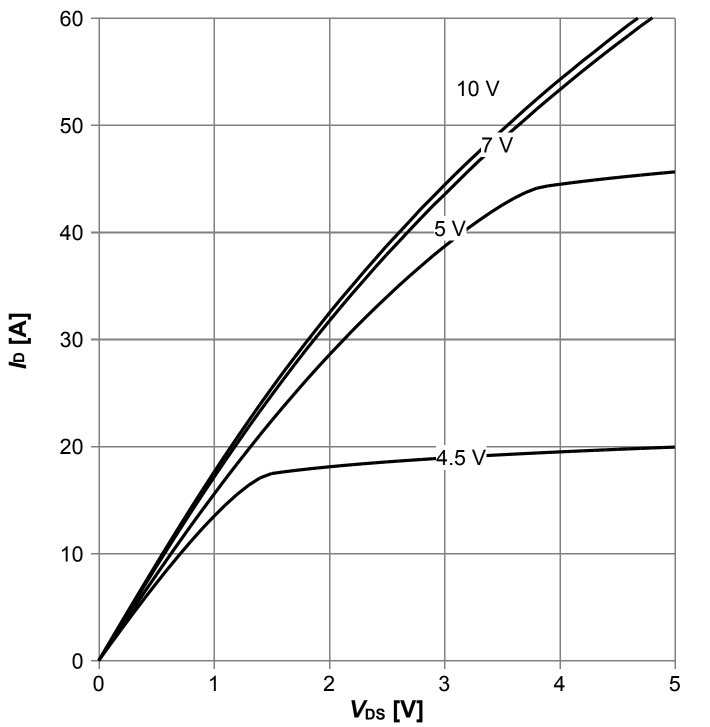

$I_D$=f($V_{DS}$); $T_C$=25 °C; $D$=0; parameter: $t_p$

**Diagram 4: Max. transient thermal impedance**



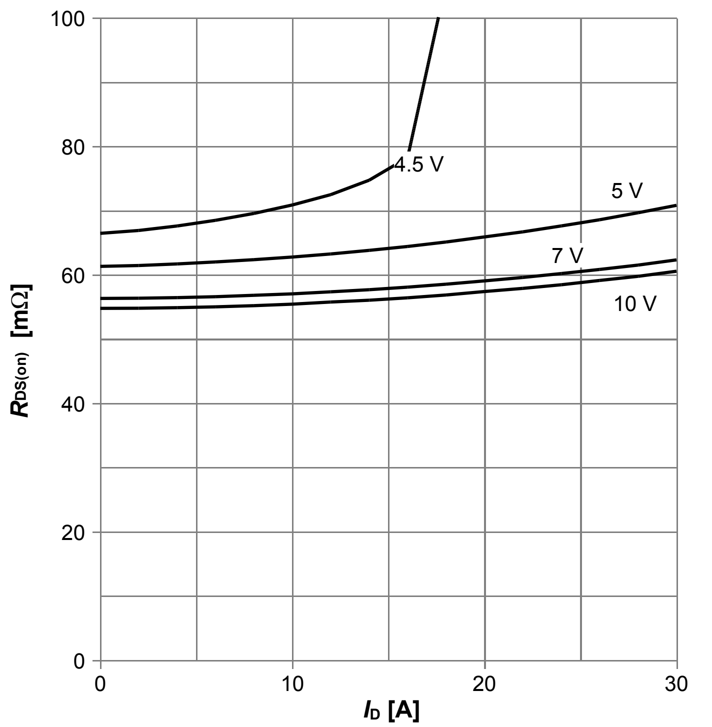

$Z_{thJC}$=f($t_p$); parameter: $D$=$t_p$/$T$

**Diagram 5: Typ. output characteristics**



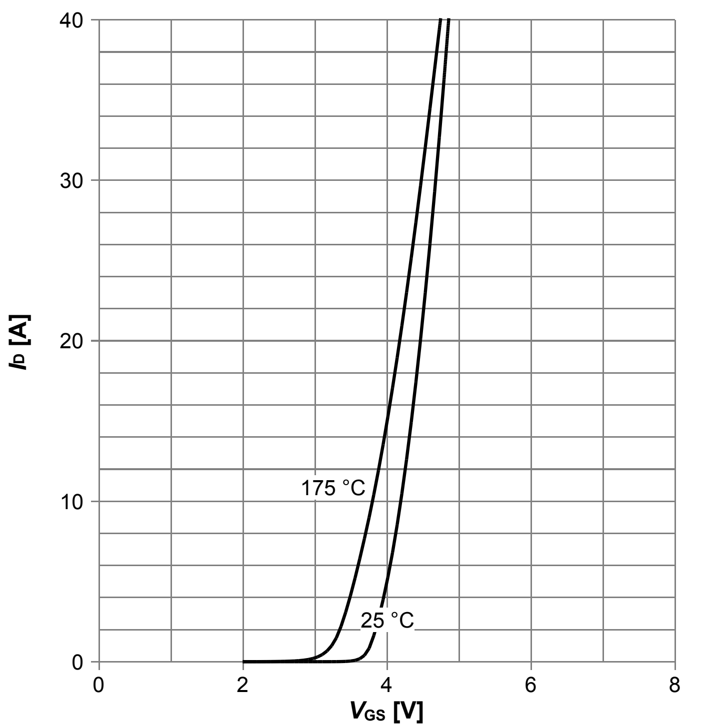

$I_D$=f($V_{DS}$); $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



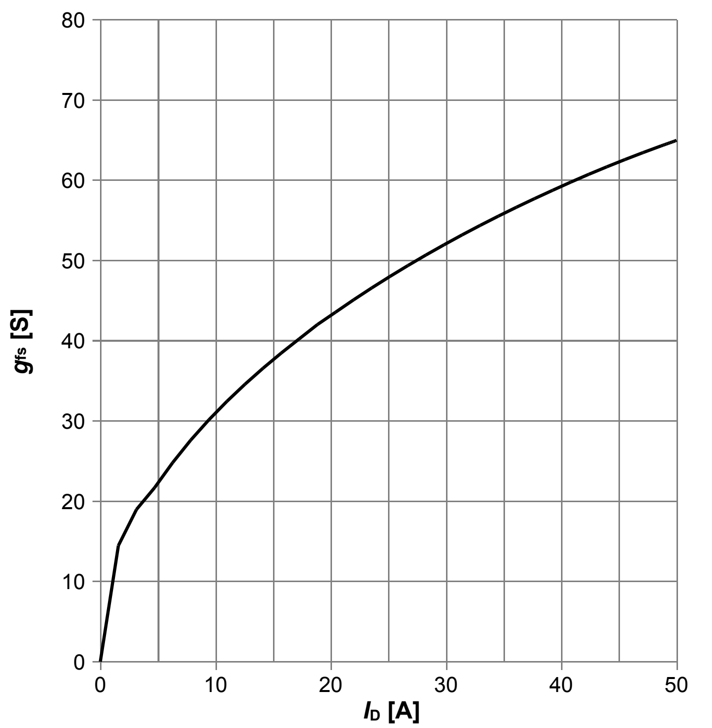

$R_{DS(on)}$=f($I_D$); $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



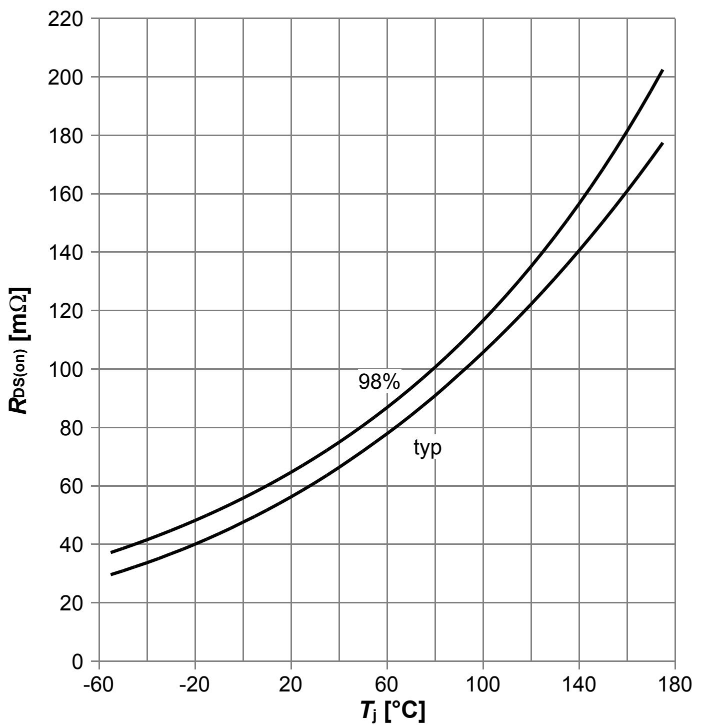

$I_D$=f($V_{GS}$); $|V_{DS}|$>2$|I_D|R_{DS(on)max}$; parameter: $T_j$

**Diagram 8: Typ. forward transconductance**



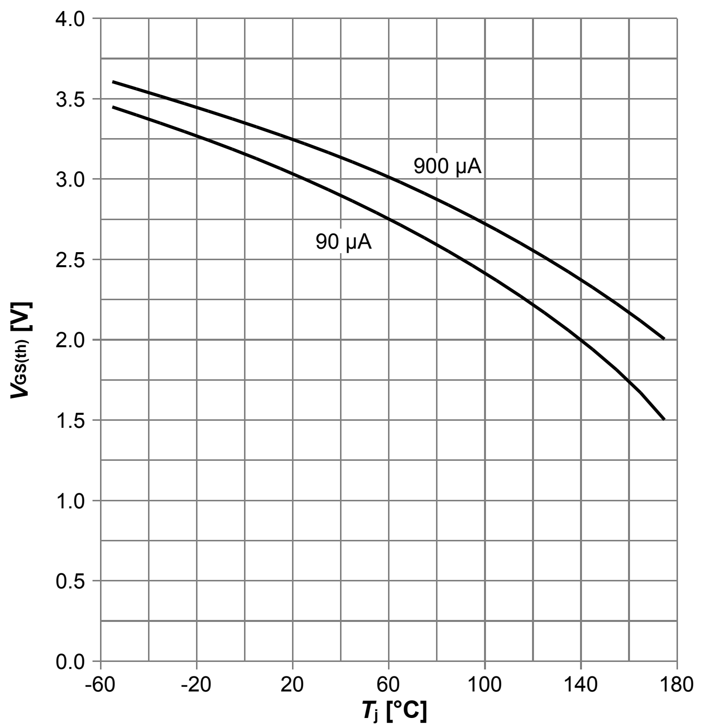

$g_{fs}$=f($I_D$); $T_j$=25 °C

**Diagram 9: Drain-source on-state resistance**



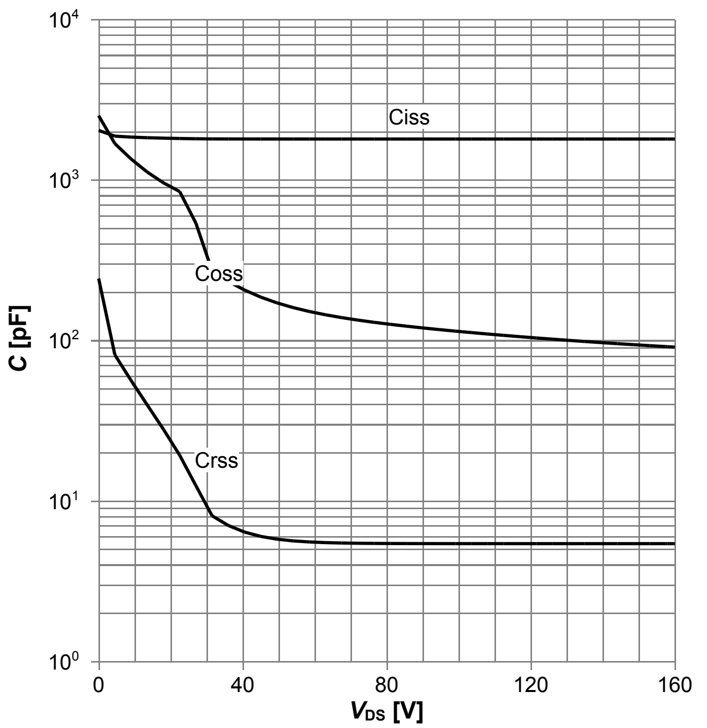

$R_{DS(on)}$=f($T_j$); $I_D$=24 A; $V_{GS}$=10 V

**Diagram 10: Typ. gate threshold voltage**



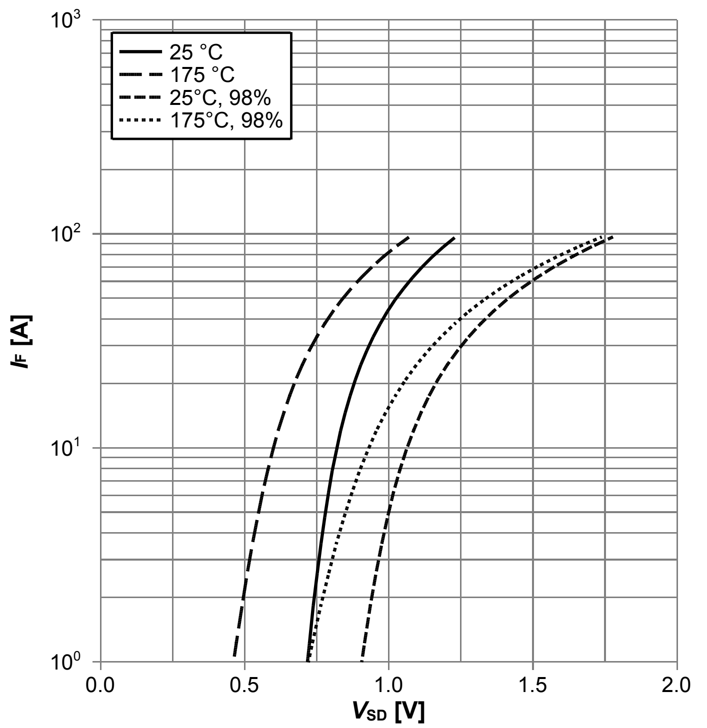

$V_{GS(th)}$=f($T_j$); $V_{GS}$=$V_{DS}$; parameter: $I_D$

**Diagram 11: Typ. capacitances**



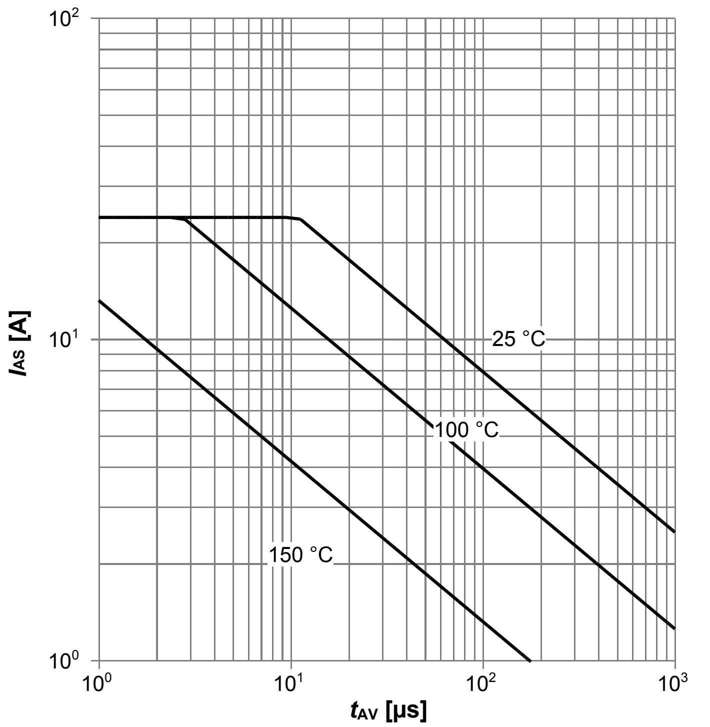

$C$=f($V_{DS}$); $V_{GS}$=0 V; $f$=1 MHz

**Diagram 12: Forward characteristics of reverse diode**



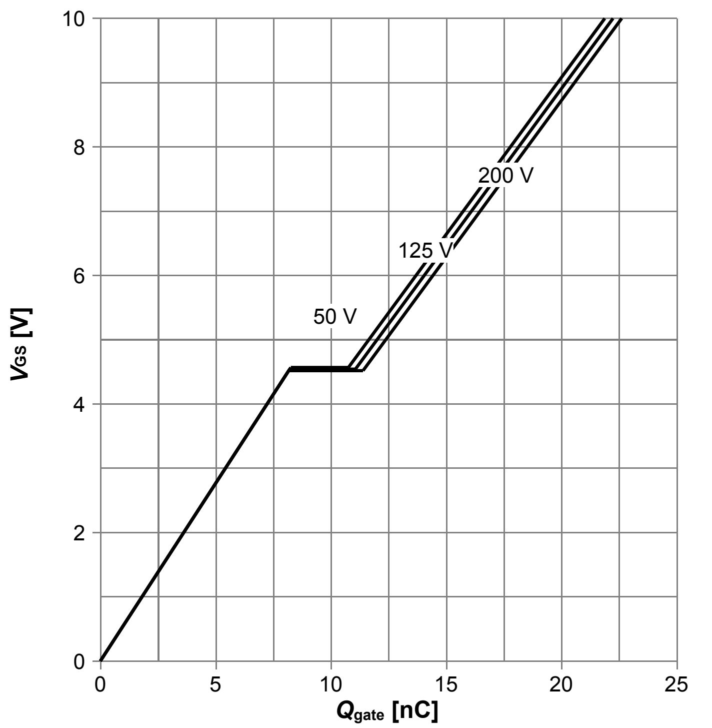

$I_F$=f($V_{SD}$); parameter: $T_j$

**Diagram 13: Avalanche characteristics**



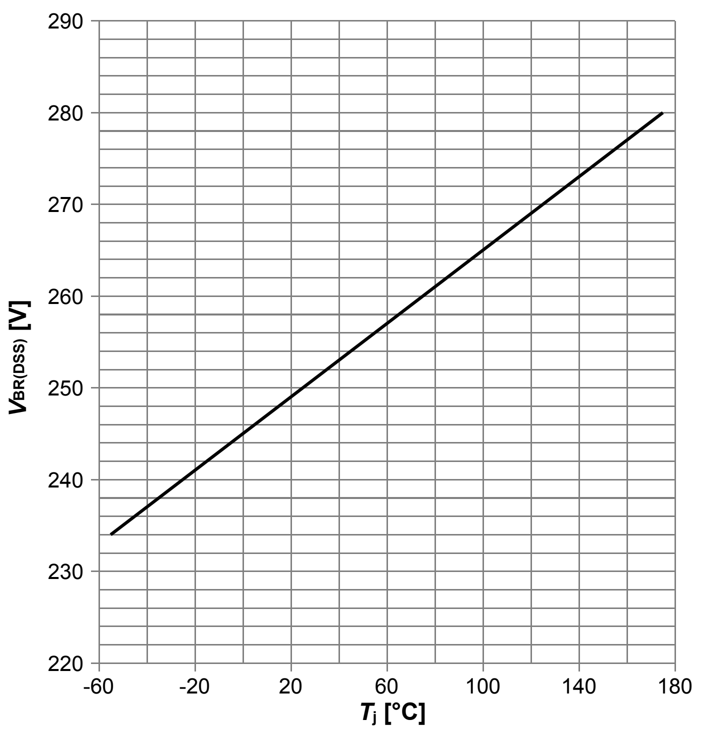

$I_{AS}$=f($t_{AV}$); $R_{GS}$=25 Ω; parameter: $T_{j(start)}$

**Diagram 14: Typ. gate charge**



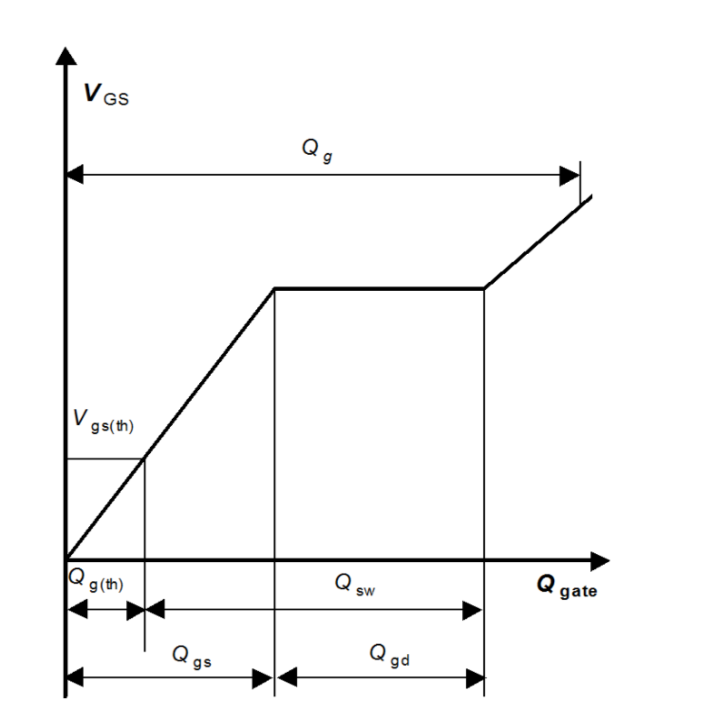

$V_{GS}$=f($Q_{gate}$); $I_D$=24 A pulsed; parameter: $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**

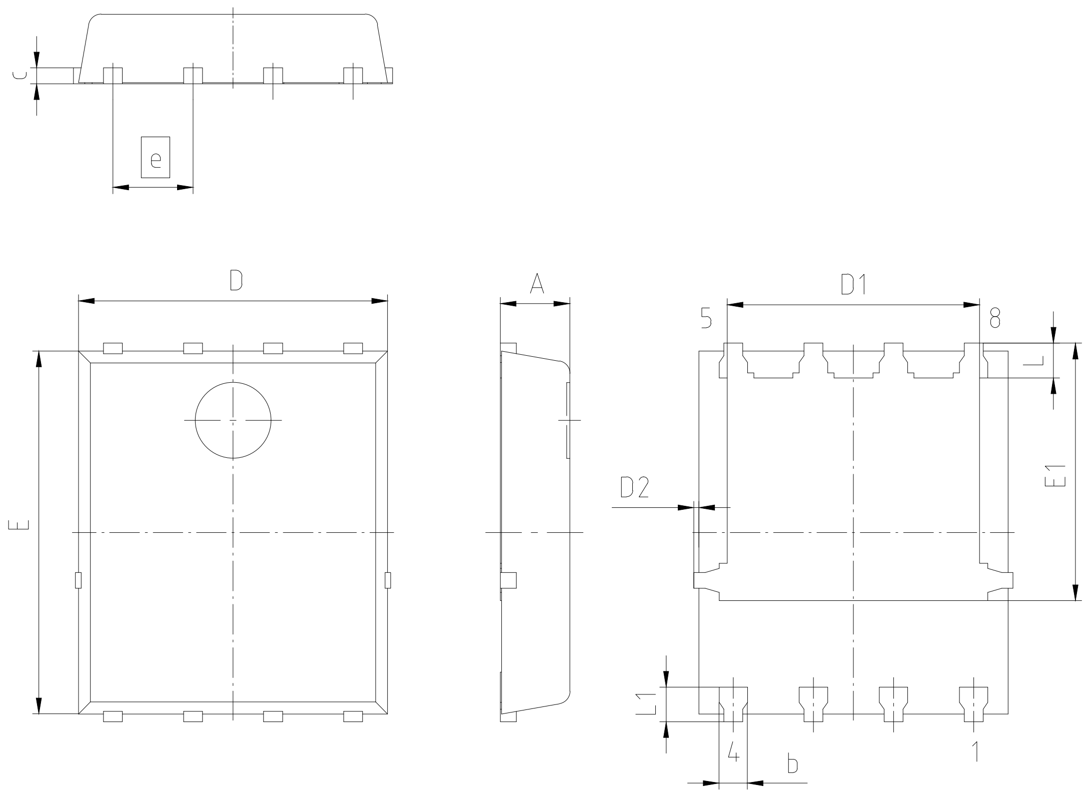



$V_{BR(DSS)}$=f($T_j$); $I_D$=1 mA

**Diagram Gate charge waveforms**



# 5 Package Outlines




| PACKAGE - GROUP NUMBER: | PG-TDSON-8-U08 | |
|---|---|---|
| DIMENSIONS | MILLIMETERS | |
| | MIN. | MAX. |
| A | 0.90 | 1.20 |
| b | 0.34 | 0.54 |
| c | 0.15 | 0.35 |
| D | 4.80 | 5.35 |
| D1 | 3.90 | 4.40 |
| D2 | 0.00 | 0.22 |
| E | 5.70 | 6.10 |
| E1 | 4.05 | 4.25 |
| e | 1.27 | |
| L | 0.45 | 0.65 |
| L1 | 0.45 | 0.65 |

1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
3) ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

**Figure 1 Outline PG-TDSON-8, dimensions in mm**

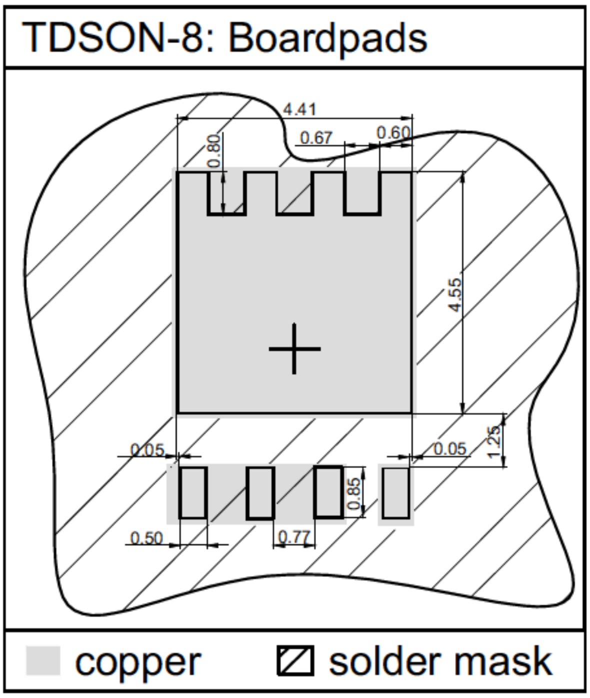



**Figure 2 Outline Footprint (TDSON-8)**

## Revision History

BSC670N25NSFD

**Revision: 2022-11-09, Rev. 2.2**

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|---|---|---|
| 2.0 | 2016-10-25 | Release of final version |
| 2.1 | 2016-12-05 | Update Eas |
| 2.2 | 2022-11-09 | Update package outline drawing |



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