



**THE DATASHEET OF
CSD13381F4**



CSD13381F4 12-V N-Channel FemtoFET™ MOSFET

1 Features

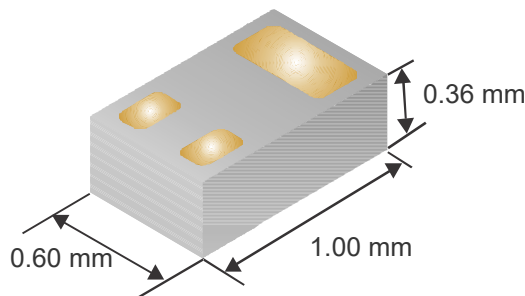
- Low on-resistance
- Low Q_g and Q_{gd}
- Low threshold voltage
- Ultra-small footprint (0402 case size)
 - 1.0 mm × 0.6 mm
- Ultra-low profile
 - Maximum height: 0.36-mm
- Integrated ESD protection diode
 - Rated > 4-kV HBM
 - Rated > 2-kV CDM
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for load switch applications
- Optimized for general purpose switching applications
- Single-cell battery applications
- Handheld and mobile applications

3 Description

This 140-m Ω , 12-V N-channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.



Typical Device Dimensions

Product Summary

| $T_A = 25^\circ\text{C}$ | | TYPICAL VALUE | | UNIT |
|--------------------------|-------------------------------|-------------------------|-----|------------|
| V_{DS} | Drain-to-source voltage | 12 | | V |
| Q_g | Gate charge total (4.5 V) | 1060 | | pC |
| Q_{gd} | Gate charge gate-to-drain | 140 | | pC |
| $R_{DS(on)}$ | Drain-to-source on-resistance | $V_{GS} = 1.8\text{ V}$ | 310 | m Ω |
| | | $V_{GS} = 2.5\text{ V}$ | 170 | m Ω |
| | | $V_{GS} = 4.5\text{ V}$ | 140 | m Ω |
| $V_{GS(th)}$ | Threshold voltage | 0.85 | | V |

Ordering Information

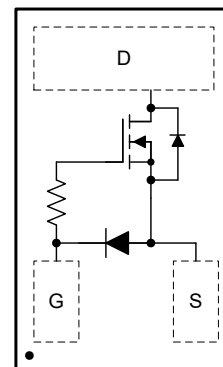
| DEVICE ⁽¹⁾ | QTY | MEDIA | PACKAGE | SHIP |
|-----------------------|------|-------------|--|---------------|
| CSD13381F4 | 3000 | 7-inch reel | Femto (0402) 1.0-mm × 0.6-mm SMD lead less | Tape and reel |
| CSD13381F4T | 250 | | | |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

| $T_A = 25^\circ\text{C}$ unless otherwise stated | | VALUE | UNIT |
|--|---|------------|------------------|
| V_{DS} | Drain-to-source voltage | 12 | V |
| V_{GS} | Gate-to-source voltage | 8 | V |
| I_D | Continuous drain current, $T_A = 25^\circ\text{C}$ ⁽¹⁾ | 2.1 | A |
| I_{DM} | Pulsed drain current, $T_A = 25^\circ\text{C}$ ⁽²⁾ | 7 | A |
| I_G | Continuous gate clamp current | 35 | mA |
| | Pulsed gate clamp current ⁽²⁾ | 350 | |
| P_D | Power dissipation ⁽¹⁾ | 500 | mW |
| ESD Rating | Human body model (HBM) | 4 | kV |
| | Charged device model (CDM) | 2 | kV |
| T_J , T_{stg} | Operating junction and storage temperature range | –55 to 150 | $^\circ\text{C}$ |
| E_{AS} | Avalanche energy, single pulse $I_D = 7.4\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\ \Omega$ | 2.7 | mJ |

- (1) Typical $R_{\theta JA} = 90^\circ\text{C/W}$ on 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu pad on a 0.06 inch (1.52 mm) thick FR4 PCB.
 (2) Pulse duration $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$



Top View



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision E (October 2021) to Revision F (January 2022) | Page |
|--|-------------|
| • Changed Maximum height from "0.35 mm" to "0.36 mm" in <i>Features</i> | 1 |
| • Changed package height from "0.35 mm" to "0.36 mm" in <i>Typical Device Dimensions</i> | 1 |
| • Changed package height from "0.35 mm" to "0.36 mm" in <i>Mechanical Dimensions</i> | 8 |
| Changes from Revision D (May 2015) to Revision E (October 2021) | Page |
| • Added footnote with link to support document..... | 9 |
| Changes from Revision C (September 2014) to Revision D (May 2015) | Page |
| • Corrected typo for I _{GSS} Test Condition | 3 |

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|----------------------------------|--|------|------|------|------|
| STATIC CHARACTERISTICS | | | | | | |
| B _V DSS | Drain-to-Source Voltage | V _{GS} = 0 V, I _{DS} = 250 μA | 12 | | | V |
| I _{DSS} | Drain-to-Source Leakage Current | V _{GS} = 0 V, V _{DS} = 9.6 V | | | 100 | nA |
| I _{GSS} | Gate-to-Source Leakage Current | V _{DS} = 0 V, V _{GS} = 8 V | | | 50 | nA |
| V _{GS(th)} | Gate-to-Source Threshold Voltage | V _{DS} = V _{GS} , I _{DS} = 250 μA | 0.65 | 0.85 | 1.10 | V |
| R _{DS(on)} | Drain-to-Source On-Resistance | V _{GS} = 1.8 V, I _{DS} = 0.5 A | | 310 | 400 | mΩ |
| | | V _{GS} = 2.5 V, I _{DS} = 0.5 A | | 170 | 225 | mΩ |
| | | V _{GS} = 4.5 V, I _{DS} = 0.5 A | | 140 | 180 | mΩ |
| g _{fs} | Transconductance | V _{DS} = 6 V, I _{DS} = 0.5 A | | 3.2 | | S |
| DYNAMIC CHARACTERISTICS | | | | | | |
| C _{iss} | Input Capacitance | V _{GS} = 0 V, V _{DS} = 6 V, f = 1 MHz | | 155 | 200 | pF |
| C _{oss} | Output Capacitance | | | 47 | 62 | pF |
| C _{rss} | Reverse Transfer Capacitance | | | 2.5 | 3.3 | pF |
| R _G | Series Gate Resistance | | | 23 | | Ω |
| Q _g | Gate Charge Total (4.5 V) | V _{DS} = 6 V, I _{DS} = 0.5 A | | 1060 | 1400 | pC |
| Q _{gd} | Gate Charge Gate-to-Drain | | | 140 | | pC |
| Q _{gs} | Gate Charge Gate-to-Source | | | 230 | | pC |
| Q _{g(th)} | Gate Charge at V _{th} | | | 155 | | pC |
| Q _{oss} | Output Charge | V _{DS} = 6 V, V _{GS} = 0 V | | 1120 | | pC |
| t _{d(on)} | Turn On Delay Time | V _{DS} = 6 V, V _{GS} = 4.5 V, I _{DS} = 0.5 A, R _G = 2 Ω | | 3.7 | | ns |
| t _r | Rise Time | | | 1.5 | | ns |
| t _{d(off)} | Turn Off Delay Time | | | 11.0 | | ns |
| t _f | Fall Time | | | 3.8 | | ns |
| DIODE CHARACTERISTICS | | | | | | |
| V _{SD} | Diode Forward Voltage | I _{SD} = 0.5 A, V _{GS} = 0 V | | 0.73 | 0.9 | V |
| Q _{rr} | Reverse Recovery Charge | V _{DS} = 6 V, I _F = 0.5 A, di/dt = 300 A/μs | | 1550 | | pC |
| t _{rr} | Reverse Recovery Time | | | 6 | | ns |

5.2 Thermal Information

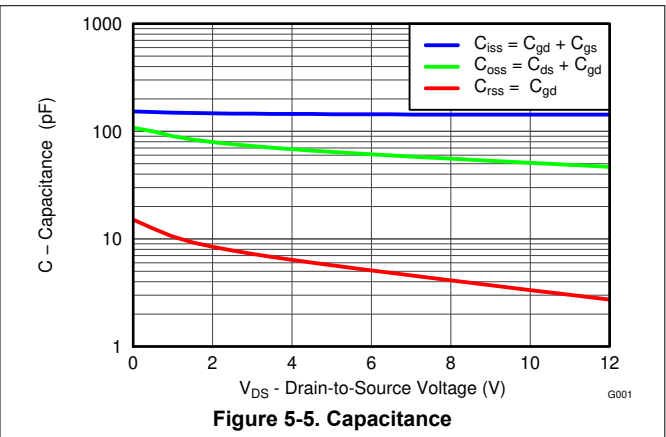
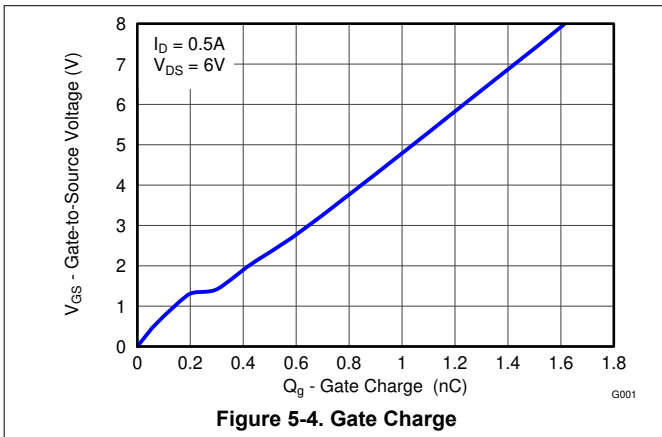
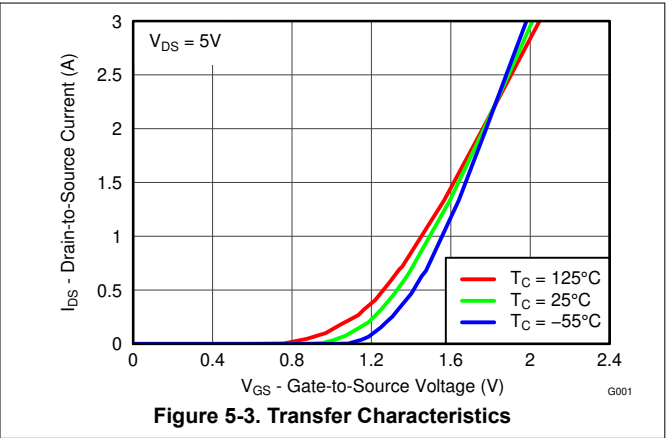
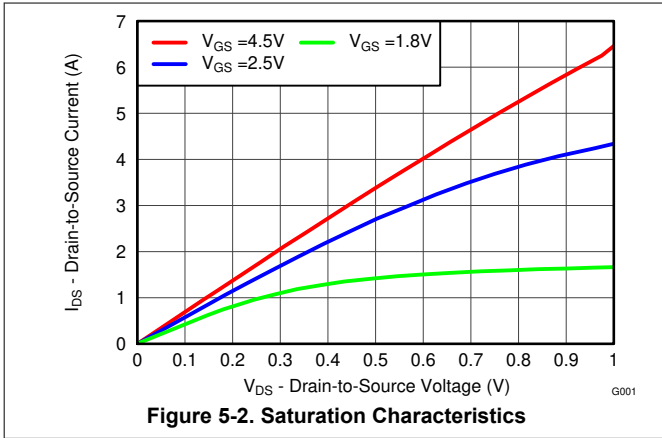
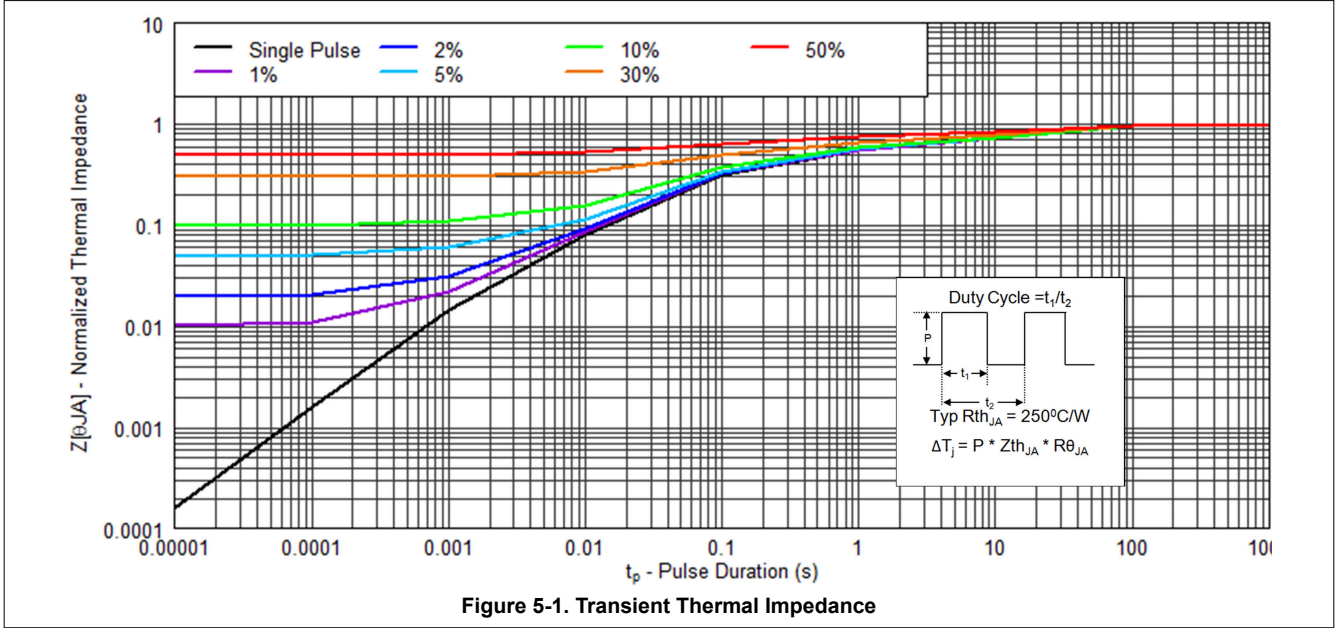
(T_A = 25°C unless otherwise stated)

| THERMAL METRIC | | TYPICAL VALUES | UNIT |
|------------------|---|----------------|------|
| R _{θJA} | Junction-to-Ambient Thermal Resistance ⁽¹⁾ | 90 | °C/W |
| | Junction-to-Ambient Thermal Resistance ⁽²⁾ | 250 | |

- (1) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)



5.3 Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

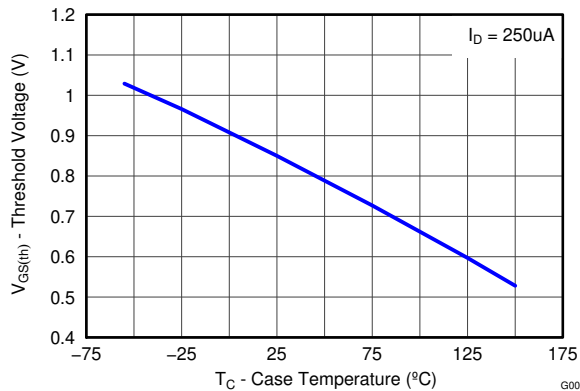


Figure 5-6. Threshold Voltage vs Temperature

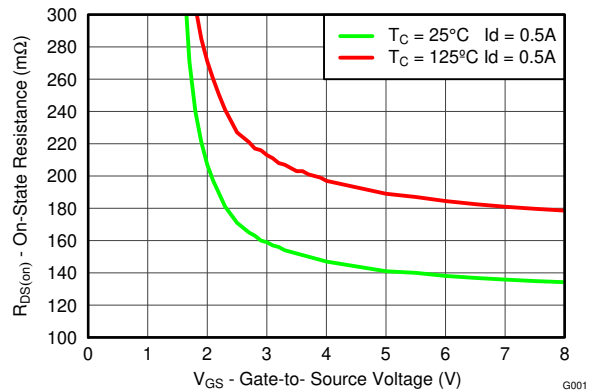


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage

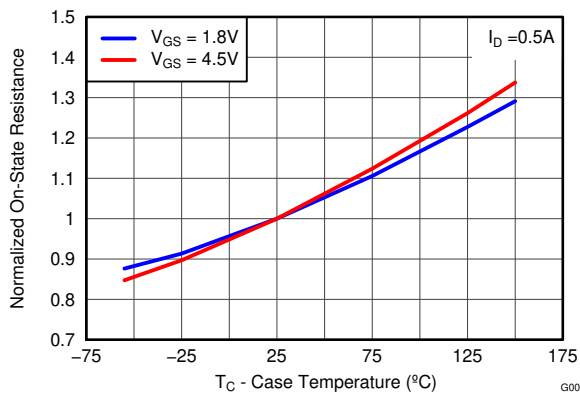


Figure 5-8. Normalized On-State Resistance vs Temperature

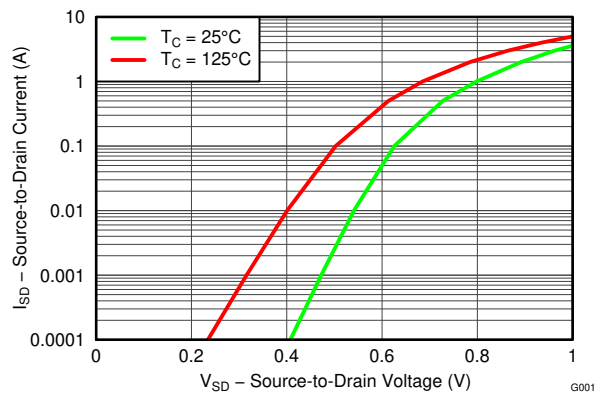


Figure 5-9. Typical Diode Forward Voltage

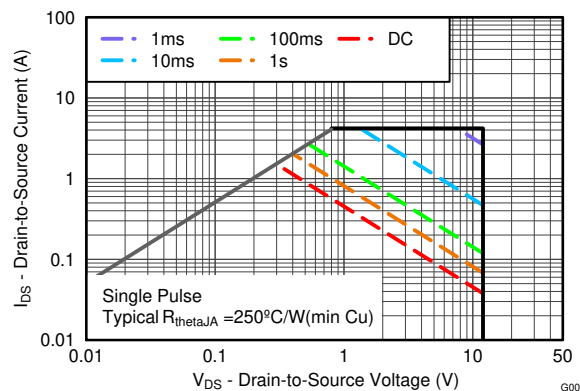


Figure 5-10. Maximum Safe Operating Area (SOA)

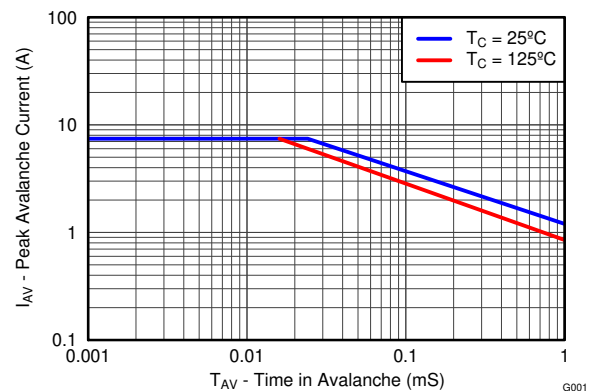


Figure 5-11. Single Pulse Unclamped Inductive Switching

5.3 Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

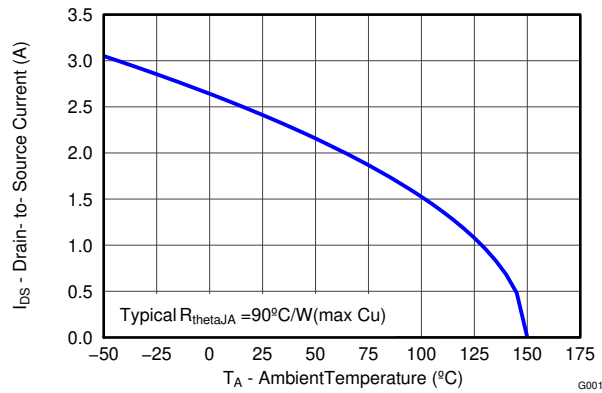


Figure 5-12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

FemtoFET™ is a trademark of Texas Instruments.
is a trademark of Texas Instruments.
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6.2 Electrostatic Discharge Caution



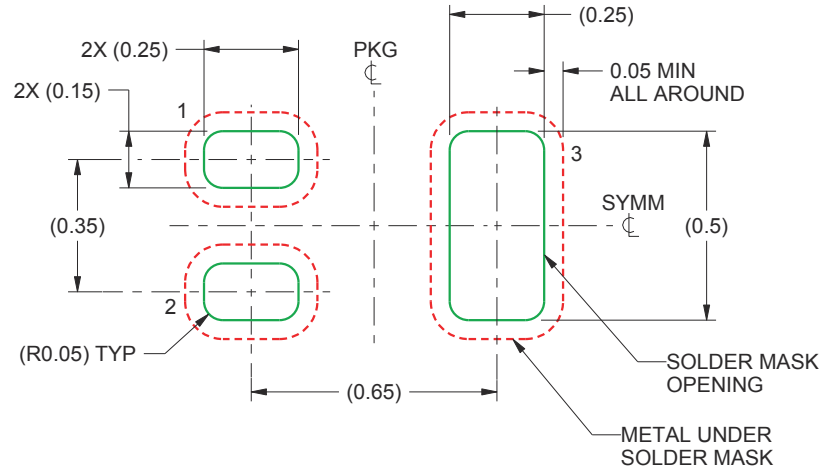
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.3 Glossary

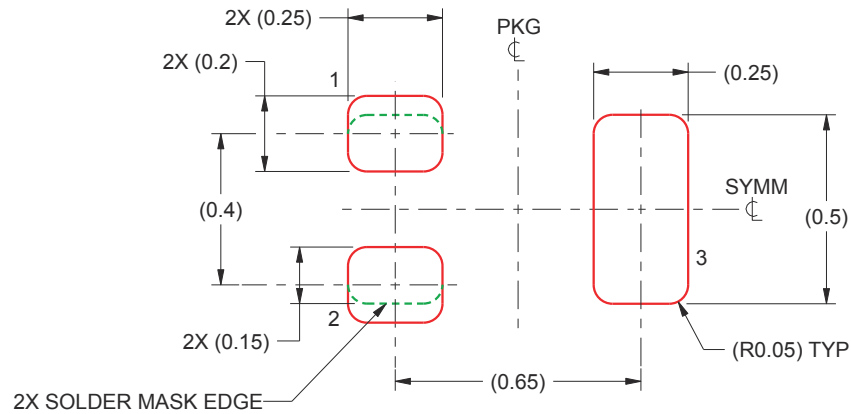
[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

7.2 Recommended Minimum PCB Layout



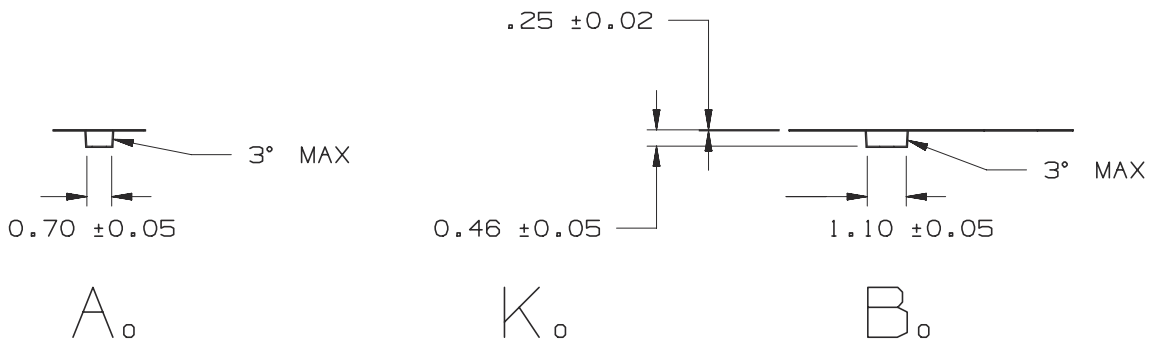
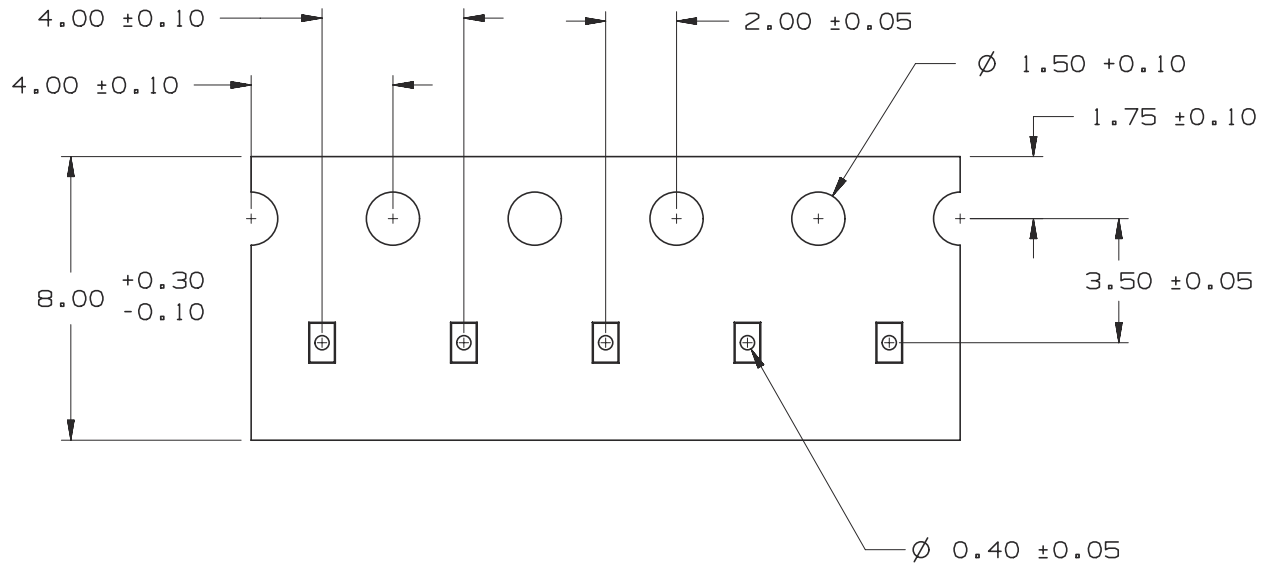
- A. All dimensions are in millimeters.
- B. For more information, see [FemtoFET Surface Mount Guide](#) (SLRA003D).

7.3 Recommended Stencil Pattern



- A. All dimensions are in millimeters.

7.4 CSD13381F4 Embossed Carrier Tape Dimensions



- A. Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CSD13381F4 | ACTIVE | PICOSTAR | YJC | 3 | 3000 | RoHS & Green | NIAU | Level-1-260C-UNLIM | -55 to 150 | DQ | Samples |
| CSD13381F4T | ACTIVE | PICOSTAR | YJC | 3 | 250 | RoHS & Green | NIAU | Level-1-260C-UNLIM | -55 to 150 | DQ | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

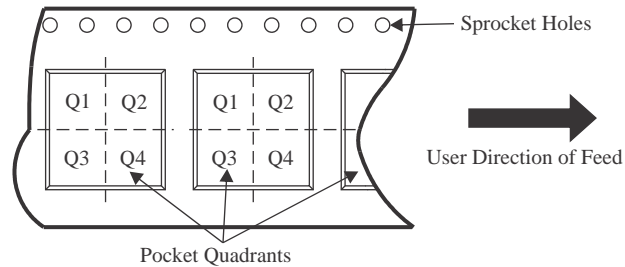
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CSD13381F4 | PICOSTAR | YJC | 3 | 3000 | 180.0 | 8.4 | 0.7 | 1.1 | 0.46 | 4.0 | 8.0 | Q2 |
| CSD13381F4T | PICOSTAR | YJC | 3 | 250 | 180.0 | 8.4 | 0.7 | 1.1 | 0.46 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CSD13381F4 | PICOSTAR | YJC | 3 | 3000 | 182.0 | 182.0 | 20.0 |
| CSD13381F4T | PICOSTAR | YJC | 3 | 250 | 182.0 | 182.0 | 20.0 |

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