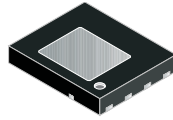




**THE DATASHEET OF  
CSD16408Q5**





## DualCool™ N-Ch NexFET™ Power MOSFET

### FEATURES

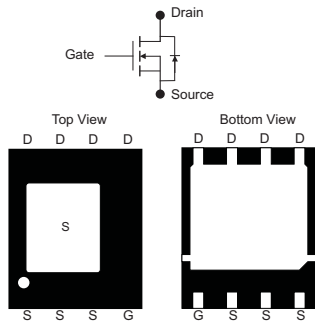
- Ultra Low  $Q_g$  and  $Q_{gd}$
- DualCool™ Package
- Optimized for 2-Sided Cooling
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm x 6-mm Plastic Package

### APPLICATIONS

- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems
- Optimized for Control FET Applications

### DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.



### PRODUCT SUMMARY

$V_{DS}$	Drain to Source Voltage	25	V
$Q_g$	Gate Charge Total (4.5V)	6.7	nC
$Q_{gd}$	Gate Charge Gate to Drain	1.9	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V$	5.4 mΩ
		$V_{GS} = 10V$	3.6 mΩ
$V_{GS(th)}$	Threshold Voltage	1.8	V

### ORDERING INFORMATION

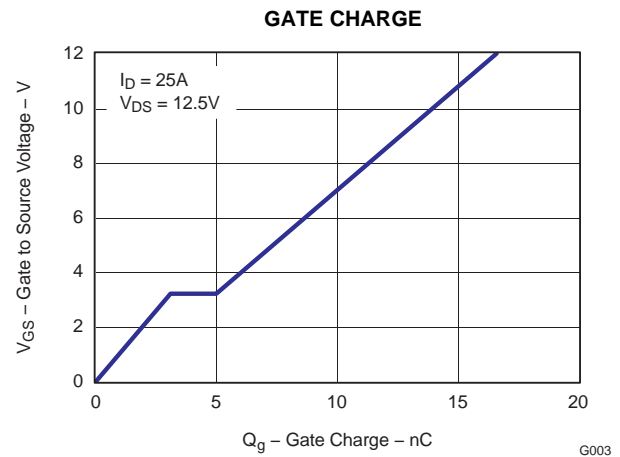
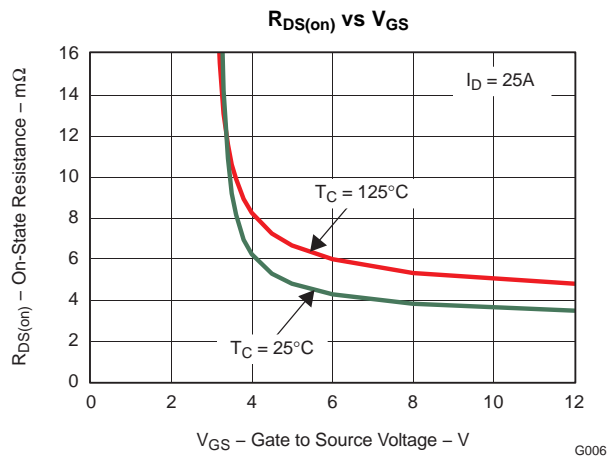
Device	Package	Media	Qty	Ship
CSD16408Q5C	SON 5-mm x 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

### ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	25	V
$V_{GS}$	Gate to Source Voltage	+16 / -12	V
$I_D$	Continuous Drain Current, $T_C = 25^\circ\text{C}$	113	A
	Continuous Drain Current <sup>(1)</sup>	22	A
$I_{DM}$	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ <sup>(2)</sup>	141	A
$P_D$	Power Dissipation <sup>(1)</sup>	3.1	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, single pulse $I_D = 23A, L = 0.1mH, R_G = 25\Omega$	126	mJ

(1) Typical  $R_{\theta JA} = 41^\circ\text{C/W}$  on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$  unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b>						
$V_{DSS}$	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu\text{A}$	25			V
$I_{DSS}$	Drain to Source Leakage	$V_{GS} = 0V, V_{DS} = 20V$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage	$V_{DS} = 0V, V_{GS} = +16/-12V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.4	1.8	2.1	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V, I_D = 25A$		5.4	6.8	m $\Omega$
		$V_{GS} = 10V, I_D = 25A$		3.6	4.5	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 15V, I_D = 25A$		60		S
<b>Dynamic Characteristics</b>						
$C_{ISS}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = 12.5V, f = 1\text{MHz}$		990	1300	pF
$C_{OSS}$	Output Capacitance			760	1000	pF
$C_{RSS}$	Reverse Transfer Capacitance			75	100	pF
$R_g$	Series Gate Resistance			0.8	1.6	$\Omega$
$Q_g$	Gate Charge Total (4.5V)	$V_{DS} = 12.5V, I_D = 25A$		6.7	8.9	nC
$Q_{gd}$	Gate Charge – Gate to Drain			1.9		nC
$Q_{gs}$	Gate Charge – Gate to Source			3.1		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			1.8		nC
$Q_{OSS}$	Output Charge	$V_{DS} = 13V, V_{GS} = 0V$		15.7		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 25A, R_G = 2\Omega$		11.3		ns
$t_r$	Rise Time			25		ns
$t_{d(off)}$	Turn Off Delay Time			11		ns
$t_f$	Fall Time			10.8		ns
<b>Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage	$I_S = 25A, V_{GS} = 0V$		0.8	1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 13V, I_F = 25A, di/dt = 300A/\mu\text{s}$		17		nC
$t_{rr}$	Reverse Recovery Time	$V_{DD} = 13V, I_F = 25A, di/dt = 300A/\mu\text{s}$		21		ns

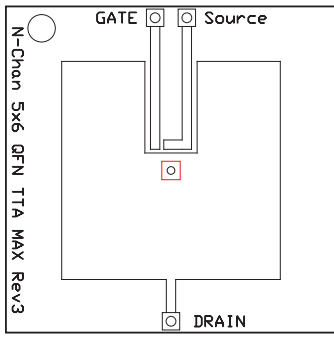
## THERMAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$  unless otherwise stated

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case (Top Source) <sup>(1)</sup>			3.1	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction to Case (Bottom Drain) <sup>(1)</sup>			1.9	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>(1) (2)</sup>			51	$^\circ\text{C/W}$

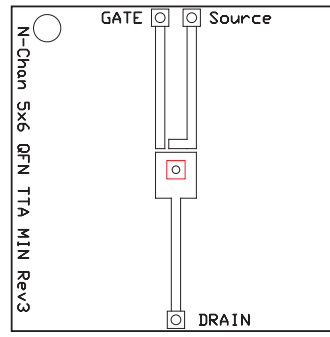
(1)  $R_{\theta JC}$  is determined with the device mounted on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.

(2) Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu.



M0137-01

Max  $R_{\theta JA} = 51^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> (6.45 cm<sup>2</sup>) of  
2-oz. (0.071-mm thick)  
Cu.

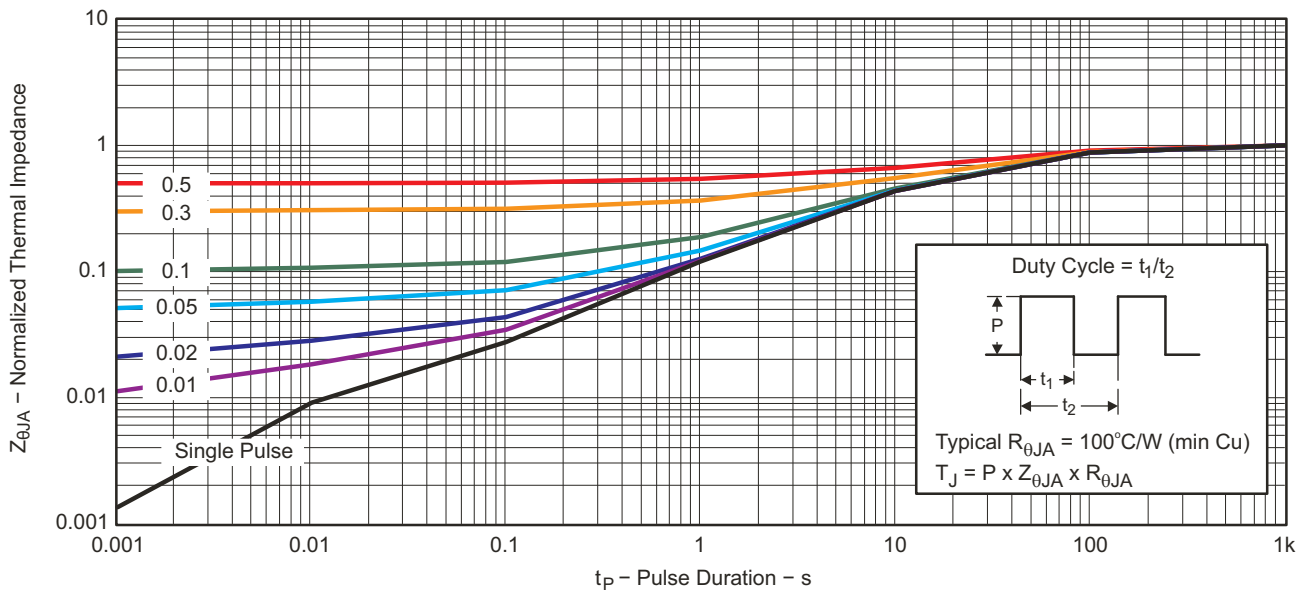


M0137-02

Max  $R_{\theta JA} = 125^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of  
2-oz. (0.071-mm thick)  
Cu.

### TYPICAL MOSFET CHARACTERISTICS

$T_A = 25^{\circ}\text{C}$  unless otherwise stated

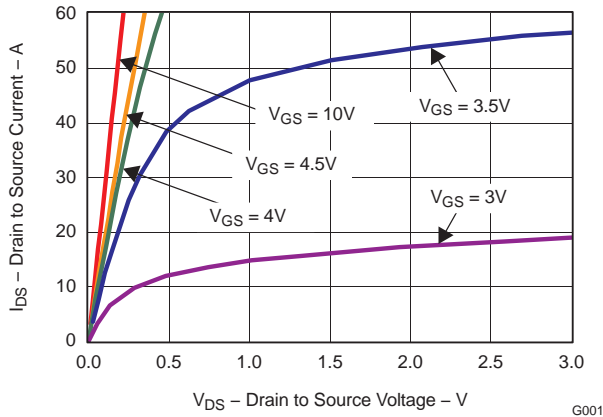


G012

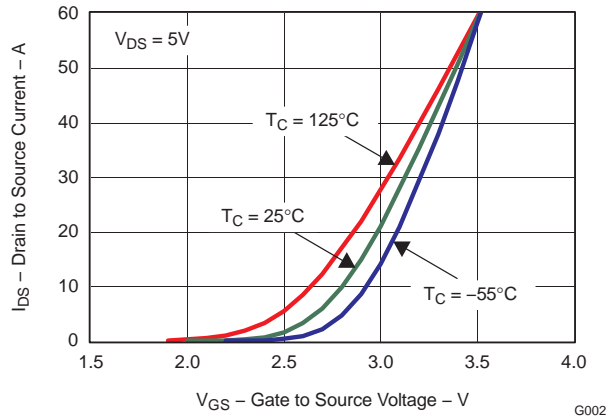
Figure 1. Transient Thermal Impedance

**TYPICAL MOSFET CHARACTERISTICS (continued)**

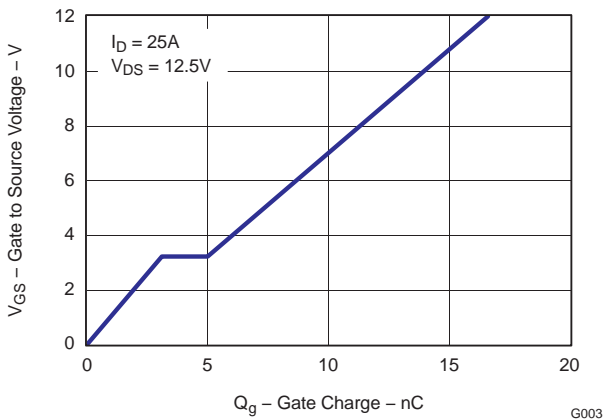
T<sub>A</sub> = 25°C unless otherwise stated



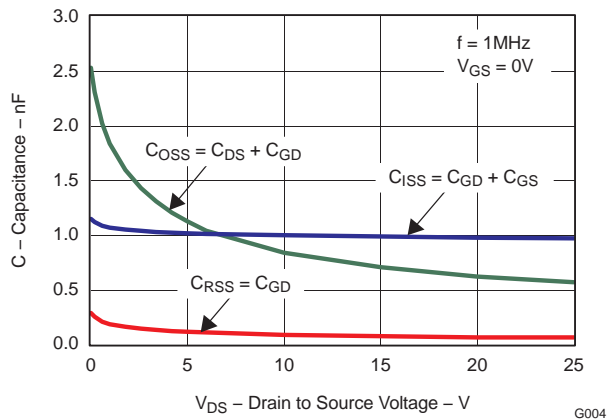
**Figure 2. Saturation Characteristics**



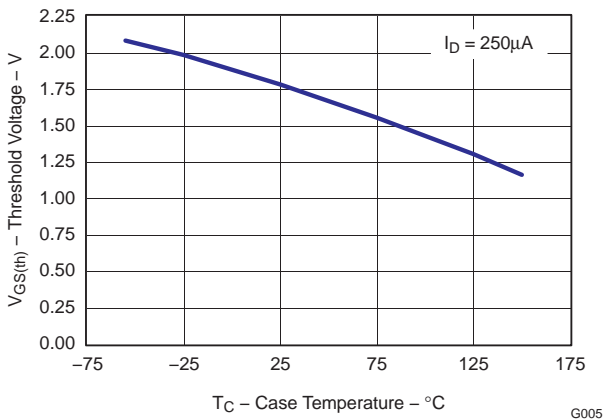
**Figure 3. Transfer Characteristics**



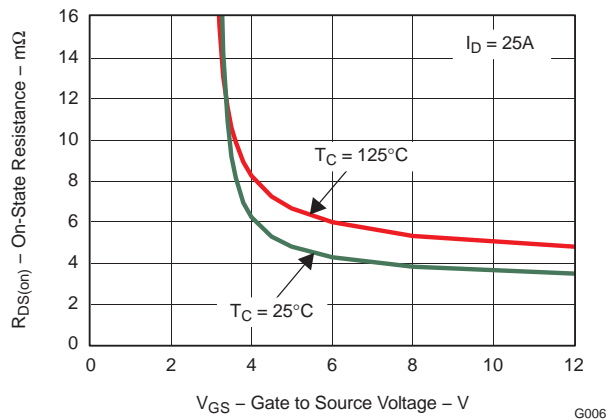
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Threshold Voltage vs. Temperature**



**Figure 7. On-State Resistance vs. Gate to Source Voltage**

TYPICAL MOSFET CHARACTERISTICS (continued)

T<sub>A</sub> = 25°C unless otherwise stated

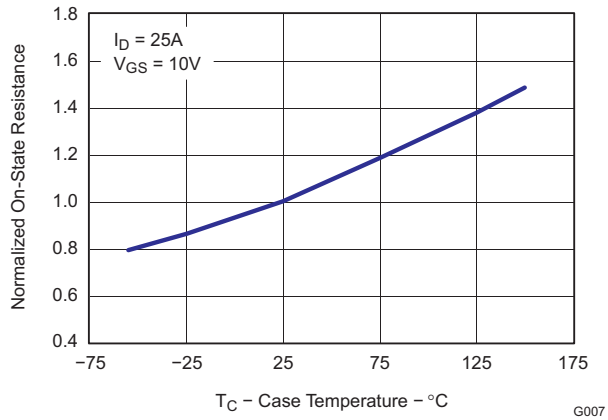


Figure 8. Normalized On-State Resistance vs. Temperature

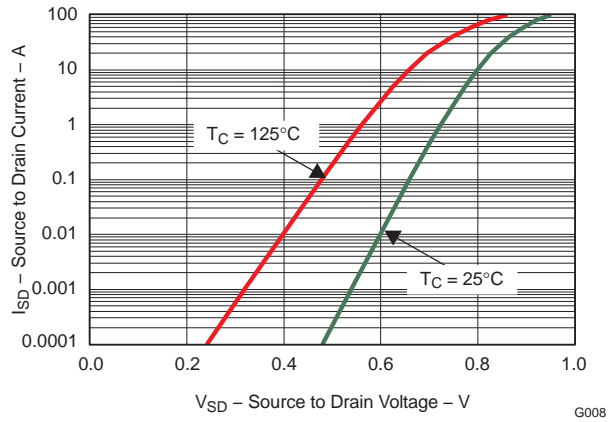


Figure 9. Typical Diode Forward Voltage

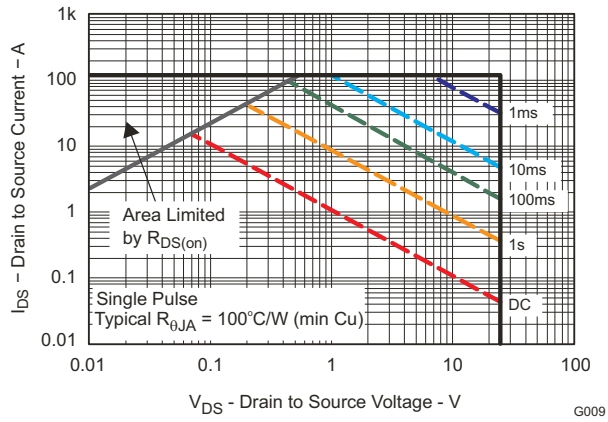


Figure 10. Maximum Safe Operating Area

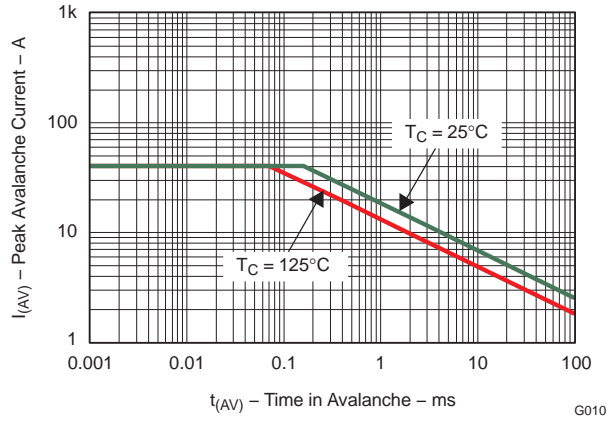


Figure 11. Single Pulse Unclamped Inductive Switching

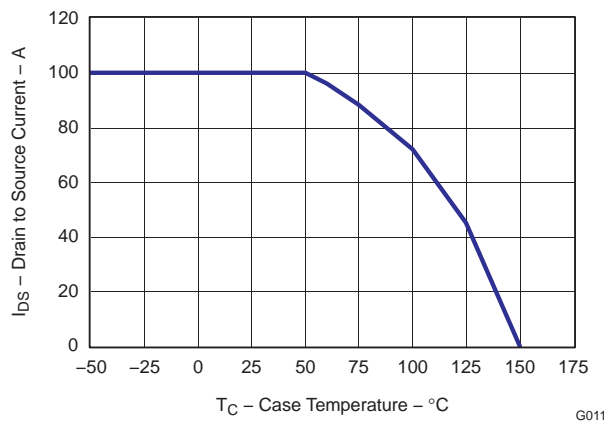
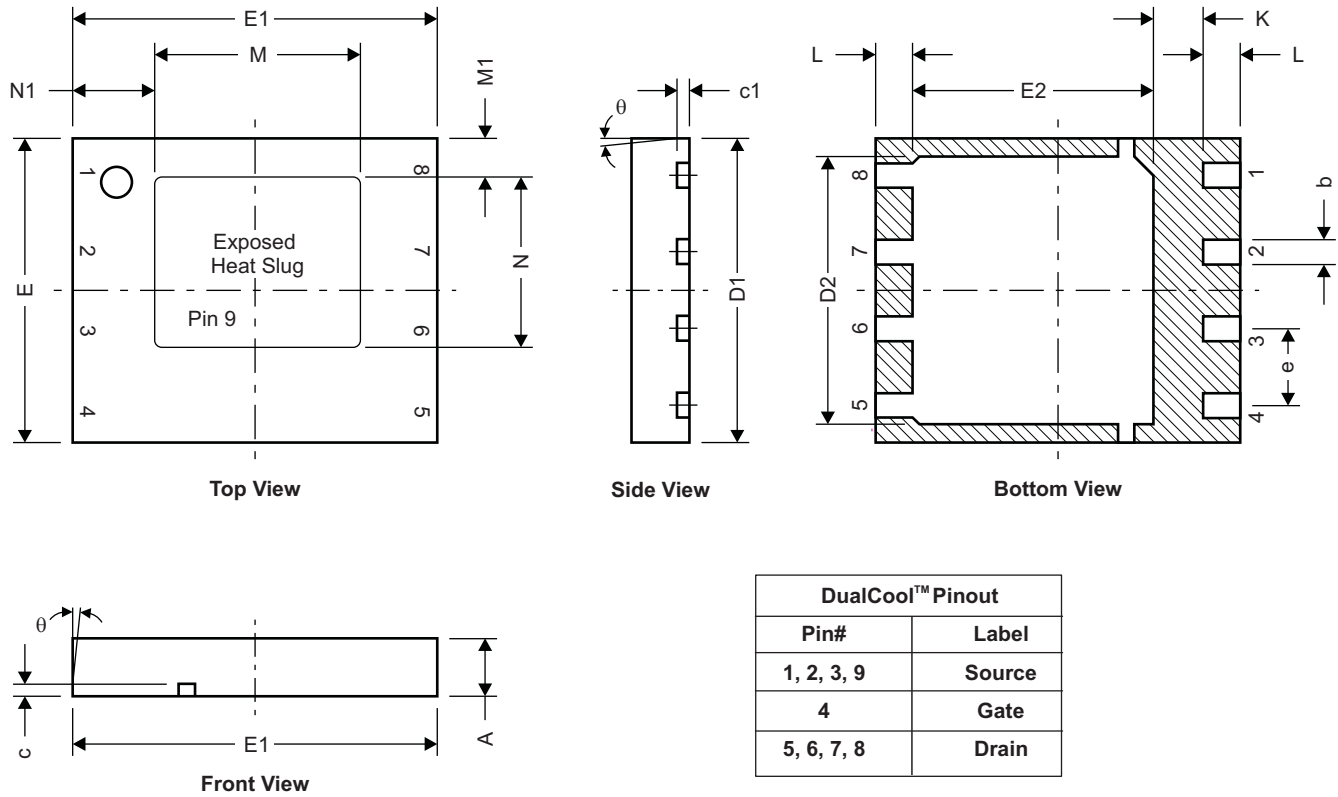


Figure 12. Maximum Drain Current vs. Temperature

**MECHANICAL DATA**

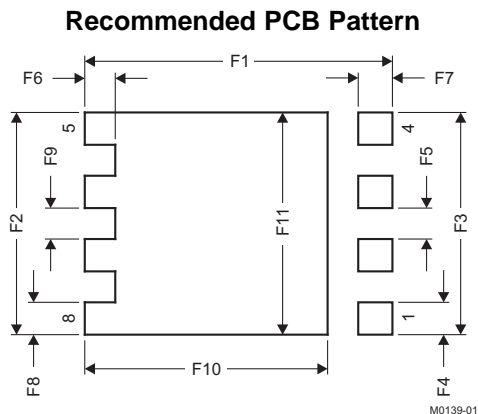
**Q5C Package Dimensions**



DualCool™ Pinout	
Pin#	Label
1, 2, 3, 9	Source
4	Gate
5, 6, 7, 8	Drain

M0162-01

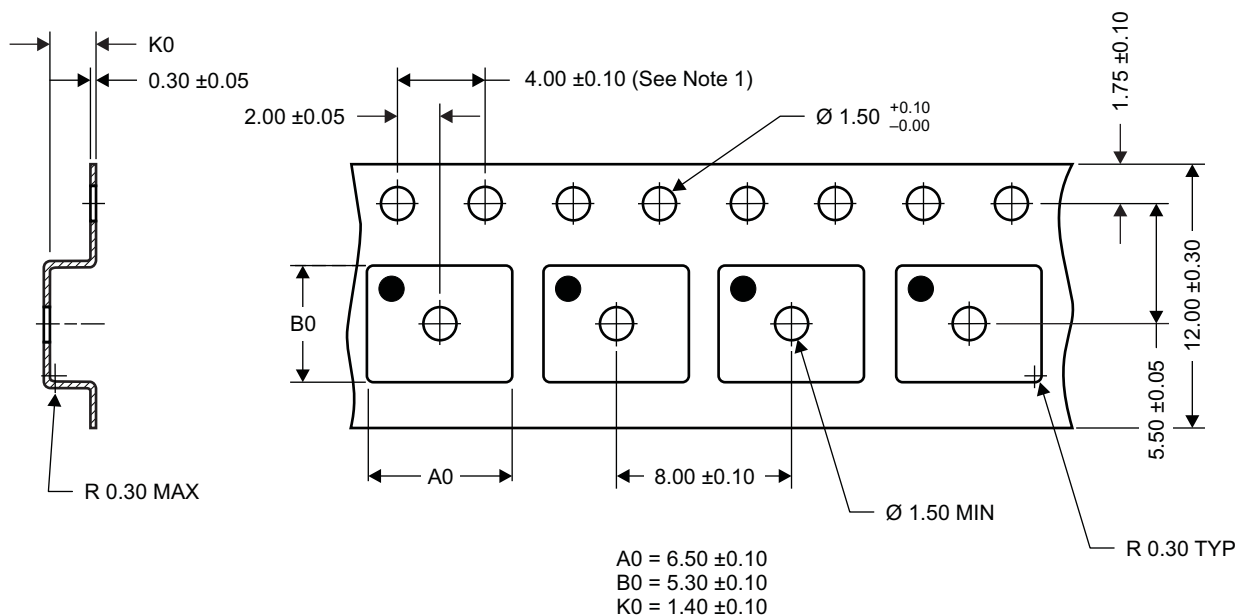
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
K	0.760	–	0.030	–
L	0.510	0.710	0.020	0.028
theta	–	–	–	–
M	3.260	3.460	0.128	0.136
M1	0.520	0.720	0.020	0.028
N	2.720	2.920	0.107	0.115
N1	1.227	1.427	0.048	0.056



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note *Reducing Ringing Through PCB Layout Techniques (SLPA005)*.

### Q5 Tape and Reel Information



M0138-01

### Notes:

- 10-sprocket hole-pitch cumulative tolerance ±0.2
- Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- Material: black static-dissipative polystyrene
- All dimensions are in mm, unless otherwise specified.
- A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
- MSL1 260°C (IR and convection) PbF reflow compatible

## REVISION HISTORY

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Changes from Original (December 2009) to Revision A	Page
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- Changed the labels on the Bottom View pinout image ..... 1
- 

Changes from Revision A (February) to Revision B	Page
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- the Package Marking Information section ..... 7
-

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16408Q5C	NRND	VSON-CLIP	DQU	8		TBD	Call TI	Call TI	0 to 0		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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