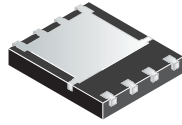




**THE DATASHEET OF
CSD16413Q5A**





N-Channel NexFET™ Power MOSFET

 Check for Samples: [CSD16413Q5A](#)

FEATURES

- Ultra Low Qg and Qgd
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5mm x 6mm Plastic Package

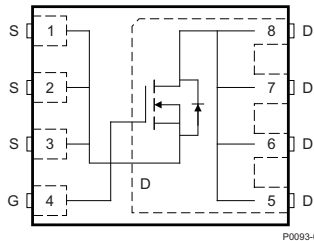
APPLICATIONS

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Control or Synchronous FET Applications

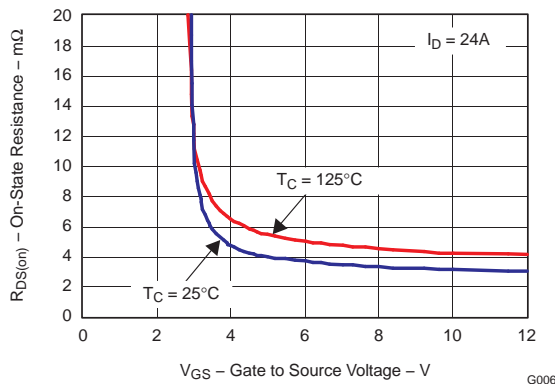
DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

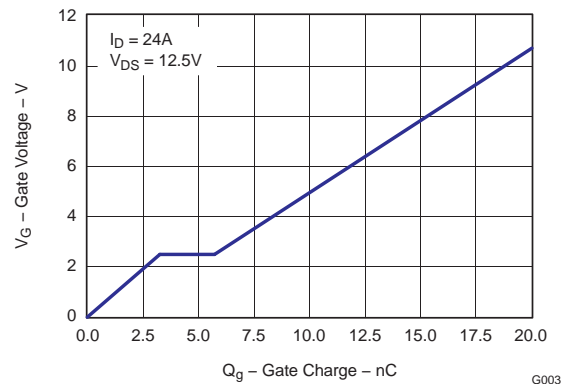
Top View



P0093-01

R_{DS(on)} vs V_{GS}


G006

Gate Charge


G003

PRODUCT SUMMARY

| | | | |
|---------------------|-------------------------------|------------------------|--------|
| V _{DS} | Drain to Source Voltage | 25 | V |
| Q _g | Gate Charge Total (4.5V) | 9 | nC |
| Q _{gd} | Gate Charge Gate to Drain | 2.5 | nC |
| R _{DS(on)} | Drain to Source On Resistance | V _{GS} = 4.5V | 4.1 mΩ |
| | | V _{GS} = 10V | 3.1 mΩ |
| V _{GS(th)} | Threshold Voltage | 1.6 | V |

ORDERING INFORMATION

| Device | Package | Media | Qty | Ship |
|-------------|---------------------------|--------------|------|---------------|
| CSD16413Q5A | SON 5 x 6 Plastic Package | 13-inch reel | 2500 | Tape and Reel |

ABSOLUTE MAXIMUM RATINGS

| T _A = 25°C unless otherwise stated | | VALUE | UNIT |
|---|---|------------|------|
| V _{DS} | Drain to Source Voltage | 25 | V |
| V _{GS} | Gate to Source Voltage | +16 / -12 | V |
| I _D | Continuous Drain Current, T _C = 25°C | 100 | A |
| | Continuous Drain Current ⁽¹⁾ | 24 | A |
| I _{DM} | Pulsed Drain Current, T _A = 25°C ⁽²⁾ | 156 | A |
| P _D | Power Dissipation ⁽¹⁾ | 3.1 | W |
| T _J , T _{STG} | Operating Junction and Storage Temperature Range | -55 to 150 | °C |
| E _{AS} | Avalanche Energy, single pulse I _D = 46A, L = 0.1mH, R _G = 25Ω | 106 | mJ |

(1) R_{θJA} = 41°C/W on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width ≤300μs, duty cycle ≤2%



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NexFET is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

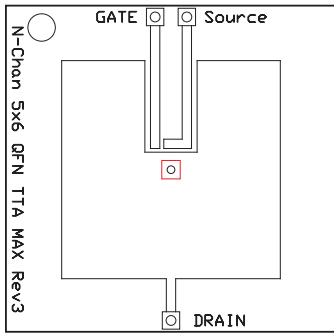
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|----------------------------------|---|-----|------|------|------------|
| Static Characteristics | | | | | | |
| BV_{DSS} | Drain to Source Voltage | $V_{GS} = 0V, I_D = 250\mu A$ | 25 | | | V |
| I_{DSS} | Drain to Source Leakage Current | $V_{GS} = 0V, V_{DS} = 20V$ | | | 1 | μA |
| I_{GSS} | Gate to Source Leakage Current | $V_{DS} = 0V, V_{GS} = +16/-12V$ | | | 100 | nA |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{DS} = V_{GS}, I_D = 250\mu A$ | 1.2 | 1.6 | 1.9 | V |
| $R_{DS(on)}$ | Drain to Source On Resistance | $V_{GS} = 4.5V, I_D = 24A$ | | 4.1 | 5.6 | m Ω |
| | | $V_{GS} = 10V, I_D = 24A$ | | 3.1 | 3.9 | m Ω |
| g_{fs} | Transconductance | $V_{DS} = 15V, I_D = 24A$ | | 95 | | S |
| Dynamic Characteristics | | | | | | |
| C_{ISS} | Input Capacitance | $V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz$ | | 1370 | 1780 | pF |
| C_{OSS} | Output Capacitance | | | 1060 | 1380 | pF |
| C_{RSS} | Reverse Transfer Capacitance | | | 84 | 109 | pF |
| R_g | Series Gate Resistance | | | 0.9 | 1.8 | Ω |
| Q_g | Gate Charge Total (4.5V) | $V_{DS} = 12.5V, I_D = 24A$ | | 9 | 11.7 | nC |
| Q_{gd} | Gate Charge Gate to Drain | | | 2.5 | | nC |
| Q_{gs} | Gate Charge Gate to Source | | | 3.5 | | nC |
| $Q_{g(th)}$ | Gate Charge at V_{th} | | | 2.2 | | nC |
| Q_{OSS} | Output Charge | $V_{DS} = 13.1V, V_{GS} = 0V$ | | 21 | | nC |
| $t_{d(on)}$ | Turn On Delay Time | $V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 24A$ $R_G = 5\Omega$ | | 9.1 | | ns |
| t_r | Rise Time | | | 15.9 | | ns |
| $t_{d(off)}$ | Turn Off Delay Time | | | 10.7 | | ns |
| t_f | Fall Time | | | 5.7 | | ns |
| Diode Characteristics | | | | | | |
| V_{SD} | Diode Forward Voltage | $I_S = 24A, V_{GS} = 0V$ | | 0.85 | 1 | V |
| Q_{rr} | Reverse Recovery Charge | $V_{DD} = 13.1V, I_F = 24A, di/dt = 300A/\mu s$ | | 32 | | nC |
| t_{rr} | Reverse Recovery Time | $V_{DD} = 13.1V, I_F = 24A, di/dt = 300A/\mu s$ | | 28 | | ns |

THERMAL CHARACTERISTICS

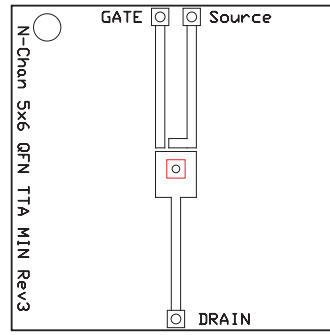
($T_A = 25^\circ\text{C}$ unless otherwise stated)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-----------------|---|-----|-----|-----|---------------------------|
| $R_{\theta JC}$ | Thermal Resistance Junction to Case ⁽¹⁾ | | | 2.6 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Thermal Resistance Junction to Ambient ^{(1) (2)} | | | 51 | $^\circ\text{C}/\text{W}$ |

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch square 2 oz. Cu pad on a 1.5 x 1.5 in .060 inch thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 Material with 1 inch² of 2 oz. Cu.



Max $R_{\theta JA} = 51^{\circ}\text{C/W}$
when mounted on 1
inch² of 2 oz. Cu.



Max $R_{\theta JA} = 118^{\circ}\text{C/W}$
when mounted on
minimum pad area of 2
oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

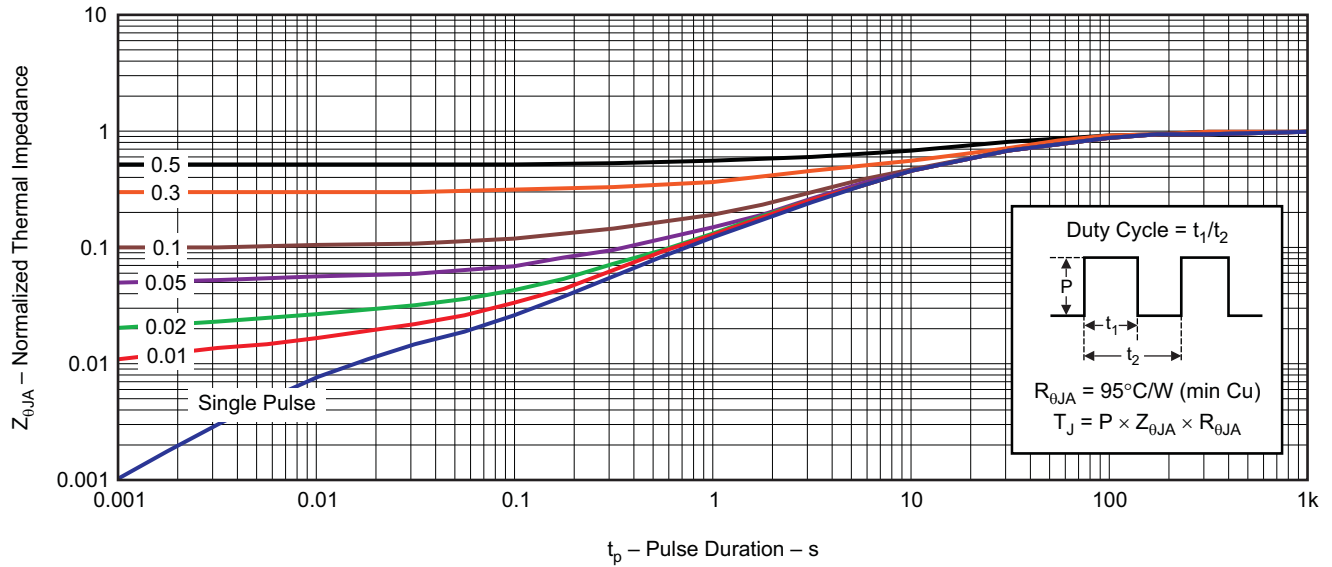


Figure 1. Transient Thermal Impedance

G012

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

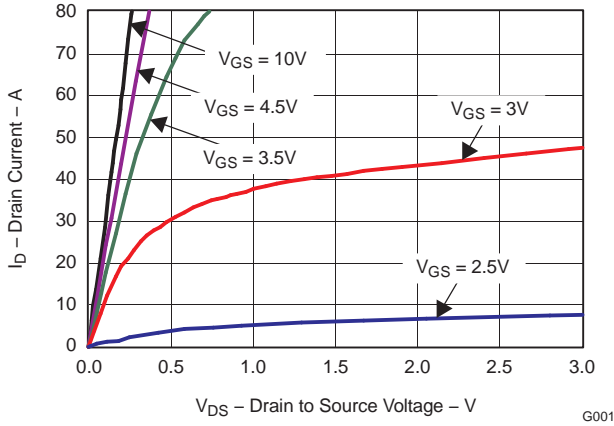


Figure 2. Saturation Characteristics

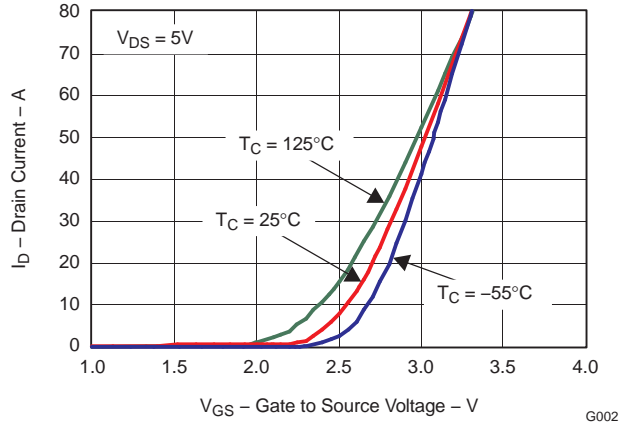


Figure 3. Transfer Characteristics

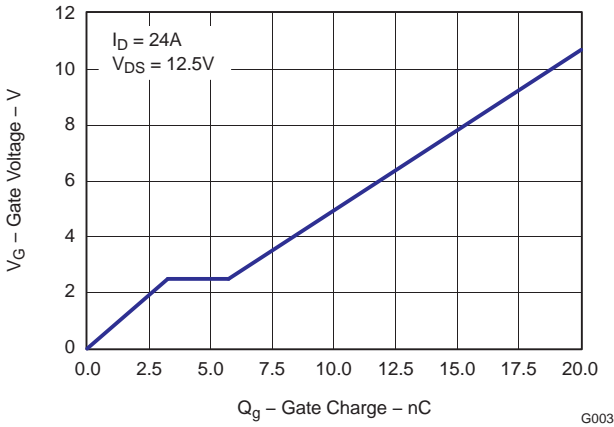


Figure 4. Gate Charge

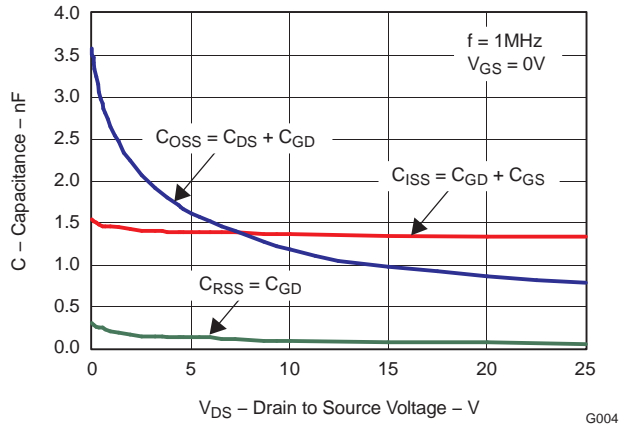


Figure 5. Capacitance

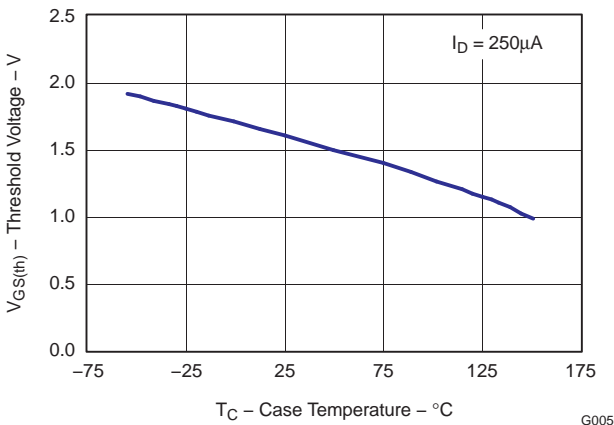


Figure 6. Threshold Voltage vs. Temperature

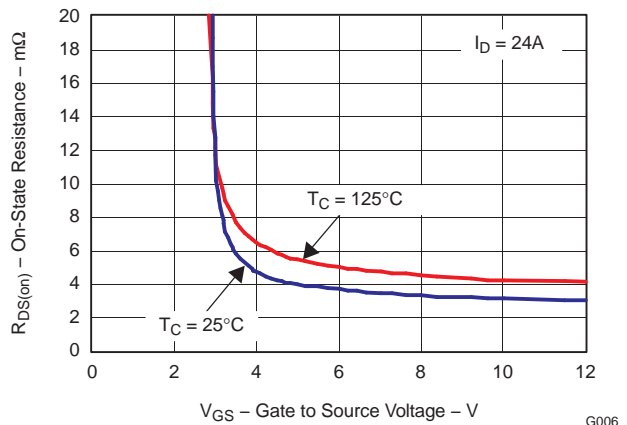


Figure 7. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

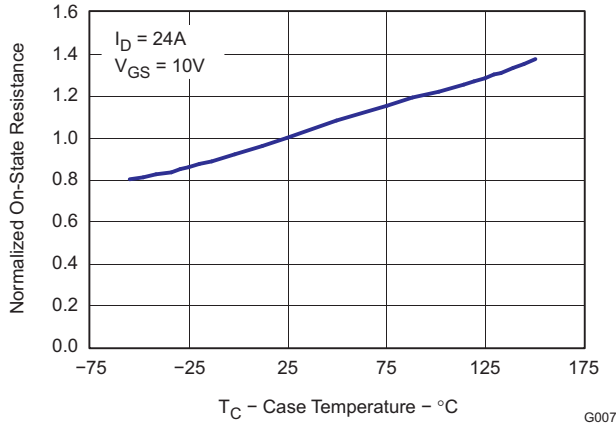


Figure 8. On Resistance vs. Temperature

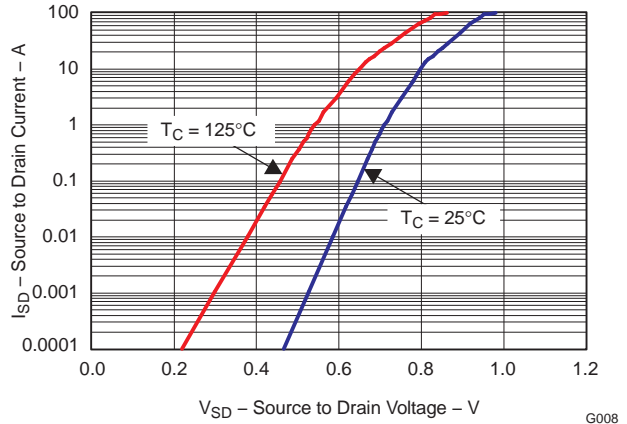


Figure 9. Typical Diode Forward Voltage

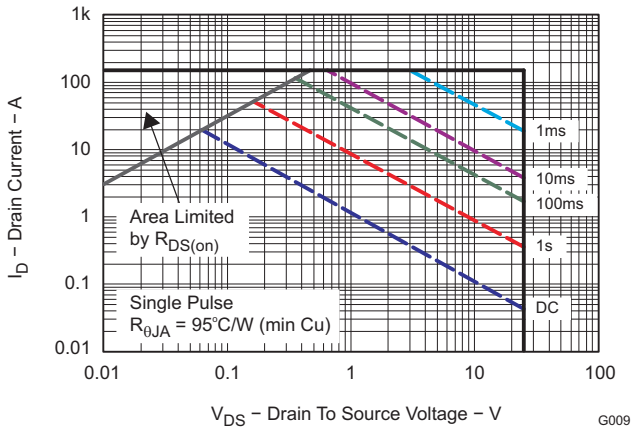


Figure 10. Maximum Safe Operating Area

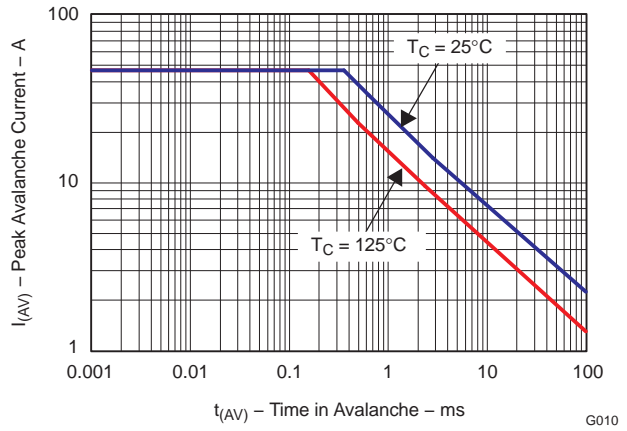


Figure 11. Single Pulse Unclamped Inductive Switching

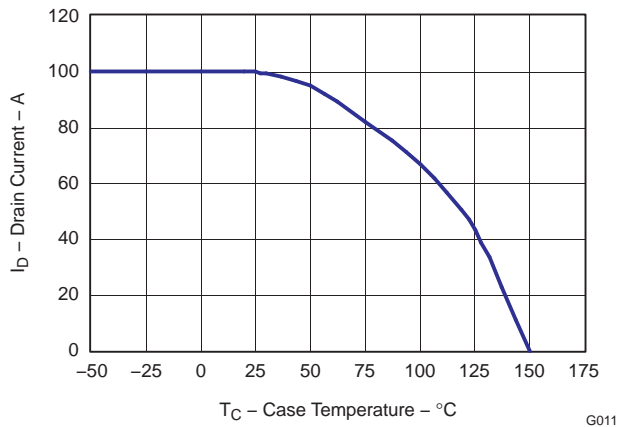
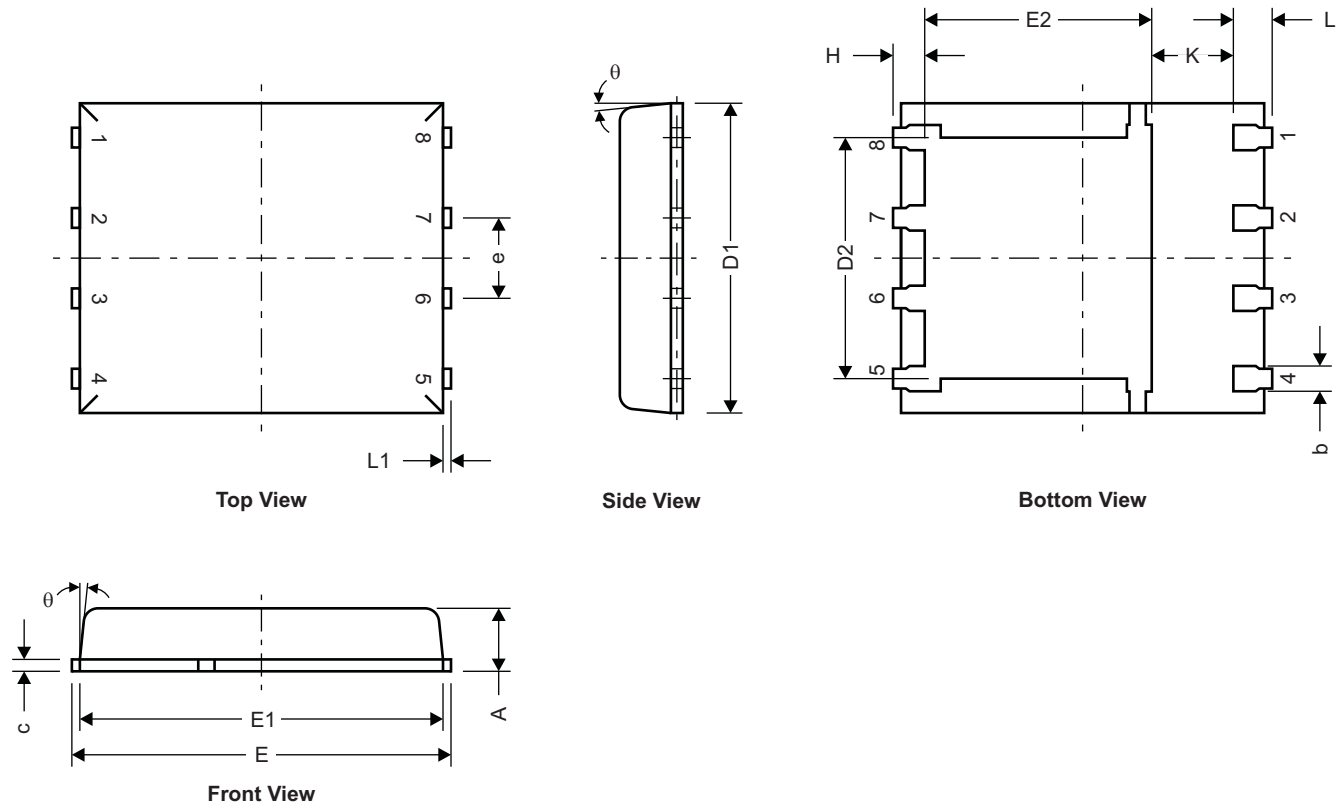


Figure 12. Maximum Drain Current vs. Temperature

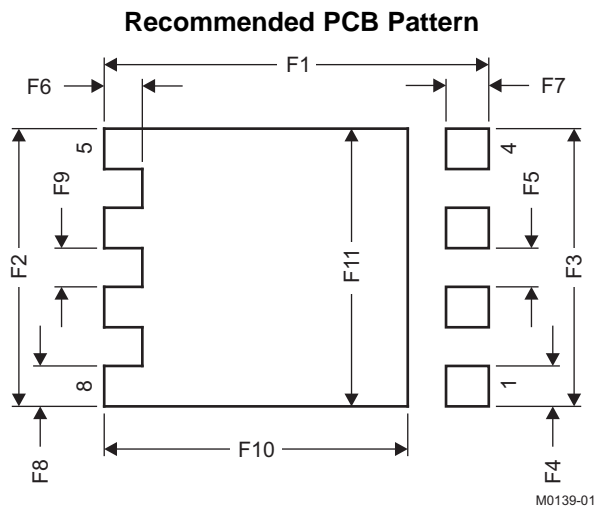
MECHANICAL DATA

Q5A Package Dimensions



M0135-01

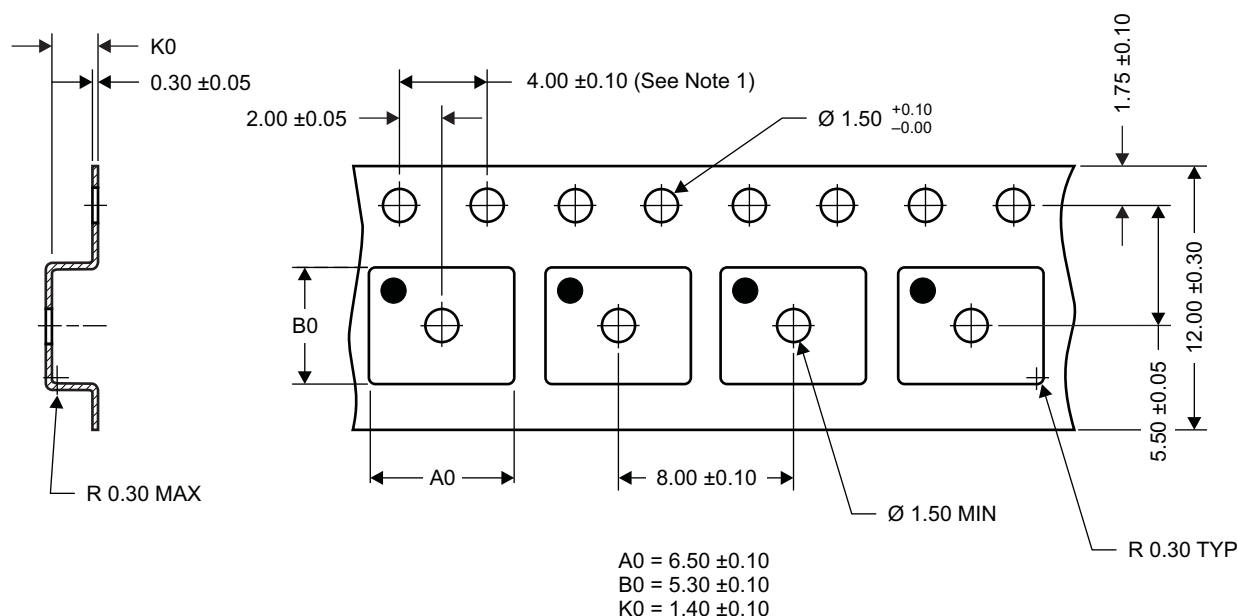
| DIM | MILLIMETERS | | |
|----------|-------------|------|------|
| | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| b | 0.33 | 0.41 | 0.51 |
| c | 0.20 | 0.25 | 0.30 |
| D1 | 4.80 | 4.90 | 5.00 |
| D2 | 3.61 | 3.81 | 3.96 |
| E | 5.90 | 6.00 | 6.10 |
| E1 | 5.70 | 5.75 | 5.80 |
| E2 | 3.38 | 3.58 | 3.78 |
| e | 1.27 BSC | | |
| H | 0.41 | 0.51 | 0.61 |
| K | 1.10 | | |
| L | 0.51 | 0.61 | 0.71 |
| L1 | 0.06 | 0.13 | 0.20 |
| θ | 0° | | 12° |



| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|--------|-------|
| | MIN | MAX | MIN | MAX |
| F1 | 6.205 | 6.305 | 0.244 | 0.248 |
| F2 | 4.46 | 4.56 | 0.176 | 0.18 |
| F3 | 4.46 | 4.56 | 0.176 | 0.18 |
| F4 | 0.65 | 0.7 | 0.026 | 0.028 |
| F5 | 0.62 | 0.67 | 0.024 | 0.026 |
| F6 | 0.63 | 0.68 | 0.025 | 0.027 |
| F7 | 0.7 | 0.8 | 0.038 | 0.031 |
| F8 | 0.65 | 0.7 | 0.026 | 0.028 |
| F9 | 0.62 | 0.67 | 0.024 | 0.026 |
| F10 | 4.9 | 5 | 0.193 | 0.197 |
| F11 | 4.46 | 4.56 | 0.176 | 0.18 |

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

Q5A Tape and Reel Information



M0138-01

Notes:

- 10 sprocket hole pitch cumulative tolerance ±0.2
- Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
- Material: black static dissipative polystyrene
- All dimensions are in mm (unless otherwise specified)
- A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
- MSL1 260°C (IR and Convection) PbF Reflow Compatible

REVISION HISTORY

| Changes from Original (August 2009) to Revision A | Page |
|---|------|
|---|------|

- Deleted the Package Marking Information section [7](#)
-

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------------|-------------------------|----------------------|--------------|-------------------------|---------|
| CSD16413Q5A | ACTIVE | VSONP | DQJ | 8 | 2500 | Pb-Free (RoHS Exempt) | CU SN | Level-1-260C-UNLIM | -55 to 150 | CSD16413 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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