



**THE DATASHEET OF
C3M0015065K**

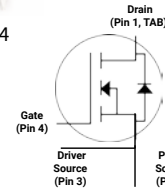


C3M0015065K

Silicon Carbide Power MOSFET
C3M™ MOSFET Technology
N-Channel Enhancement Mode



TO-247-4



Package Types: TO-247-4
PN's: C3M0015065K

Features

- C3M™ SiC MOSFET technology
- Optimized package with separate driver source pin
- 8 mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

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Applications

- EV chargers
- Solar inverters
- UPS
- SMPS
- DC/DC converters

Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			650	v	$T_c = 25^\circ\text{C}$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			120	A	$V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Fig. 19 Note 2
				96		$V_{GS} = 15\text{ V}, T_c = 100^\circ\text{C}, T_J \leq 175^\circ\text{C}$	
Pulsed Drain Current	I_{DM}			418		t_{Pmax} limited by T_{Jmax} $V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}$	Fig. 22
Power Dissipation	P_D			416	W	$T_c = 25^\circ\text{C}, T_J = 175^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-40 to +175	°C		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	
Mounting Torque	M_D			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Recommended turn-on gate voltage is 15V with $\pm 5\%$ regulation tolerance, see Application Note PRD-04814 for additional details

Note (2): Verified by design


Electrical Characteristics ($T_C = 25\text{ }^\circ\text{C}$ Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	650				$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.3	3.6	V	$V_{DS} = V_{GS}, I_D = 15.5\text{ mA}$	Fig. 11
			1.9			$V_{DS} = V_{GS}, I_D = 15.5\text{ mA}, T_J = 175\text{ }^\circ\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}		1	50	μA	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	
Gate-Source Leakage Current	I_{GSS}		10	250	nA	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance	$R_{DS(on)}$		15	21	m Ω	$V_{GS} = 15\text{ V}, I_D = 55.8\text{ A}$	Fig. 4, 5, 6
			20			$V_{GS} = 15\text{ V}, I_D = 55.8\text{ A}, T_J = 175\text{ }^\circ\text{C}$	
Transconductance	g_{fs}		42		S	$V_{DS} = 20\text{ V}, I_{DS} = 55.8\text{ A}$	Fig. 7
			40			$V_{DS} = 20\text{ V}, I_{DS} = 55.8\text{ A}, T_J = 175\text{ }^\circ\text{C}$	
Input Capacitance	C_{iss}		5011		pF	$V_{GS} = 0\text{ V}, V_{DS} = 400\text{ V}$ $f = 100\text{ kHz}$ $V_{AC} = 25\text{ mV}$	Fig. 17, 18
Output Capacitance	C_{oss}		289				
Reverse Transfer Capacitance	C_{rss}		31				
Effective Output Capacitance (Energy Related)	$C_{o(er)}$		357				Note: 3
Effective Output Capacitance (Time Related)	$C_{o(tr)}$		516				
C_{oss} Stored Energy	E_{oss}		29		μJ		Fig. 16
Turn-On Switching Energy (Body Diode)	E_{ON}		252		μJ	$V_{DS} = 400\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 55.8\text{ A},$ $R_{G(ext)} = 2.5\text{ }\Omega, L = 36\text{ }\mu\text{H}, T_J = 175\text{ }^\circ\text{C}$ FWD = Internal Body Diode of MOSFET	Fig. 25
Turn-Off Switching Energy (Body Diode)	E_{OFF}		180				
Turn-On Switching Energy (External Diode)	E_{ON}		189		μJ	$V_{DS} = 400\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}, I_D = 55.8\text{ A},$ $R_{G(ext)} = 2.5\text{ }\Omega, L = 36\text{ }\mu\text{H}, T_J = 175\text{ }^\circ\text{C}$ FWD = External SiC Diode	Fig. 25
Turn-Off Switching Energy (External Diode)	E_{OFF}		192				
Turn-On Delay Time	$t_{d(on)}$		16		ns	$V_{DD} = 400\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 55.8\text{ A}, R_{G(ext)} = 2.5\text{ }\Omega,$ Timing Relative to V_{DS} Inductive Load	Fig. 26
Rise Time	t_r		24				
Turn-Off Delay Time	$t_{d(off)}$		43				
Fall Time	t_f		12				
Internal Gate Resistance	$R_{G(int)}$		1.5		Ω	$f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$	
Gate to Source Charge	Q_{gs}		49		nC	$V_{DS} = 400\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 55.8\text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}		55				
Total Gate Charge	Q_g		188				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V.

$C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V.



Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ Unless Otherwise Specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Note
Diode Forward Voltage	V_{SD}	4.7		V	$V_{GS} = -4\text{ V}, I_{SD} = 27.9\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.2			$V_{GS} = -4\text{ V}, I_{SD} = 27.9\text{ A}, T_J = 175^\circ\text{C}$	
Continuous Diode Forward Current	I_S		79	A	$V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$	
Diode Pulse Current	$I_{S, pulse}$		223		$V_{GS} = -4\text{ V}, \text{Pulse Width } t_p \text{ Limited by } T_{Jmax}$	
Reverse Recovery Time	t_{rr}	19		ns	$V_{GS} = -4\text{ V}, I_{SD} = 55.8\text{ A}, V_R = 400\text{ V}$ $dif/dt = 6080\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Reverse Recovery Charge	Q_{rr}	510		nC		
Peak Reverse Recovery Current	I_{rrm}	60		A		
Reverse Recovery Time	t_{rr}	24		ns	$V_{GS} = -4\text{ V}, I_{SD} = 55.8\text{ A}, V_R = 400\text{ V}$ $dif/dt = 1850\text{ A}/\mu\text{s}, T_J = 175^\circ\text{C}$	
Reverse Recovery Charge	Q_{rr}	432		nC		
Peak Reverse Recovery Current	I_{rrm}	30		A		

Thermal Characteristics

Parameter	Symbol	Typ.	Unit	Test Conditions	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.35	$^\circ\text{C}/\text{W}$		Fig. 21
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	40			



Typical Performance

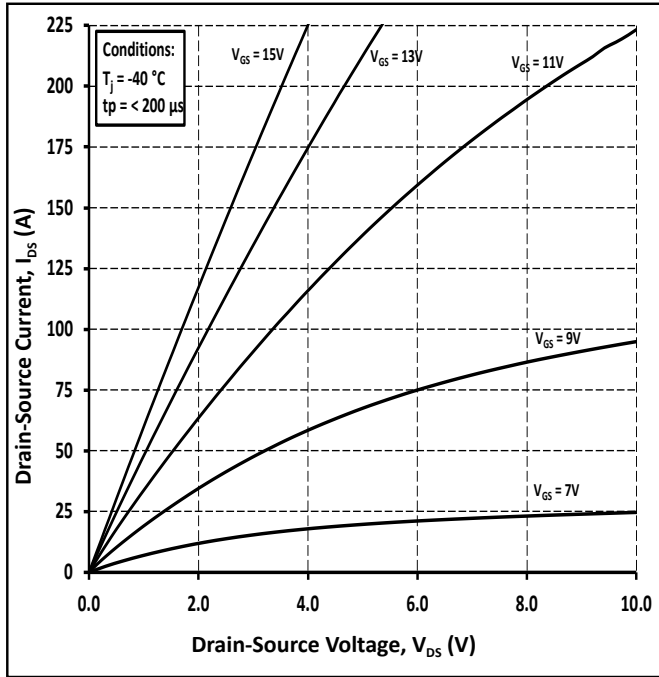


Figure 1. Output Characteristics $T_j = -40\text{ }^\circ\text{C}$

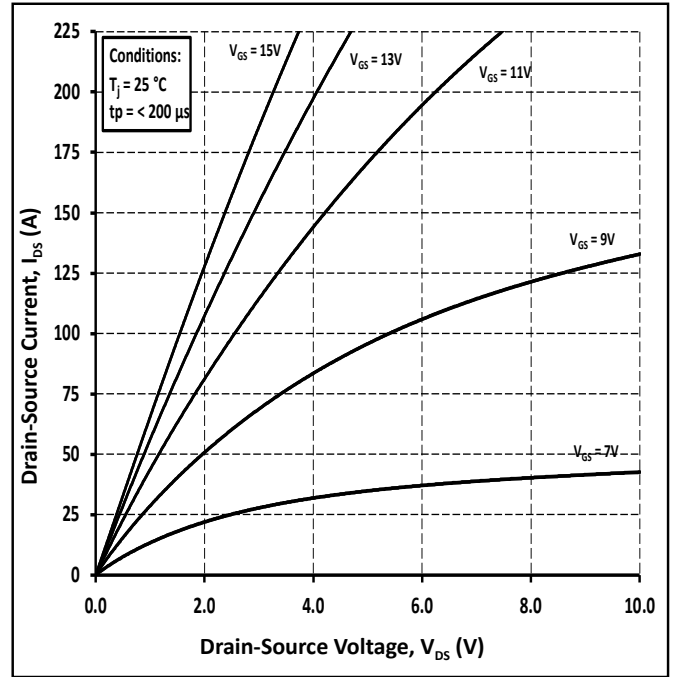


Figure 2. Output Characteristics $T_j = 25\text{ }^\circ\text{C}$

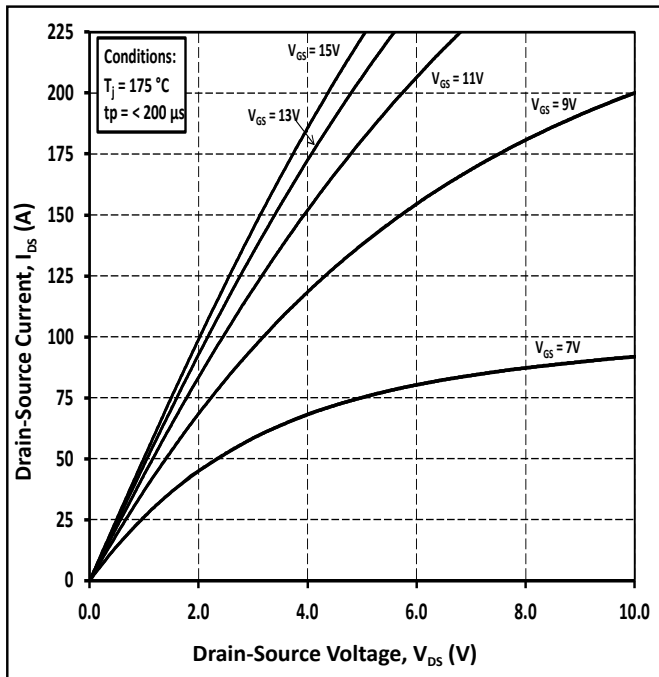


Figure 3. Output Characteristics $T_j = 175\text{ }^\circ\text{C}$

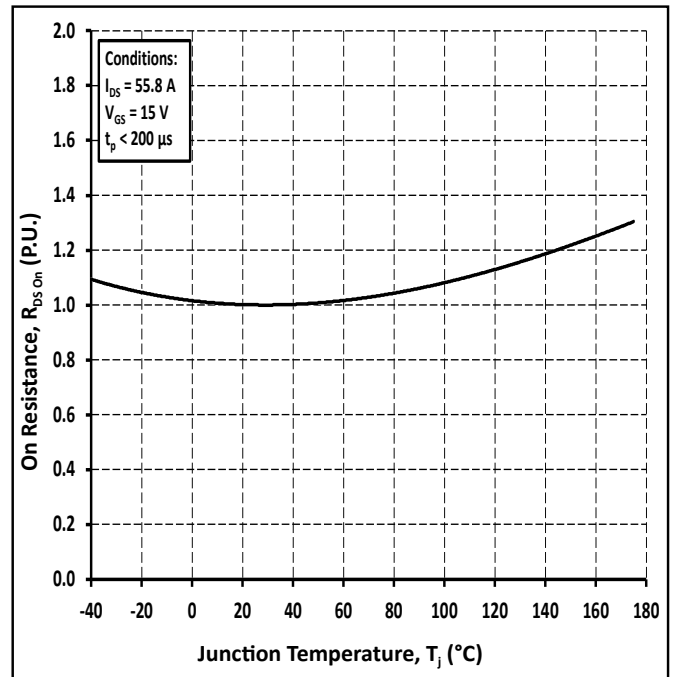


Figure 4. Normalized On-Resistance vs Temperature



Typical Performance

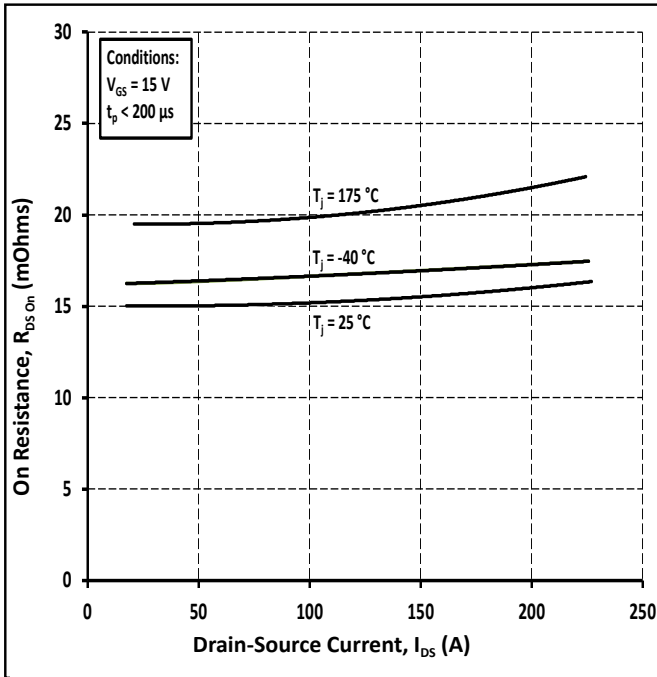


Figure 5. On-Resistance vs Drain Current for Various Temperatures

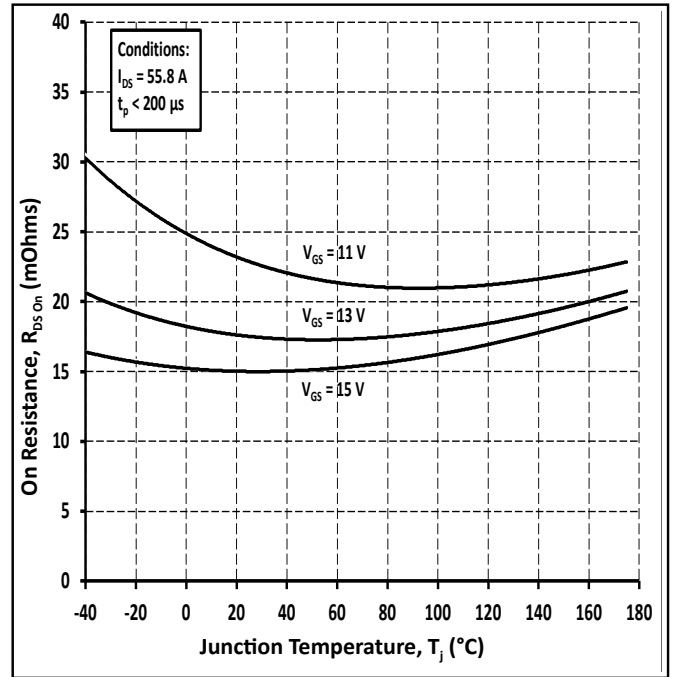


Figure 6. On-Resistance vs Temperature for Various Gate Voltage

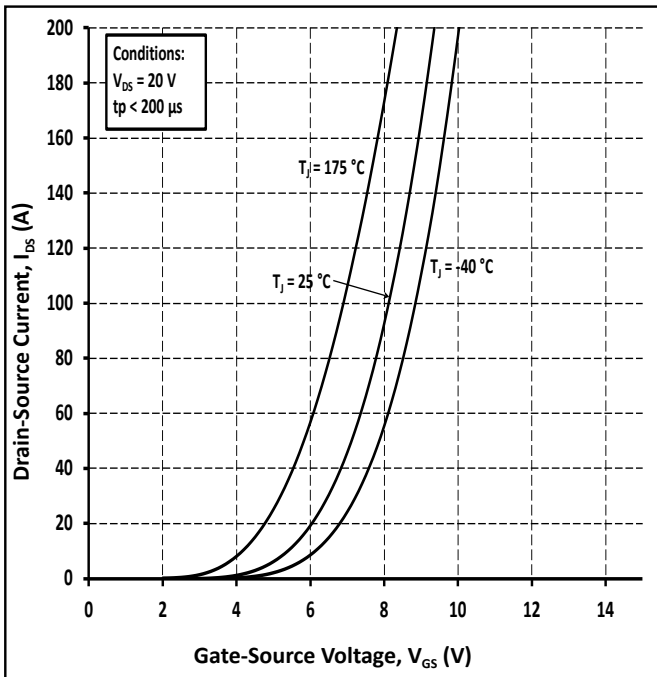


Figure 7. Transfer Characteristic for Various Junction Temperatures

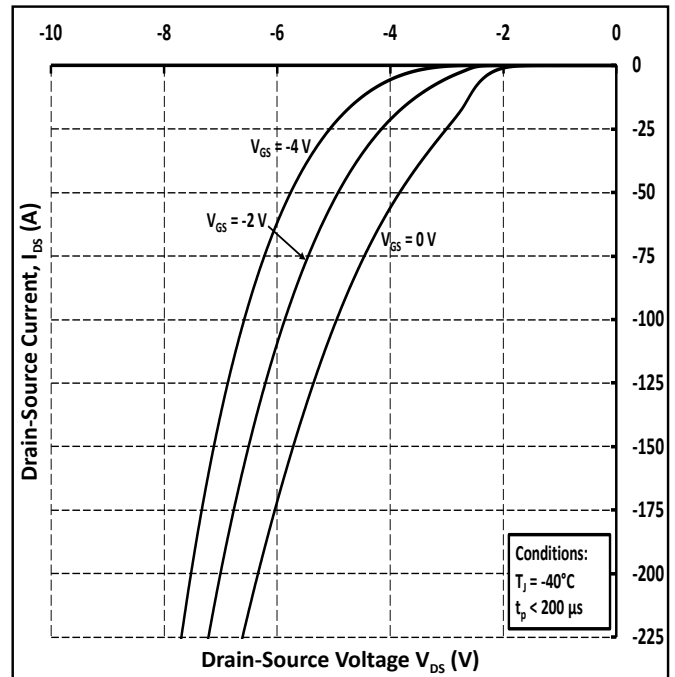


Figure 8. Body Diode Characteristic at -40 °C



Typical Performance

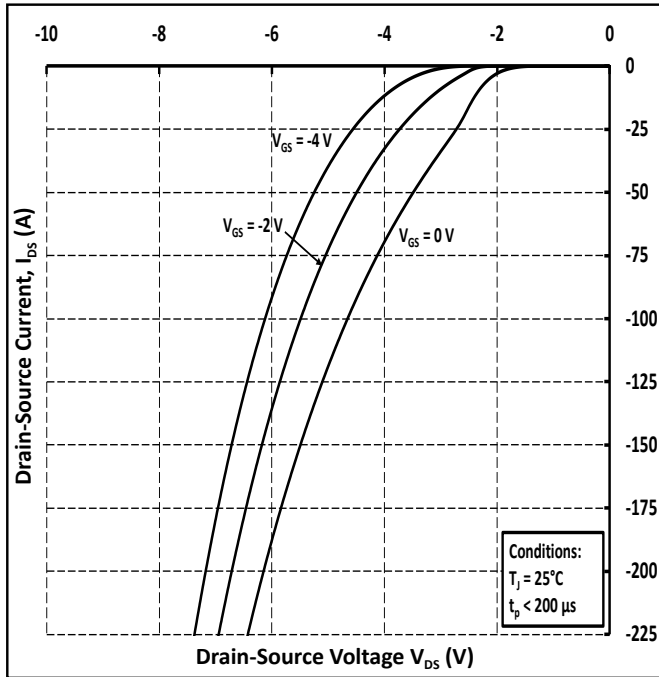


Figure 9. Body Diode Characteristic at 25 °C

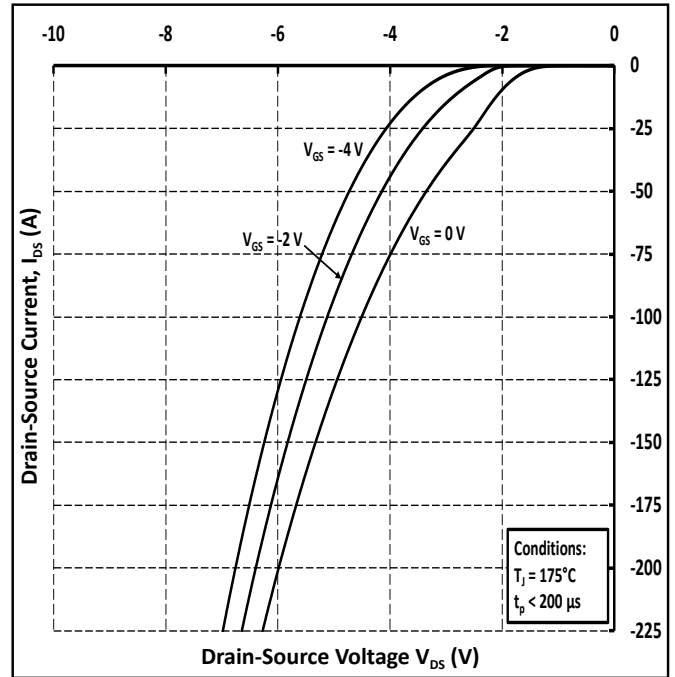


Figure 10. Body Diode Characteristic at 175 °C

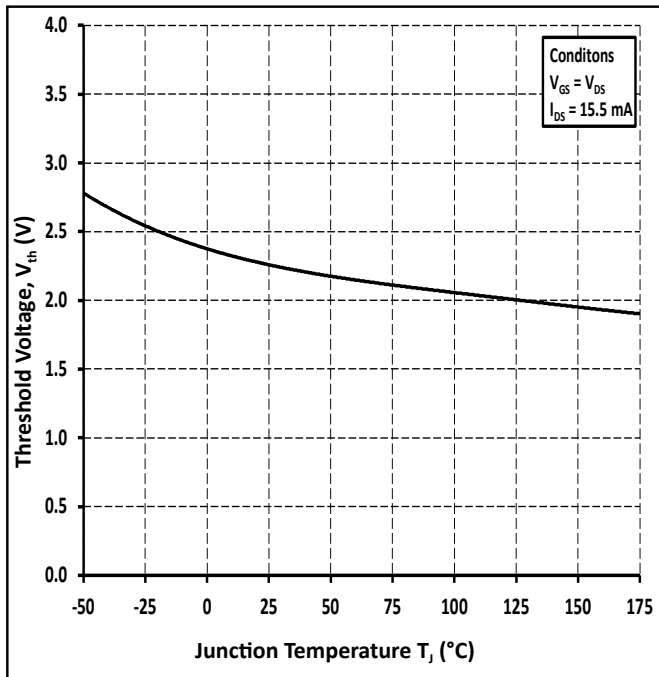


Figure 11. Threshold Voltage vs Temperature

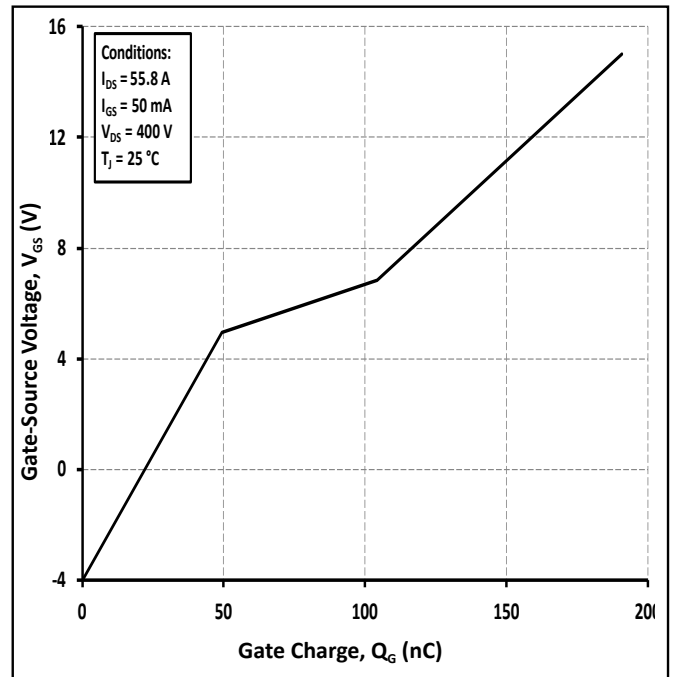


Figure 12. Gate Charge Characteristic



Typical Performance

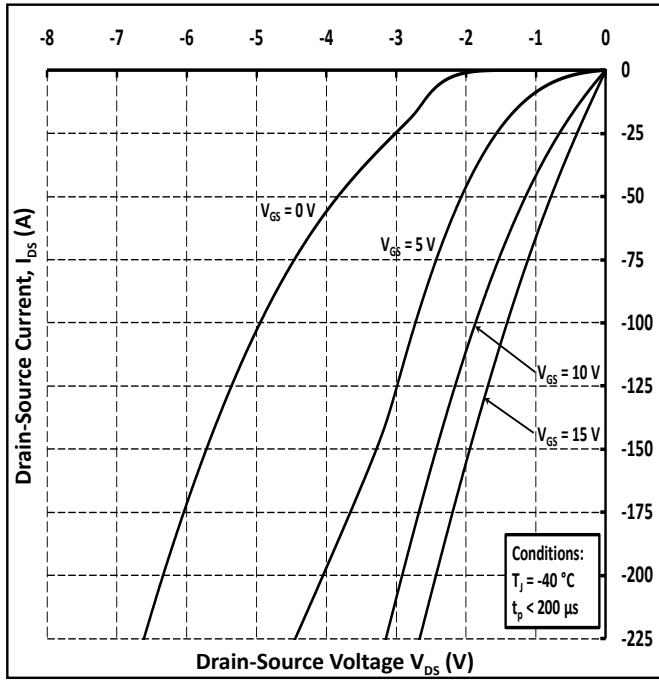


Figure 13. 3rd Quadrant Characteristic at -40 °C

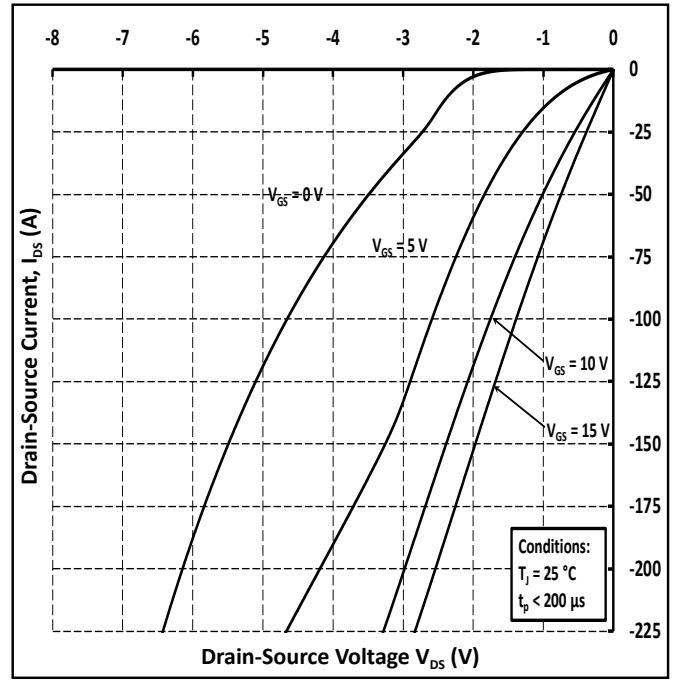


Figure 14. 3rd Quadrant Characteristic at 25 °C

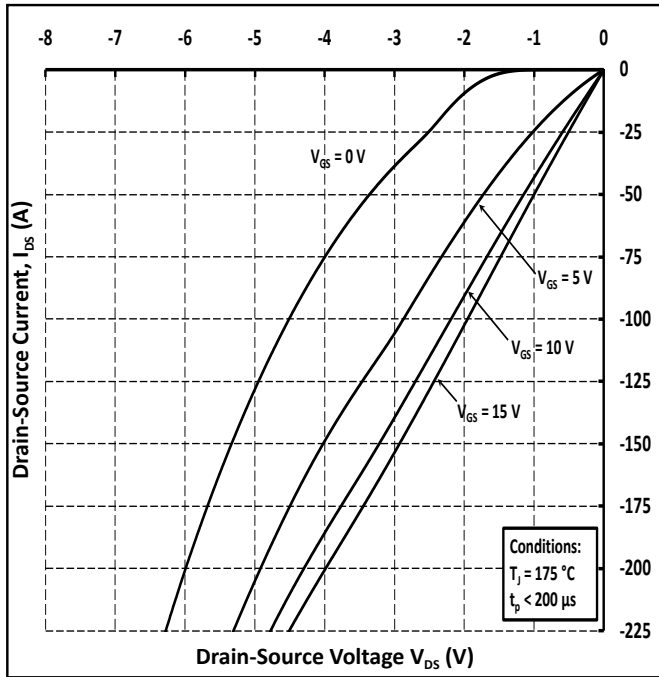


Figure 15. 3rd Quadrant Characteristic at 175 °C

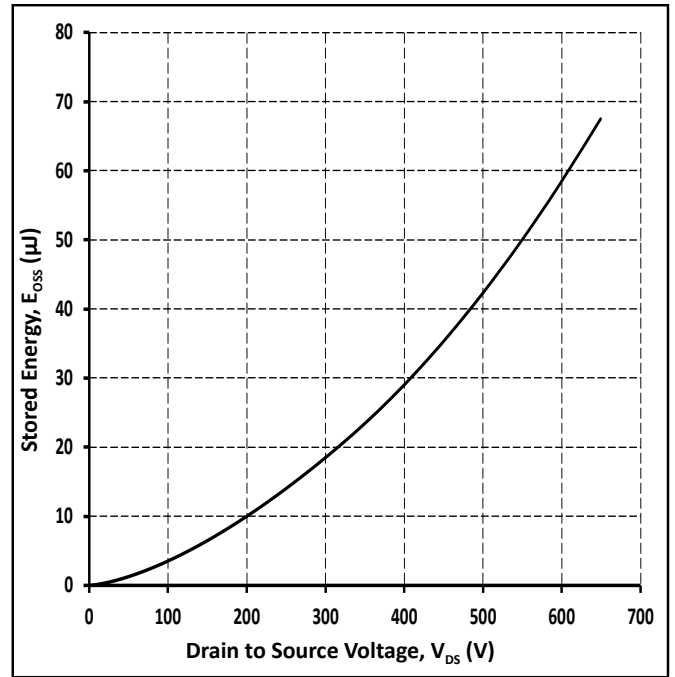


Figure 16. Output Capacitor Stored Energy



Typical Performance

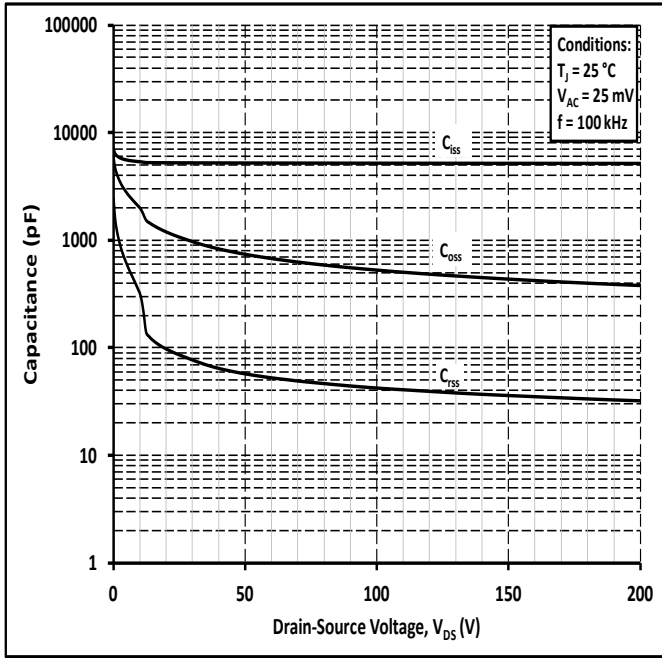


Figure 17. Capacitances vs Drain-Source Voltage (0-200 V)

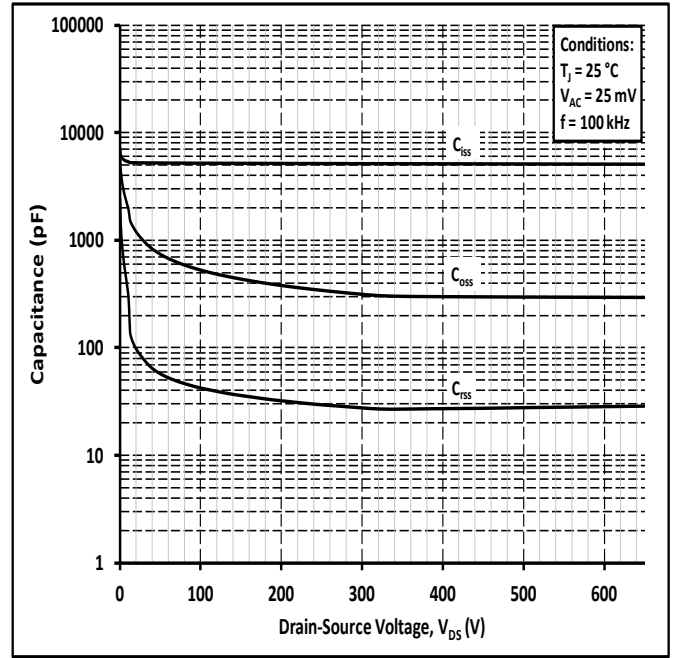


Figure 18. Capacitances vs Drain-Source Voltage (0-650 V)

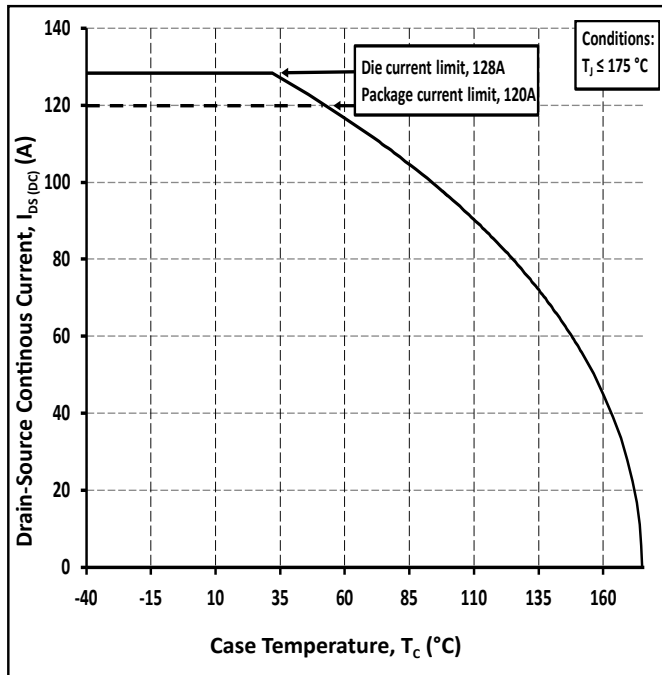


Figure 19. Continuous Drain Current Derating vs Case Temperature

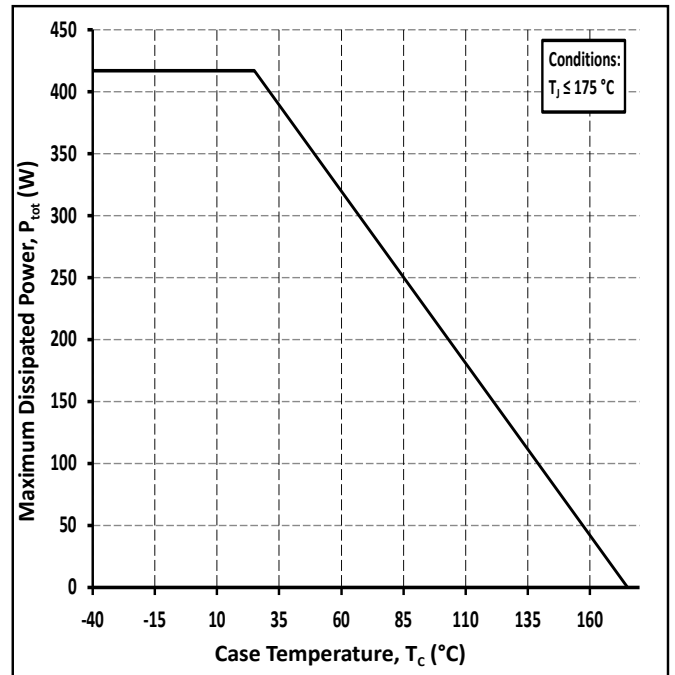


Figure 20. Maximum Power Dissipation Derating vs Case Temperature

Typical Performance

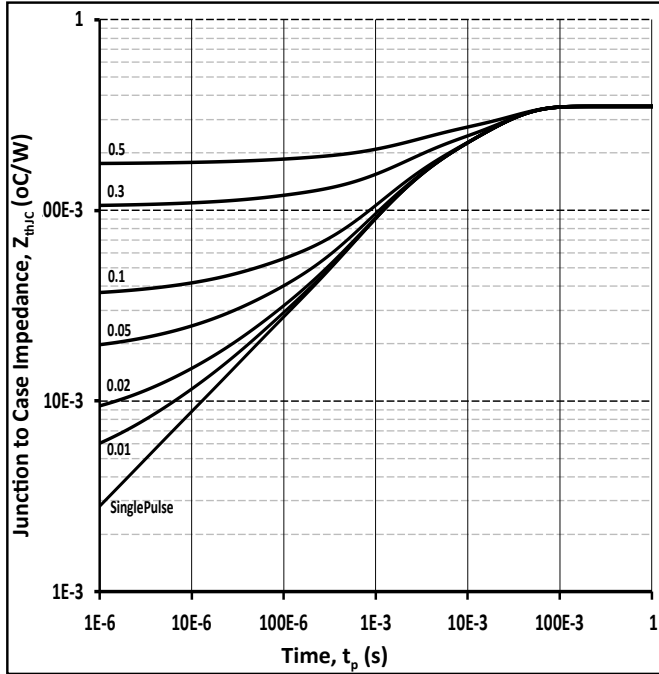


Figure 21. Transient Thermal Impedance (Junction - Case)

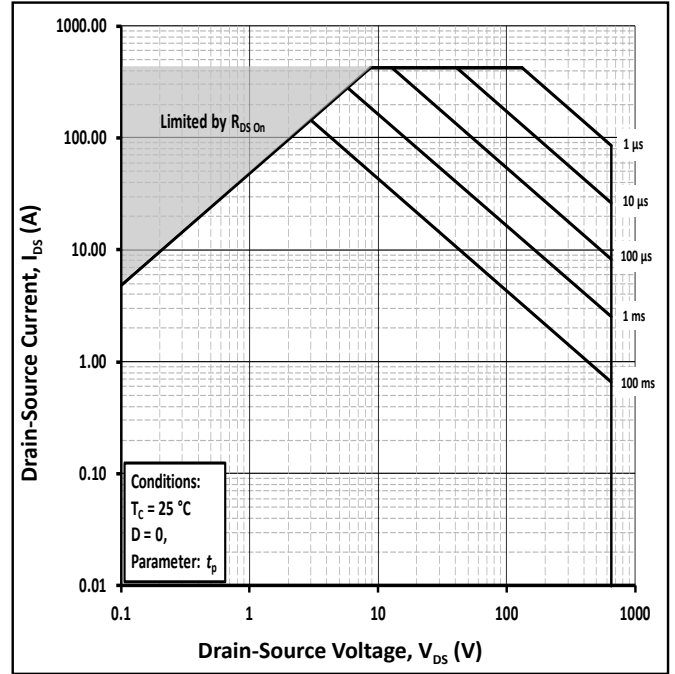


Figure 22. Safe Operating Area

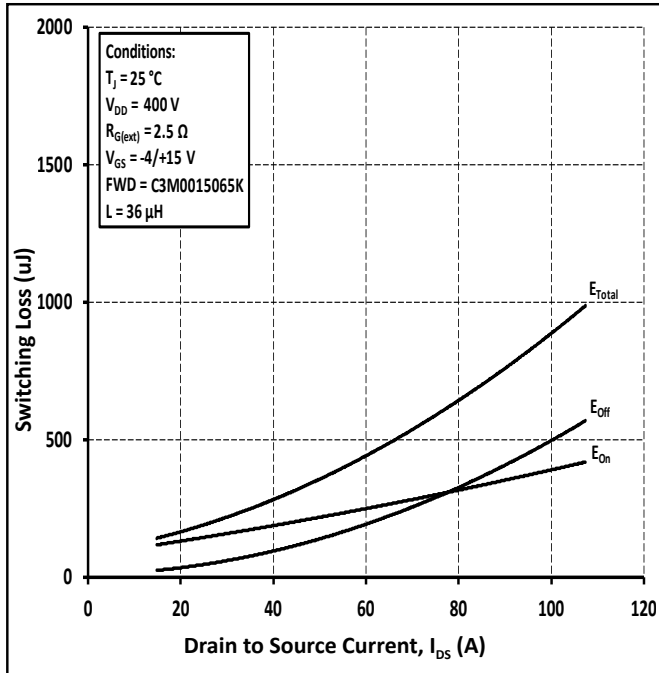


Figure 23. Clamped Inductive Switching Energy vs Drain Current ($V_{DD} = 400\text{ V}$)

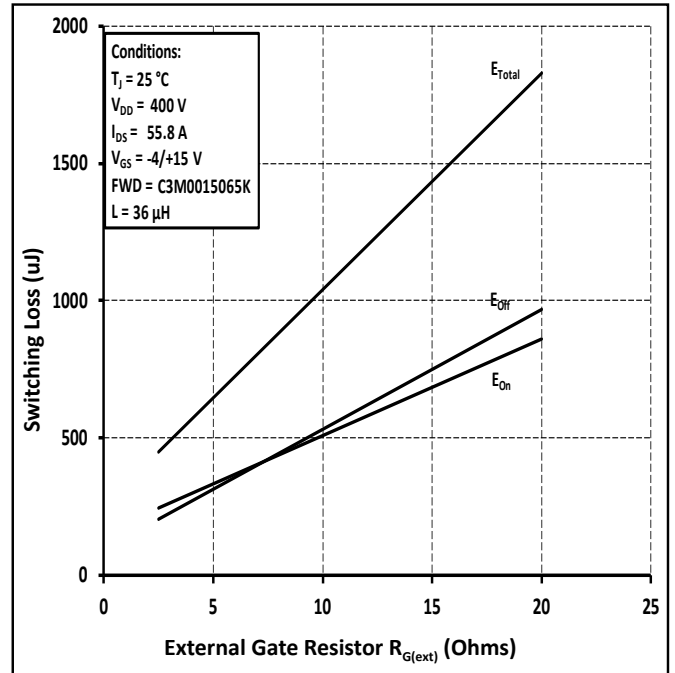


Figure 24. Clamped Inductive Switching Energy vs $R_{G(ext)}$



Typical Performance

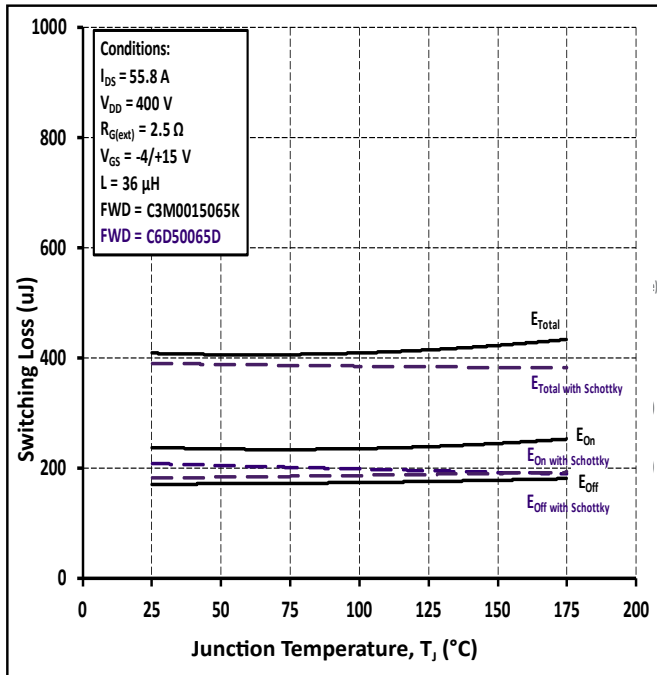


Figure 25. Clamped Inductive Switching Energy vs Temperature

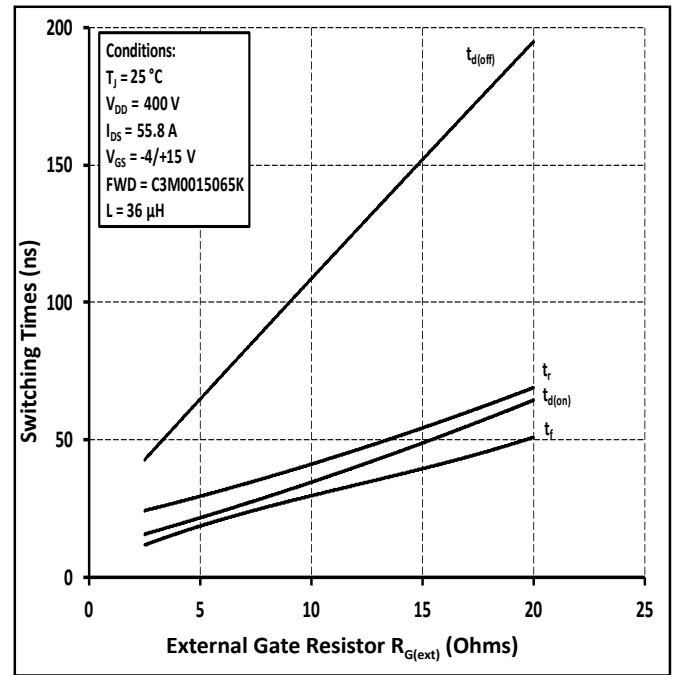


Figure 26. Switching Times vs $R_{G(ext)}$

Test Circuit Schematic

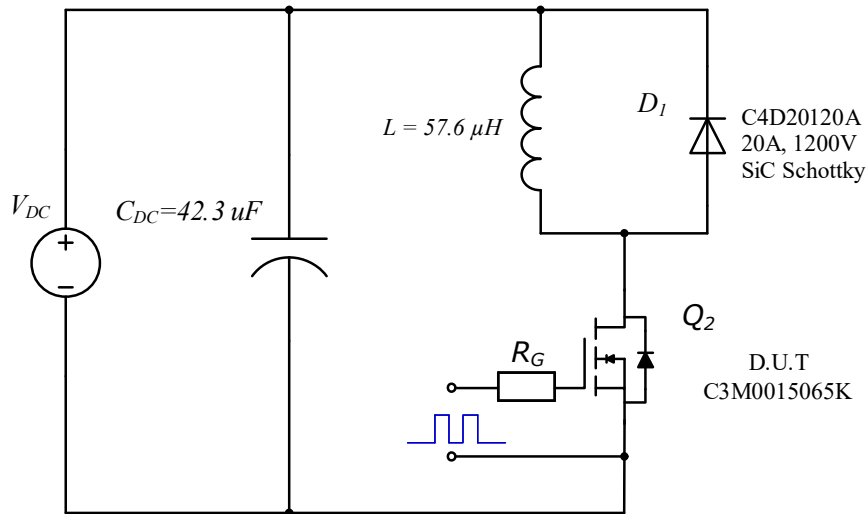


Figure 27. Clamped Inductive Switching Waveform Test Circuit

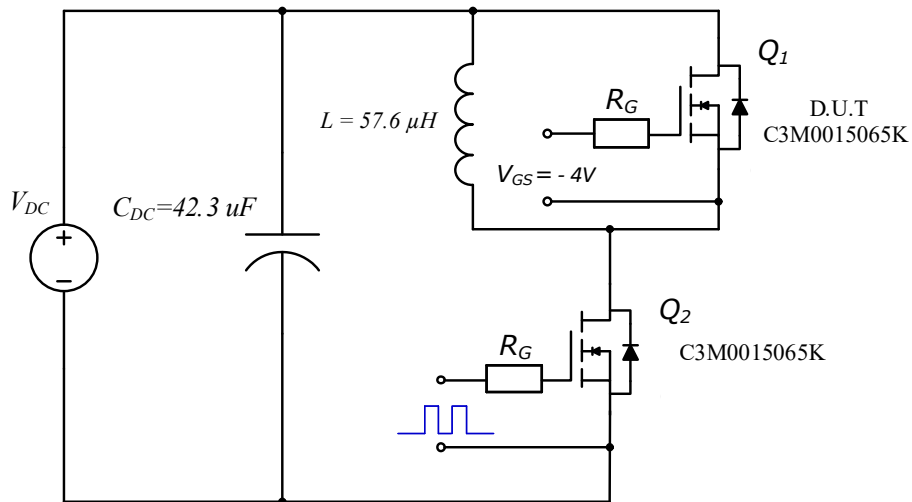
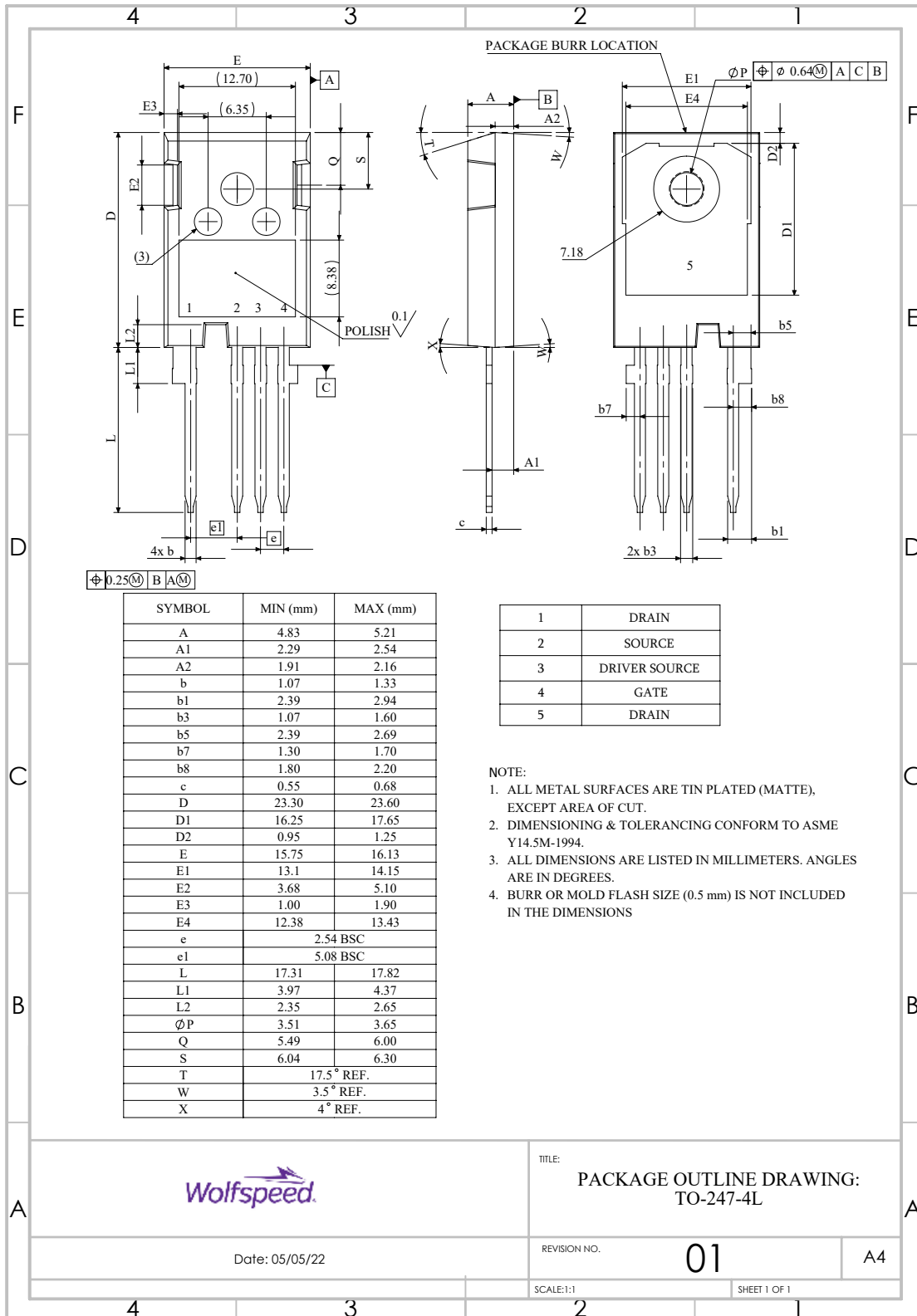


Figure 28. Body Diode Recovery Test Circuit



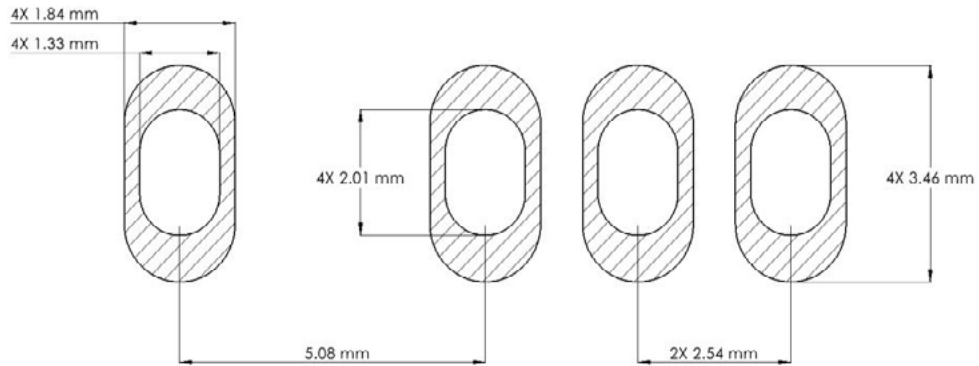
Package Dimensions

Package: TO-247-4L





Recommended Solder Pad Layout



Part Number	Package	Marking
C3M0015065K	TO-247-4L	C3M0015065K



Revision History

Current Revision	Date of Release	Description of Changes
6	September-2023	N/A
7	December-2023	Updated Wolfspeed branding, package drawing, and solder pad layout, package image, added revision history, Table 1 layout revised
8	April-2024	RDSO LSL Removed, Dynamic Data updated for 2.5 Ω and Fig 12, 23, 24, 25, and 26 updated accordingly



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