



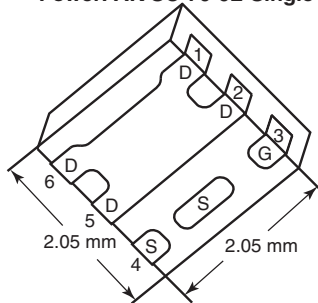
**THE DATASHEET OF
SIA477EDJ-T1-GE3**



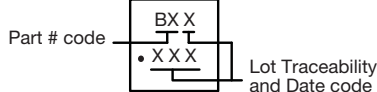
P-Channel 12 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A) ^a	Q _g (Typ.)
- 12	0.0140 at V _{GS} = - 4.5 V	- 12	34.7 nC
	0.0160 at V _{GS} = - 3.7 V	- 12	
	0.0190 at V _{GS} = - 2.5 V	- 12	
	0.0330 at V _{GS} = - 1.8 V	- 12	

PowerPAK SC-70-6L-Single



Marking Code



Ordering Information: SiA477EDJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

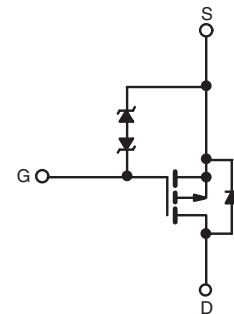
- TrenchFET[®] Power MOSFET
- Thermally Enhanced PowerPAK[®] SC-70 Package
- Small Footprint Area
- Low On-Resistance
- 100 % R_g Tested
- Built in ESD Protection with Zener Diode
- Typical ESD Performance: 3800 V (HBM)
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Portable Devices such as Smart Phones, Tablet PCs and Mobile Computing
- Battery Switch
- Load Switch
- Power Management



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 12	V
Gate-Source Voltage	V _{GS}	± 8	V
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 12 ^a
		T _C = 70 °C	- 12 ^a
		T _A = 25 °C	- 12 ^{a,b,c}
		T _A = 70 °C	- 10.6 ^{b,c}
Pulsed Drain Current (t = 300 μs)	I _{DM}	- 40	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	- 12 ^a
		T _A = 25 °C	- 2.9 ^{b,c}
Maximum Power Dissipation	P _D	T _C = 25 °C	19
		T _C = 70 °C	12
		T _A = 25 °C	3.5 ^{b,c}
		T _A = 70 °C	2.2 ^{b,c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	28	36	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	5.3	6.5		

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- t = 5 s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 80 °C/W.

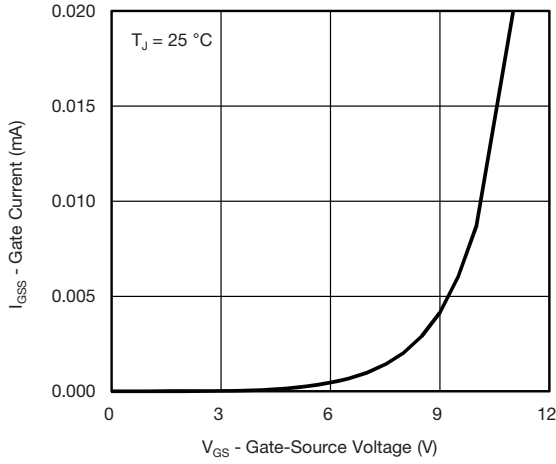
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-12			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-4		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.9		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.4		-1	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			± 30	μA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$			± 1	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}$			-1	
		$V_{DS} = -12\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-20			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -7\text{ A}$		0.0116	0.0140	Ω
		$V_{GS} = -3.7\text{ V}, I_D = -5\text{ A}$		0.0130	0.0160	
		$V_{GS} = -2.5\text{ V}, I_D = -3\text{ A}$		0.0158	0.0190	
		$V_{GS} = -1.8\text{ V}, I_D = -1\text{ A}$		0.0250	0.0330	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -6\text{ V}, I_D = -7\text{ A}$		31		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -6\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2970		pF
Output Capacitance	C_{oss}			710		
Reverse Transfer Capacitance	C_{rss}			724		
Total Gate Charge	Q_g	$V_{DS} = -6\text{ V}, V_{GS} = -8\text{ V}, I_D = -13.3\text{ A}$		58	87	nC
Gate-Source Charge		$V_{DS} = -6\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -13.3\text{ A}$		34.7	52	
Gate-Drain Charge	Q_{gd}			5.5		
Gate Resistance	R_g		$f = 1\text{ MHz}$	1	5	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\text{ V}, R_L = 0.6\text{ }\Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$		30	45	ns
Rise Time	t_r			28	42	
Turn-Off Delay Time	$t_{d(off)}$			74	111	
Fall Time	t_f			45	68	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\text{ V}, R_L = 0.6\text{ }\Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -8\text{ V}, R_g = 1\text{ }\Omega$		10	20	
Rise Time	t_r			9	18	
Turn-Off Delay Time	$t_{d(off)}$			80	120	
Fall Time	t_f			40	60	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			-12	A
Pulse Diode Forward Current	I_{SM}				-40	
Body Diode Voltage	V_{SD}	$I_S = -10\text{ A}, V_{GS} = 0\text{ V}$		-0.8	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		18	27	ns
Body Diode Reverse Recovery Charge	Q_{rr}			6	12	nC
Reverse Recovery Fall Time	t_a			11		ns
Reverse Recovery Rise Time	t_b			7		

Notes:

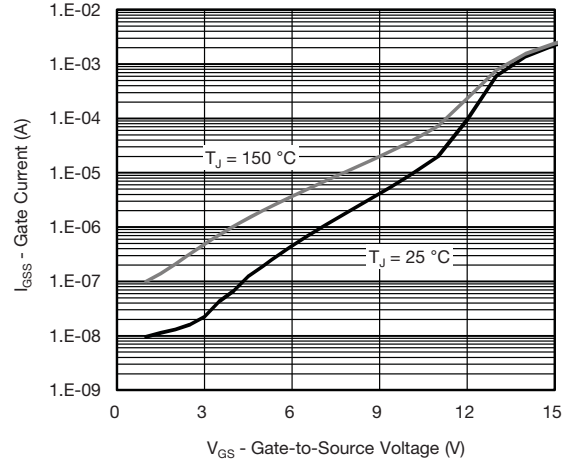
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

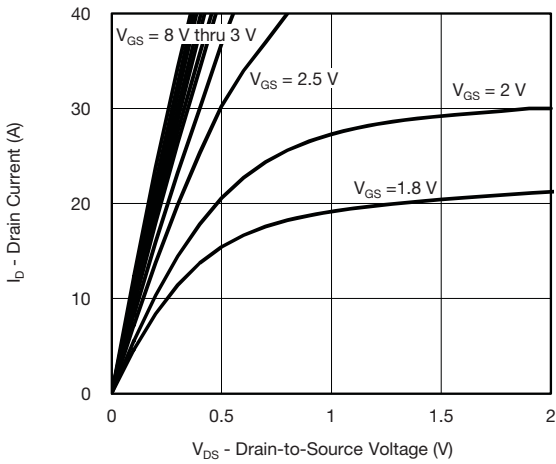
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



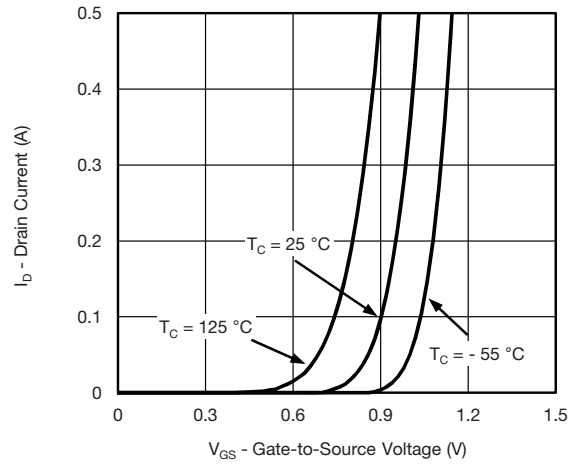
Gate-Source Voltage vs. Gate Current



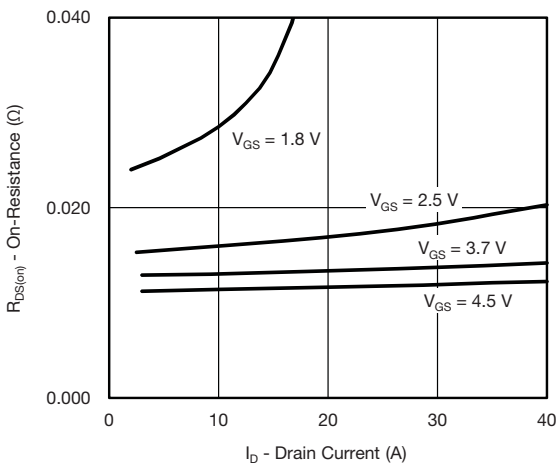
Gate-Source Voltage vs. Gate Current



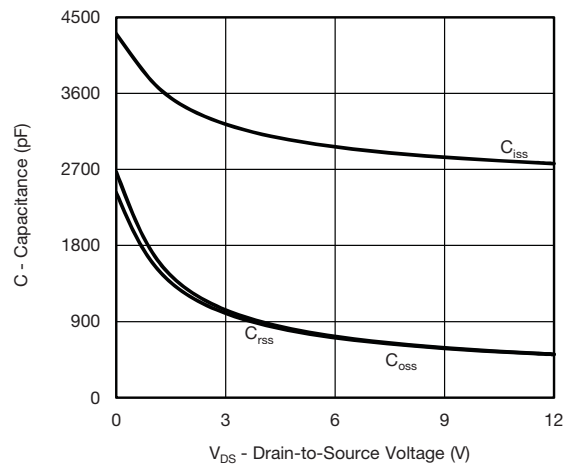
Output Characteristics



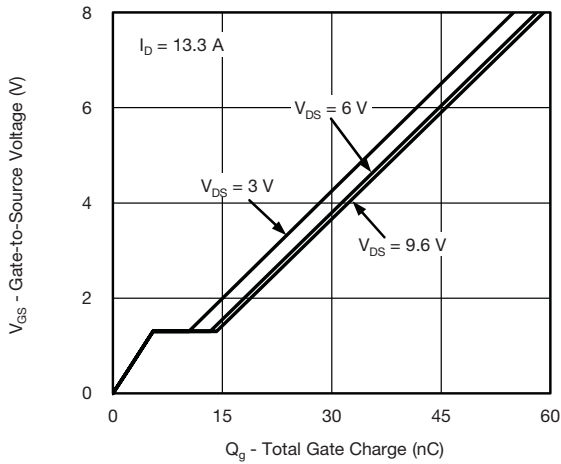
Transfer Characteristics



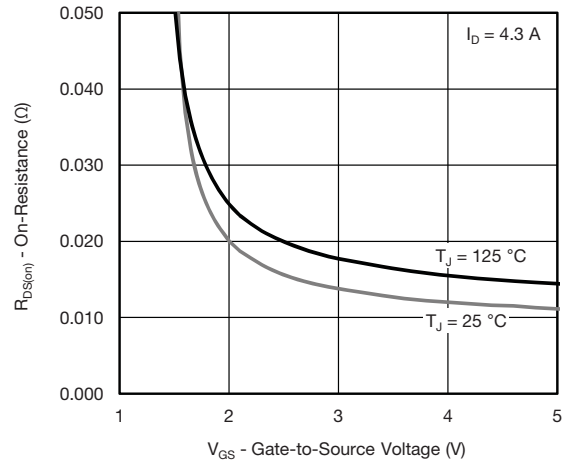
On-Resistance vs. Drain Current



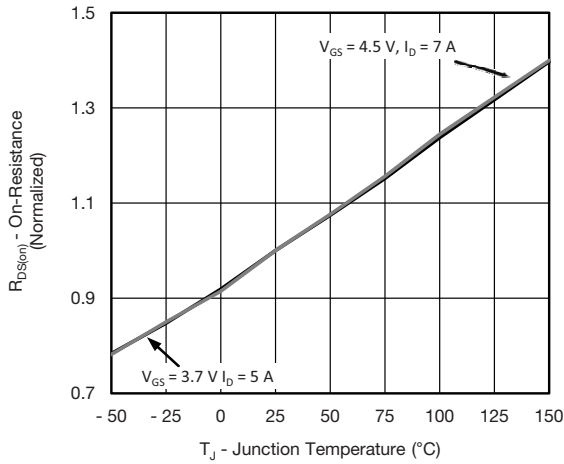
Capacitance



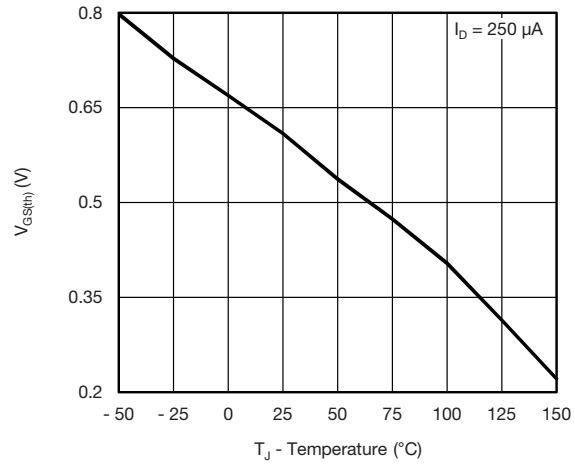
Gate Charge



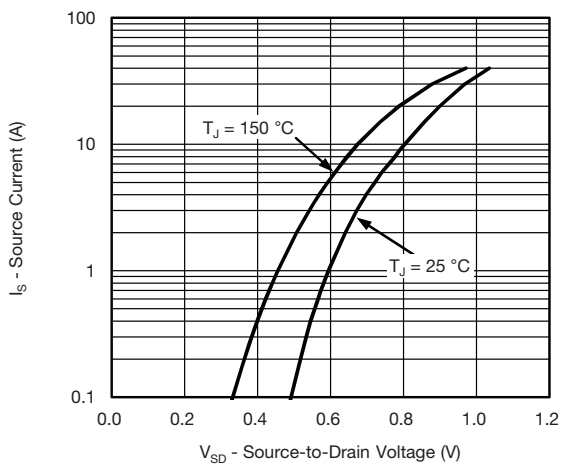
On-Resistance vs. Gate-to-Source Voltage



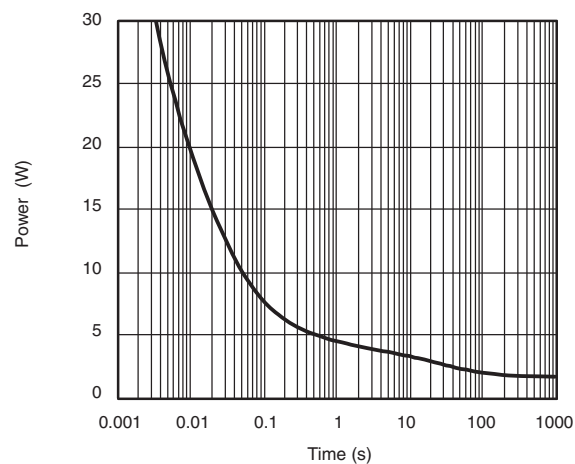
On-Resistance vs. Junction Temperature



Threshold Voltage

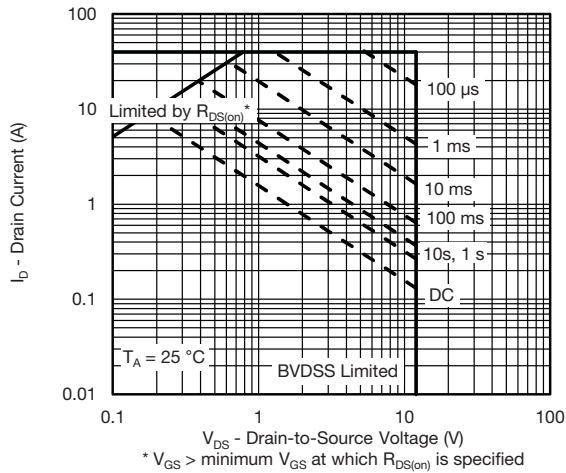


Source-Drain Diode Forward Voltage

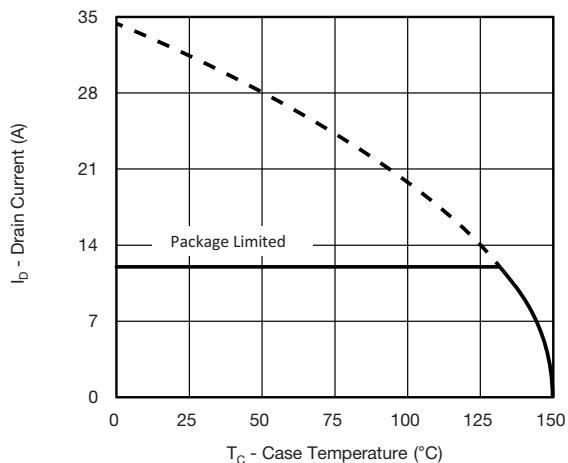


Single Pulse Power, Junction to Ambient

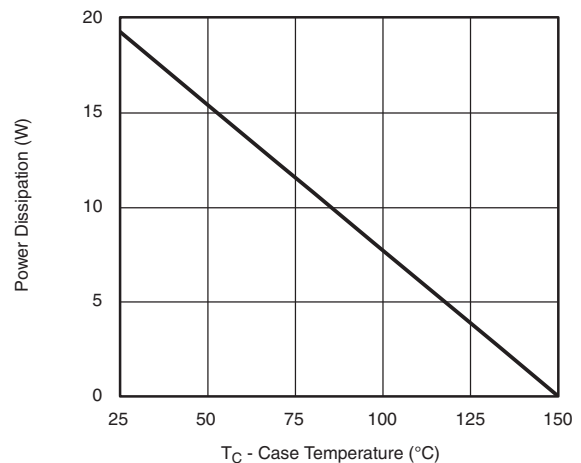
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



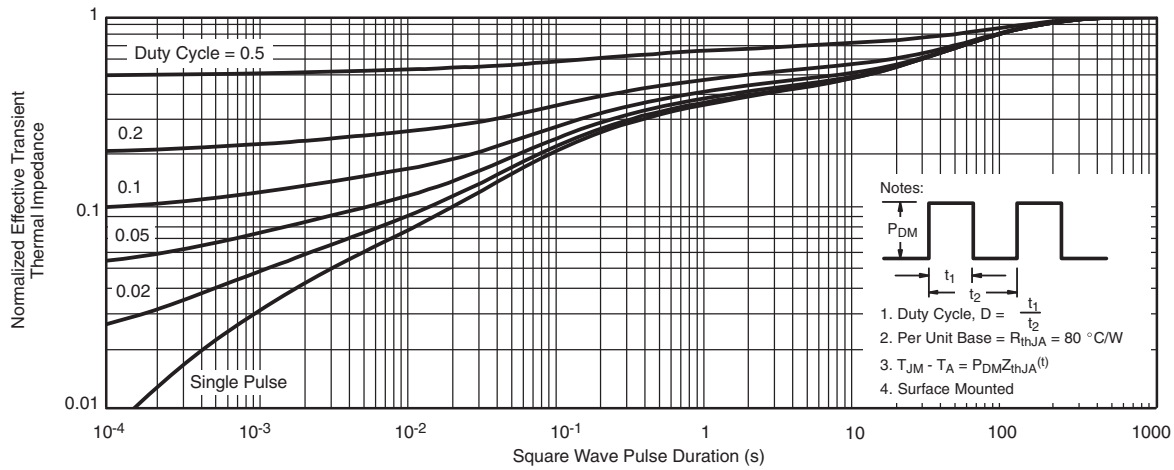
Current Derating*



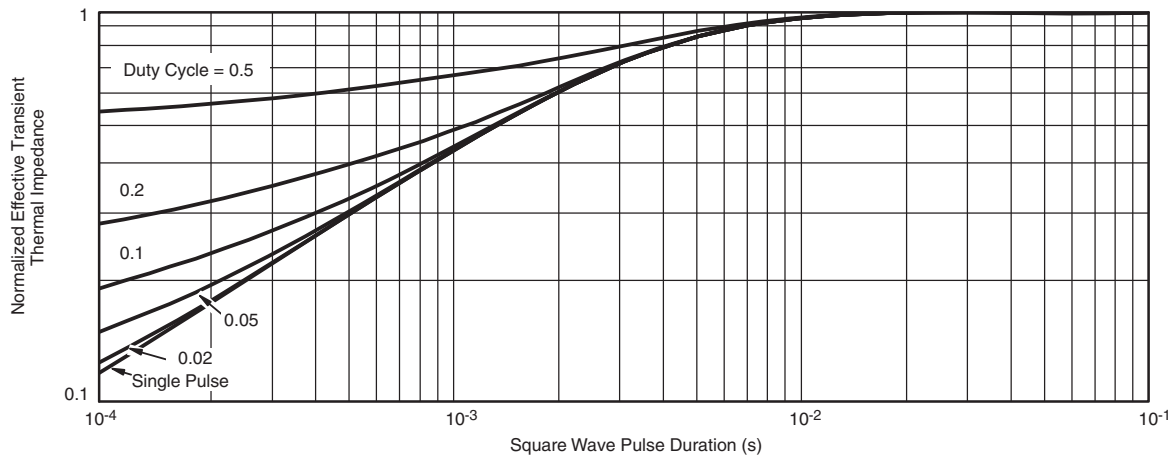
Power Derating

* The power dissipation P_D is based on $T_{J(max.)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



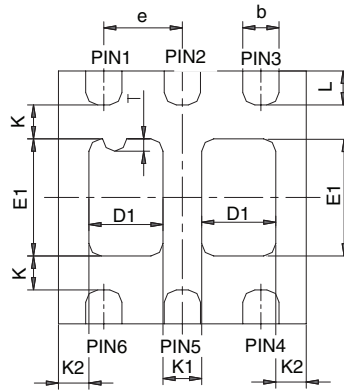
Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62798

PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE



BACKSIDE VIEW OF DUAL



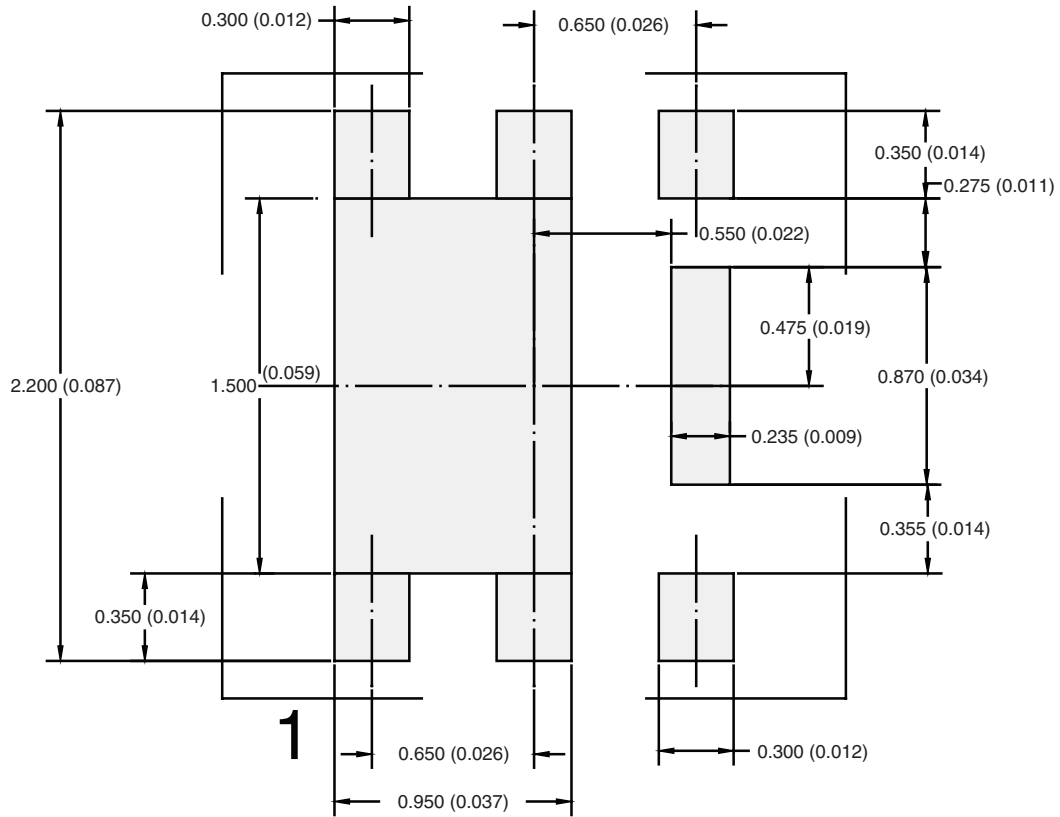
Notes:

1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C-07431 – Rev. C, 06-Aug-07
DWG: 5934

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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