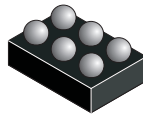




**THE DATASHEET OF
CSD75301W1015**





P-Channel NexFET™ Power MOSFET

 Check for Samples: [CSD75301W1015](#)

FEATURES

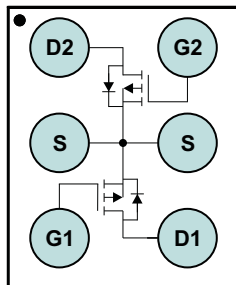
- Dual P-Ch MOSFETs
- Common Source Configuration
- Small Footprint 1mm x 1.5mm
- Low Profile – 0.62mm
- Ultra Low Qg and Qgd
- Pb Free / RoHS Compliant
- Halogen Free

APPLICATIONS

- Battery Management
- Load Switch
- Battery Protection

DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile.

Figure 1. Top View


PRODUCT SUMMARY

(Per MOSFET unless otherwise stated)			
V_{DS}	Drain to Source Voltage	-20	V
Q_g	Gate Charge Total (4.5V)	1.5	nC
Q_{gd}	Gate Charge Gate to Drain	0.3	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -1.8V$	150 mΩ
		$V_{GS} = -2.5V$	105 mΩ
		$V_{GS} = -4.5V$	80 mΩ
$V_{GS(th)}$	Voltage threshold	-0.7	V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD75301W1015	1 x 1.5 Wafer Level Package	7-inch reel	3000	Tape and Reel

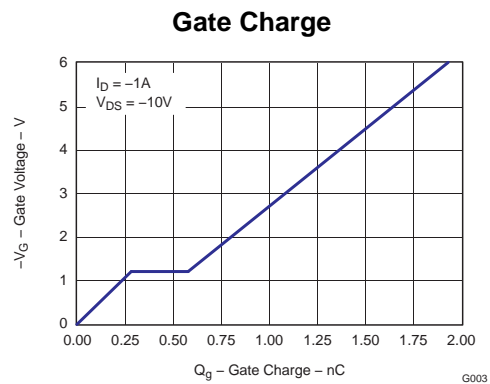
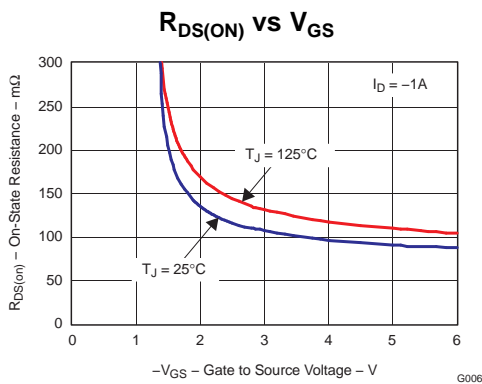
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Continuous Drain Current, $T_C = 25^\circ\text{C}^{(1) (2)}$	-1.2	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}^{(1) (2) (3)}$	-17.5	A
P_D	Power Dissipation ^{(1) (2)}	0.8	W
T_J , T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C

(1) Per device, both devices in conduction.

(2) $R_{\theta JA} = 74^\circ\text{C/W}$ on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.

(3) Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated) (Per MOSFET unless otherwise stated)

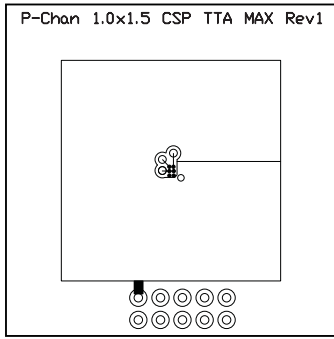
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = -16V$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = -8V$			-100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.4	-0.7	-1.0	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -1.8V, I_D = -1A$		150	190	m Ω
		$V_{GS} = -2.5V, I_D = -1A$		105	135	m Ω
		$V_{GS} = -4.5V, I_D = -1A$		80	100	m Ω
g_{fs}	Transconductance	$V_{DS} = -10V, I_D = -1A$		5.2		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{GS} = 0V, V_{DS} = -10V, f = 1MHz$		150	195	pF
C_{OSS}	Output Capacitance			67	87	pF
C_{RSS}	Reverse Transfer Capacitance			24	31	pF
Q_g	Gate Charge Total (-4.5V)	$V_{DS} = -10V, I_D = -1A$		1.5	2.1	nC
Q_{gd}	Gate Charge Gate to Drain			0.3		nC
Q_{gs}	Gate Charge Gate to Source			0.28		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.12		nC
Q_{OSS}	Output Charge	$V_{DS} = -9.5V, V_{GS} = 0V$		1.1		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = -10V, V_{GS} = -4.5V, I_D = -1A$ $R_G = 30\Omega$		3		ns
t_r	Rise Time			1.7		ns
$t_{d(off)}$	Turn Off Delay Time			38		ns
t_f	Fall Time			16		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_S = -1A, V_{GS} = 0V$	-0.81		-1	V
Q_{rr}	Reverse Recovery Charge	$V_{dd} = -9.5V, I_F = -1A, di/dt = 200A/\mu s$		2		nC
t_{rr}	Reverse Recovery Time	$V_{dd} = -9.5V, I_F = -1A, di/dt = 200A/\mu s$		7.5		ns

THERMAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

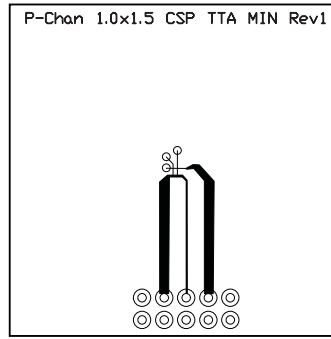
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Ambient ^{(1) (2)}			136	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^{(2) (3)}			93	$^\circ\text{C/W}$

- (1) Device mounted on FR4 material with Minimum Cu mounting area.
- (2) Measured with both devices biased in a parallel condition.
- (3) Device mounted on FR4 material with 1in^2 of 2 oz Cu.



Max $R_{\theta JA} = 93^{\circ}\text{C/W}$
when mounted on
1inch² of 2 oz. Cu.

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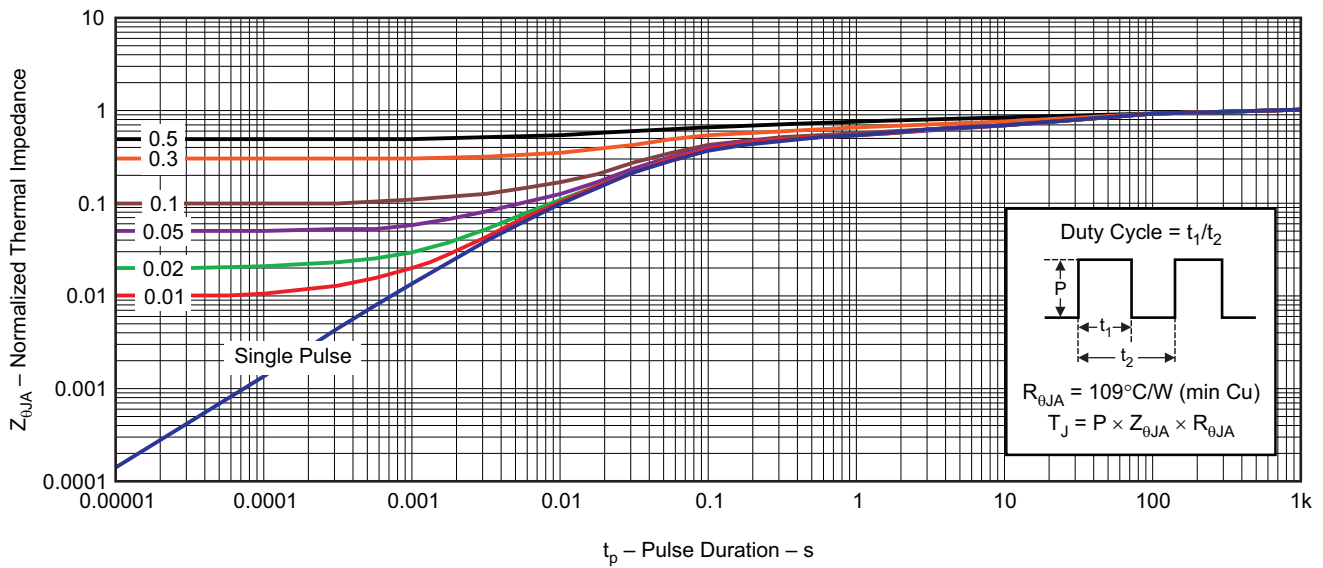


Max $R_{\theta JA} = 136^{\circ}\text{C/W}$
when mounted on
minimum pad area of 2
oz. Cu.

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TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



G012

Figure 2. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

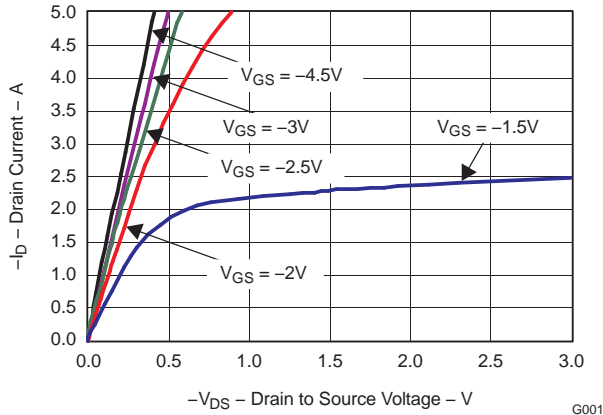


Figure 3. Saturation Characteristics

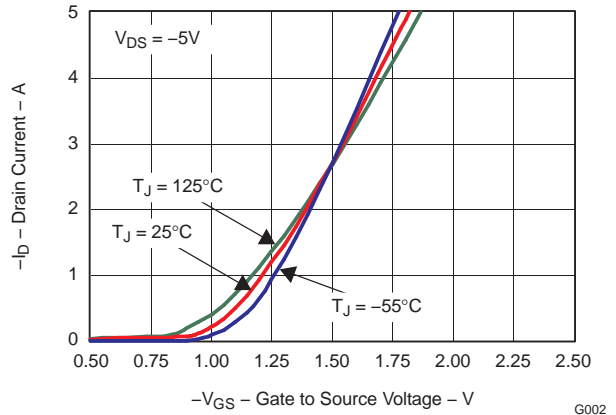


Figure 4. Transfer Characteristics

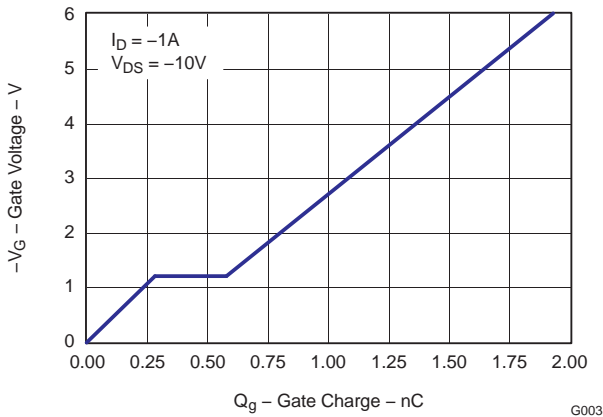


Figure 5. Gate Charge

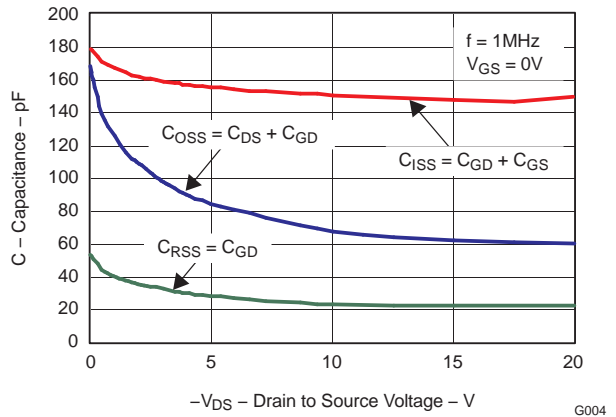


Figure 6. Capacitance

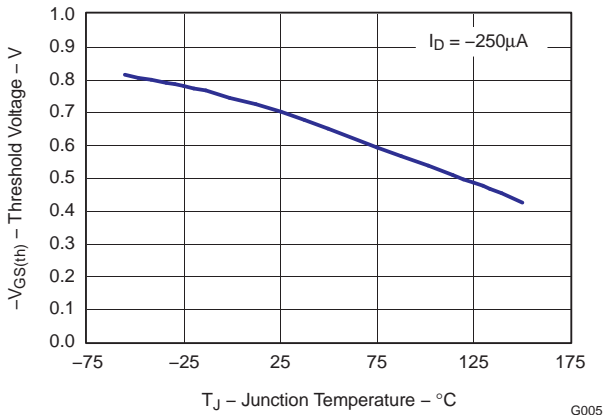


Figure 7. Threshold Voltage vs. Temperature

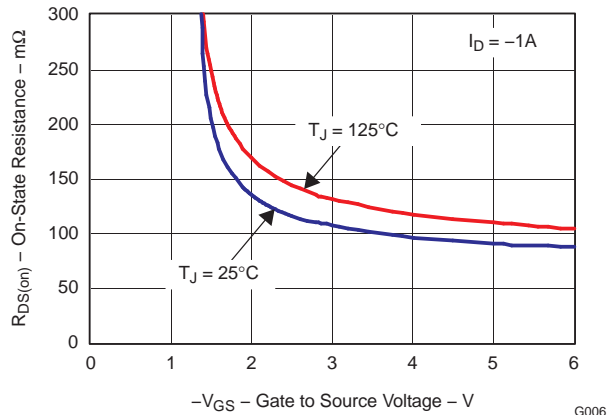


Figure 8. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

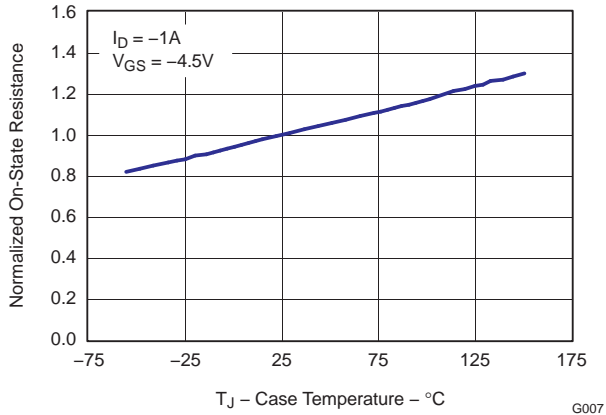


Figure 9. On Resistance vs. Temperature

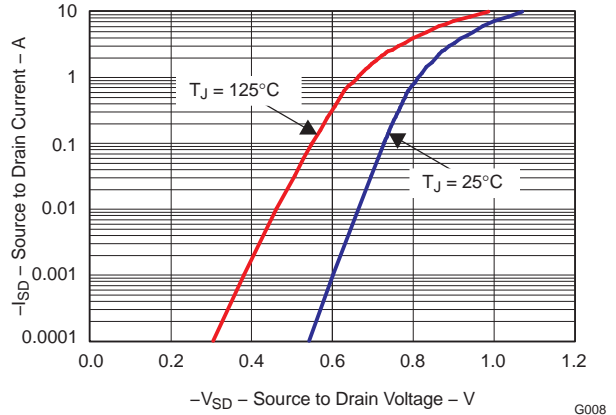


Figure 10. Typical Diode Forward Voltage

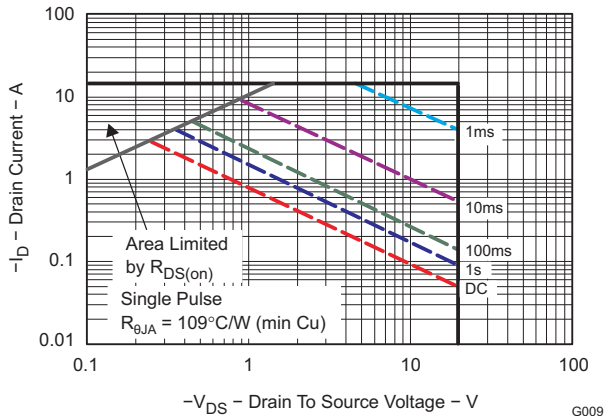


Figure 11. Maximum Safe Operating Area

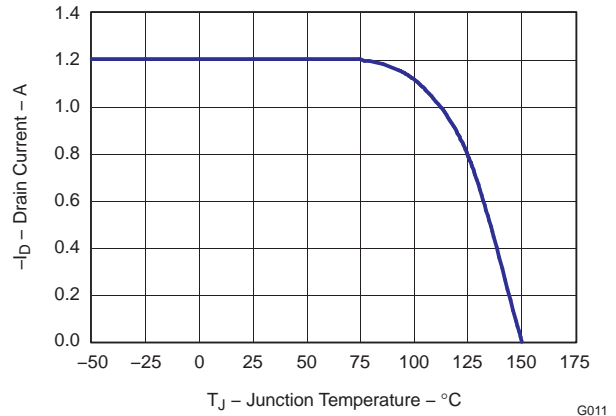
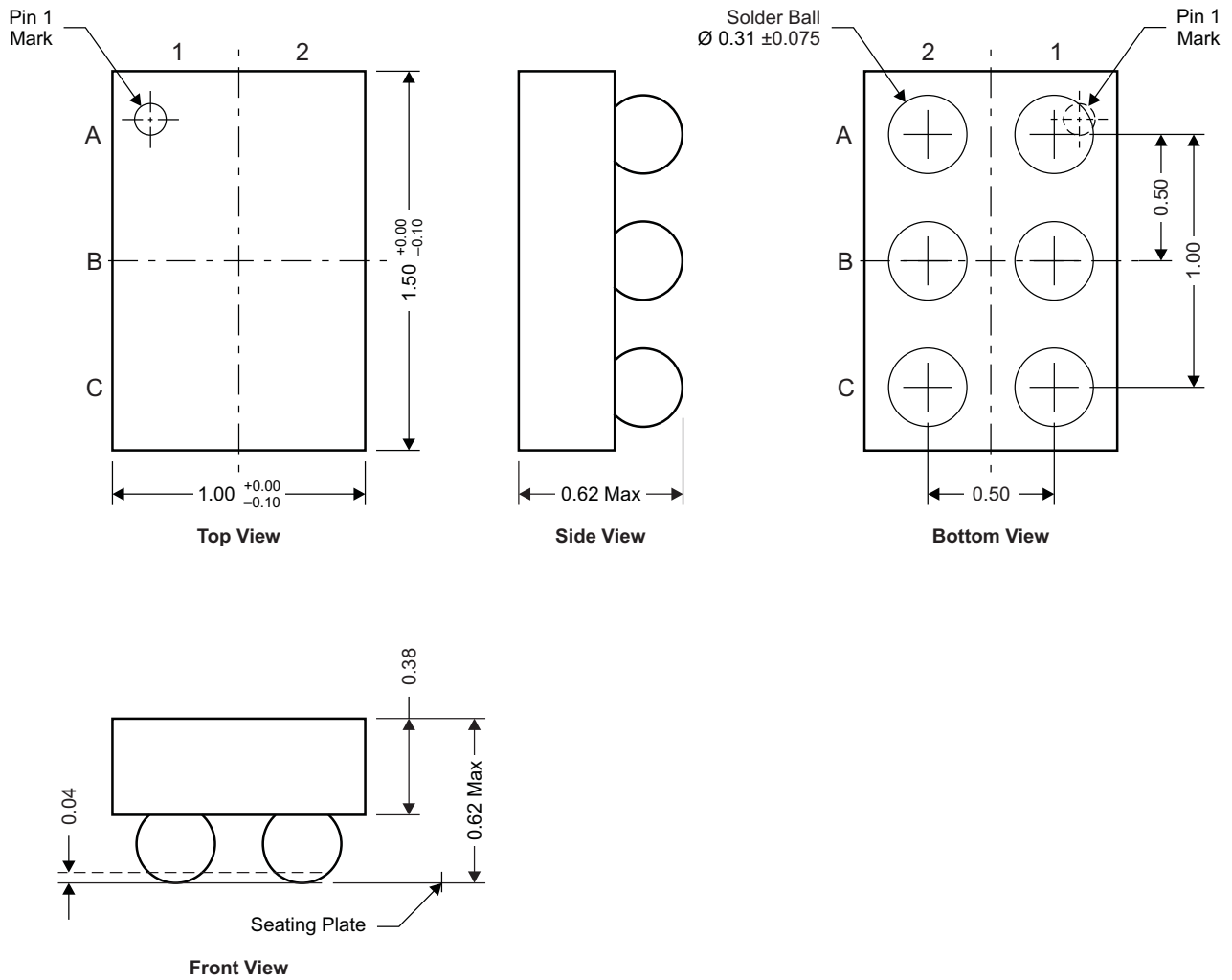


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

CSD75301W1015 Package Dimensions



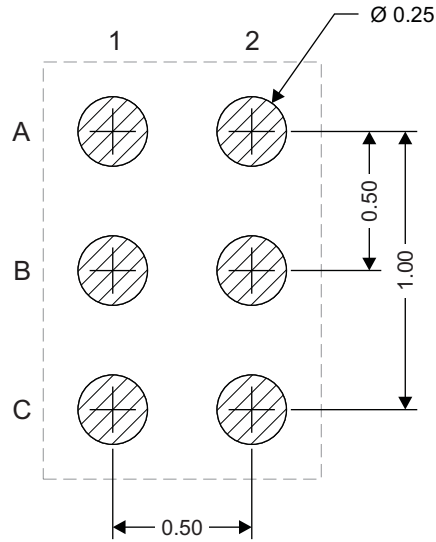
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NOTE: All dimensions are in mm (unless otherwise specified)

Pinout

POSITION	DESIGNATION
B1, B2	Source
C1	Gate1
C2	Drain1
A2	Gate2
A1	Drain2

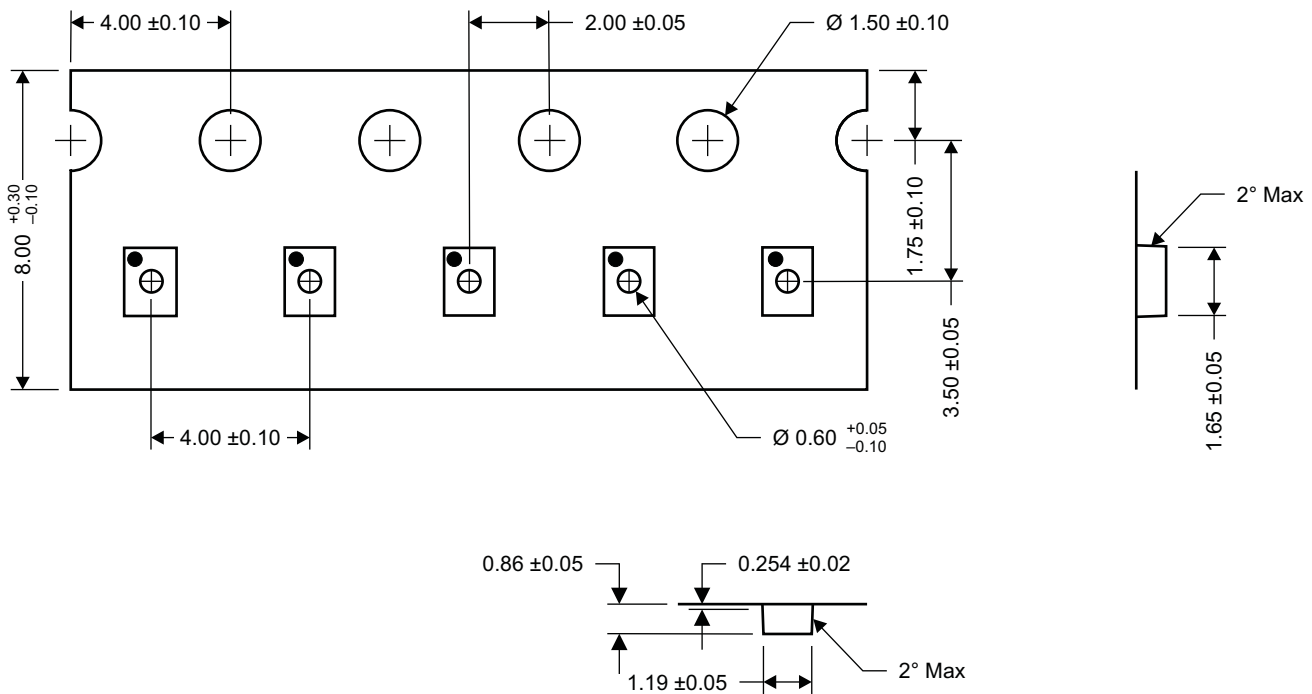
Land Pattern Recommendation



M0158-01

NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information



M0159-01

NOTE: All dimensions are in mm (unless otherwise specified)

REVISION HISTORY

Changes from Original (August 2009) to Revision A **Page**

- Changed location of the Pin 1 indicator dot in the pin out illustration. 1

Changes from Revision A (November 2009) to Revision B **Page**

- Deleted the Package Marking Information section 7

Changes from Revision B (November 2009) to Revision C **Page**

- Changed the CSD75301W1015 Package Dimensions section. Top View From: 15.00 To: 1.50 6

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