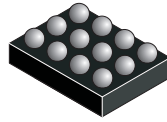




**THE DATASHEET OF  
CSD86311W1723**





## Dual N-Channel NexFET™ Power MOSFET

 Check for Samples: [CSD86311W1723](#)

### FEATURES

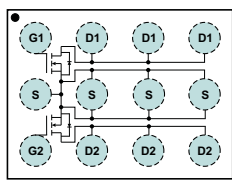
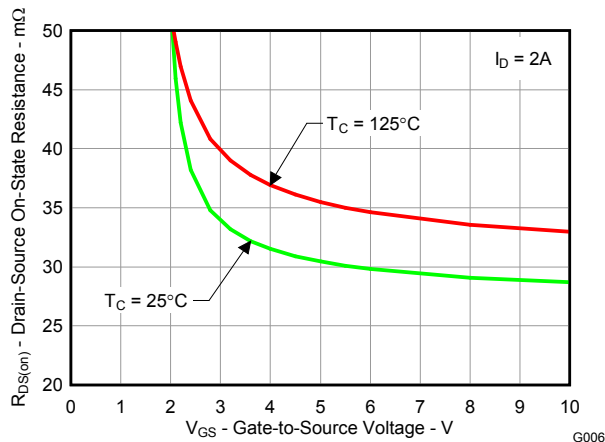
- Dual N-Ch MOSFETs
- Common Source Configuration
- Small Footprint 1.7 mm × 2.3 mm
- Ultra Low  $Q_g$  and  $Q_{gd}$
- Pb Free
- RoHS Compliant
- Halogen Free

### APPLICATIONS

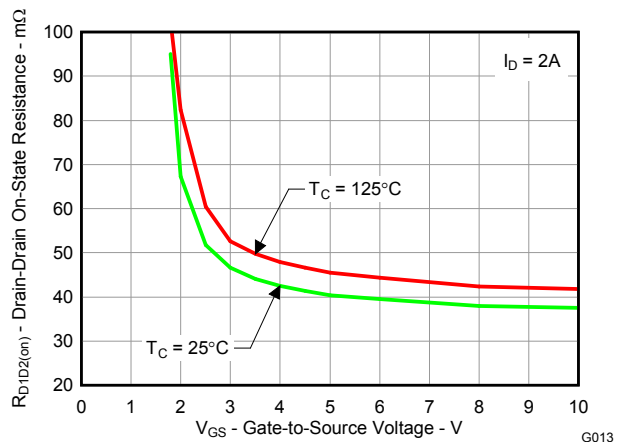
- Battery Management
- Battery Protection
- DC-DC Converters

### DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with thermal characteristics in an ultra low profile. Low on resistance and gate charge coupled with the small footprint and low profile make the device ideal for battery operated space constrained application in load management as well as DC-DC converter applications

**Top View**

 **$R_{DS(on)}$  VS  $V_{GS}$** 


G006

 **$R_{D1D2(on)}$  VS  $V_{GS}$** 


G013

### PRODUCT SUMMARY

$V_{DS}$	Drain to Source Voltage	25	V
$Q_g$	Gate Charge Total (4.5V)	3.1	nC
$Q_{gd}$	Gate Charge Gate to Drain	0.33	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 2.5V$	37 mΩ
		$V_{GS} = 4.5V$	31 mΩ
		$V_{GS} = 8V$	29 mΩ
$V_{GS(th)}$	Threshold Voltage	1	V

### ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD86311W1723	1.7-mm × 2.3-mm Wafer Level Package	7-inch reel	3000	Tape and Reel

### ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	25	V
$V_{GS}$	Gate to Source Voltage	+10 / -8	V
$I_D$	Continuous Drain Current <sup>(1)</sup> <sup>(2)(3)</sup>	4.5	A
	Pulsed Drain Current <sup>(1)</sup> <sup>(2)(3)</sup>		
$I_G$	Continuous Gate Clamp Current <sup>(4)</sup>	6	A
	Pulsed Gate Clamp Current <sup>(4)</sup>		
$P_D$	Power Dissipation <sup>(1)</sup>	1.5	W
$T_J$ , $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

- (1) May be limited by Max source current
- (2) Based on Min Cu footprint
- (3) Per MOSFET
- (4) Total for device



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

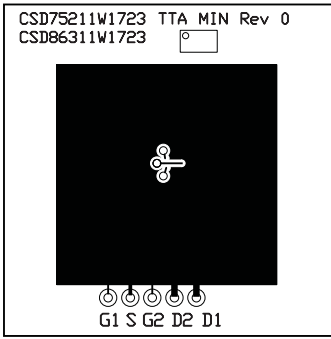
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b>						
$BV_{DSS}$	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	25			V
$I_{DSS}$	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 20V$			1	$\mu A$
$I_{GSS}$	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +10 / -8V$			$\pm 100$	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.85	1	1.4	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 2.5V, I_{DS} = 2A$		37	51	m $\Omega$
		$V_{GS} = 4.5V, I_{DS} = 2A$		31	42	m $\Omega$
		$V_{GS} = 8V, I_{DS} = 2A$		29	39	m $\Omega$
$R_{DD(on)}$	Drain to Drain On Resistance	$V_{GS} = 2.5V, I_D = 2A$		52	75	m $\Omega$
		$V_{GS} = 4.5V, I_{DS} = 2A$		41	55	m $\Omega$
		$V_{GS} = 8V, I_{DS} = 2A$		38	50	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 10V, I_D = 2A$		6.4		S
<b>Dynamic Characteristics</b>						
$C_{ISS}$	Input Capacitance	$V_{GS} = 0V,$ $V_{DS} = 12.5V,$ $f = 1MHz$		450	585	pF
$C_{OSS}$	Output Capacitance			250	325	pF
$C_{RSS}$	Reverse Transfer Capacitance			10	13	pF
$R_G$	Series Gate Resistance			1.4	2.8	$\Omega$
$Q_g$	Gate Charge Total (4.5V)	$V_{DS} = 12.5V,$ $I_D = 2A$		3.1	4	nC
$Q_{gd}$	Gate Charge Gate to Drain			0.33		nC
$Q_{gs}$	Gate Charge Gate to Source			0.85		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			0.48		nC
$Q_{OSS}$	Output Charge	$V_{DS} = 12.2V, V_{GS} = 0V$		4.5		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 12.5V, V_{GS} = 4.5V,$ $I_D = 2A, R_G = 2\Omega$		5.4		ns
$t_r$	Rise Time			4.3		ns
$t_{d(off)}$	Turn Off Delay Time			13.2		ns
$t_f$	Fall Time			2.9		ns
<b>Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage	$I_S = 2A, V_{GS} = 0V$		0.78	1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{dd} = 12.2V, I_F = 2A,$ $di/dt = 300A/\mu s$		4.2		nC
$t_{rr}$	Reverse Recovery Time			13.4		ns

## THERMAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

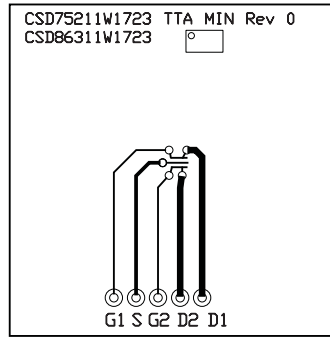
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (Minimum Cu area) <sup>(1)</sup> <sup>(2)</sup>			165	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (1 in <sup>2</sup> Cu area) <sup>(2)</sup> <sup>(3)</sup>			68	$^\circ\text{C}/\text{W}$

- (1) Device mounted on FR4 material with minimum Cu mounting area.
- (2) Measured with both devices biased in a parallel condition.
- (3) Device mounted on FR4 material with 1 in<sup>2</sup> of 2oz. Cu.



M0182-01

Max  $R_{\theta JA} = 68^{\circ}\text{C/W}$   
when mounted on  
1inch<sup>2</sup> of 2 oz. Cu.

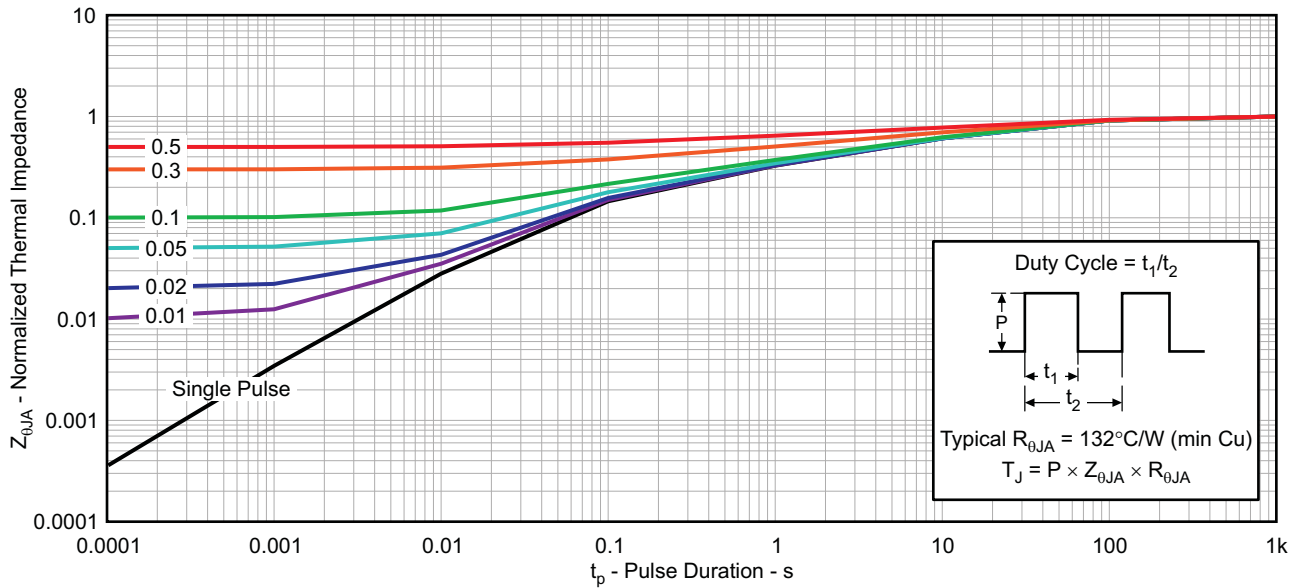


M0183-01

Max  $R_{\theta JA} = 165^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of 2  
oz. Cu.

### TYPICAL MOSFET CHARACTERISTICS

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)

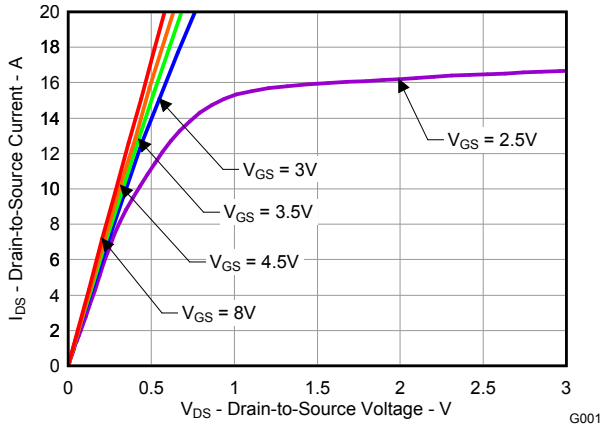


G012

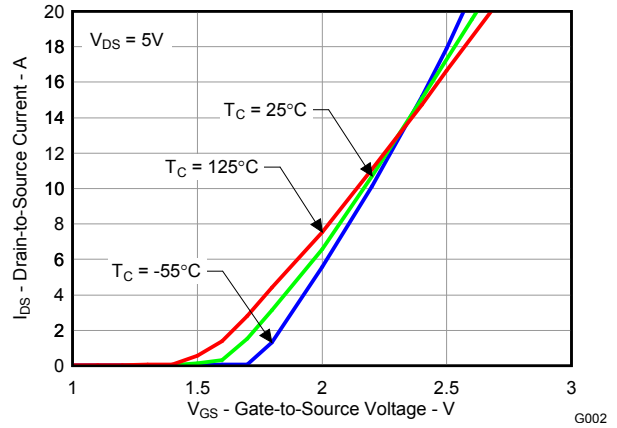
Figure 1. Transient Thermal Impedance

**TYPICAL MOSFET CHARACTERISTICS (continued)**

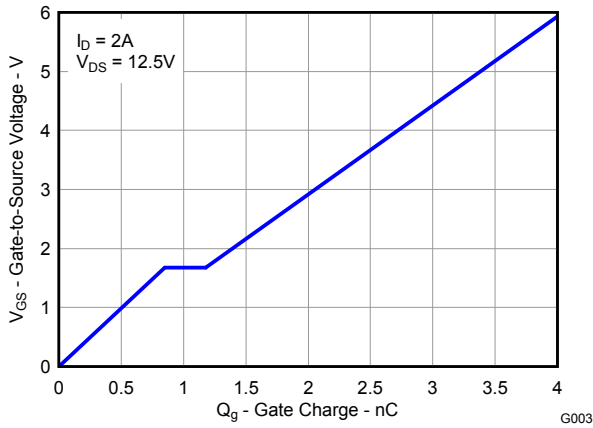
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



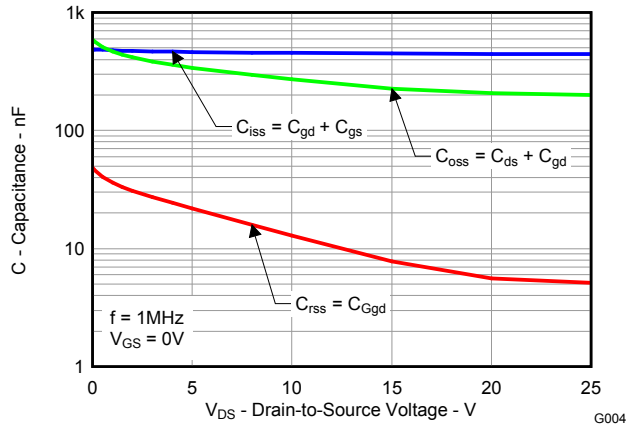
**Figure 2. Saturation Characteristics**



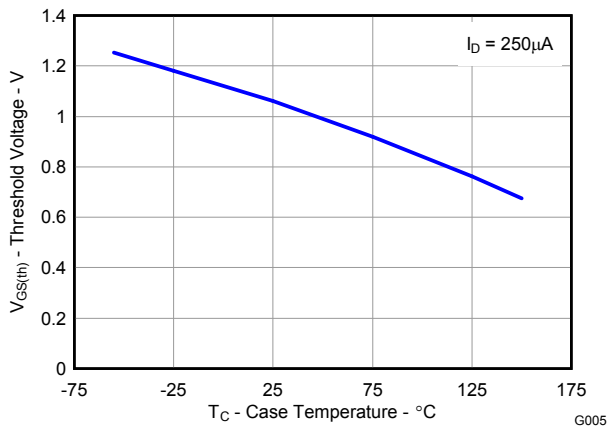
**Figure 3. Transfer Characteristics**



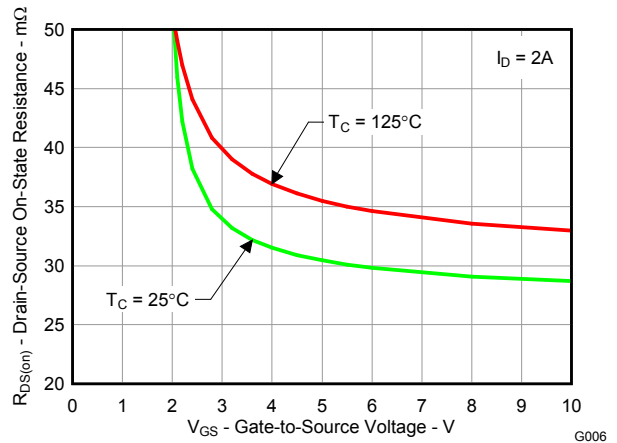
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Threshold Voltage vs. Temperature**



**Figure 7.  $R_{DS(on)}$  vs. Gate-to-Source Voltage**

TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

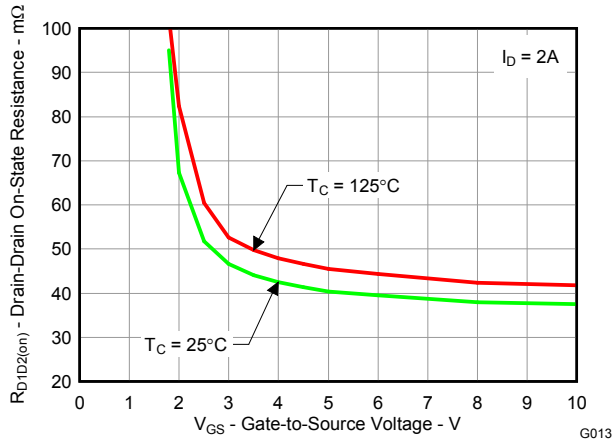


Figure 8.  $R_{D1D2(on)}$  vs. Gate-to-Source Voltage

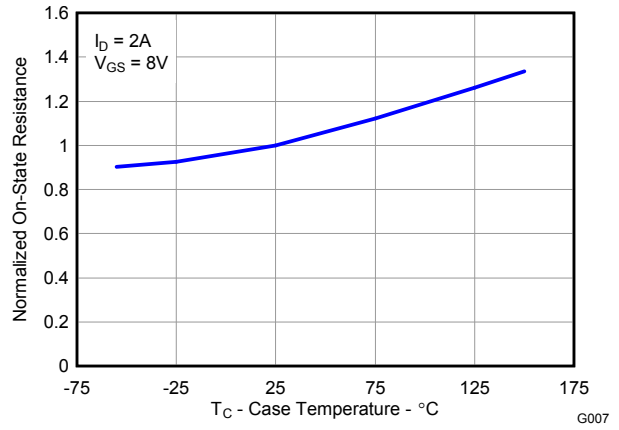


Figure 9. On Resistance vs. Temperature

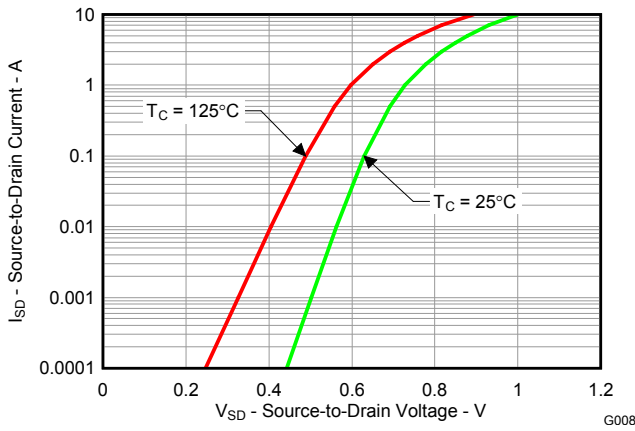


Figure 10. Typical Diode Forward Voltage

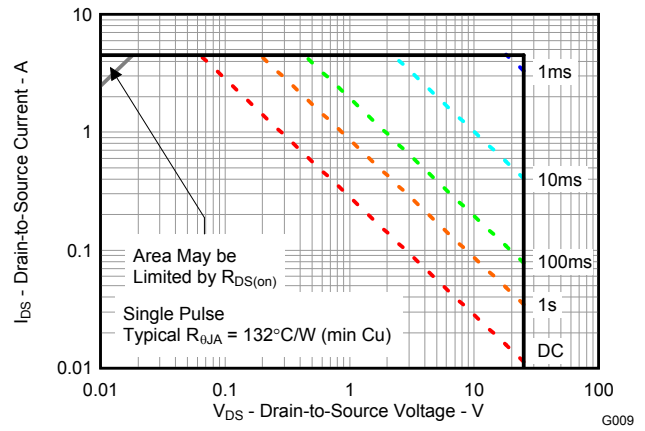


Figure 11. Maximum Safe Operating Area

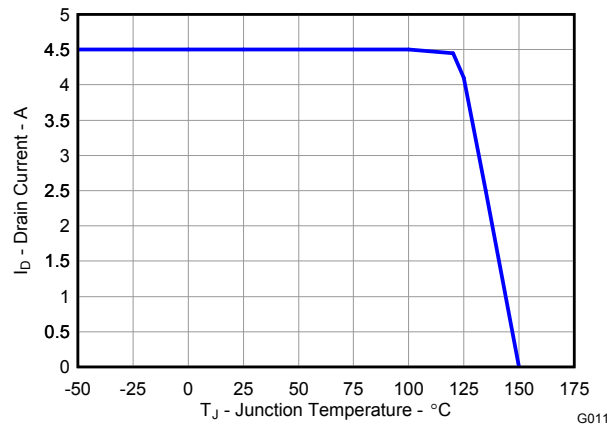
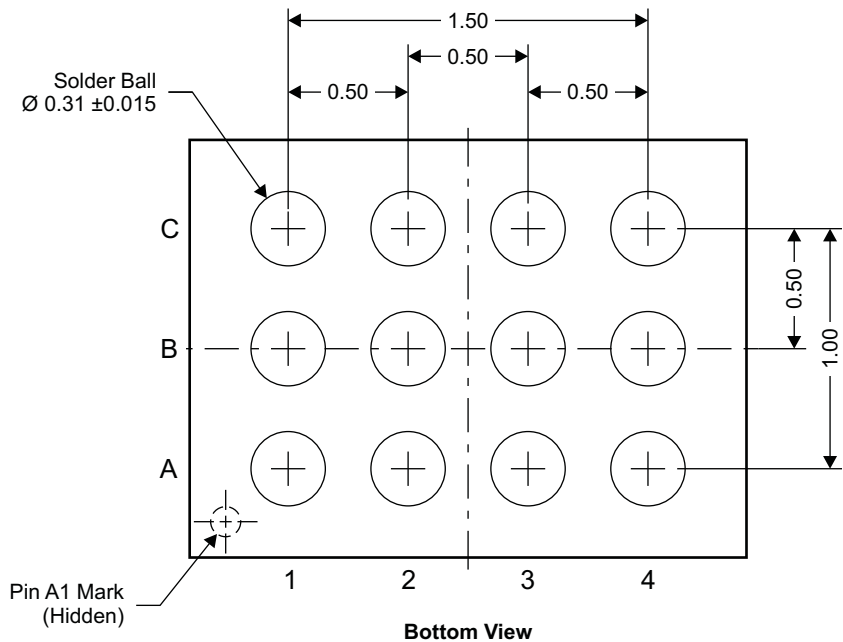
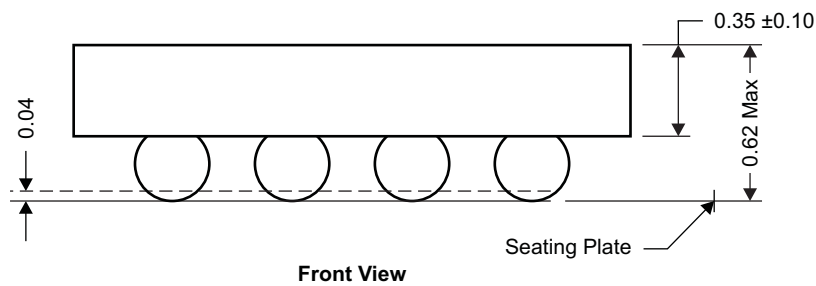
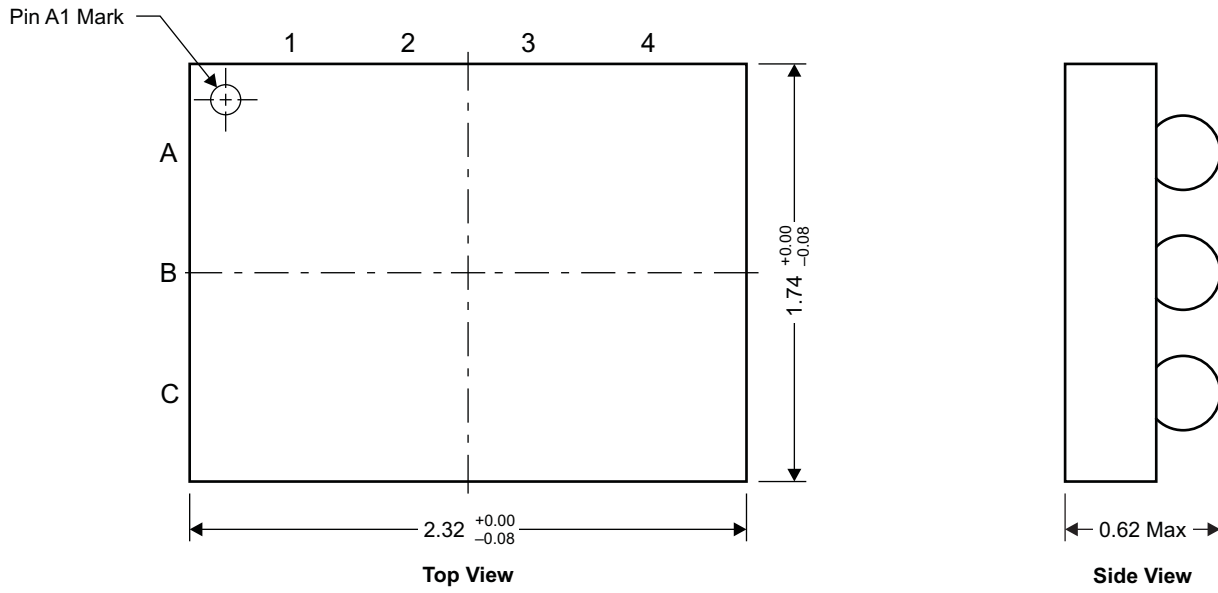


Figure 12. Maximum Drain Current vs. Temperature

**MECHANICAL DATA**

**CSD86311W1723 Package Dimensions**

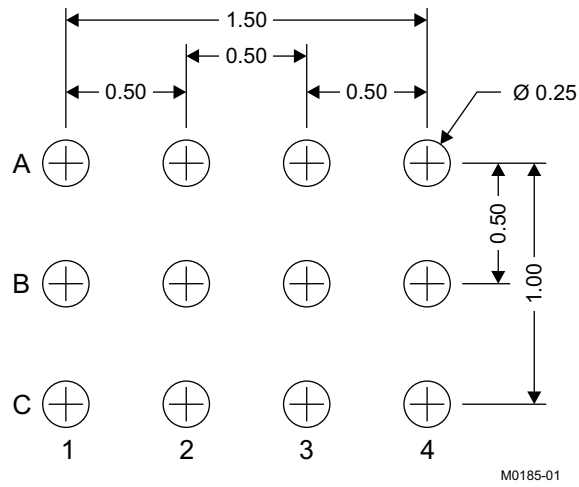


Pinout	
Position	Designation
A2, A3, A4	Drain 1
C2, C3, C4	Drain 2
A1	Gate 1
C1	Gate 2
B1, B2, B3, B4	Source

NOTE: All dimensions are in mm (unless otherwise specified)

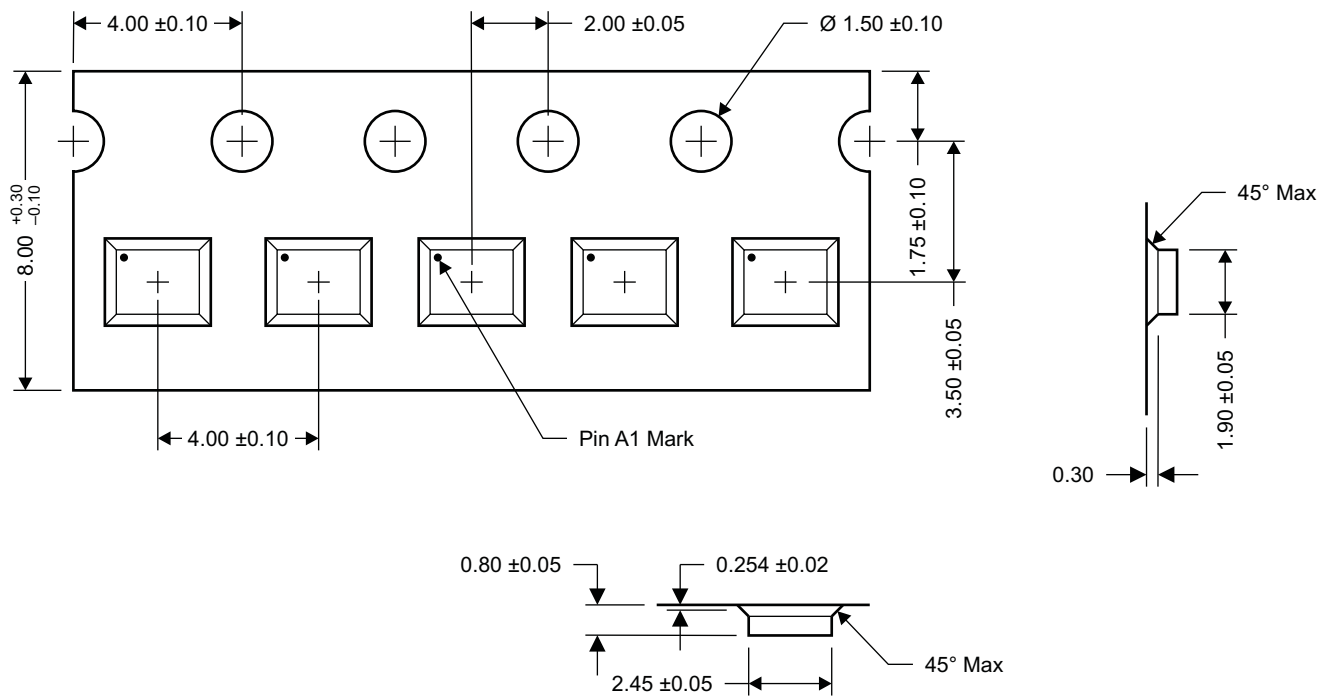
M0184-01

### Land Pattern Recommendation



NOTE: All dimensions are in mm (unless otherwise specified)

### Tape and Reel Information



NOTE: All dimensions are in mm (unless otherwise specified)

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD86311W1723	DSBGA	YZG	12	3000	179.0	14.4	2.45	1.9	0.8	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD86311W1723	DSBGA	YZG	12	3000	199.0	211.0	35.0

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