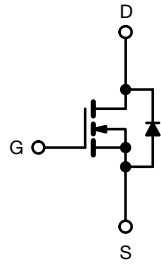
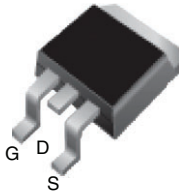




**THE DATASHEET OF  
SIHB24N65EF-GE3**



## E Series Power MOSFET with Fast Body Diode

 D<sup>2</sup>PAK (TO-263)


N-Channel MOSFET

### FEATURES

- Fast body diode MOSFET using E series technology
- Reduced  $t_{rr}$ ,  $Q_{rr}$ , and  $I_{RRM}$
- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Low switching losses due to reduced  $Q_{rr}$
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Telecommunications
  - Server and telecom power supplies
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Consumer and computing
  - ATX power supplies
- Industrial
  - Welding
  - Battery chargers
- Renewable energy
  - Solar (PV inverters)
- Switch mode power supplies (SMPS)
- Applications using the following topologies
  - LCC
  - Phase shifted bridge (ZVS)
  - 3-level inverter
  - AC/DC bridge

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	700	
$R_{DS(on)}$ max. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V	0.156
$Q_g$ max. (nC)	122	
$Q_{gs}$ (nC)	17	
$Q_{gd}$ (nC)	36	
Configuration	Single	

### ORDERING INFORMATION

Package	D <sup>2</sup> PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHB24N65EF-GE3
	SiHB24N65EFT1-GE3
	SiHB24N65EFT5-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)


PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	$V_{DS}$	650	V	
Gate-source voltage	$V_{GS}$	$\pm 30$		
Continuous drain current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	24	A
		$T_C = 100$ °C	15	
Pulsed drain current <sup>a</sup>	$I_{DM}$	65		
Linear derating factor		2	W/°C	
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	691	mJ	
Maximum power dissipation	$P_D$	250	W	
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C	
Drain-source voltage slope	$dV/dt$	$T_J = 125$ °C	70	V/ns
Reverse diode $dV/dt$ <sup>d</sup>		50		
Soldering recommendations (peak temperature) <sup>c</sup>	for 10 s	300	°C	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 7$  A
- 1.6 mm from case
- $I_{SD} \leq I_D$ ,  $dI/dt = 900$  A/ $\mu$ s, starting  $T_J = 25$  °C



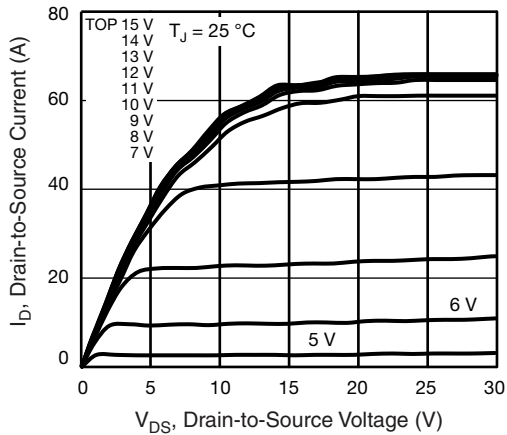
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R <sub>thJA</sub>	-	62	°C/W
Maximum junction-to-case (drain)	R <sub>thJC</sub>	-	0.5	

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)									
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT		
<b>Static</b>									
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		650	-	-	V		
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.68	-	V/°C		
Gate-source threshold voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2	-	4	V		
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA		
		V <sub>GS</sub> = ± 30 V		-	-	± 1	μA		
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 520 V, V <sub>GS</sub> = 0 V		-	-	1	μA		
		V <sub>DS</sub> = 520 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	500			
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 12 A	-	0.13	0.156	Ω		
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 12 A		-	7.2	-	S		
<b>Dynamic</b>									
Input capacitance	C <sub>iSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, f = 1 MHz		-	2774	-	pF		
Output capacitance	C <sub>oss</sub>			-	128	-			
Reverse transfer capacitance	C <sub>rSS</sub>			-	4	-			
Effective output capacitance, energy related <sup>a</sup>	C <sub>o(er)</sub>			V <sub>DS</sub> = 0 V to 520 V, V <sub>GS</sub> = 0 V		-		96	-
Effective output capacitance, time related <sup>b</sup>	C <sub>o(tr)</sub>			V <sub>DS</sub> = 0 V to 520 V, V <sub>GS</sub> = 0 V		-		333	-
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 12 A, V <sub>DS</sub> = 520 V	-	81	122	nC		
Gate-source charge	Q <sub>gs</sub>			-	17	-			
Gate-drain charge	Q <sub>gd</sub>			-	36	-			
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 520 V, I <sub>D</sub> = 12 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 9.1 Ω		-	24	48	ns		
Rise time	t <sub>r</sub>			-	34	68			
Turn-off delay time	t <sub>d(off)</sub>			-	80	120			
Fall time	t <sub>f</sub>			-	46	92			
Gate input resistance	R <sub>g</sub>			f = 1 MHz, open drain		0.2		0.5	1.0
<b>Drain-Source Body Diode Characteristics</b>									
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	24	A		
Pulsed diode forward current	I <sub>SM</sub>			-	-	65			
Diode forward voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 12 A, V <sub>GS</sub> = 0 V		-	0.9	1.2	V		
Reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 12 A, di/dt = 100 A/μs, V <sub>R</sub> = 400 V		-	151	288	ns		
Reverse recovery charge	Q <sub>rr</sub>			-	0.9	2.1	μC		
Reverse recovery current	I <sub>RRM</sub>			-	13	-	A		

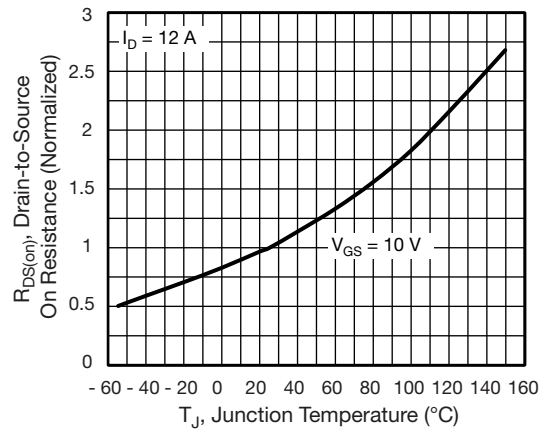
**Notes**

- a. C<sub>oss(er)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DSS</sub>
- b. C<sub>oss(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DSS</sub>

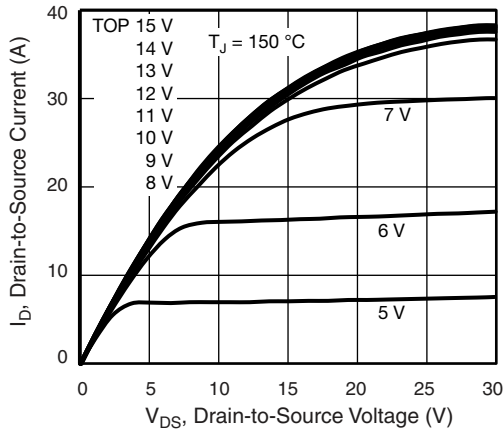
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



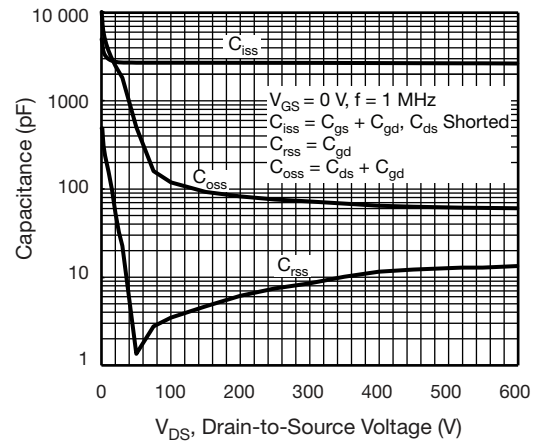
**Fig. 1 - Typical Output Characteristics**



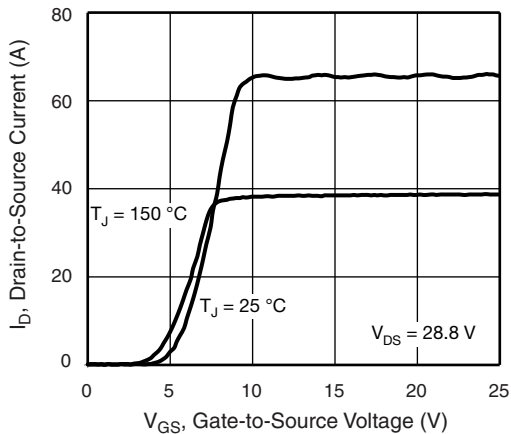
**Fig. 4 - Normalized On-Resistance vs. Temperature**



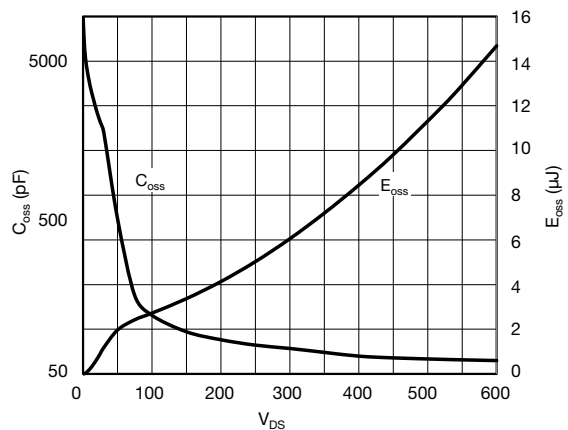
**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 - C<sub>oss</sub> and E<sub>oss</sub> vs. V<sub>DS</sub>**

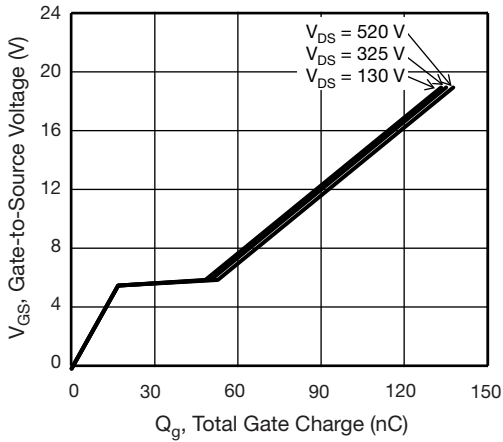


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

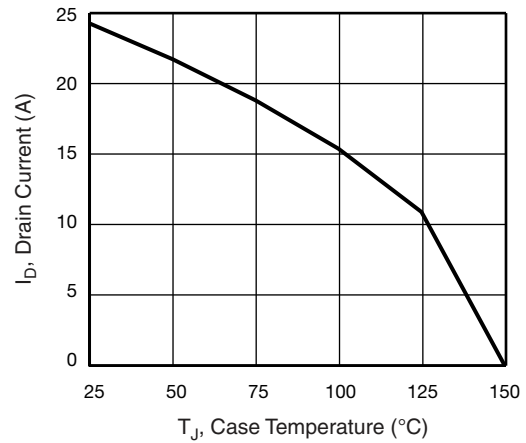


Fig. 10 - Maximum Drain Current vs. Case Temperature

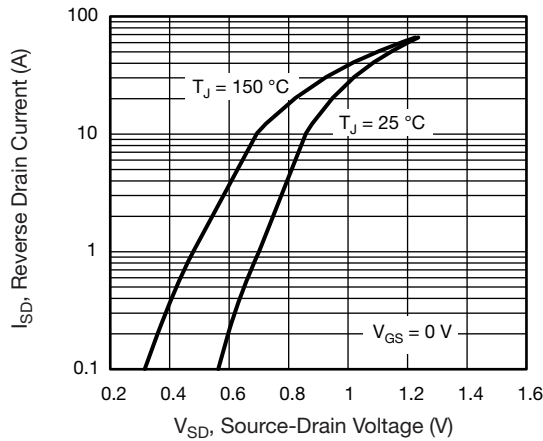


Fig. 8 - Typical Source-Drain Diode Forward Voltage

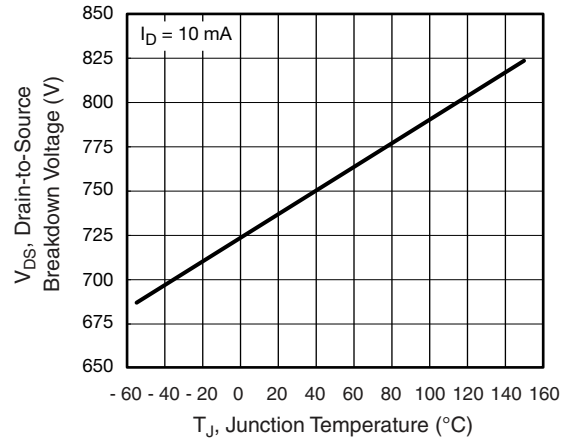


Fig. 11 - Temperature vs. Drain-to-Source Voltage

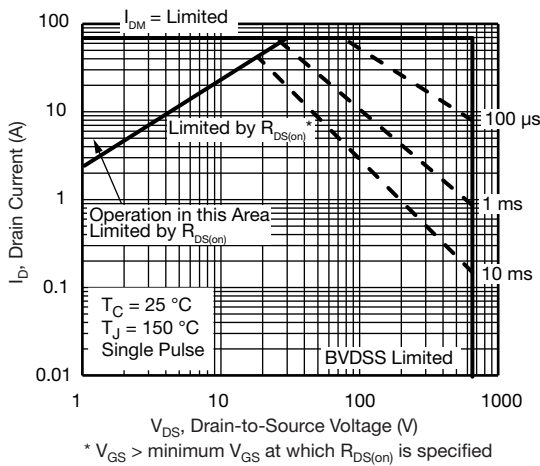


Fig. 9 - Maximum Safe Operating Area

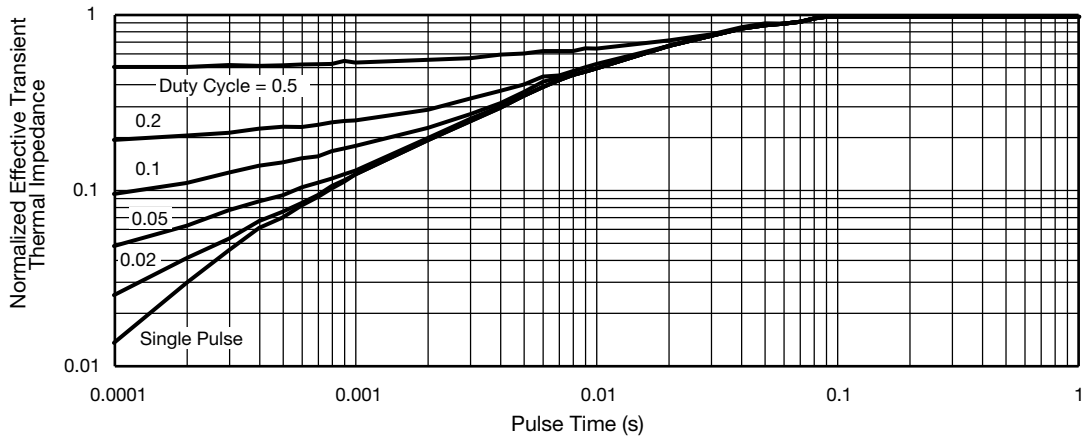


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

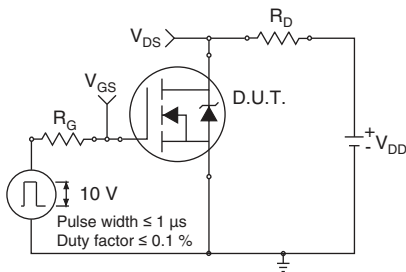


Fig. 13 - Switching Time Test Circuit

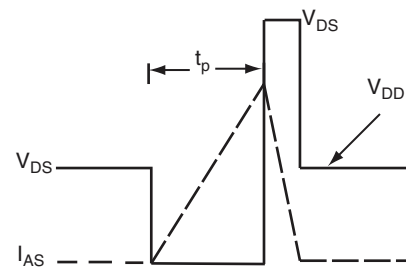


Fig. 16 - Unclamped Inductive Waveforms

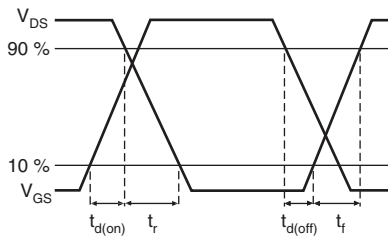


Fig. 14 - Switching Time Waveforms

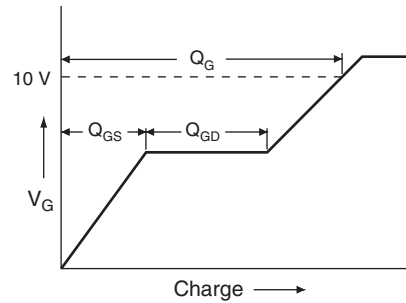


Fig. 17 - Basic Gate Charge Waveform

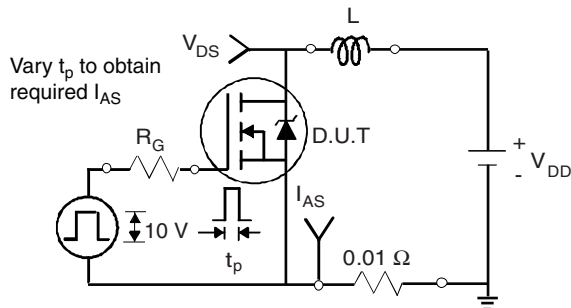


Fig. 15 - Unclamped Inductive Test Circuit

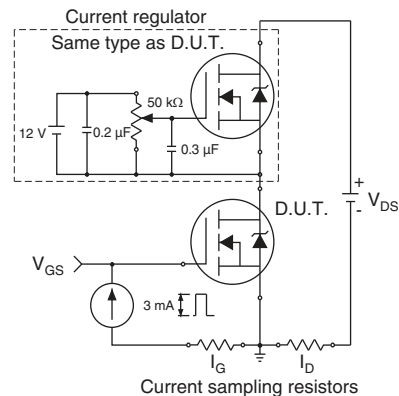
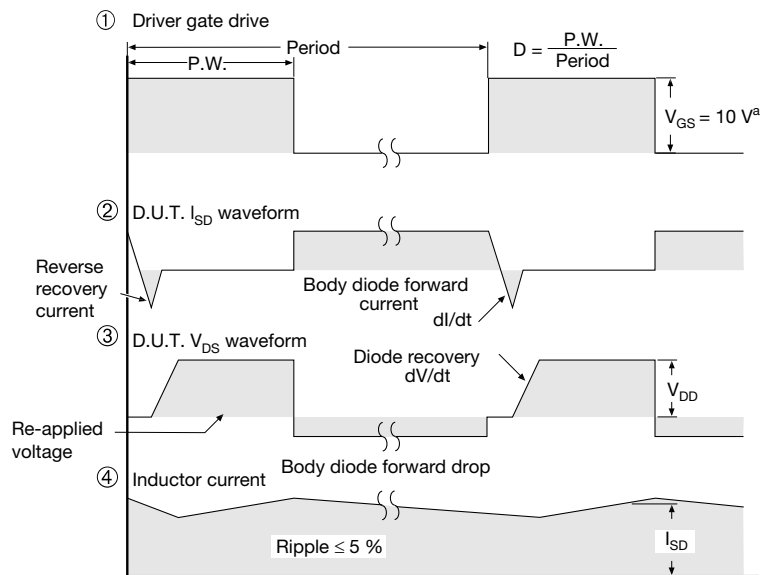
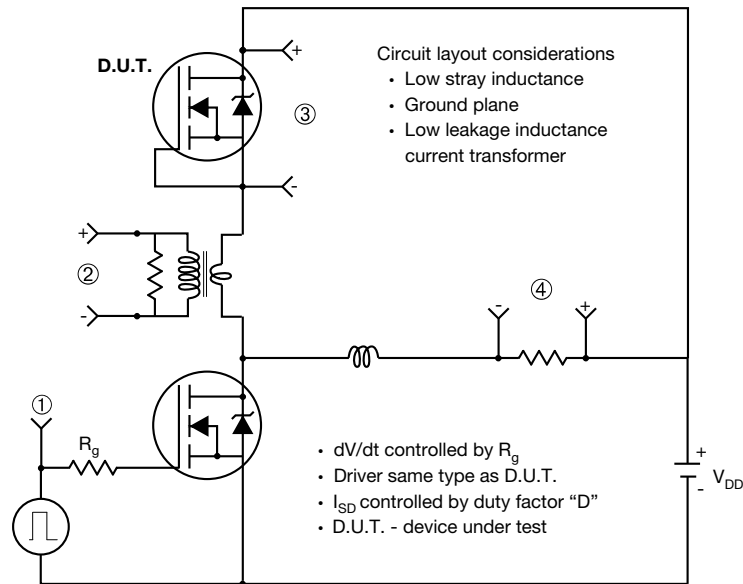


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a.  $V_{GS} = 5 V$  for logic level devices

Fig. 19 - For N-Channel

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