



**THE DATASHEET OF
SQD40N10-25-T4_GE3**



Automotive N-Channel 100 V (D-S) 175 °C MOSFET

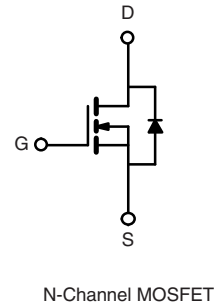
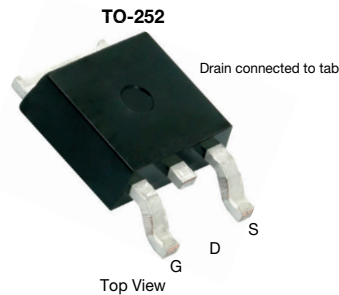
 AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY	
V_{DS} (V)	100
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.025
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.029
I_D (A)	40
Configuration	Single
Package	TO-252

FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- 100 % R_g and UIS tested
- AEC-Q101 qualified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	$T_C = 25$ °C ^a	40
		$T_C = 125$ °C	26
Continuous Source Current (Diode Conduction) ^a	I_S	40	A
Pulsed Drain Current ^b	I_{DM}	160	
Single Pulse Avalanche Current	I_{AS}	L = 0.1 mH	40
Single Pulse Avalanche Energy			E_{AS}
Maximum Power Dissipation ^b	P_D	$T_C = 25$ °C	136
		$T_C = 125$ °C	45
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	50	°C/W
Junction-to-Case (Drain)			

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).



SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		100	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		1.5	-	2.5	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 100\text{ V}$	-	-	1.0	μA
		$V_{GS} = 0\text{ V}$	$V_{DS} = 100\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 100\text{ V}$, $T_J = 175\text{ }^\circ\text{C}$	-	-	250	
On-State Drain Current ^a	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	50	-	-	A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 40\text{ A}$	-	0.019	0.025	Ω
		$V_{GS} = 10\text{ V}$	$I_D = 40\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$	-	-	0.050	
		$V_{GS} = 10\text{ V}$	$I_D = 40\text{ A}$, $T_J = 175\text{ }^\circ\text{C}$	-	-	0.063	
		$V_{GS} = 4.5\text{ V}$	$I_D = 20\text{ A}$	-	0.021	0.029	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 40\text{ A}$		-	73	-	S
Dynamic ^b							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$	-	2703	3380	pF
Output Capacitance	C_{oss}			-	312	390	
Reverse Transfer Capacitance	C_{rss}			-	127	160	
Total Gate Charge ^c	Q_g	$V_{GS} = 10\text{ V}$	$V_{DS} = 50\text{ V}$, $I_D = 40\text{ A}$	-	46	70	nC
Gate-Source Charge ^c	Q_{gs}			-	8.2	-	
Gate-Drain Charge ^c	Q_{gd}			-	13	-	
Gate Resistance	R_g	$f = 1\text{ MHz}$		0.9	1.8	3.1	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 50\text{ V}$, $R_L = 1.25\text{ }\Omega$ $I_D \cong 40\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$		-	11	17	ns
Rise Time ^c	t_r			-	11	17	
Turn-Off Delay Time ^c	$t_{d(off)}$			-	27	41	
Fall Time ^c	t_f			-	6	9	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I_{SM}			-	-	160	A
Forward Voltage	V_{SD}	$I_F = 40\text{ A}$, $V_{GS} = 0\text{ V}$		-	0.9	1.5	V

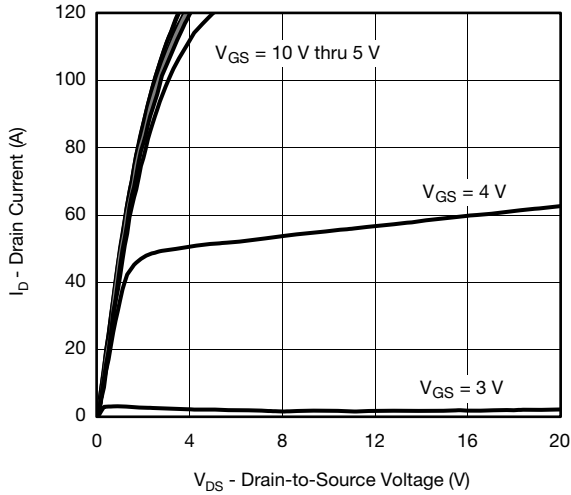
Notes

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

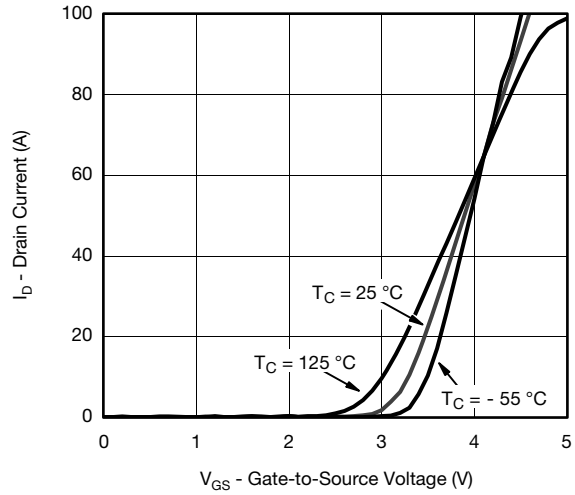
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



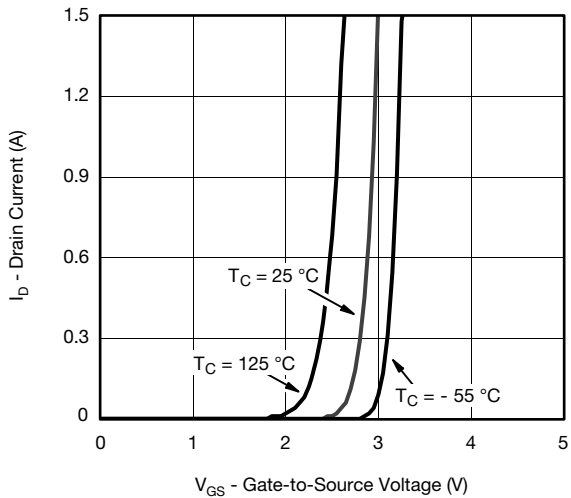
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



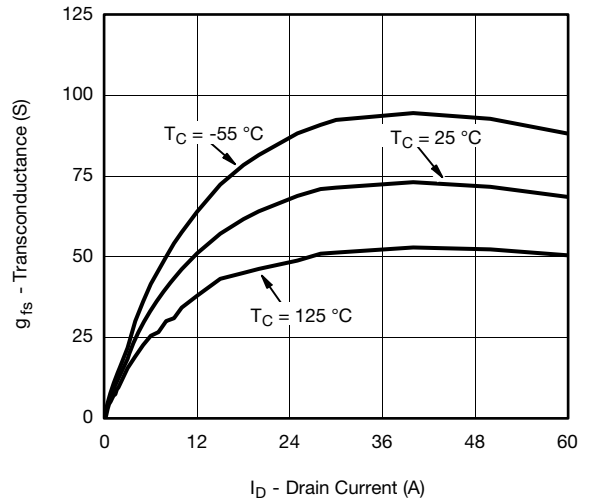
Output Characteristics



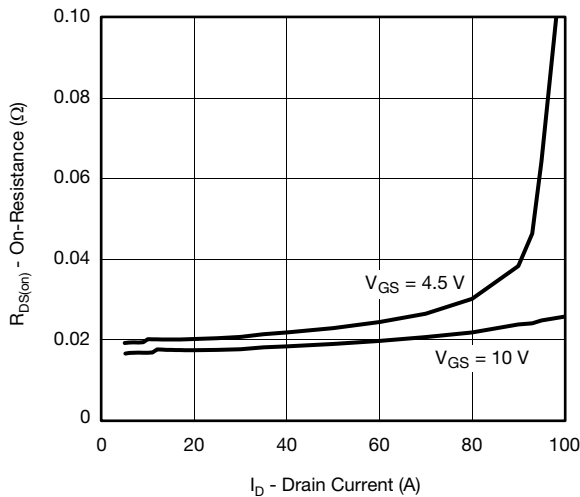
Transfer Characteristics



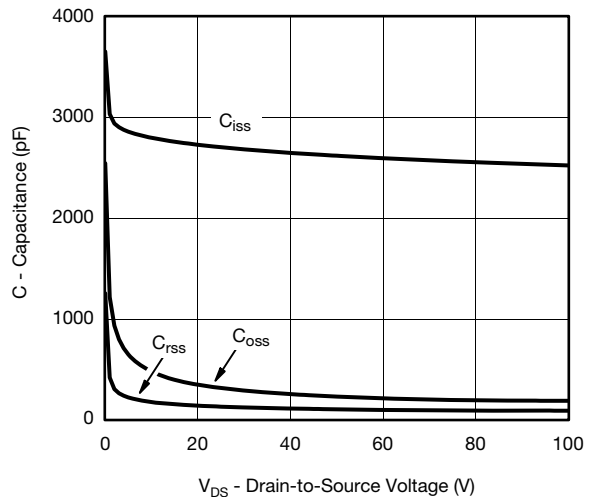
Transfer Characteristics



Transconductance



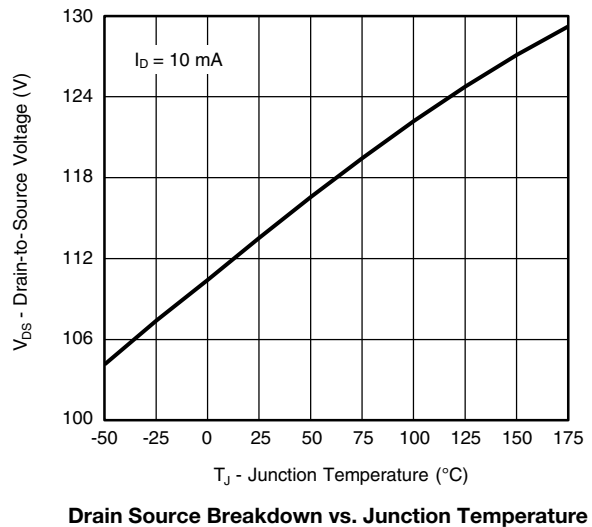
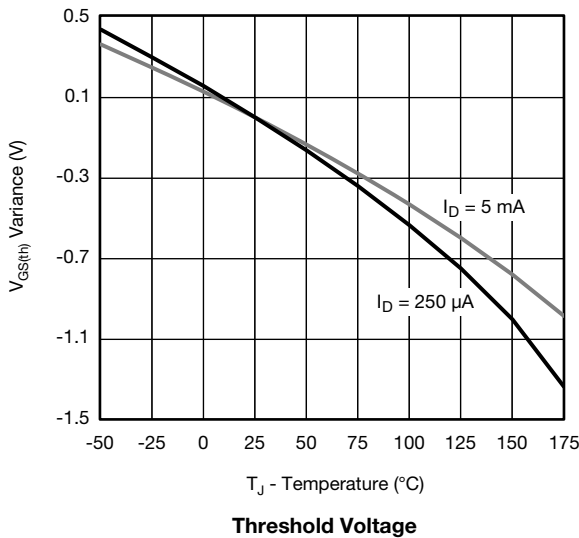
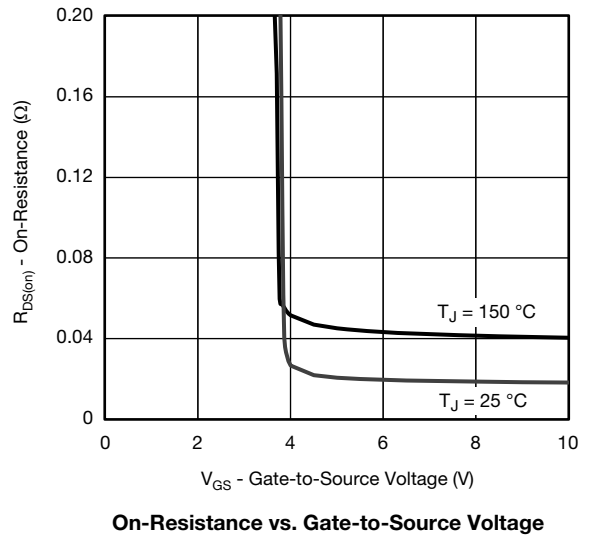
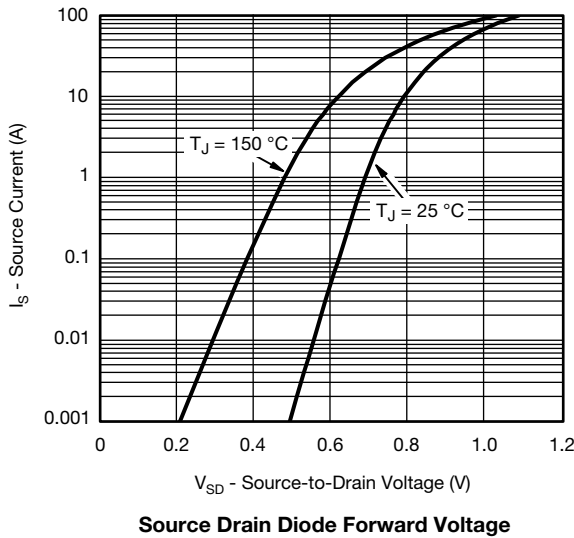
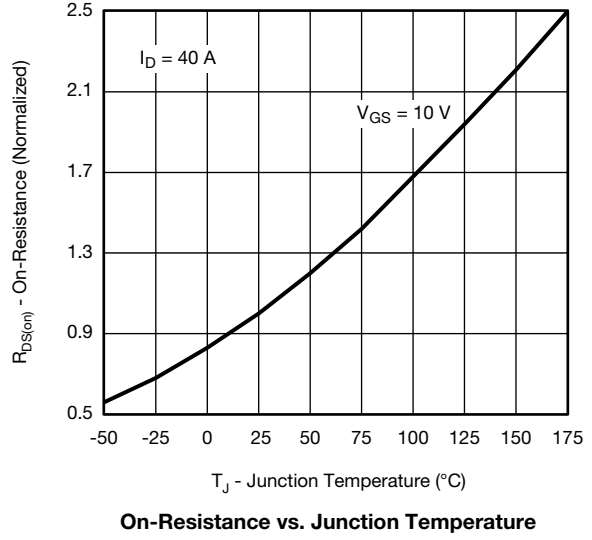
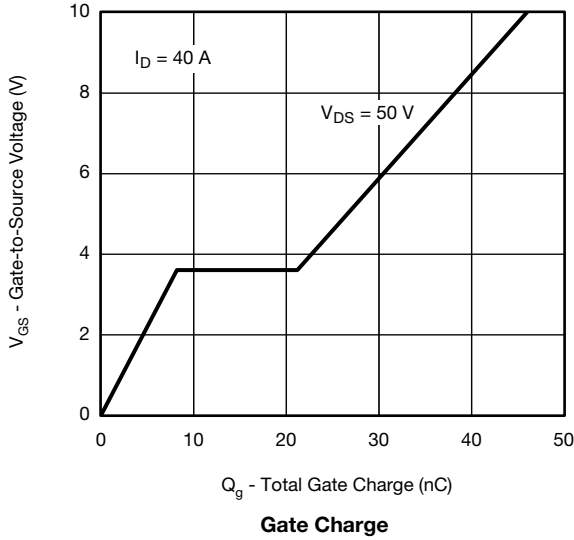
On-Resistance vs. Drain Current



Capacitance

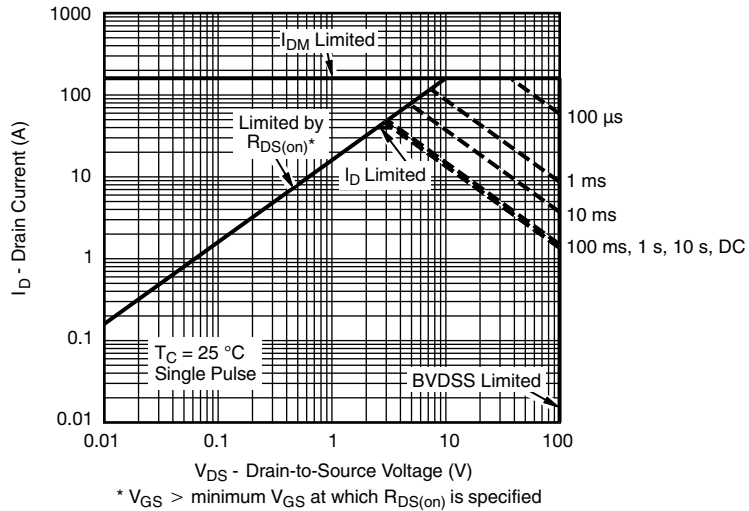


TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

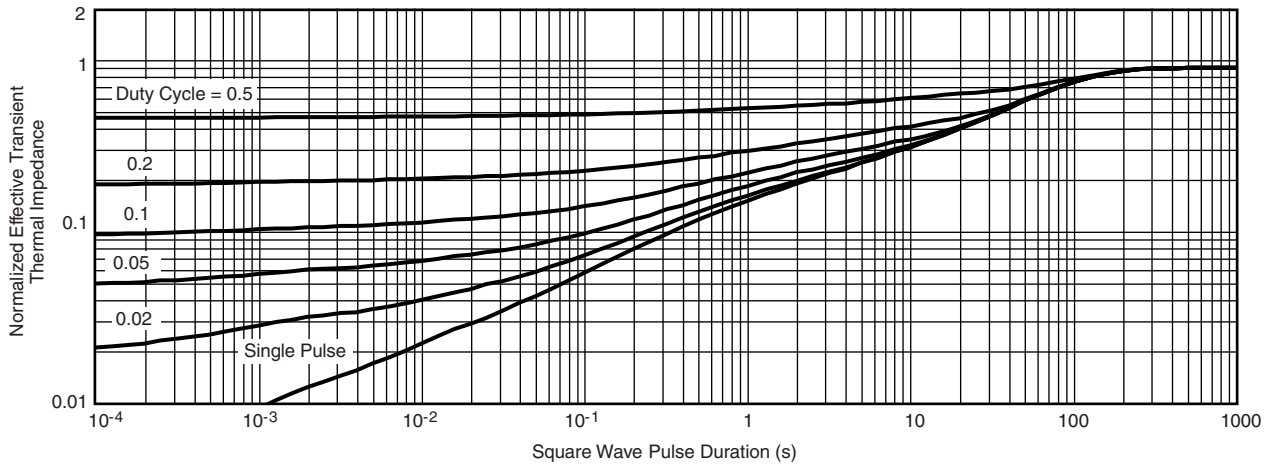




THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



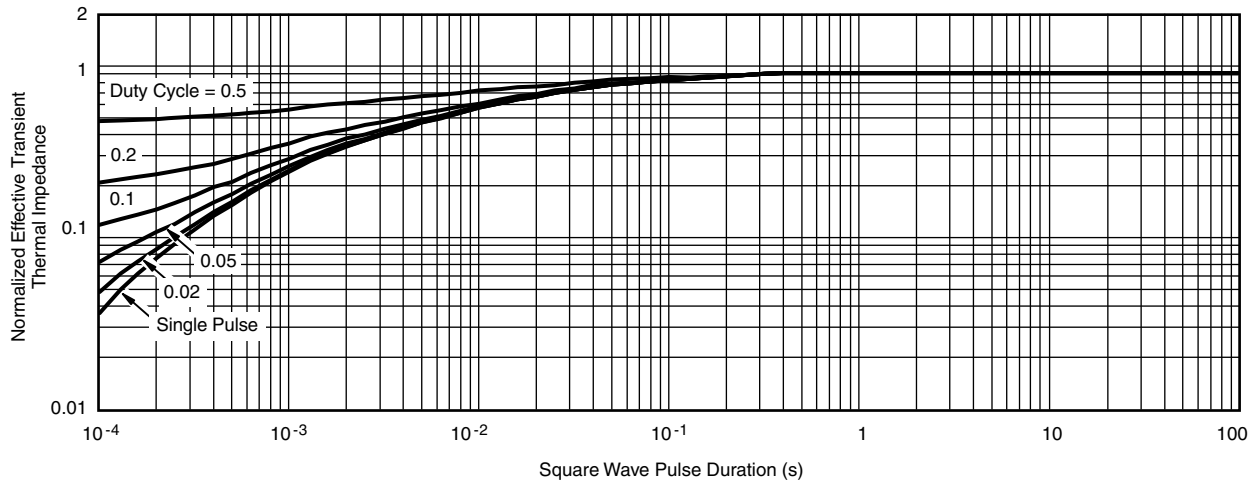
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction to Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction to Case (25 °C)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69064.



REVISION HISTORY ^a		
REVISION	DATE	DESCRIPTION OF CHANGE
E	04-Aug-15	• Revised R _g minimum limit

Note

a. As of April 2014



TO-252AA Case Outline



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T13-0592-Rev. A, 02-Sep-13 DWG: 6019				

Note

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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