

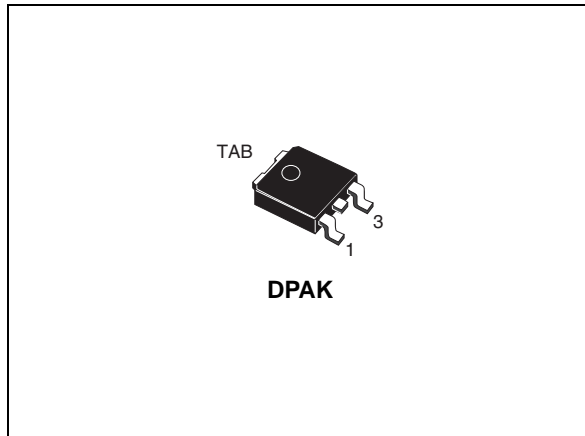
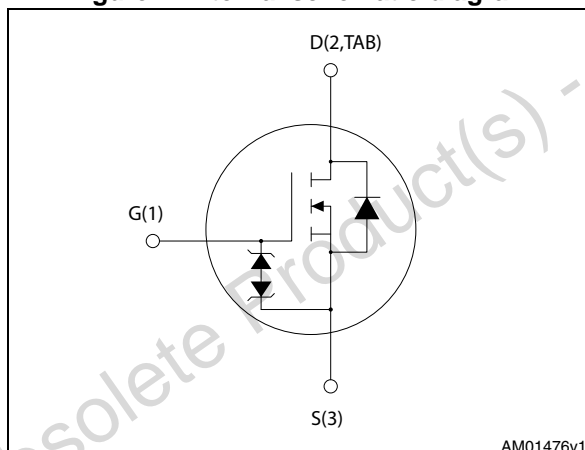


THE DATASHEET OF STDLED625H



N-channel 620 V, 1.7 Ω , 4.5 A Power MOSFET in a DPAK package

Datasheet – preliminary data


Figure 1. Internal schematic diagram


Features

Order code	V_{DS}	$R_{DS(on)max}$	I_D	P_{TOT}
STDLED625H	620 V	2 Ω	4.5 A	70 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- LED lighting applications

Description

These Power MOSFETs boast extremely low on-resistance and very good dv/dt capability, rendering them suitable for buck-boost and flyback topologies.

Table 1. Device summary

Order code	Marking	Package	Packaging
STDLED625H	LED625H	DPAK	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
2.1	Electrical characteristics (curves)	6
3	Test circuits	9
4	Package mechanical data	10
5	Packaging mechanical data	14
6	Revision history	16

Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	620	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	4.5	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	2.3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	18.0	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	3.8	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{V}$)	115	mJ
$V_{ESD(G-S)}$	Gate source ESD(HBM-C = 100 pF, R = 1.5 k Ω)	2500	V
dv/dt ⁽²⁾	Peak diode recovery voltage slope	12	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; $T_C = 25\text{ }^\circ\text{C}$)		V
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 3.8\text{ A}$, $di/dt = 400\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$, $V_{DS\text{ peak}} \leq V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.79	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	50	$^\circ\text{C}/\text{W}$

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	620			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 620\text{V}$			1	μA
		$V_{GS} = 0, V_{DS} = 620\text{V}, T_C = 125\text{ °C}$			50	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 50\text{ }\mu\text{A}$	3	3.6	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 1.9\text{ A}$		1.7	2	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	560 43 7.5	-	pF pF pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }496\text{ V}, V_{GS} = 0$	-	27	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	2	5	10	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 496\text{ V}, I_D = 3.8\text{ A}, V_{GS} = 10\text{ V}$ (see Figure 16)	-	23 4 13	-	nC nC nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	$V_{DD} = 300\text{ V}, I_D = 1.9\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 15)	-	10 9 29 19	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		3.8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		15.2	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 3.8 \text{ A}, V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 3.8 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 20)	-	220		ns
Q_{rr}	Reverse recovery charge			1.4		μC
I_{RRM}	Reverse recovery current			13		A
t_{rr}	Reverse recovery time	$I_{SD} = 3.8 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see Figure 20)	-	270		ns
Q_{rr}	Reverse recovery charge			1.9		μC
I_{RRM}	Reverse recovery current			14		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}, I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

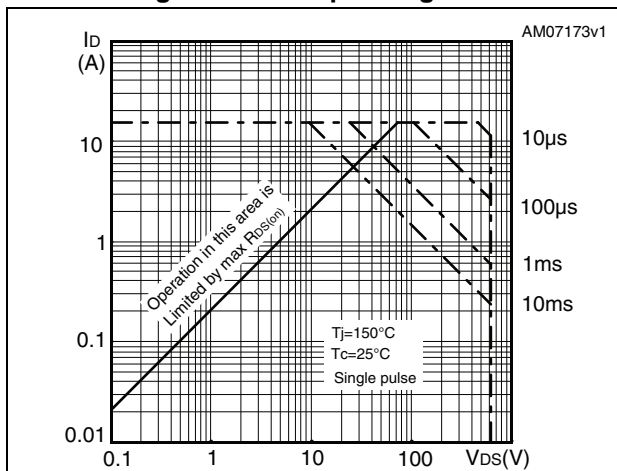


Figure 3. Thermal impedance

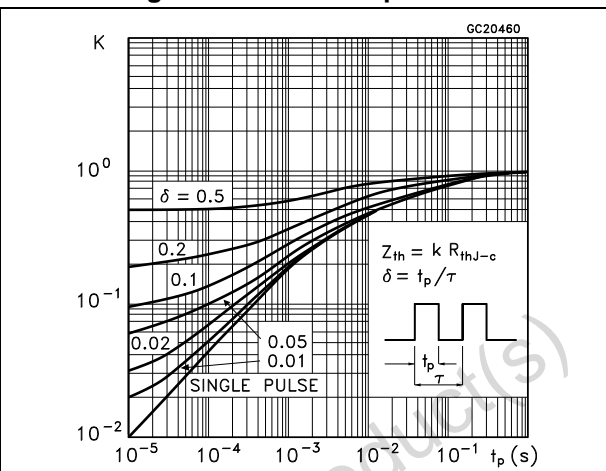


Figure 4. Output characteristics

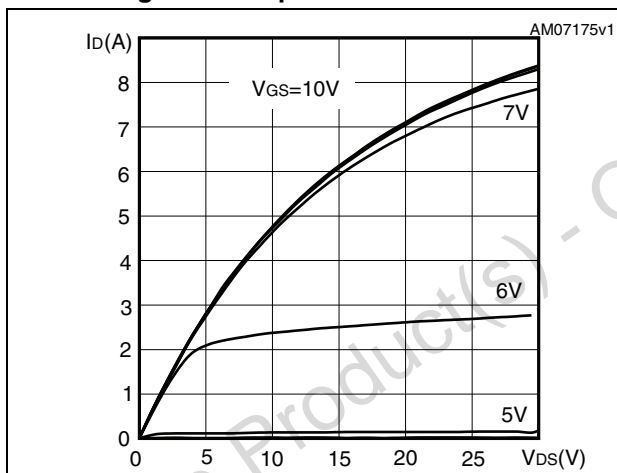


Figure 5. Transfer characteristics

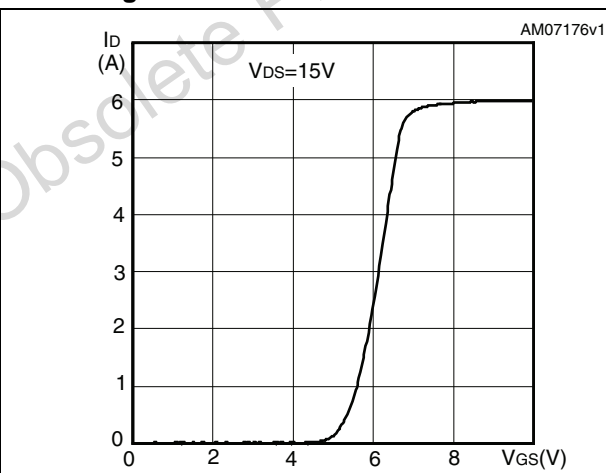


Figure 6. Gate charge vs gate-source voltage

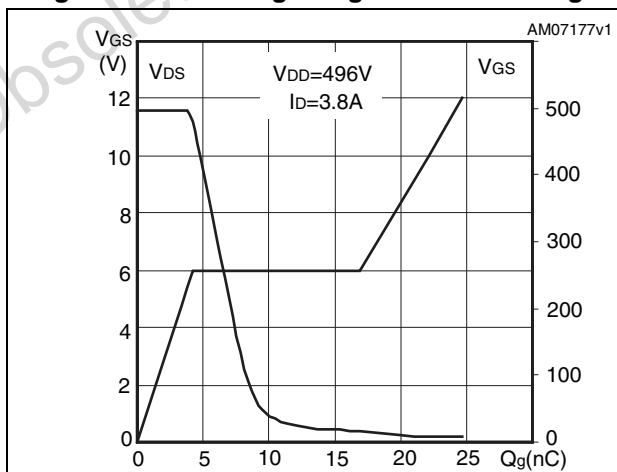


Figure 7. Static drain-source on-resistance

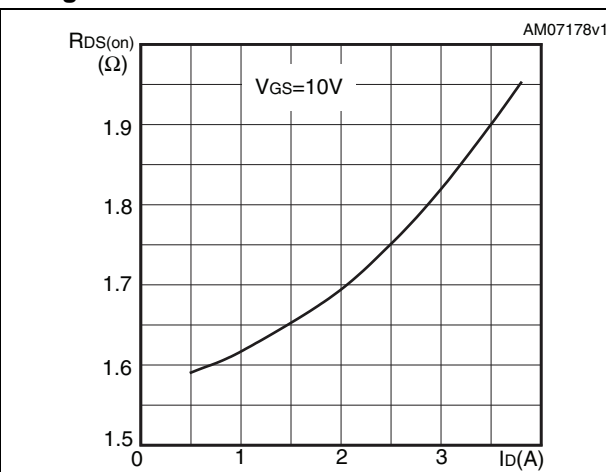


Figure 8. Capacitance variations

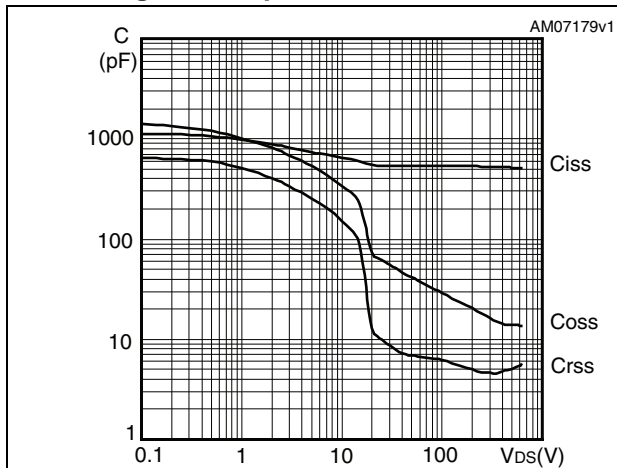


Figure 9. Output capacitance stored energy

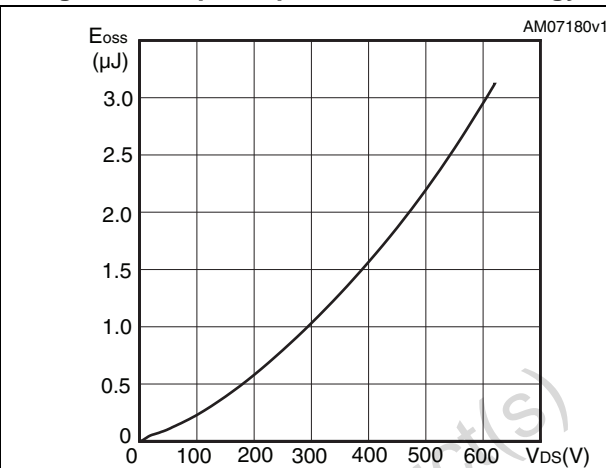


Figure 10. Normalized gate threshold voltage vs temperature

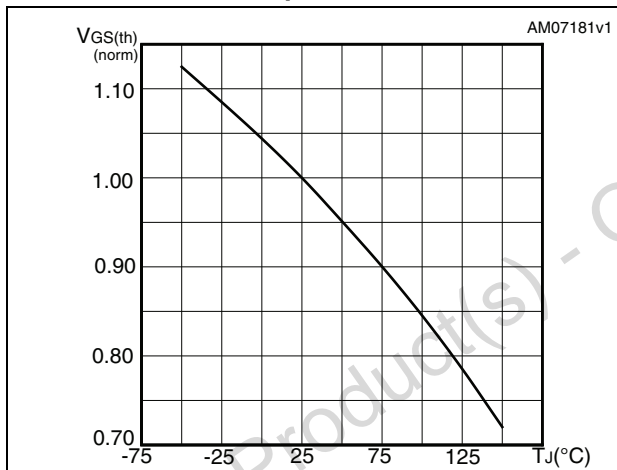


Figure 11. Normalized on-resistance vs temperature

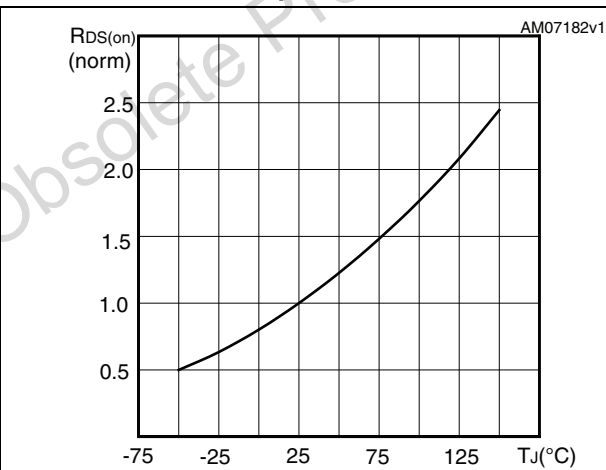


Figure 12. Maximum avalanche energy vs starting Tj

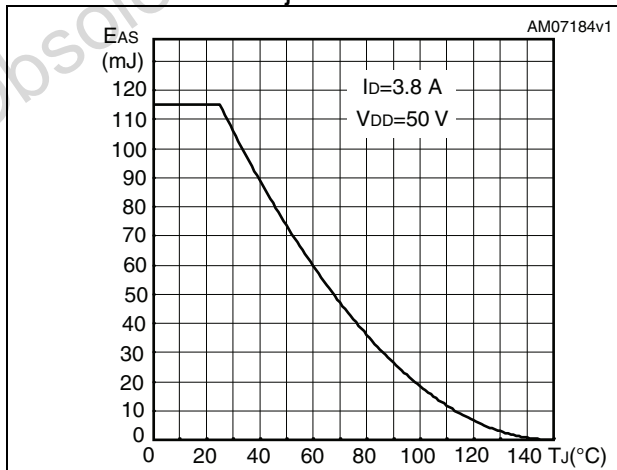


Figure 13. Normalized B_{VDS} vs temperature

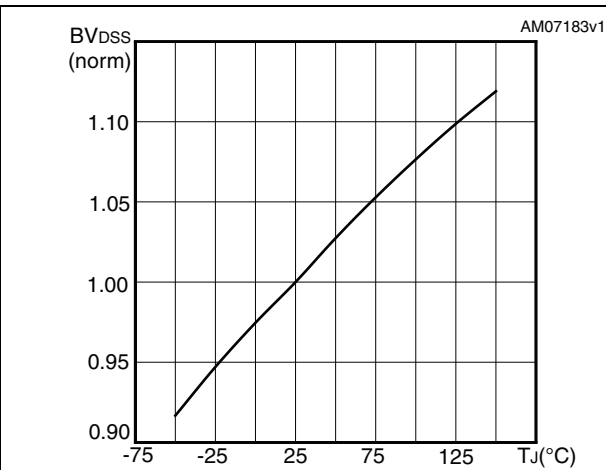
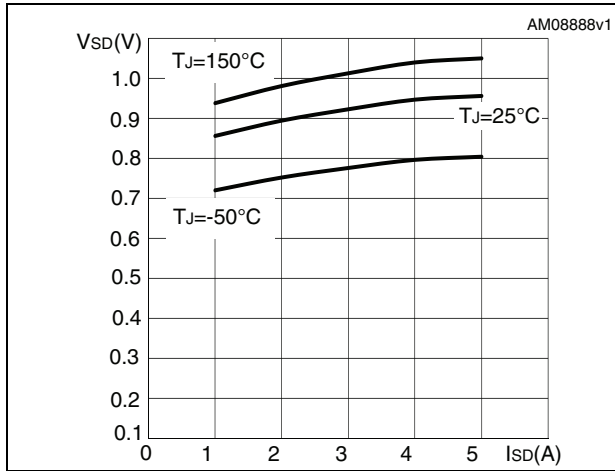


Figure 14. Source-drain diode forward characteristics



Obsolete Product(s) - Obsolete Product(s)

3 Test circuits

Figure 15. Switching times test circuit for resistive load

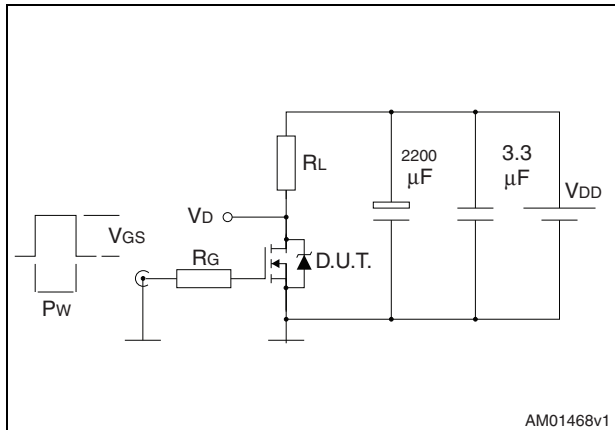


Figure 16. Gate charge test circuit

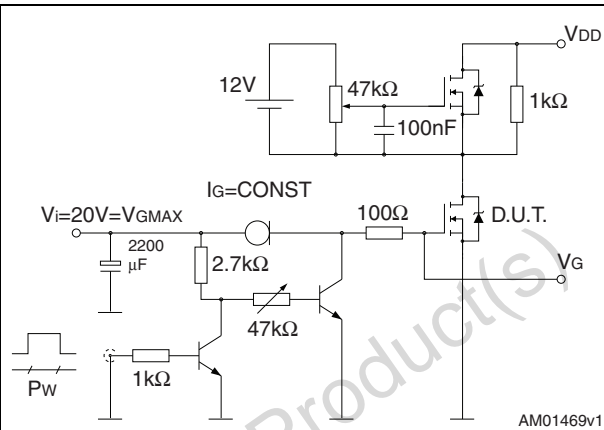


Figure 17. Test circuit for inductive load switching and diode recovery times

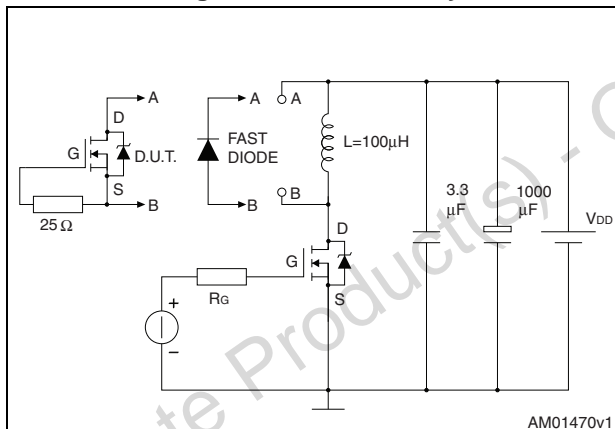


Figure 18. Unclamped Inductive load test circuit

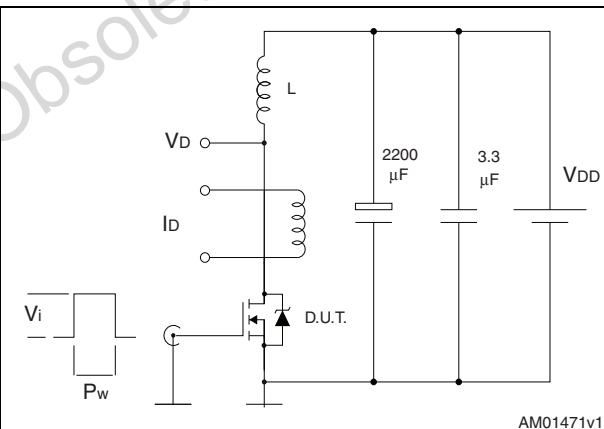


Figure 19. Unclamped inductive waveform

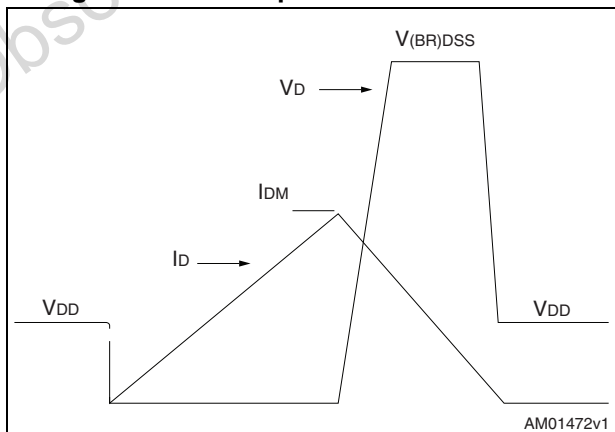
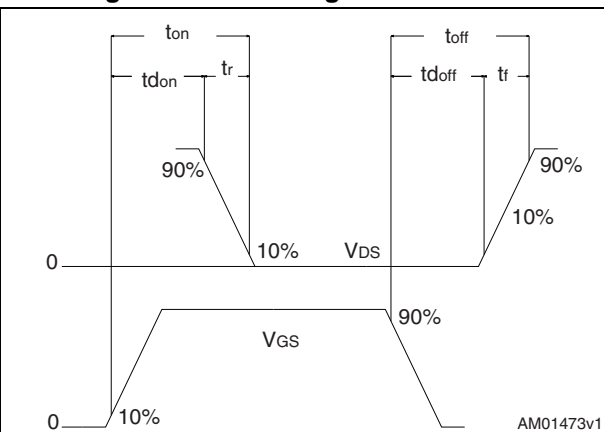


Figure 20. Switching time waveform



4 Package mechanical data

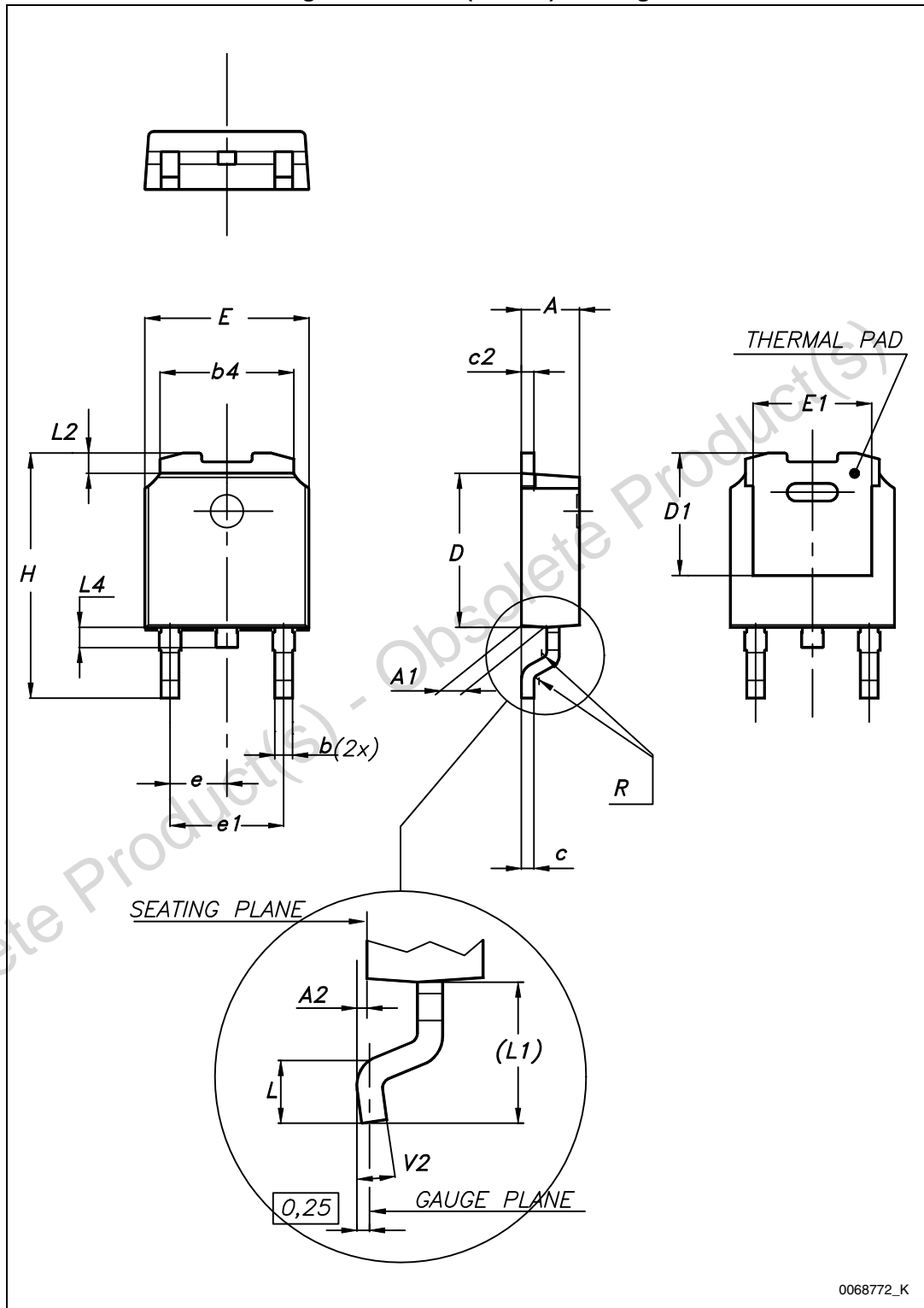
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Obsolete Product(s) - Obsolete Product(s)

Table 9. DPAK (TO-252) mechanical data

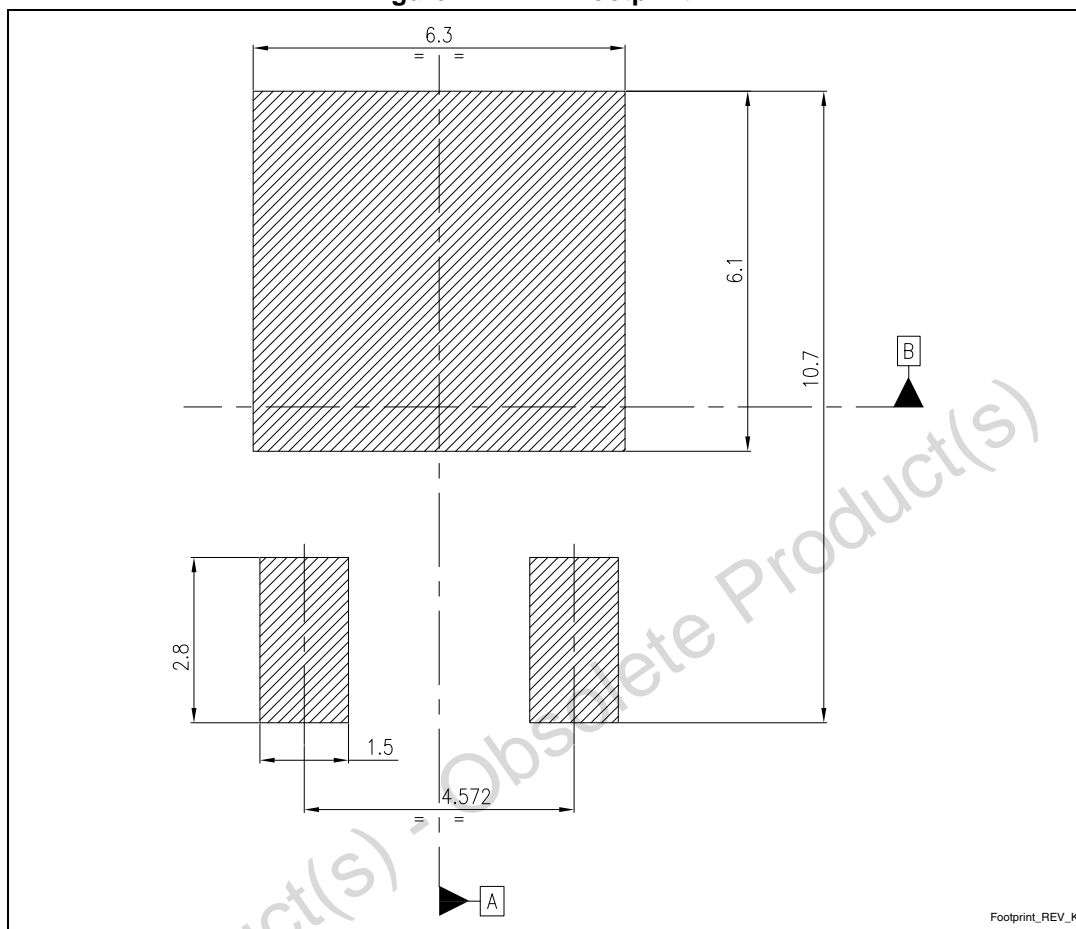
Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 21. DPAK (TO-252) drawing



0068772_K

Figure 22. DPAK footprint (a)



a. All dimensions are in millimeters

5 Packaging mechanical data

Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 23. Tape for DPAK (TO-252)

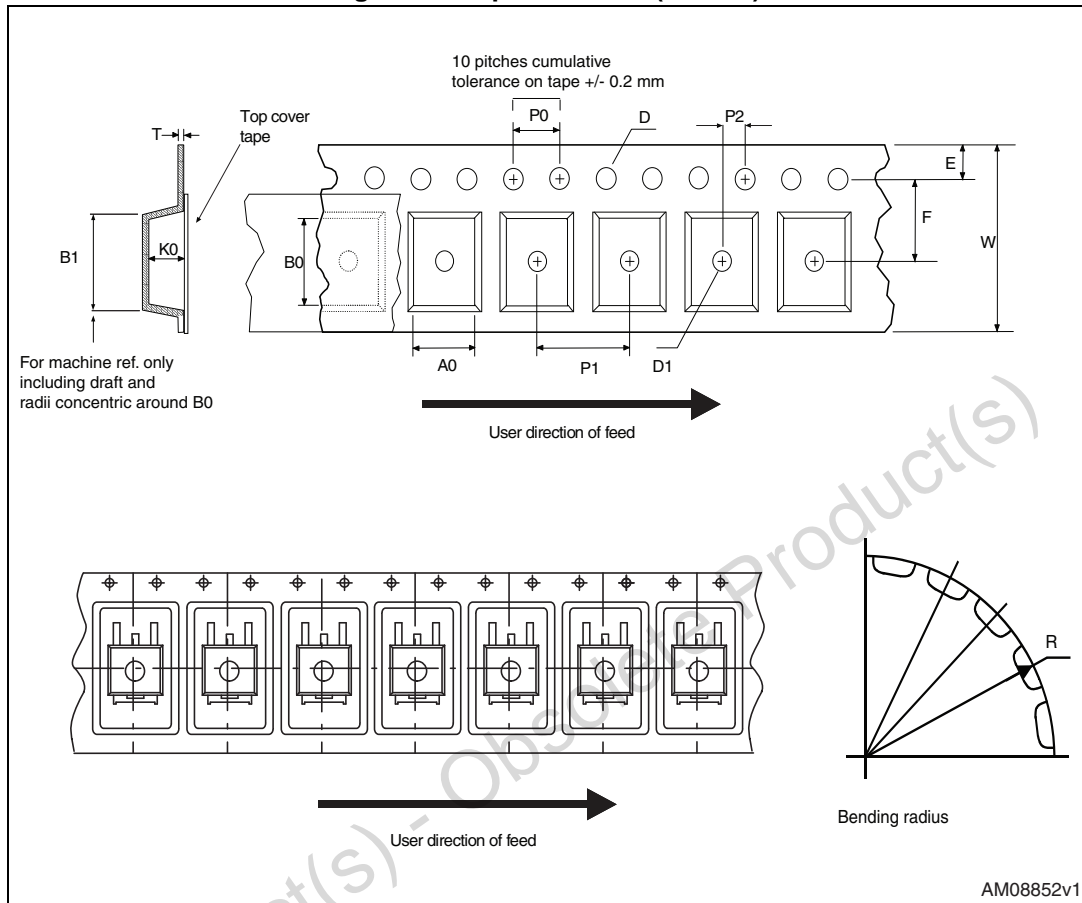
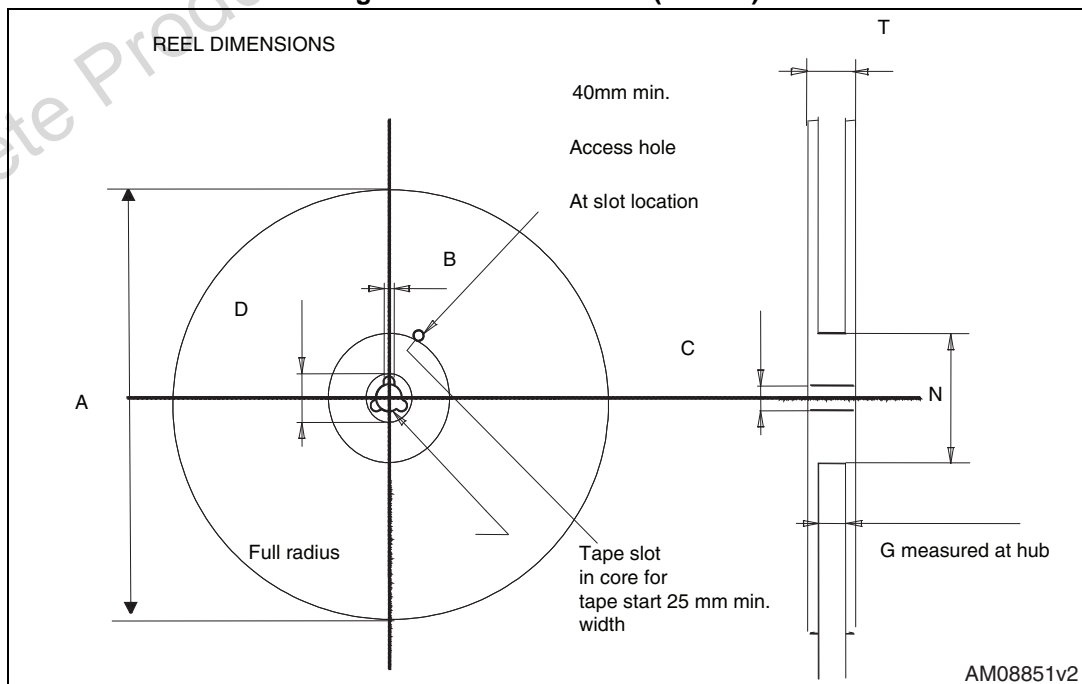


Figure 24. Reel for DPAK (TO-252)



6 Revision history

Table 11. Document revision history

Date	Revision	Changes
22-Mar-2013	1	First release.

Obsolete Product(s) - Obsolete Product(s)

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT AUTHORIZED FOR USE IN WEAPONS. NOR ARE ST PRODUCTS DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies



Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com



Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View STDLED625H on WIN SOURCE](#)
-  [STMicroelectronics Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management