



**THE DATASHEET OF
STD5407NNT4G**



NTD5407N, STD5407N, NVD5407N

MOSFET – Power, Single, N-Channel, DPAK 40 V, 38 A



ON Semiconductor®

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Features

- Low $R_{DS(on)}$
- High Current Capability
- Low Gate Charge
- STD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable*
- These Devices are Pb-Free and are RoHS Compliant

Applications

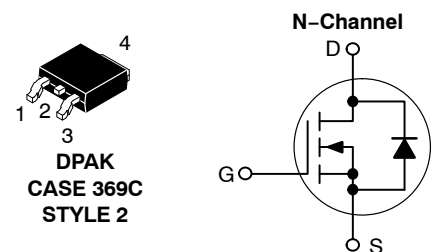
- Electronic Brake Systems
- Electronic Power Steering
- Bridge Circuits

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

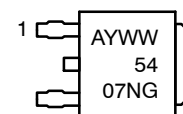
Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DSS}	40	V	
Gate-to-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Current – $R_{\theta JC}$	Steady State	$T_C = 25^\circ\text{C}$	I_D	38	A
			$T_C = 100^\circ\text{C}$	27	
Power Dissipation – $R_{\theta JC}$	Steady State	$T_C = 25^\circ\text{C}$	P_D	75	W
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	7.6	A
		$T_A = 100^\circ\text{C}$		5.3	
Power Dissipation – $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D	2.9	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$		I_{DM}	75	A
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to 175		$^\circ\text{C}$
Source Current (Body Diode)		I_S	36		A
Single Pulse Drain-to-Source Avalanche Energy – ($V_{DD} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{PK} = 17 \text{ A}, L = 1 \text{ mH}, R_G = 25 \Omega$)		EAS	150		mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	I_D MAX (Note 1)
40 V	21 m Ω @ 10 V	38 A



MARKING DIAGRAM



A = Assembly Location*
 Y = Year
 WW = Work Week
 5407N = Specific Device Code
 G = Pb-Free Device

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

Device	Package	Shipping†
NTD5407NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
STD5407NT4G*	DPAK (Pb-Free)	2500 / Tape & Reel
NVD5407NT4G*	DPAK (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL RESISTANCE RATINGS (Note 1)

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	2.0	°C/W
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	52	°C/W

1. Surface mounted on FR4 board using 1 sq in pad size,
(Cu Area 1.127 sq in [2 oz] including traces).

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			39		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 40 V	T _J = 25°C		1.0	μA
			T _J = 100°C		10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±30 V			±100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.5		3.5	V
Gate Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-6.0		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		21	26	mΩ
		V _{GS} = 5.0 V, I _D = 10 A		32	40	
Forward Transconductance	g _{FS}	V _{GS} = 10 V, I _D = 18 A		15		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 32 V		615	1000	pF
Output Capacitance	C _{OSS}			173		
Reverse Transfer Capacitance	C _{RSS}			80		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 32 V, I _D = 38 A		20		nC
Gate-to-Source Charge	Q _{GS}			2.25		
Gate-to-Drain Charge	Q _{GD}			10.5		

SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DD} = 32 V, I _D = 38 A, R _G = 2.5 Ω		6.8		ns
Rise Time	t _r			17		
Turn-Off Delay Time	t _{d(OFF)}			66		
Fall Time	t _f			51		

SWITCHING CHARACTERISTICS, V_{GS} = 5 V (Note 3)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 5 V, V _{DD} = 20 V, I _D = 20 A, R _G = 2.5 Ω		10		ns
Rise Time	t _r			175		
Turn-Off Delay Time	t _{d(OFF)}			13		
Fall Time	t _f			23		

DRAIN-SOURCE DIODE CHARACTERISTICS (Note 2)

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 5.0 A	T _J = 25°C		0.9	1.1	V
			T _J = 125°C		0.75		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 15 A		38		ns	
Charge Time	t _a			20.5			
Discharge Time	t _b			17			
Reverse Recovery Charge	Q _{RR}			40		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

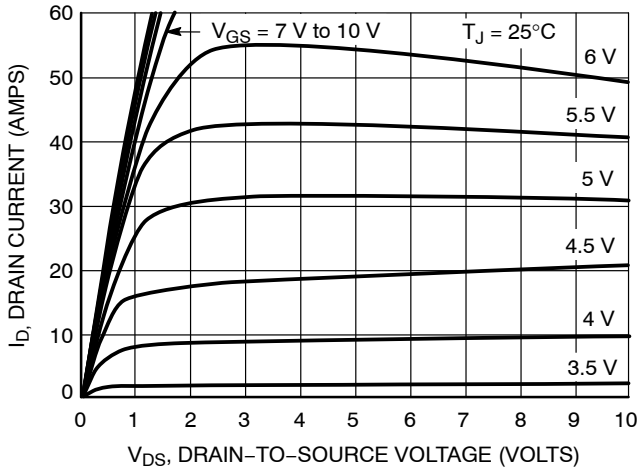


Figure 1. On-Region Characteristics

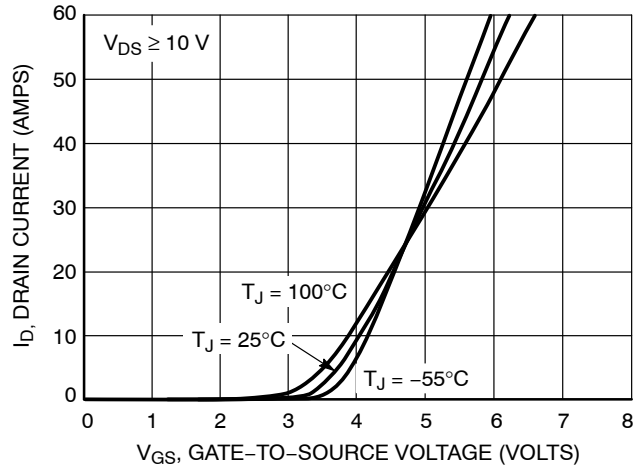


Figure 2. Transfer Characteristics

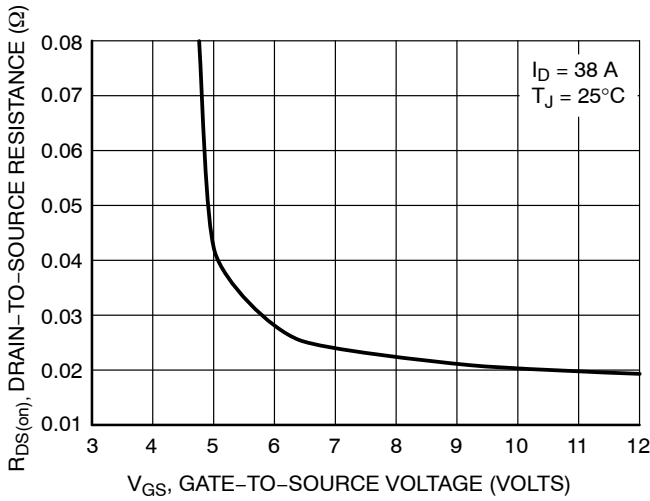


Figure 3. On-Resistance vs. Gate-to-Source Voltage

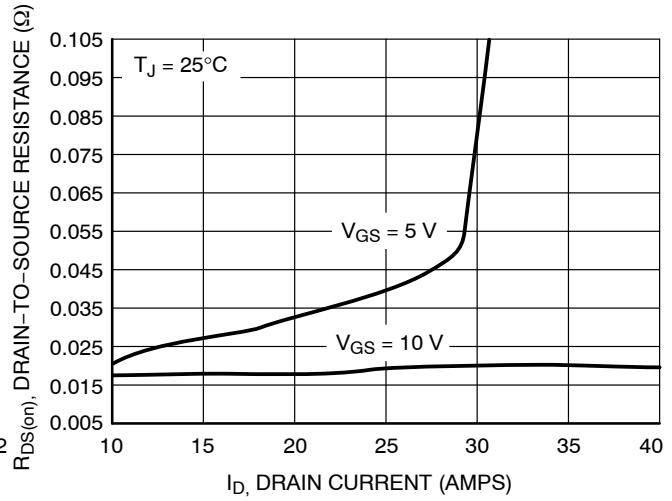


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

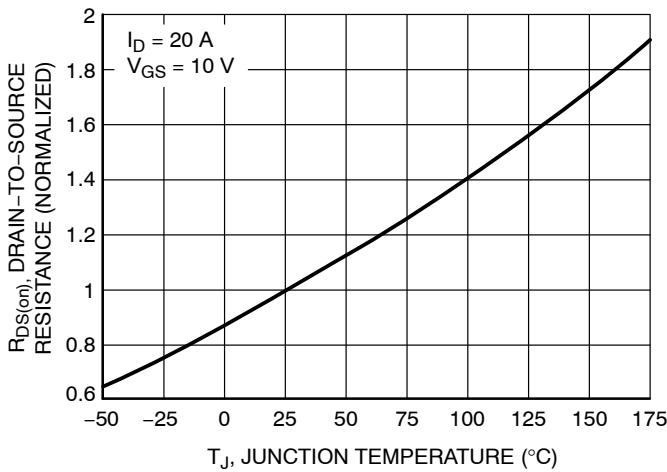


Figure 5. On-Resistance Variation with Temperature

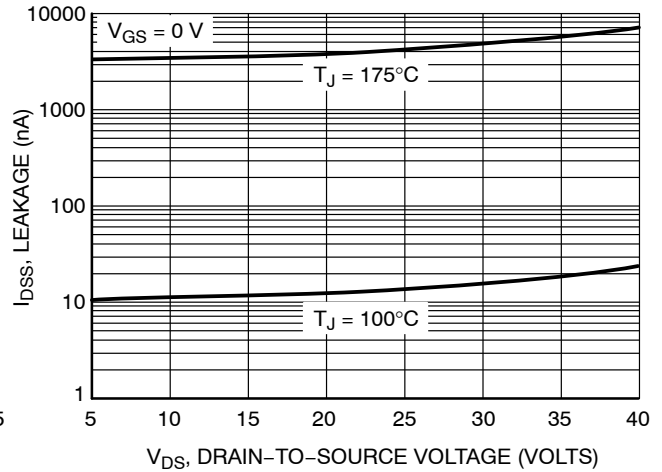


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

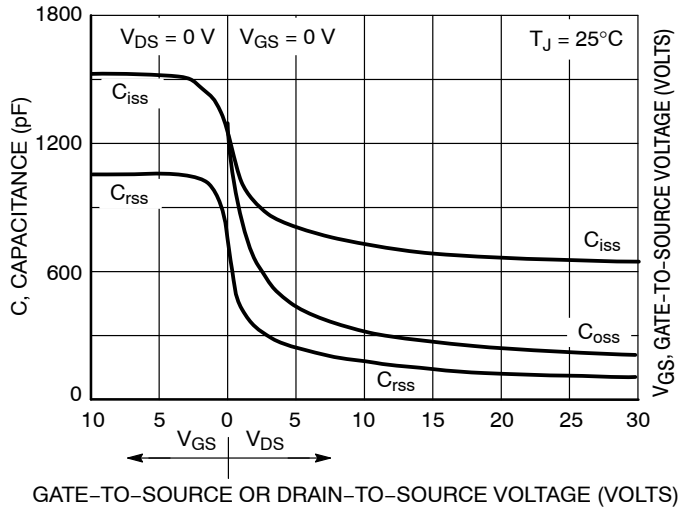


Figure 7. Capacitance Variation

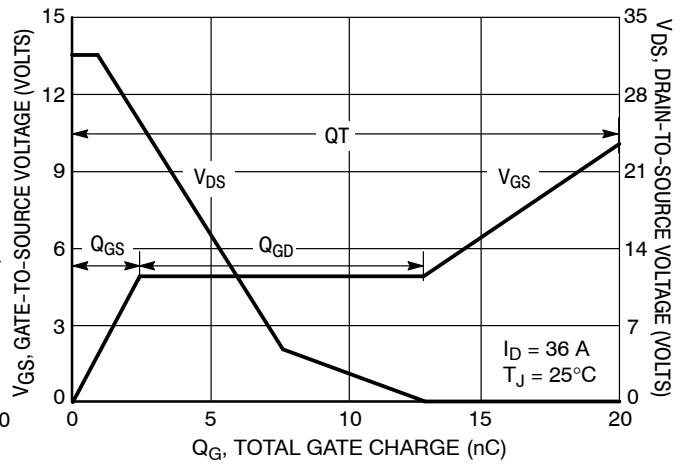


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

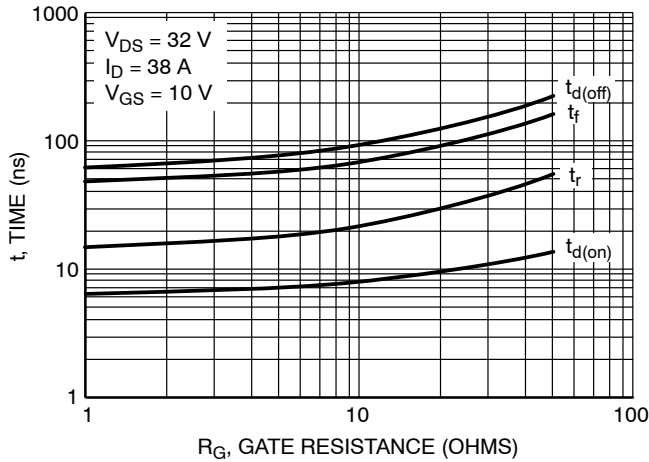


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

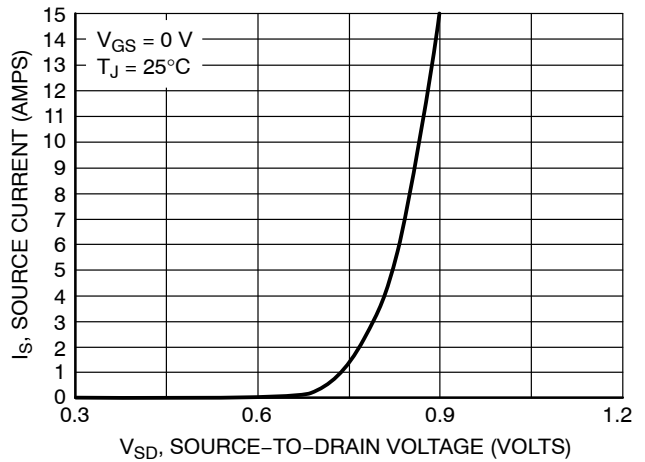


Figure 10. Diode Forward Voltage vs. Current

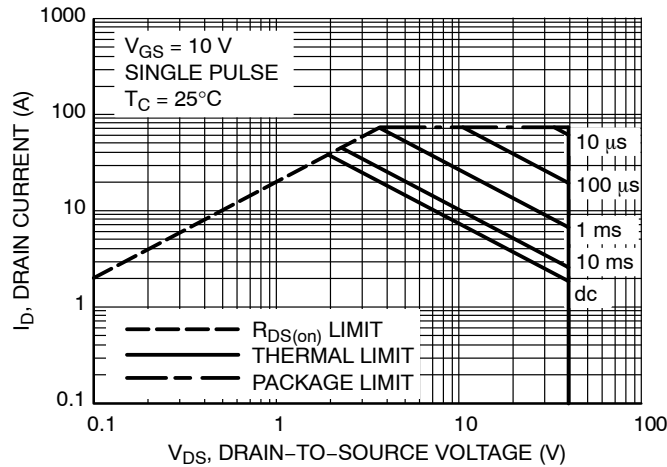


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NTD5407N, STD5407N, NVD5407N

TYPICAL PERFORMANCE CURVES

r(t), EFFECTIVE TRANSIENT THERMAL RESISTANCE

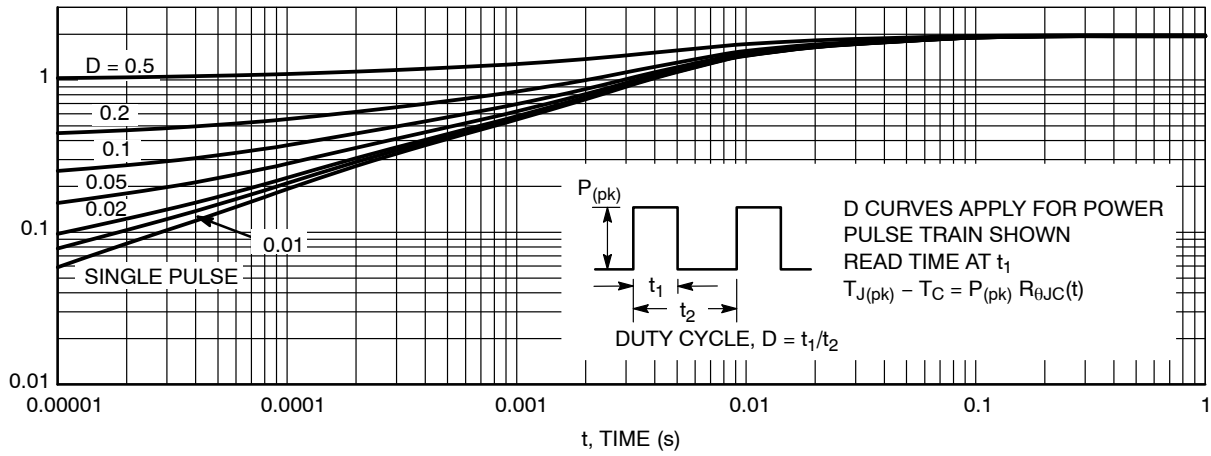
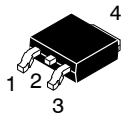


Figure 12. Thermal Response

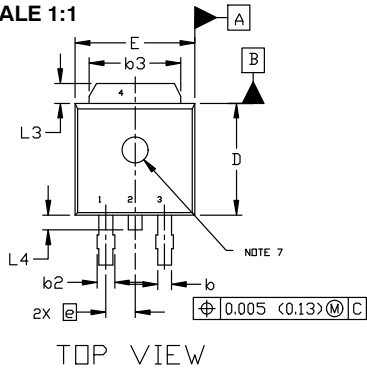
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



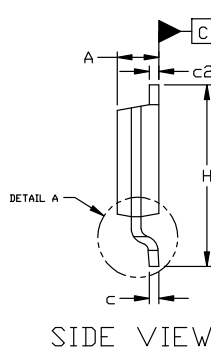
DPAK (SINGLE GAUGE) CASE 369C ISSUE G

DATE 31 MAY 2023

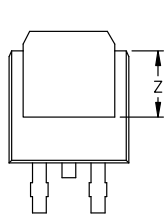
SCALE 1:1



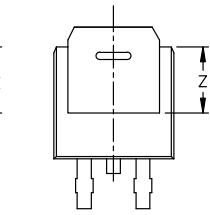
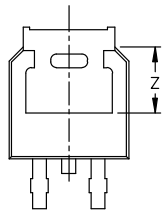
TOP VIEW



SIDE VIEW

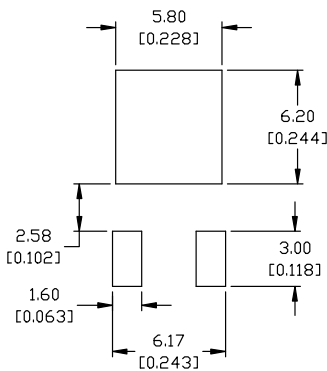


BOTTOM VIEW



BOTTOM VIEW

ALTERNATE CONSTRUCTIONS



RECOMMENDED MOUNTING FOOTPRINT*

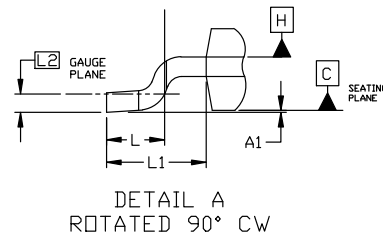
*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

- | | | | | |
|--|--|---|---|--|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE | STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE | STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE |
| STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2 | STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE | STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE | STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE |

NOTES:

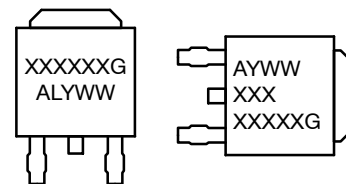
- DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
- OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---



DETAIL A
ROTATED 90° CW

GENERIC MARKING DIAGRAM*



- IC**
 XXXXXX = Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 WW = Work Week
 G = Pb-Free Package
- Discrete**
 AYWW
 XXX
 XXXXXG

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

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