THE DATASHEET OF

BSZ036NE2LSATMA1

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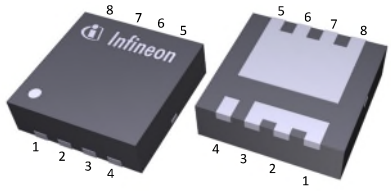
MOSFET

OptiMOS™ Power-MOSFET, 25 V

PG-TSDSON-8 FL



Features

- Optimized for high performance buck converter (Server,VGA)
- Very low $FOMQ_{OSS}$ for high frequency SMPS
- Low $FOMQ_{SW}$ for high frequency SMPS
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

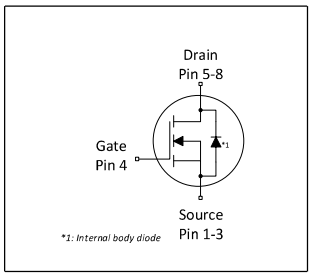


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	25	V
$R_{DS(on),max}$, V_{GS}=10 V	3.6	mΩ
$R_{DS(on),max}$, V_{GS}=4.5 V	5.1	mΩ
I_D	79	A

Type / Ordering Code	Package	Marking	Related Links
BSZ036NE2LS	PG-TSDSON-8 FL	036NE2L	-

[1] J-STD20 and JESD22

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1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - - - -	- - - - -	79 50 66 42 16	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_C=25 °C V_{GS}=4.5 V, T_C=100 °C V_{GS}=4.5V,T_A=25°C,R_{thJA}=60K/W
Pulsed drain current[2]	$I_{D,pulse}$	-	-	316	A	T_C=25 °C
Avalanche current, single pulse[3]	I_{AS}	-	-	20	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	40	mJ	I_D=20 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	37 2.1	W	T_C=25 °C T_A=25 °C, R_{thJA}=60 K/W
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.4	K/W	-
Device on PCB, 6 cm^2 cooling area[4]	R_{thJA}	-	-	60	K/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] See Diagram 3 for more detailed information
[3] See Diagram 13 for more detailed information
[4] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	25	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2.0	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1.0 100	µA	V_{DS}=25 V, V_{GS}=0 V, T_j=25 °C V_{DS}=25 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	4.1 3.0	5.1 3.6	mΩ	V_{GS}=4.5 V, I_D=20 A V_{GS}=10 V, I_D=20 A
Gate resistance	R_G	0.5	0.9	1.8	Ω	-
Transconductance	g_{fs}	44	89	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=30 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	1200	1596	pF	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	470	625	pF	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	51	-	pF	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	3.3	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	2.8	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	15	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	2.2	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge[1)]	Q_{gs}	-	3.1	4.1	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	1.9	-	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate to drain charge[1)]	Q_{gd}	-	1.9	2.8	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	3.1	-	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total[1)]	Q_g	-	7.7	10	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.7	-	V	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total[1)]	Q_g	-	16	21	-	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	6.7	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge[1)]	Q_{oss}	-	9.4	13	-	V_{DD}=12 V, V_{GS}=0 V

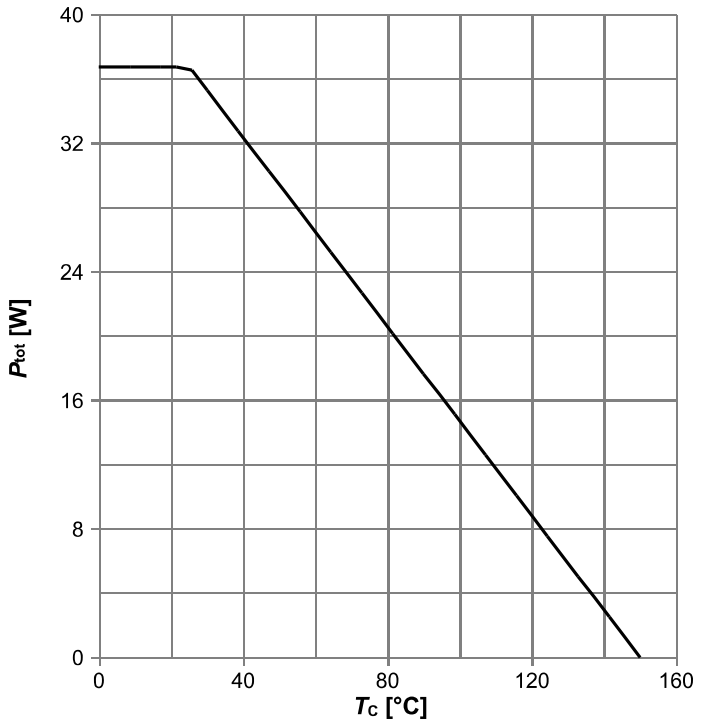
[1)] Defined by design. Not subject to production test
[2)] See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	37	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	316	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.85	1.0	V	V_{GS}=0 V, I_F=20 A, T_j=25 °C
Reverse recovery charge	Q_{rr}	-	10	-	nC	V_R=15 V, I_F=30A, di_F/dt=400 A/µs

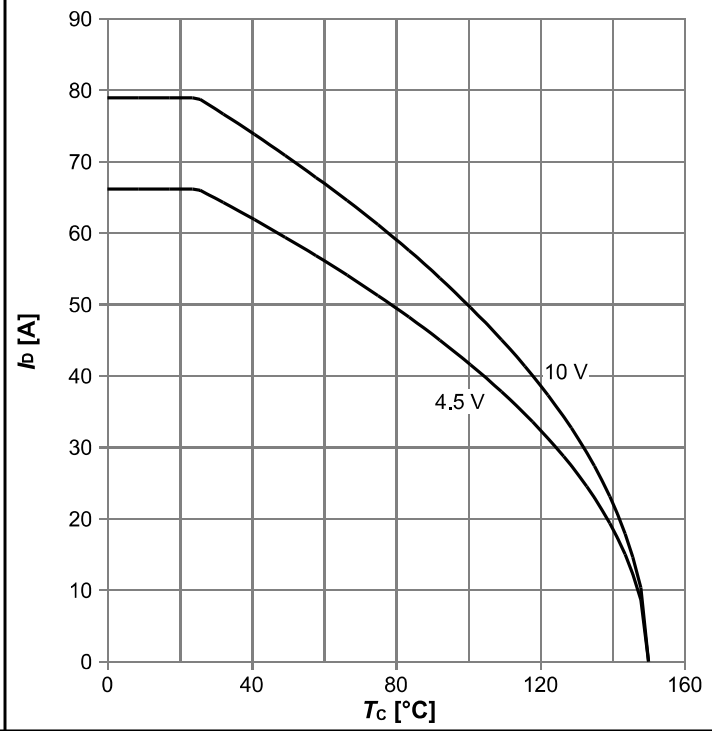
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



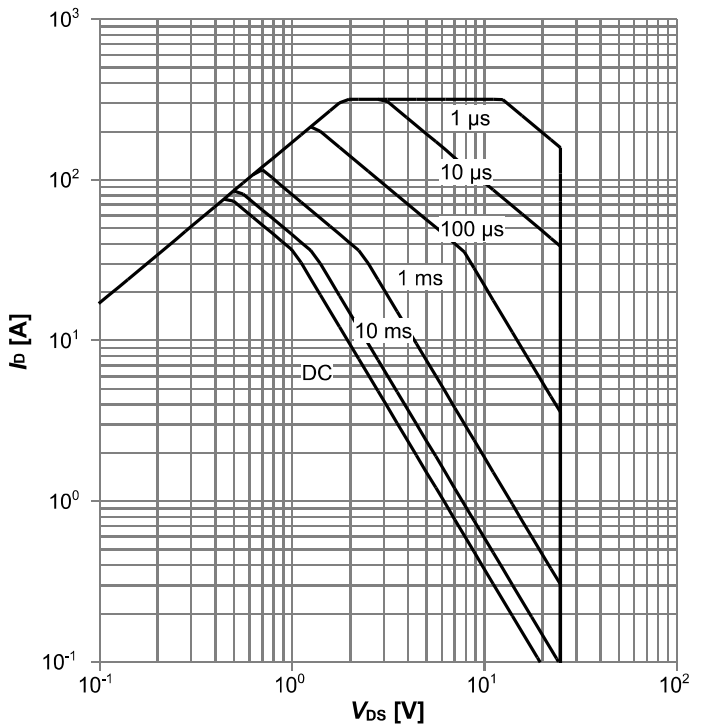
P_{tot}=f(T_C)

Diagram 2: Drain current



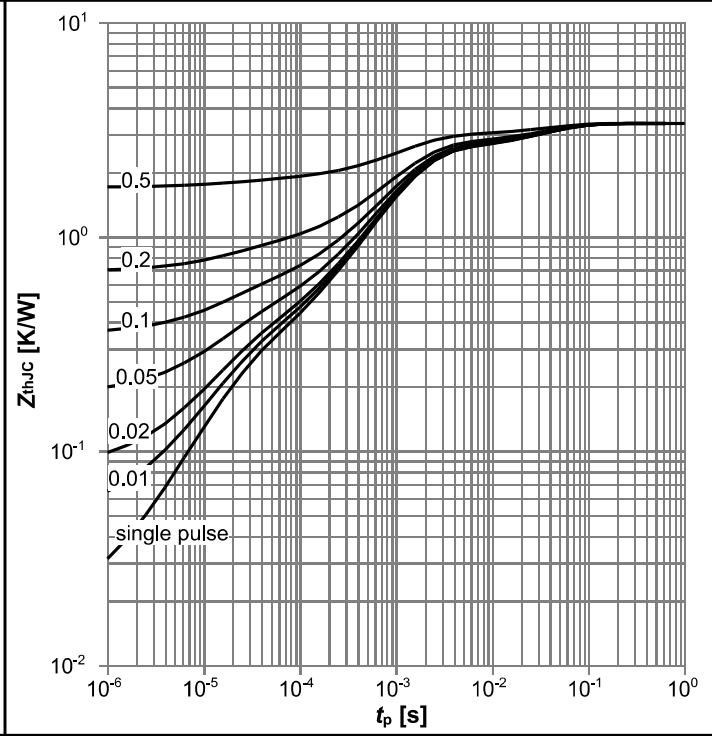
I_D=f(T_C); parameter: V_{GS}

Diagram 3: Safe operating area



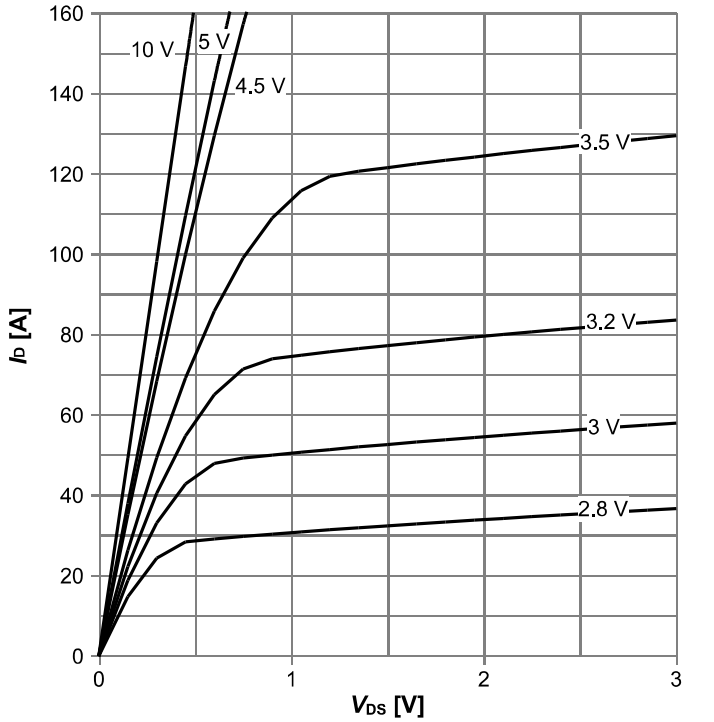
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



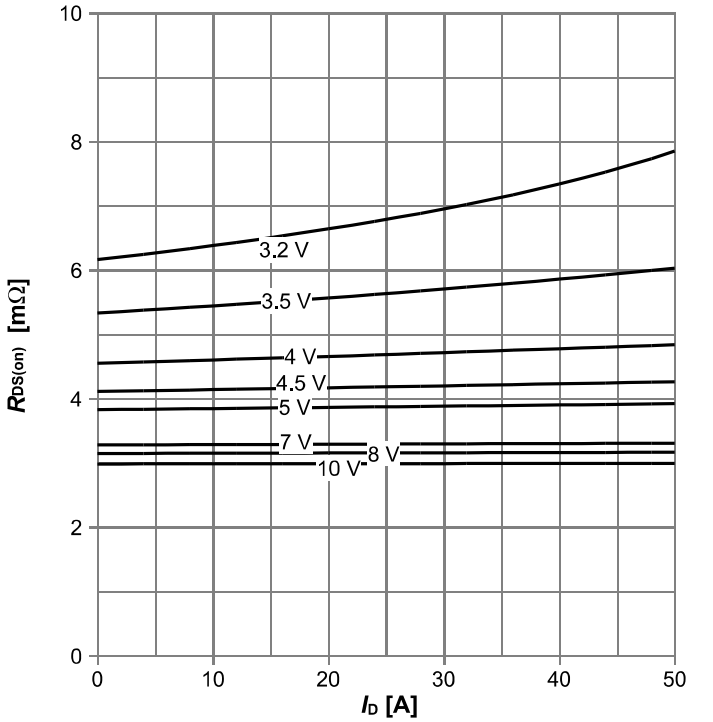
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



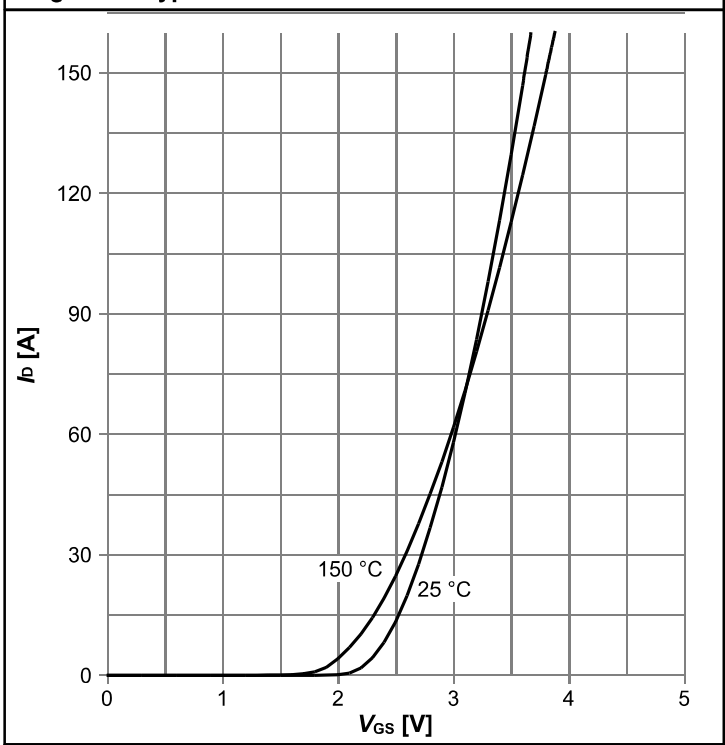
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



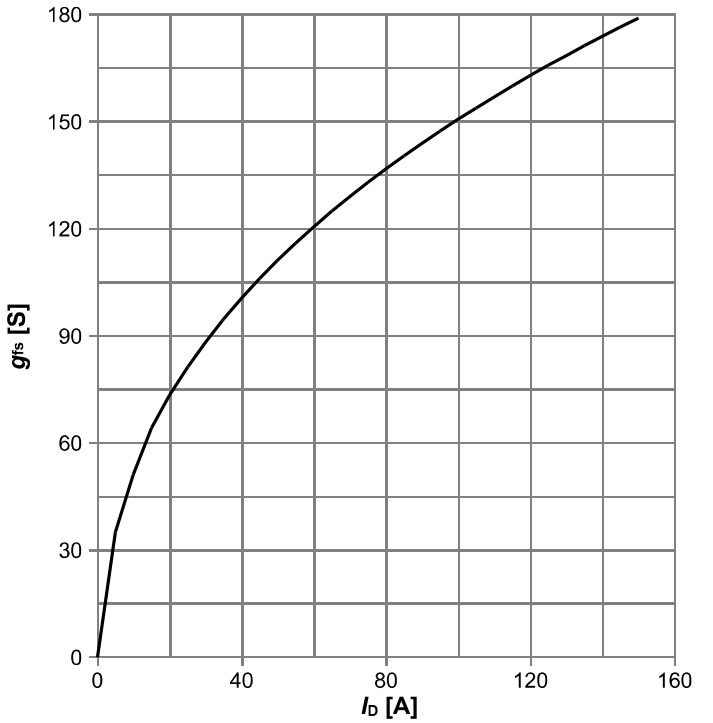
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



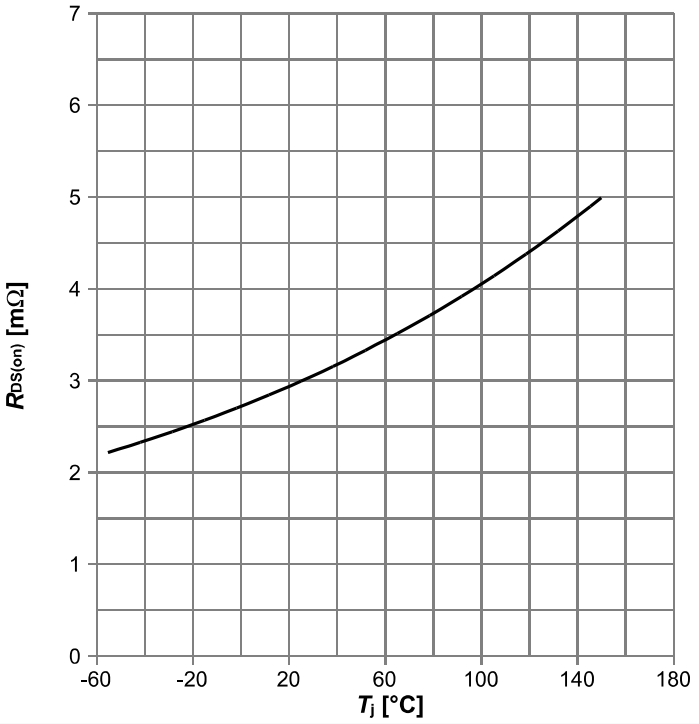
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



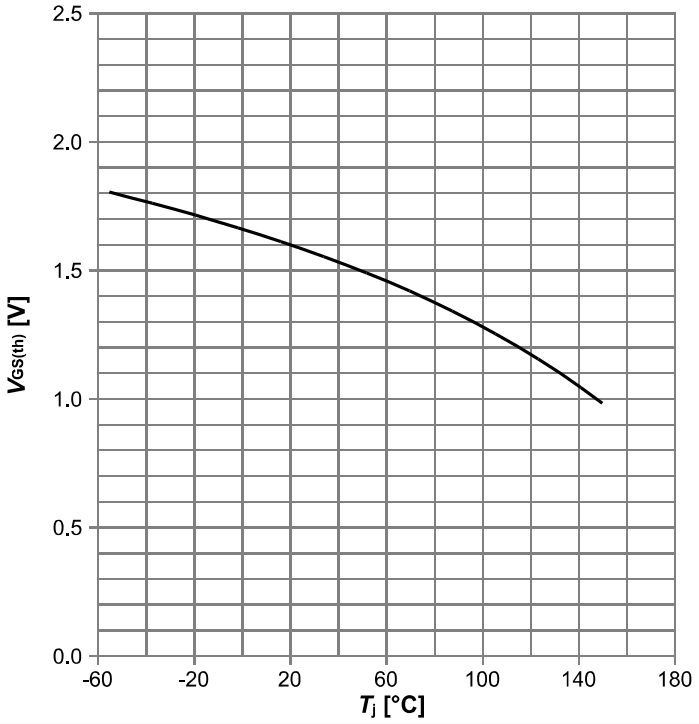
g_{fs}=f(I_D); T_j=25 °C

Diagram 9: Drain-source on-state resistance



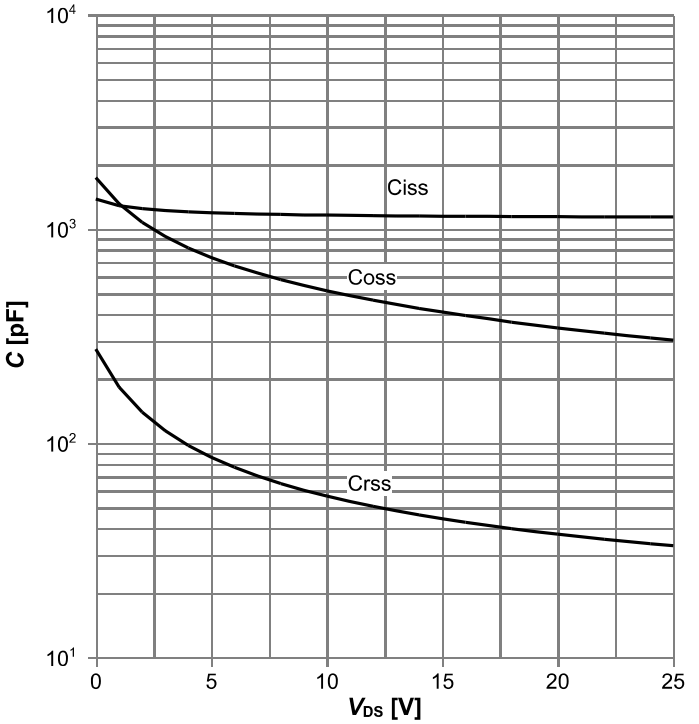
$R_{DS(on)}$=f(T_j); I_D=20 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



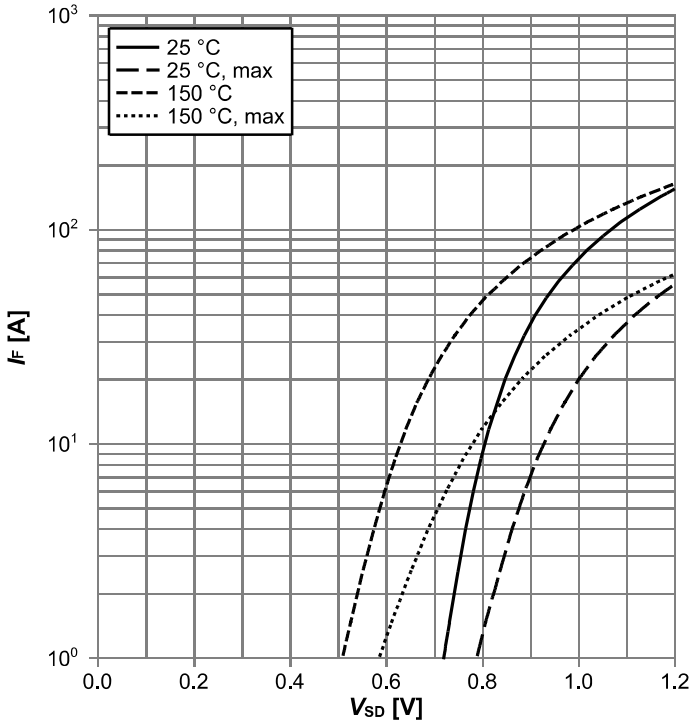
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=250 µA

Diagram 11: Typ. capacitances



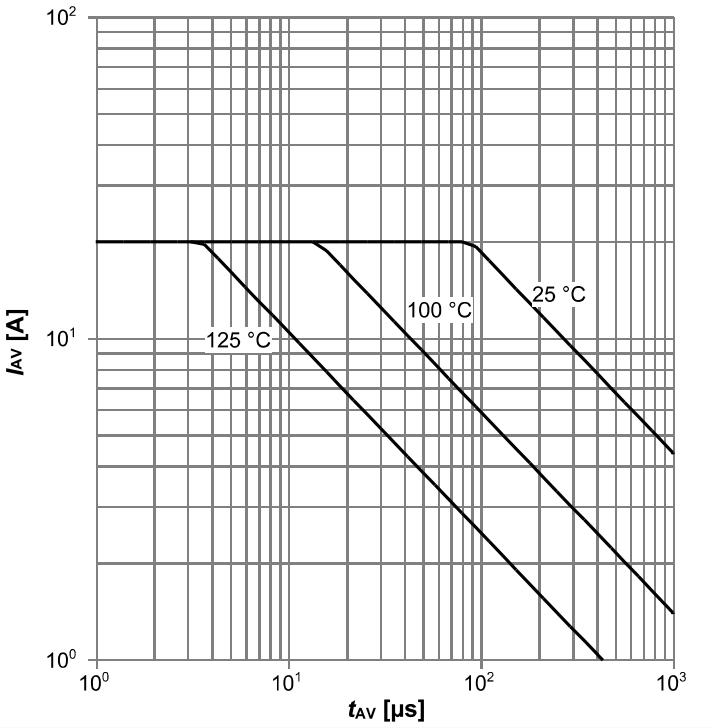
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



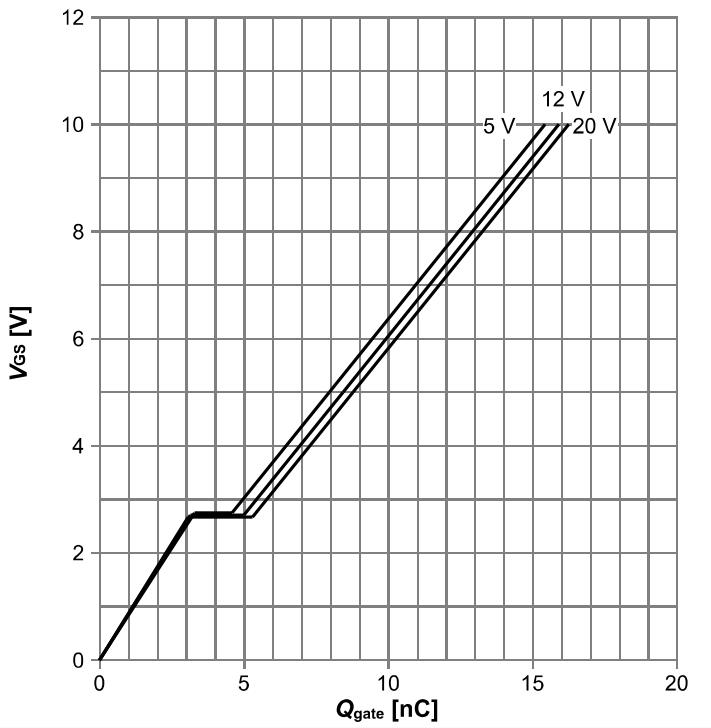
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



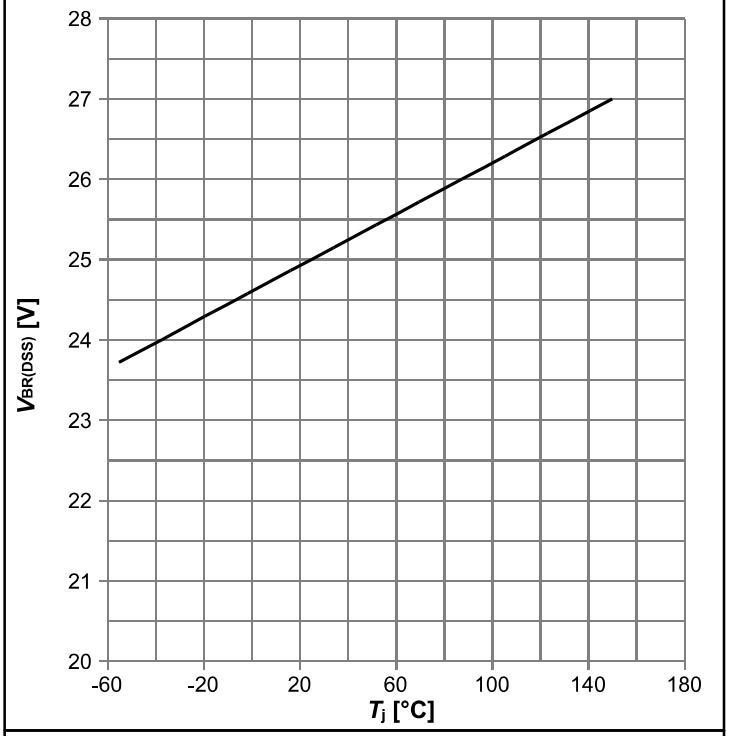
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



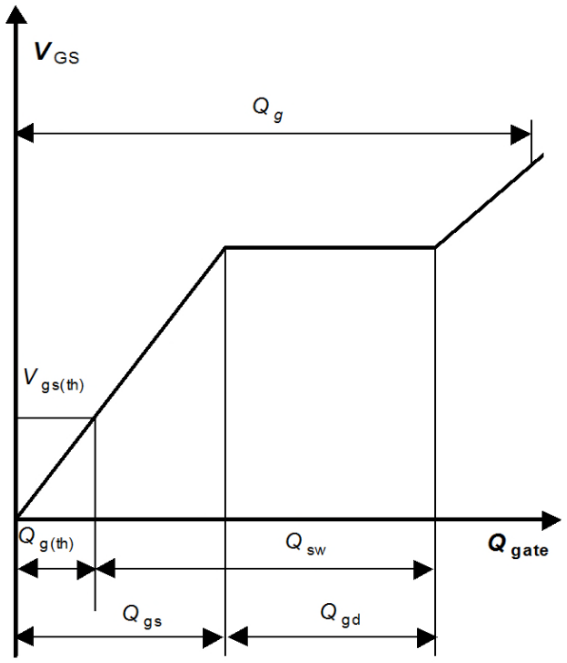
V_{GS}=f(Q_{gate}); I_D=30 A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

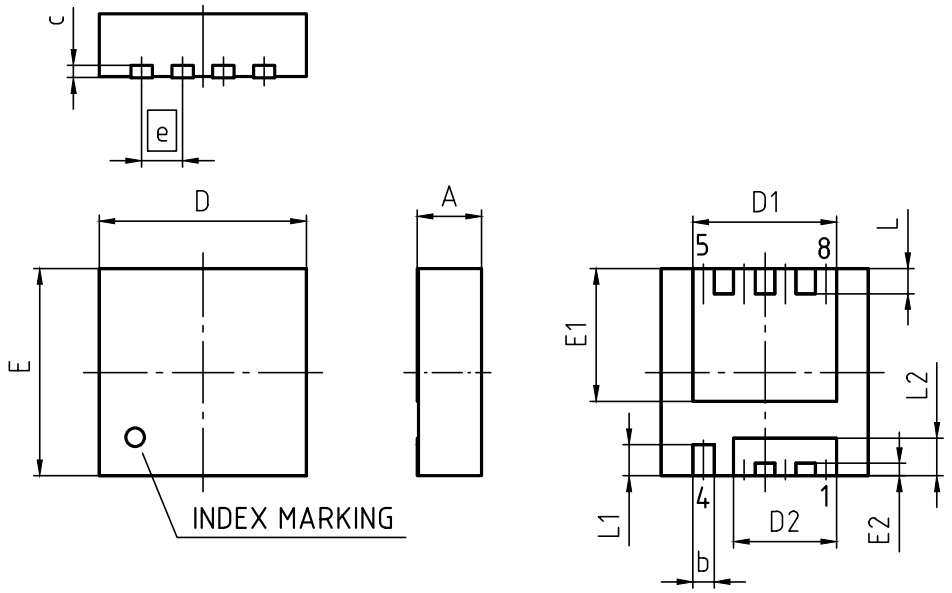


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-TSDSON-8-U03	
REVISION: 03	DATE: 20.10.2020	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.10
b	0.24	0.44
c	(0.20)	
D	3.20	3.40
D1	2.19	2.39
D2	1.54	1.74
E	3.20	3.40
E1	2.01	2.21
E2	0.10	0.30
e	0.65	
L	0.30	0.50
L1	0.40	0.60
L2	0.50	0.70
aaa	0.06	

Figure 1 Outline PG-TSDSON-8 FL, dimensions in mm

Revision History

BSZ036NE2LS

Revision: 2021-06-07, Rev. 2.4

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.3	2020-11-13	Update package drawing and footnotes
2.4	2021-06-07	Update current rating and add max ratings to Diagram 12

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