THE DATASHEET OF

SPB42N03S2L13T

OptiMOS® Power-Transistor

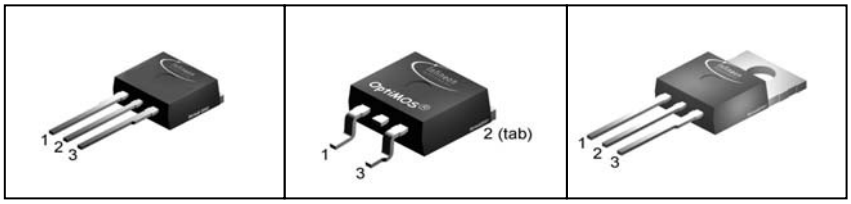
Features

- N-channel
- Enhancement mode
- Logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Superior thermal resistance
- 175 °C operating temperature
- Avalanche rated
- dv/dt rated

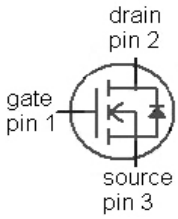
Product Summary

V_{DS}	30	V
$R_{DS(on),max}$	12.9	mΩ
I_D	42	A

P-TO262-3-1 P-TO263-3-2 P-TO220-3-1



Type	Package	Ordering Code	Marking
SPP42N03S2L-13	P-TO220-3-1	Q67042-S4034	2N03L13
SPB42N03S2L-13	P-TO263-3-2	Q67042-S4035	2N03L13
SPI42N03S2L-13	P-TO262-3-1	Q67042-S4104	2N03L13



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current[1)]	I_D	T_C=25 °C	42	A
		T_C=100 °C	42	
Pulsed drain current	$I_{D,pulse}$	T_C=25 °C	248	
Avalanche energy, single pulse	E_{AS}	I_D=42 A, R_{GS}=25 Ω	110	mJ
Repetitive avalanche energy	E_{AR}	limited by T_{jmax} [2)]	8	mJ
Reverse diode dv/dt	dv/dt	I_D=42 A, V_{DS}=24 V, di/dt=200 A/µs, $T_{j,max}$=175 °C	6	kV/µs
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	83	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	1.2	1.8	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[3)]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=37 µA	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=30 V, V_{GS}=0 V, T_j=25 °C	-	0.01	1	µA
		V_{DS}=30 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	1	100	nA
Drain-source on-state resistance[4)]	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=21 A	-	14.9	19.9	mΩ
		V_{GS}=4.5 V, I_D=21 A, SMD version	-	14.5	19.6	
		V_{GS}=10 V, I_D=21 A	-	10.3	12.9	
		V_{GS}=10 V, I_D=21 A, SMD version	-	9.9	12.6	
Gate resistance	R_G		-	1	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=42 A	21	42	-	S

[1)] Current is limited by bondwire; with an R_{thJC}=1.8 K/W the chip is able to carry 64 A at 25°C, for detailed information see app.-note ANPS071E at www.infineon.com/optimos.

[2)] Defined by design. Not subject to production test.

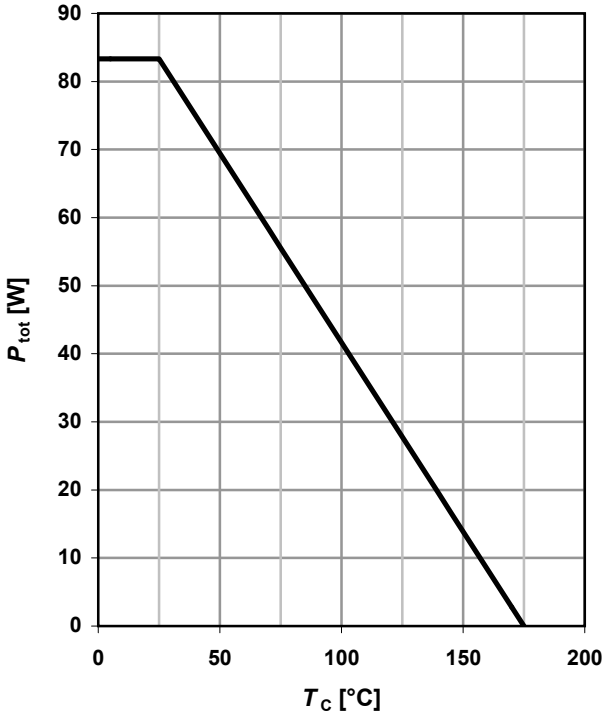
[3)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[4)] Diagrams are related to straight lead versions.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=25 V, f=1 MHz	-	850	1130	pF
Output capacitance	C_{oss}		-	330	440	
Reverse transfer capacitance	C_{rss}		-	90	130	
Turn-on delay time	$t_{d(on)}$	V_{DD}=15 V, V_{GS}=10 V, I_D=21 A, R_G=7.8 Ω	-	6.5	9.8	ns
Rise time	t_r		-	12	18	
Turn-off delay time	$t_{d(off)}$		-	24	36	
Fall time	t_f		-	14.5	21.8	
Gate Charge Characteristics						
Gate to source charge	Q_{gs}	V_{DD}=24 V, I_D=21 A, V_{GS}=0 to 10 V	-	2.7	3.6	nC
Gate to drain charge	Q_{gd}		-	7.9	11.9	
Gate charge total	Q_g		-	22.9	30.5	
Gate plateau voltage	$V_{plateau}$		-	3.5	-	V
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	42	A
Diode pulse current	$I_{S,pulse}$		-	-	248	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=42 A, T_j=25 °C	-	0.95	1.25	V
Reverse recovery time	t_{rr}	V_R=15 V, I_F=I_S, di_F/dt=100 A/µs	-	24	31	ns
Reverse recovery charge	Q_{rr}		-	18	23	nC

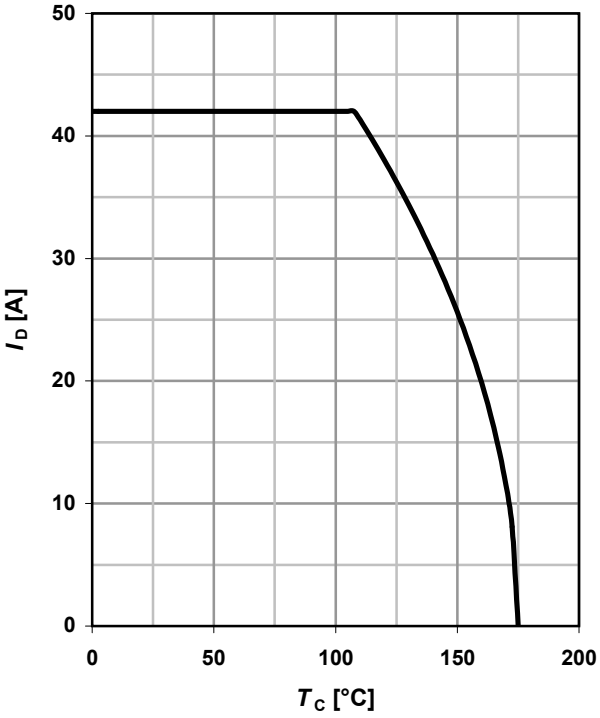
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

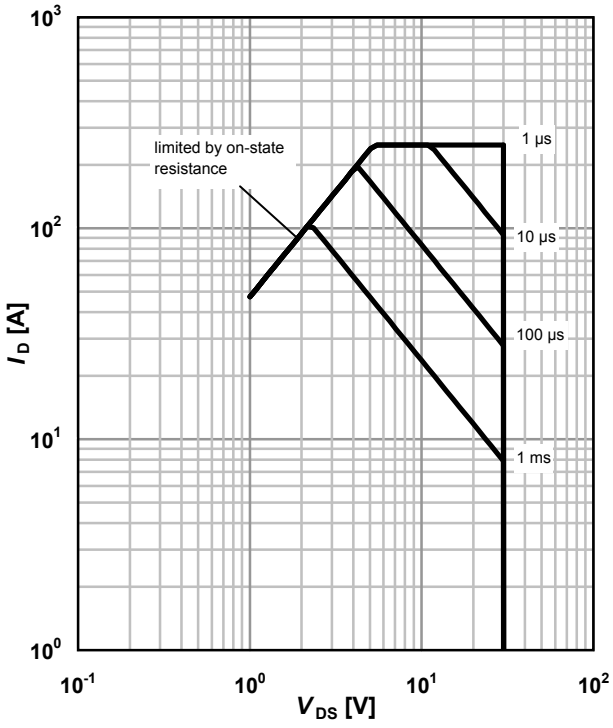
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

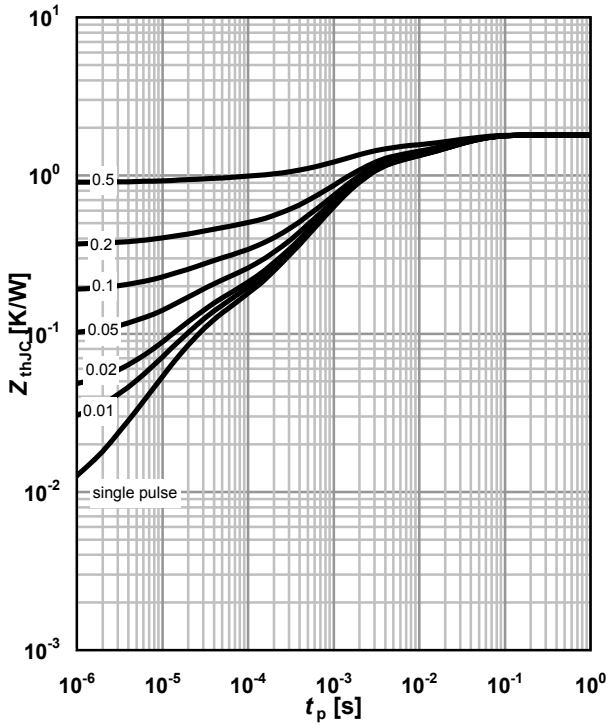
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

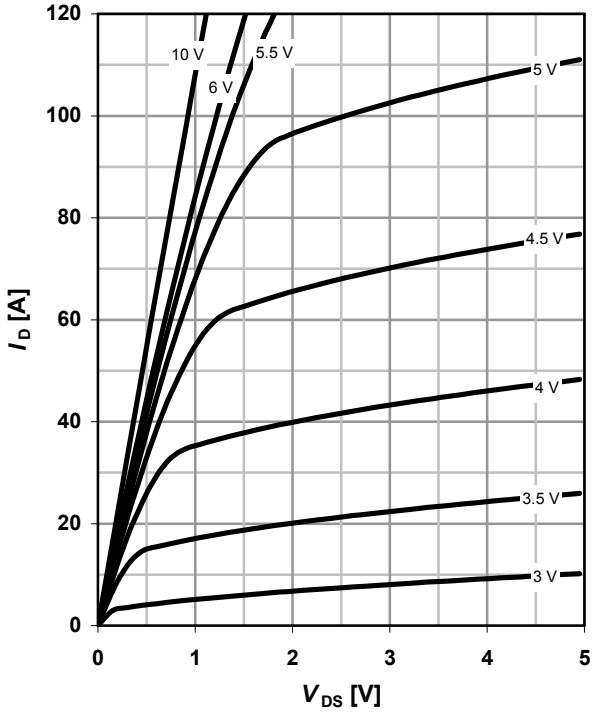
parameter: $D=t_p/T$



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

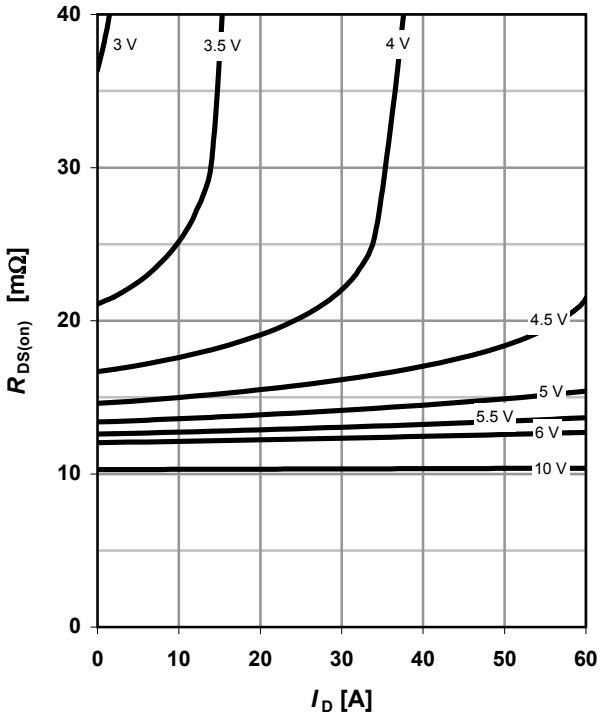
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

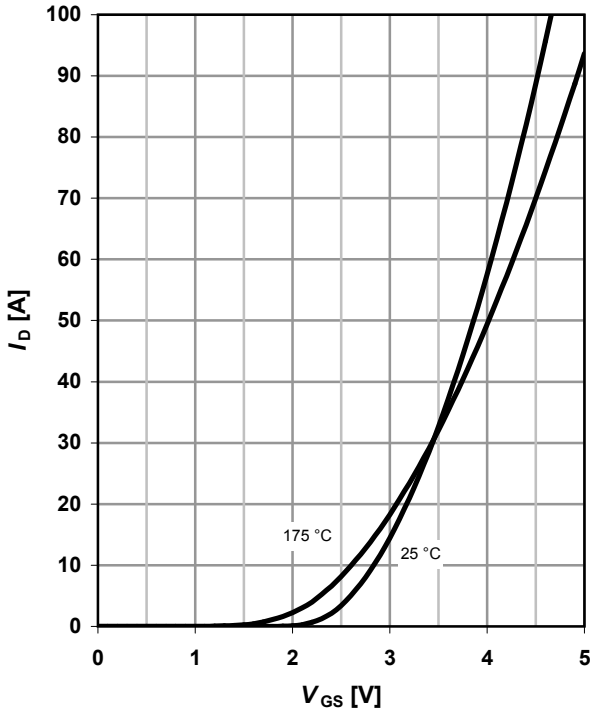
parameter: V_{GS}



7 Typ. transfer characteristics

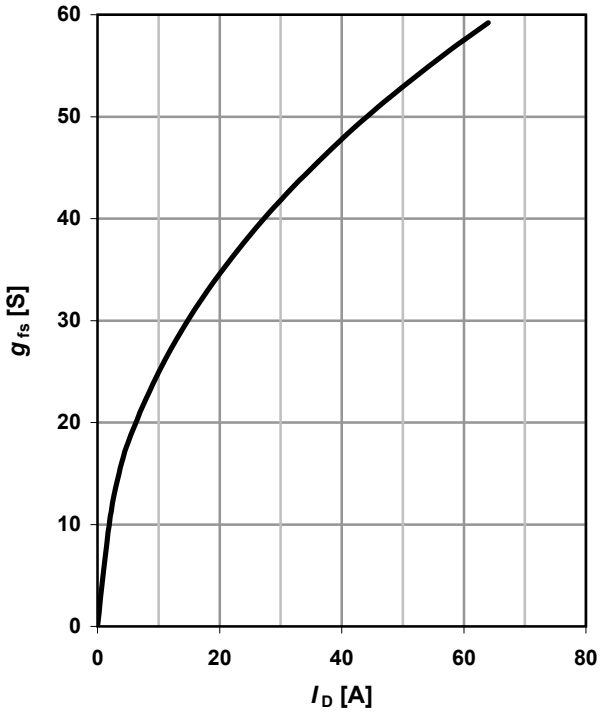
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



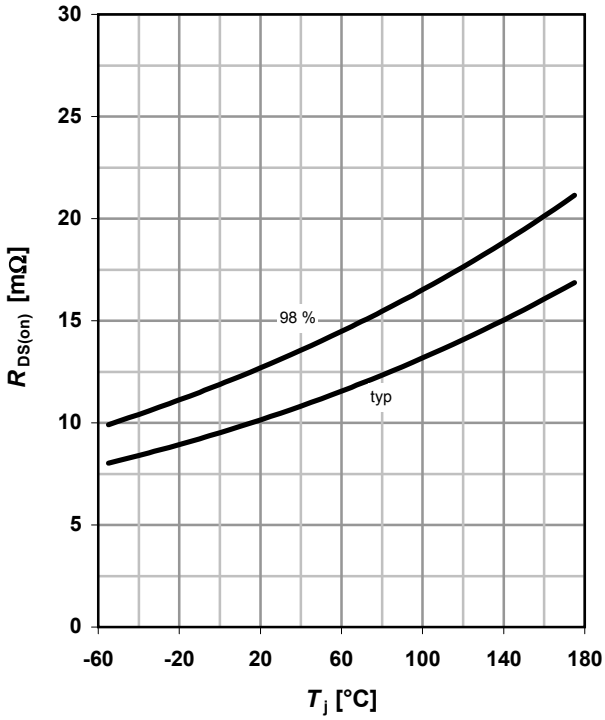
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



9 Drain-source on-state resistance

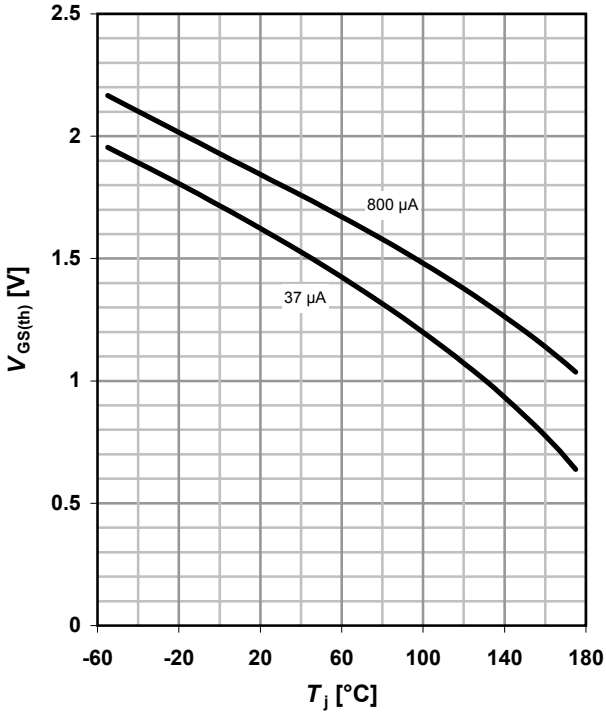
$R_{DS(on)}=f(T_j)$; $I_D=21$ A; $V_{GS}=10$ V



10 Typ. gate threshold voltage

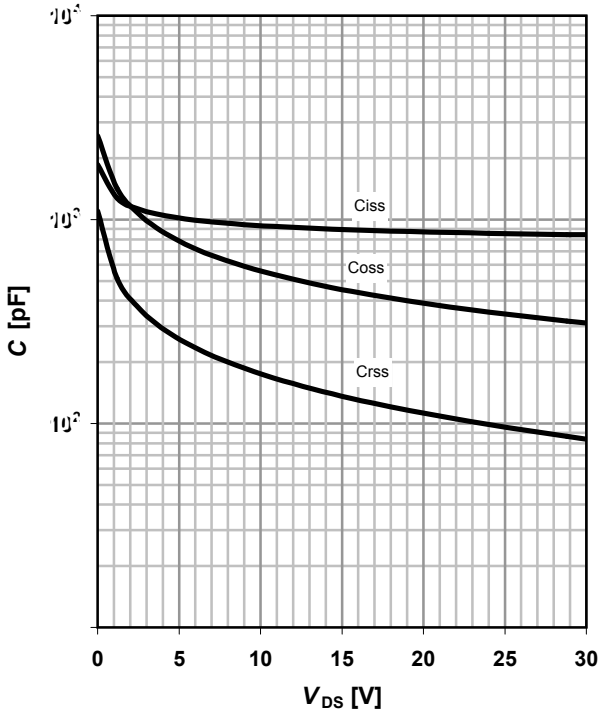
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

parameter: I_D



11 Typ. capacitances

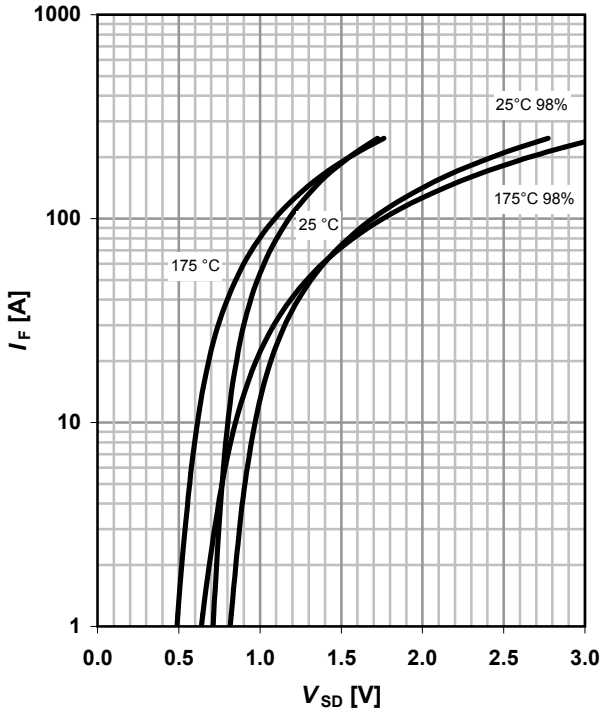
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

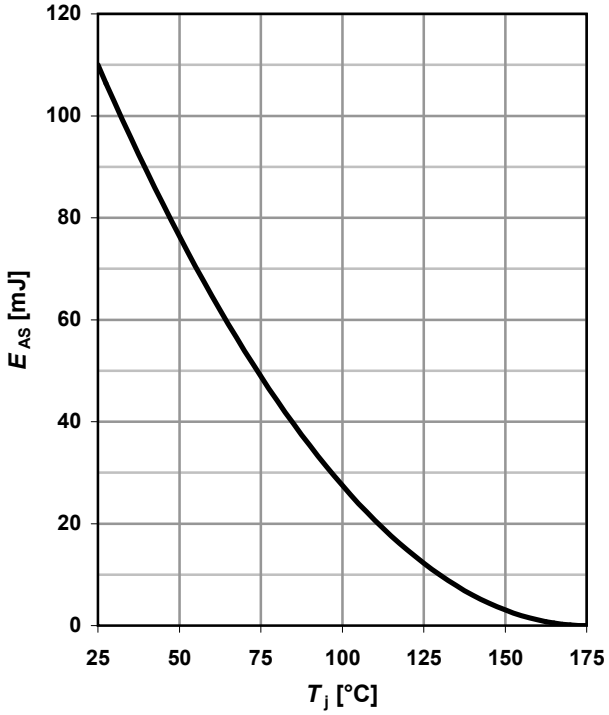
parameter: T_j



13 Avalanche characteristics

E_{AS}=f(T_j)

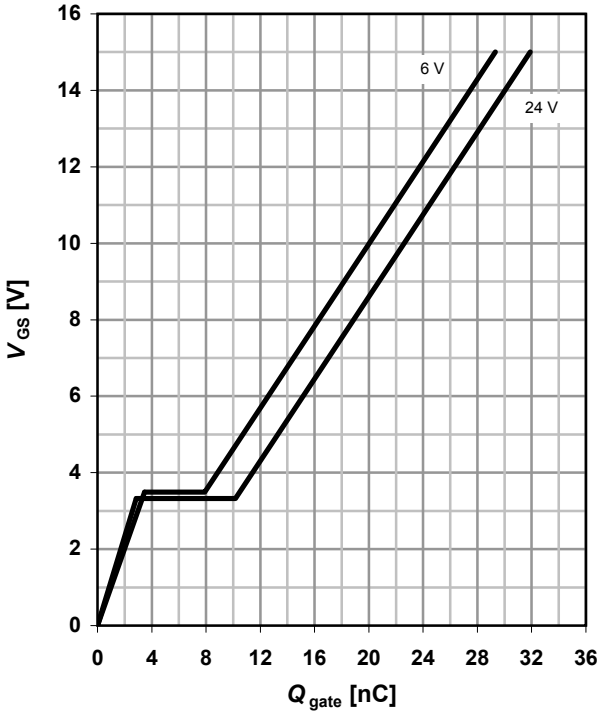
parameter: I_D=42A, V_{DD}=25V, R_{GS}=25Ω



14 Typ. gate charge

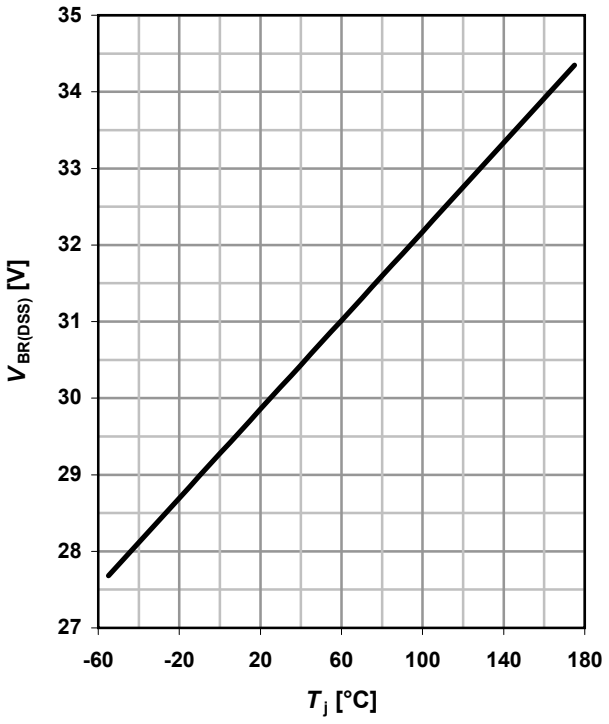
V_{GS}=f(Q_{gate}); I_D=21 A pulsed

parameter: V_{DD}

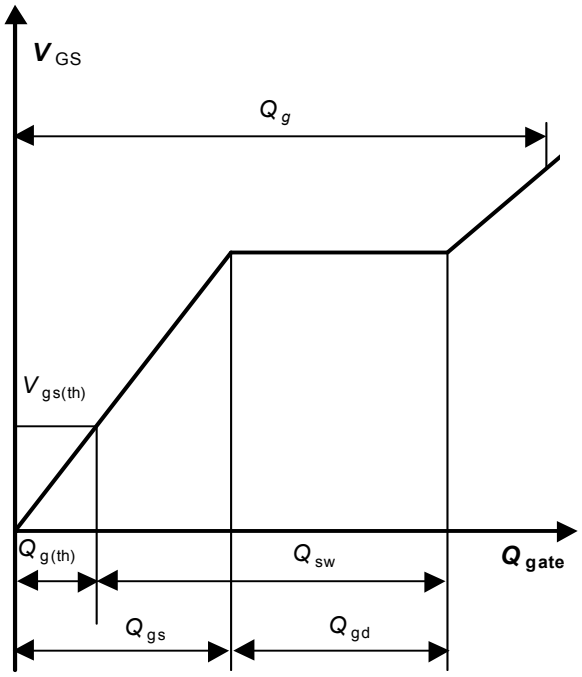


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA

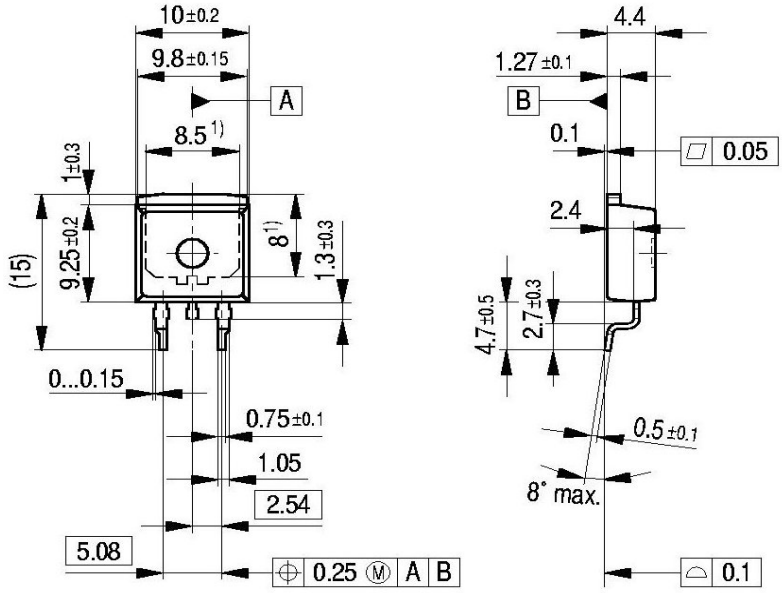


16 Gate charge waveforms

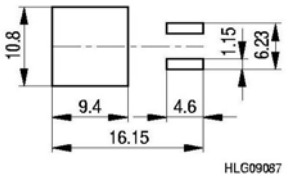


Package Outline

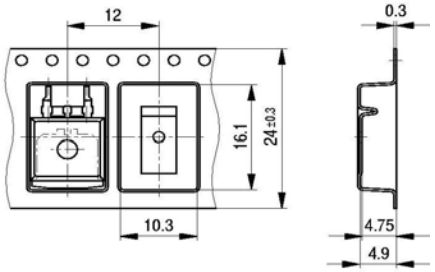
P-TO263-3-2: Outline



Footprint



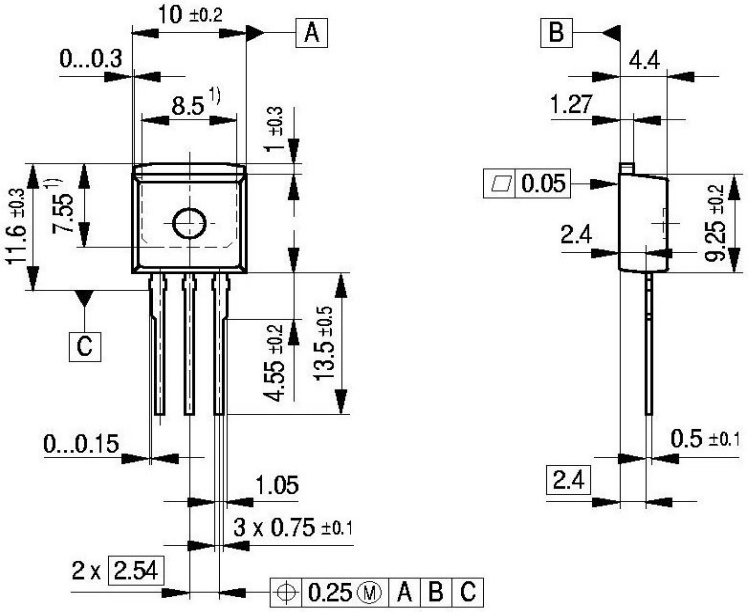
Packaging



1) Typical
All metal surfaces tin plated, except area of cut.

GPT09085

P-TO262-3-1: Outline

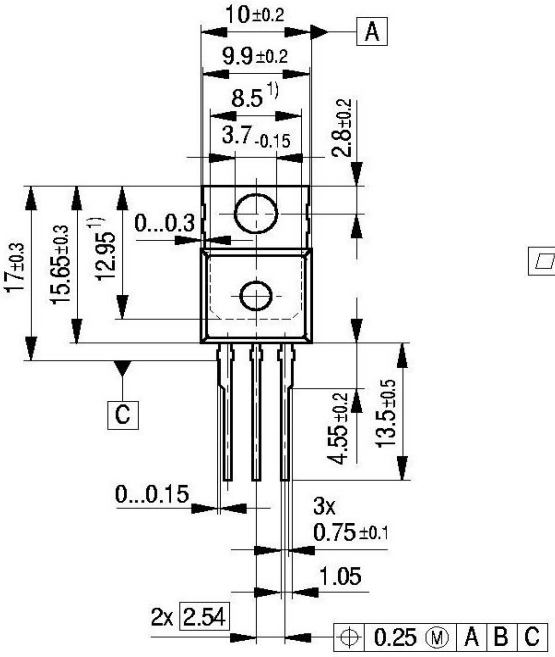


1) Typical
Metal surface min. X = 7.25, Y = 6.9
All metal surfaces tin plated, except area of cut.

Dimensions in mm

Package Outline

P-TO220-3-1: Outline



1) Typical

All metal surfaces tin plated, except area of cut.
Metal surface min. x=7.25, y=12.3

Dimensions in mm

Packaging

Published by
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Bereich Kommunikation
St.-Martin-Straße 53
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Further information
Please note that the part number is BSPP42N03S2L-13, BSPB42N03S2L-13 and BSPI42N0ß3S2L, for simplicity the device is refered to by the term SPP42N03S2L-13, SPB42N03S2L-13, SPI42N03S2L-13 throughout this documentation.

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