



THE DATASHEET OF SP8J5FRATB



4V Drive Pch+Pch MOS FET

SP8J5 FRA

●Structure

Silicon P-channel MOS FET

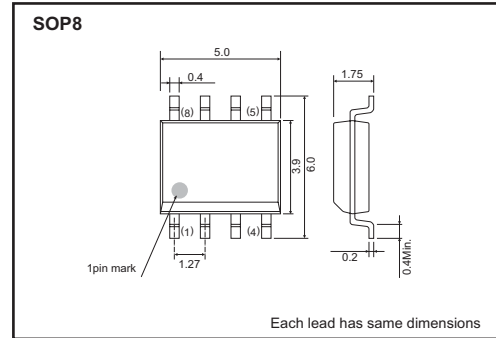
●Features

- 1) Low On-resistance. (25mΩ at 4.5V)
- 2) High Power Package. (PD=2.0W)
- 3) High speed switching.
- 4) Low voltage drive. (4V)

●Applications

Power switching, DC-DC converter

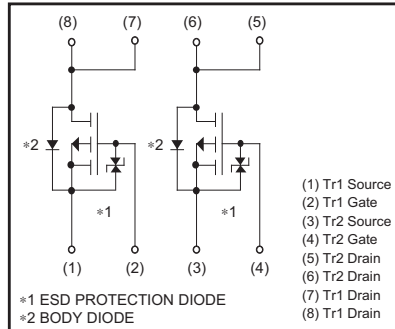
●External dimensions (Unit : mm)



●Packaging specifications

Type	Package	Taping
	Code	TB
	Quantity (pcs)	2500
SP8J5 FRA		○

●Inner circuit



●Absolute maximum ratings (Ta=25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V _{DSS}	-30	V	
Gate-source voltage	V _{GSS}	±20	V	
Drain current	Continuous	I _D	±7.0	A
	Pulsed	I _{DP} *1	±28	A
Source current (Body diode)	Continuous	I _S	-1.6	A
	Pulsed	I _{SP} *1	-28	A
Total power dissipation	P _D *2	2.0	W	
Channel temperature	T _{ch}	150	°C	
Range of Storage temperature	T _{stg}	-55 to +150	°C	

*1 Pw≤10μs, Duty cycle≤1%
 *2 Mounted on a ceramic board

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	R _{th(ch-a)} *	62.5	°C / W

* Mounted on a ceramic board.

Transistors

●Electrical characteristics (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	± 10	μA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	–30	–	–	V	$I_D = -1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	$V_{DS} = -30V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	–1.0	–	–2.5	V	$V_{DS} = -10V, I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	–	20	28	m Ω	$I_D = -7A, V_{GS} = -10V$
		–	25	35	m Ω	$I_D = -3.5A, V_{GS} = -4.5V$
		–	30	42	m Ω	$I_D = -3.5A, V_{GS} = -4.0V$
Forward transfer admittance	$ Y_{fs} $ *	6.0	–	–	S	$V_{DS} = -10V, I_D = -3.5A$
Input capacitance	C_{iss}	–	2600	–	pF	$V_{DS} = -10V$
Output capacitance	C_{oss}	–	450	–	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	–	350	–	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	–	20	–	ns	$I_D = -3.5A$
Rise time	t_r *	–	50	–	ns	$V_{DD} = -15V$
Turn-off delay time	$t_{d(off)}$ *	–	110	–	ns	$V_{GS} = -10V$
Fall time	t_f *	–	70	–	ns	$R_L=4.3\Omega$
Total gate charge	Q_g *	–	25	–	nC	$V_{DD} = -15V$
Gate-source charge	Q_{gs} *	–	5.5	–	nC	$V_{GS} = -5V$
Gate-drain charge	Q_{gd} *	–	10	–	nC	$I_D = -7A$

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}	–	–	–1.2	V	$I_S = -1.6A, V_{GS}=0V$

Transistors

●Electrical characteristic curves

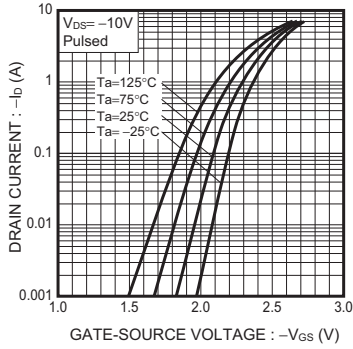


Fig.1 Typical Transfer Characteristics

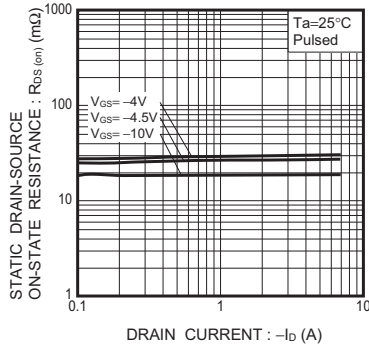


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current

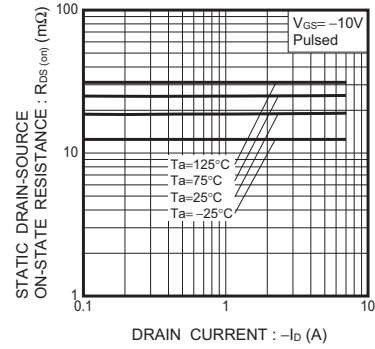


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

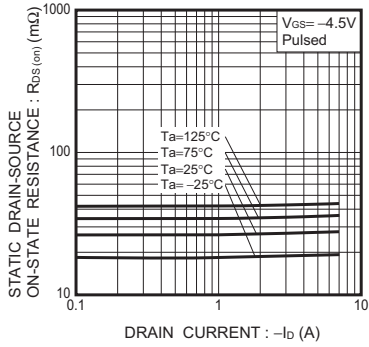


Fig.4 Static Drain-Source On-State vs. Drain Current

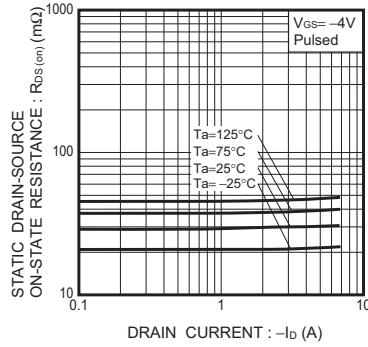


Fig.5 Static Drain-Source On-State vs. Drain Current

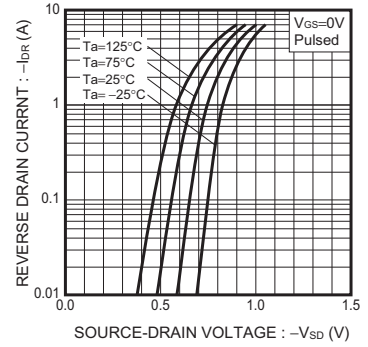


Fig.6 Reverse Drain Current Source-Drain Current

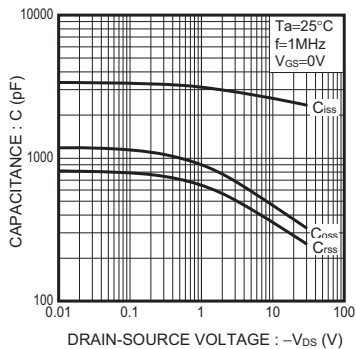


Fig.7 Typical Capacitance vs. Drain-Source Voltage

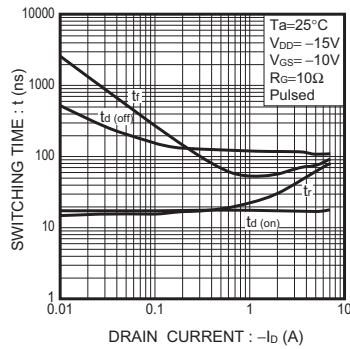


Fig.8 Switching Characteristics

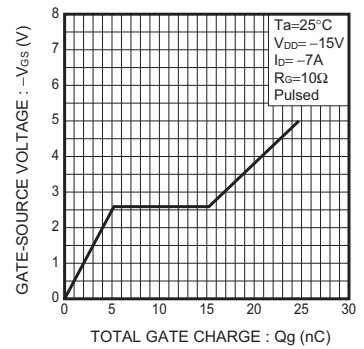


Fig.9 Dynamic Input Characteristics

Transistors

●Measurement circuits

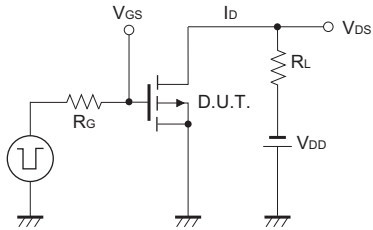


Fig.10 Switching Time Test Circuit

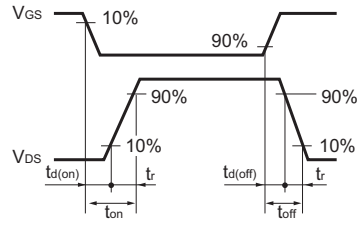


Fig.11 Switching Time Waveforms

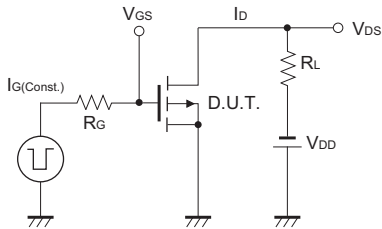


Fig.12 Gate Charge Test Circuit

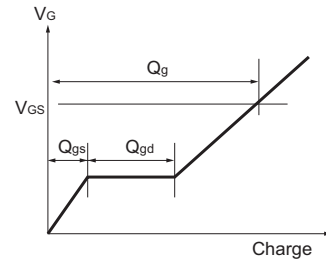


Fig.13 Gate Charge Waveform

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