



## CRYSTAL-LESS PCI-EXPRESS GEN1 DUAL OUTPUT CLOCK GENERATOR

### Features

- Crystal-less clock generator with integrated CMEMS
- PCI-Express Gen 1 compliant
- Two PCIe 100 MHz differential HCSL outputs
- One 25 MHz single-ended LVCMOS output
- Supports Serial (ATA) at 100 MHz
- Low power differential output buffers
- No termination resistors required for differential output clocks
- Triangular spread spectrum profile for maximum EMI reduction (Si50122-A2)
- Industrial Temperature -40 to 85 °C
- 2.5 V, 3.3 V Power supply
- Small package 10-pin TDFN (2.0 x 2.5 mm)
- Si50122-A1 does not support spread spectrum outputs
- Si50122-A2 supports 0.5% down spread outputs

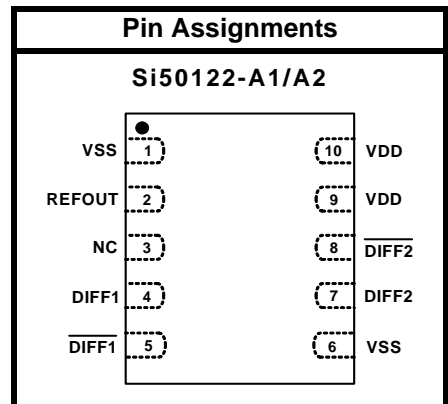


### Applications

- Network Attached Storage
- Multi-function Printer
- Digital TV
- Set top box
- Solid State Drives (SSD)
- Wireless Access Point
- Home Gateway
- Digital Video Camera

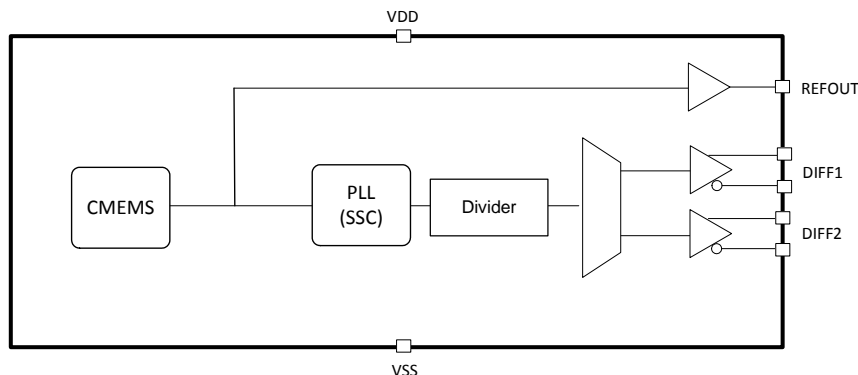
### Description

Si50122-A1/A2 is a high-performance, crystal-less PCIe clock generator that can generate two 100 MHz PCIe clock and one 25 MHz LVCMOS clock outputs. The differential clock outputs are compliant to PCIe Gen1 specifications. The ultra-small footprint (2.0 x 2.5 mm) and industry leading low-power consumption makes Si50122-A1/A2 the ideal clock solution for consumer and embedded applications where board space is limited and low power is needed.



Patents pending

### Functional Block Diagram





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# Si50122-A1/A2

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## 1. Electrical Specifications

**Table 1. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage (3.3 V Supply)	$V_{DD}$	$3.3\text{ V} \pm 10\%$	2.97	3.3	3.63	V
Supply Voltage (2.5 V Supply)	$V_{DD}$	$2.5\text{ V} \pm 10\%$	2.25	2.5	2.75	V

**Table 2. DC Electrical Specifications**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage ( $V_{DD} = 3.3\text{ V}$ )	$V_{DD}$	$3.3\text{ V} \pm 10\%$	2.97	3.30	3.63	V
Operating Voltage ( $V_{DD} = 2.5\text{ V}$ )	$V_{DD}$	$2.5\text{ V} \pm 10\%$	2.25	2.5	2.75	V
Operating Supply Current	$I_{DD}$	Full Active; $3.3\text{ V} \pm 10\%$	—	20	23	mA
		Full Active; $2.5\text{ V} \pm 10\%$	—	18	21	mA
Input Pin Capacitance	$C_{IN}$	Input Pin Capacitance	—	3	5	pF
Output Pin Capacitance	$C_{OUT}$	Output Pin Capacitance	—	—	5	pF

Table 3. AC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>DIFF Clocks</b>						
Duty Cycle	$T_{DC}$	Measured at 0 V differential	45	—	55	%
Skew	$T_{SKEW}$	Measured at 0 V differential	—	—	100	ps
Output Frequency	$F_{OUT}$	$V_{DD} = 3.3 V$	—	100	—	MHz
Frequency Accuracy	$F_{ACC}$	All output clocks	—	—	100	ppm
Slew rate	$t_{r/f2}$	Measured differentially from $\pm 150 mV$	0.6	—	5.0	V/ns
PCIe Gen1 Pk-Pk Jitter	$Pk-Pk_{GEN1}$	PCIe Gen 1, $V_{DD} = 3.3 V \pm 10\%$	—	20.7	35	ps
PCIe Gen1 Pk-Pk Jitter	$Pk-Pk_{GEN1}$	PCIe Gen 1, $V_{DD} = 2.5 V \pm 10\%$	—	25	40	ps
Crossing Point Voltage at 0.7 V Swing	$V_{OX}$		300	—	550	mV
Voltage High	$V_{HIGH}$		—	—	1.15	V
Voltage Low	$V_{LOW}$		-0.3	—	—	V
Spread Range	$S_{RNG}$	Down Spread, -A2 only	—	—	-0.5	%
Modulation Frequency	$F_{MOD}$	-A2 only	30	31.5	33	kHz
<b>25 MHz at 3.3 V</b>						
Duty Cycle	$T_{DC}$	Measurement at 1.5 V	45	—	55	%
Output Rise Time	$t_r$	$C_L = 10 pF$ , 20% to 80%	—	1.2	3.0	ns
Output Fall Time	$t_f$	$C_L = 10 pF$ , 20% to 80%	—	1.2	3.0	ns
Cycle to Cycle Jitter	$T_{CCJ}$	Measurement at 1.5 V	—	—	250	ps
Long Term Accuracy	$L_{ACC}$	Measured at 1.5 V	—	—	100	ppm
<b>Powerup Time</b>						
Clock Stabilization from Powerup	$T_{STABLE}$	First power up to first output	—	—	10	ms
<b>*Note:</b> Visit <a href="http://www.pcisig.com">www.pcisig.com</a> for complete PCIe specifications.						

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**Table 4. Thermal Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature, Storage	$T_S$	Non-functional	-65		150	°C
Temperature, Operating Ambient	$T_A$	Functional	-40		85	°C
Temperature, Junction	$T_J$	Functional	—		150	°C
Dissipation, Junction to Case	$\theta_{JC}$	JEDEC (JESD 51)	—		38.3	°C/W
Dissipation, Junction to Ambient	$\theta_{JA}$	JEDEC (JESD 51)	—		90.4	°C/W

**Table 5. Absolute Maximum Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main Supply Voltage	$V_{DD\_3.3V}$		—		4.6	V
Input Voltage	$V_{IN}$	Relative to $V_{SS}$	-0.5		4.6	$V_{DC}$
ESD Protection (Human Body Model)	$ESD_{HBM}$	JEDEC (JESD 22 - A114)	2000		—	V
Flammability Rating	UL-94	UL (Class)	V-0			

**Note:** While using multiple power supplies, the voltage on any input or I/O pin cannot exceed the power pin during powerup. Power supply sequencing is *not* required.

## 2. Test and Measurement Setup

Figure 1–Figure 3 show the test load configuration for the differential clock signals.

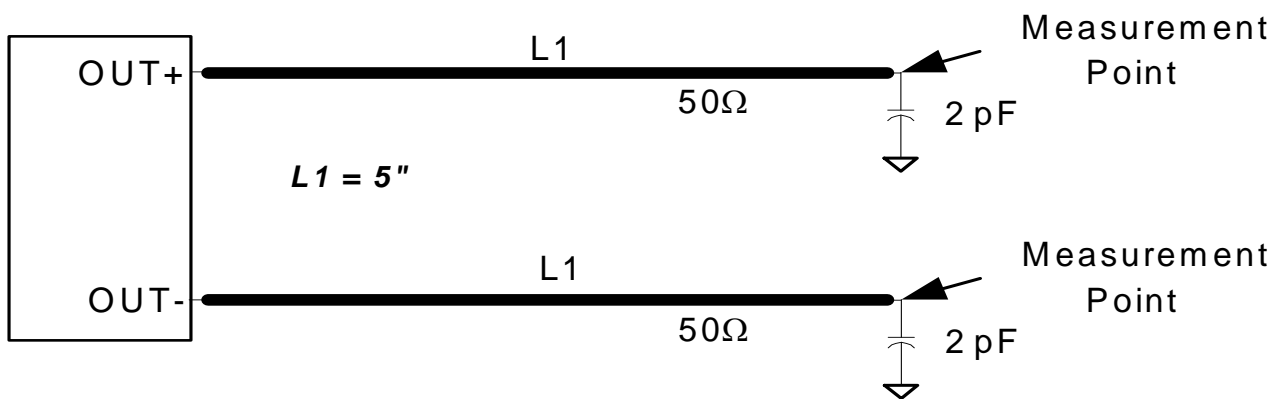


Figure 1. 0.7 V Differential Load Configuration

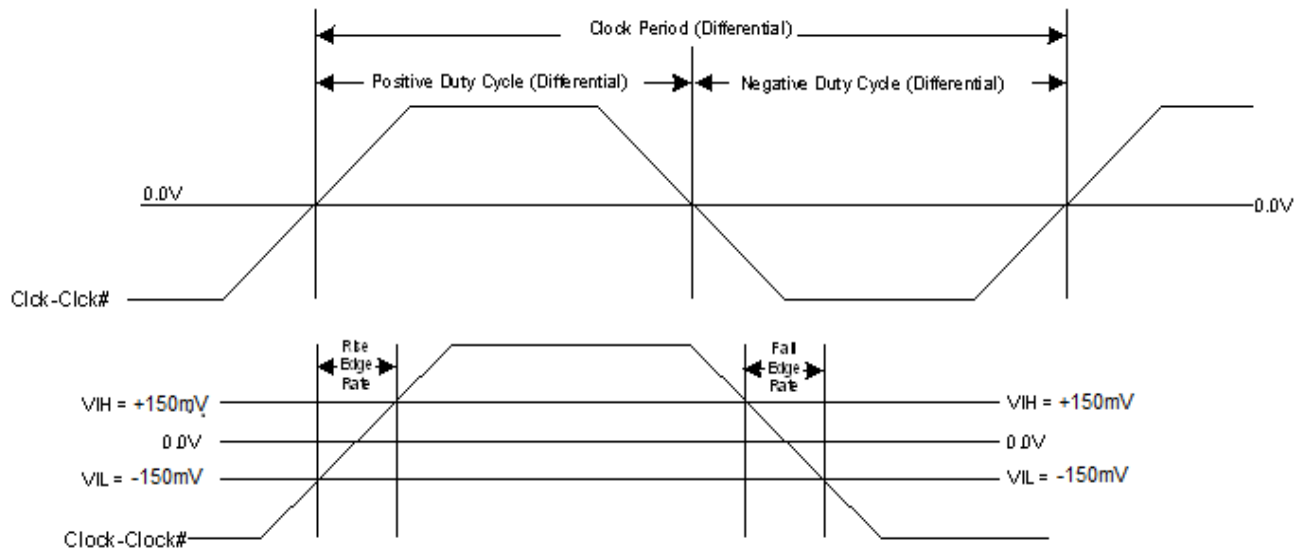
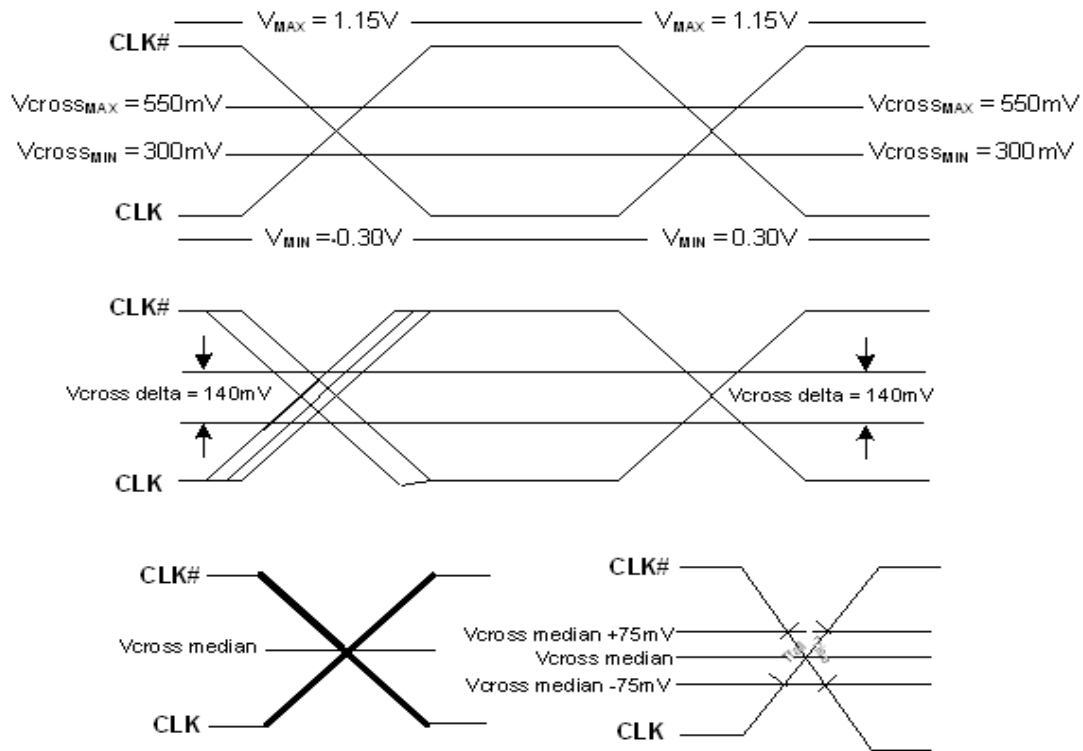
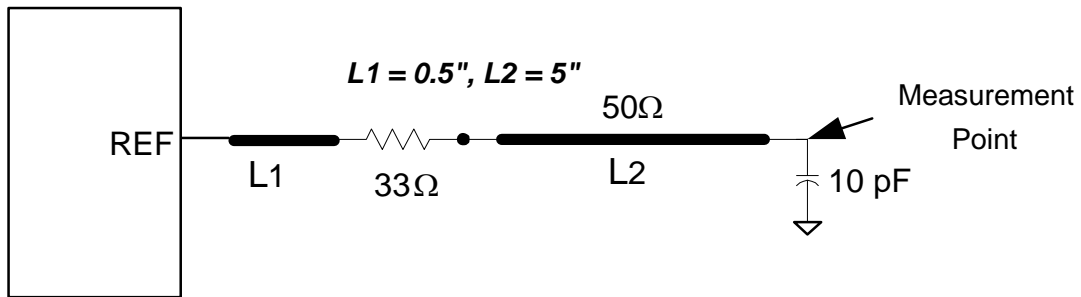


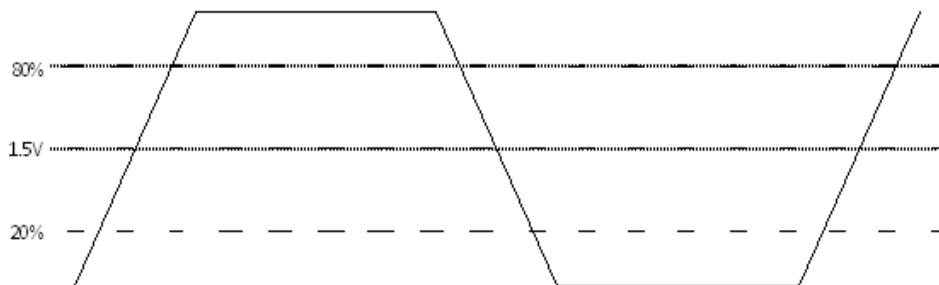
Figure 2. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)



**Figure 3. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)**



**Figure 4. Single-ended Clocks with Single Load Configuration**



**Figure 5. Single-ended Output Signal (for AC Parameter Measurement)**

### 3. Pin Descriptions

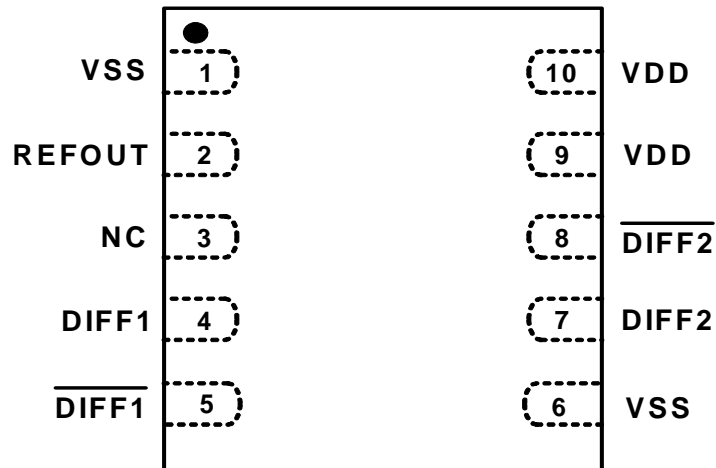


Figure 6. 10-Pin TDFN

Table 6. Si50122-Ax-GM 10-Pin TDFN Descriptions

Pin #	Name	Type	Description
1	VSS	GND	Connect to Ground
2	REFOUT	O, SE	25 MHz LVCMOS clock output
3	NC	NC	No Connect; do not connect this pin to anything.
4	DIFF1	O, DIF	0.7 V, 100 MHz differential clock output
5	$\overline{\text{DIFF1}}$	O, DIF	0.7 V, 100 MHz differential clock output
6	VSS	GND	Connect to Ground
7	DIFF2	O, DIF	0.7 V, 100 MHz differential clock output
8	$\overline{\text{DIFF2}}$	O, DIF	0.7 V, 100 MHz differential clock output
9	V <sub>DD</sub>	PWR	Power supply
10	V <sub>DD</sub>	PWR	Power supply

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## 4. Ordering Guide

Part Number	Spread Option	Package Type	Temperature
Si50122-A1-GM	No Spread	10-pin TDFN	Industrial, -40 to 85 °C
Si50122-A1-GMR	No Spread	10-pin TDFN—Tape and Reel	Industrial, -40 to 85 °C
Si50122-A2-GM	-0.5% Spread	10-pin TDFN	Industrial, -40 to 85 °C
Si50122-A2-GMR	-0.5% Spread	10-pin TDFN—Tape and Reel	Industrial, -40 to 85 °C

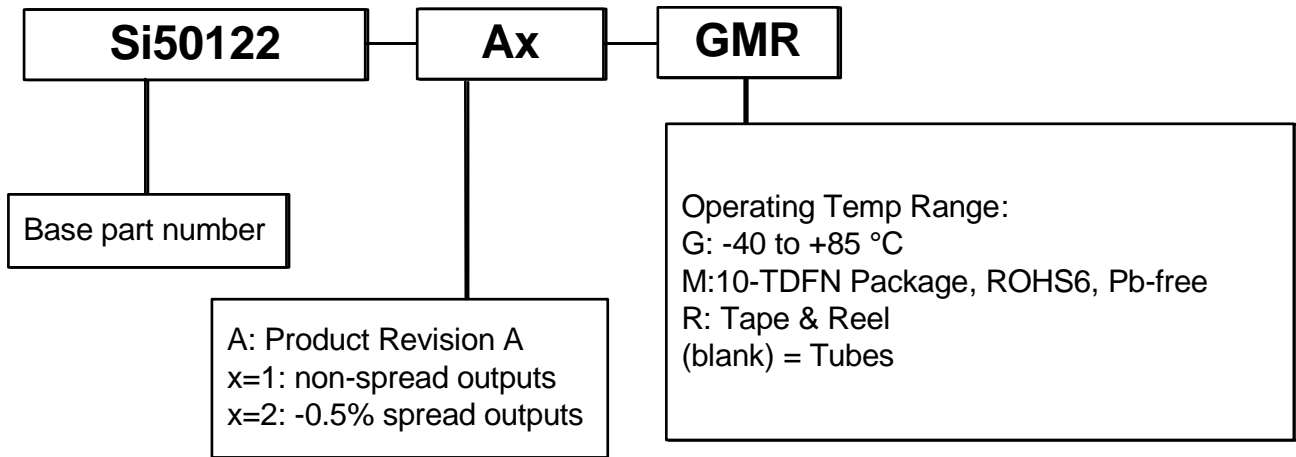


Figure 7. Ordering Information

5. Package Outlines

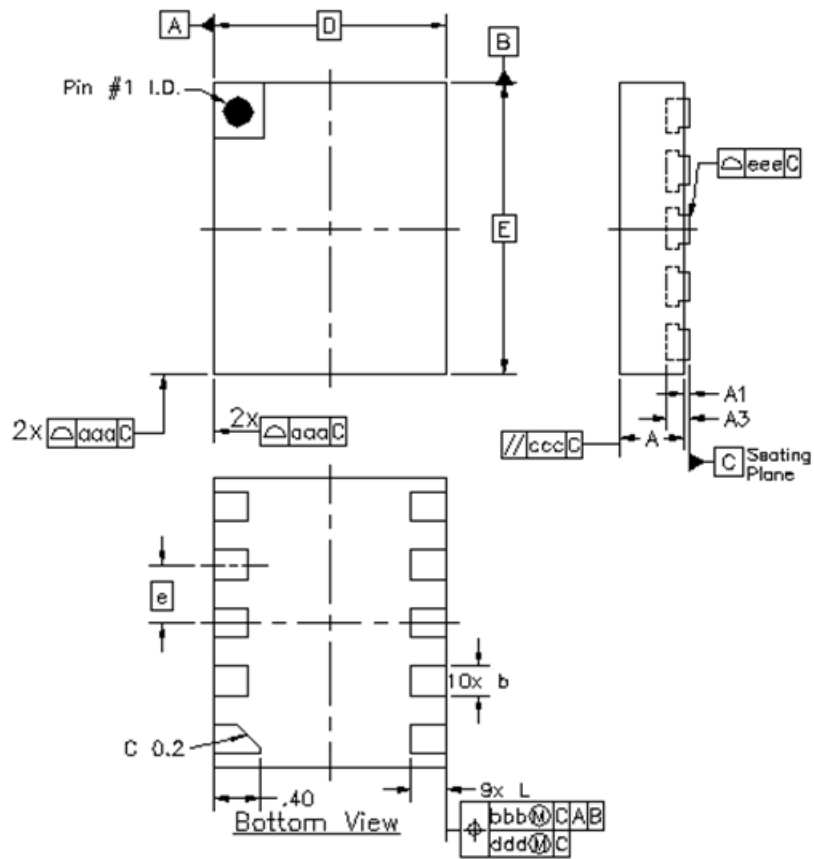
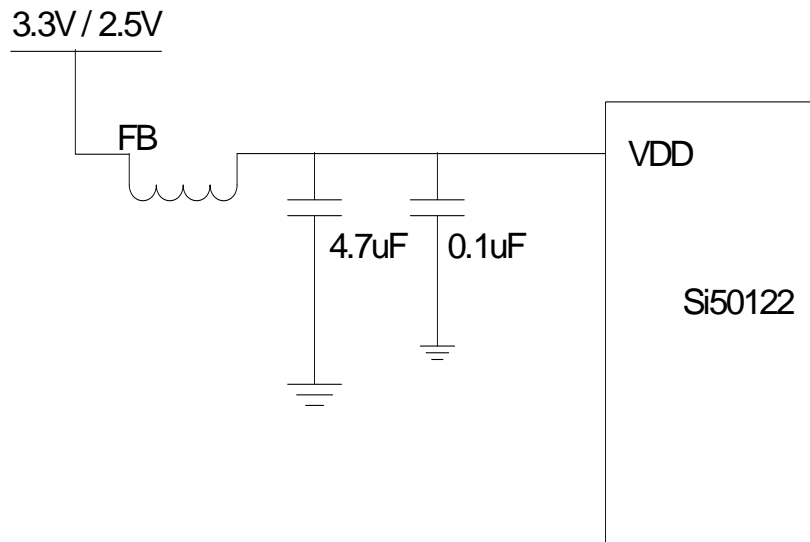


Figure 8. 10-Pin TDFN Package Drawing

**Table 7. Package Diagram Dimensions**

Symbol	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	—	0.05
A3	0.203 REF.		
b	0.20	0.25	0.30
D	2.00 BSC.		
e	0.50 BSC		
E	2.50 BSC.		
L	0.35	0.4	0.45
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
<b>Notes:</b>			
1. All dimensions shown are in millimeters (mm) unless otherwise noted.			
2. Dimensioning and Tolerances per ANSI Y14.5M-1994.			
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.			
4. This drawing conforms to the JEDEC Solid State Outline MO-229.			

## 6. Recommended Design Guideline



**Figure 9. Recommended Application Schematic**

**Note:** FB Specifications: DC resistance 0.1–0.3  $\Omega$ , Impedance at 100 MHz  $\geq$  1000  $\Omega$ .



## ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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