



**THE DATASHEET OF
CY2305SC-1H**



Low-Cost 3.3V Zero Delay Buffer

Features

- 10 MHz to 100-/133 MHz operating range, compatible with CPU and PCI bus frequencies
- Zero input-output propagation delay
- 60 ps typical cycle-to-cycle jitter (high drive)
- Multiple low-skew outputs
 - 85 ps typical output-to-output skew
 - One input drives five outputs (CY2305)
 - One input drives nine outputs, grouped as 4 + 4 + 1 (CY2309)
- Compatible with Pentium-based systems
- Test Mode to bypass phase-locked loop (PLL) (CY2309 only [see "Select Input Decoding" on page 3])
- Available in space-saving 16-pin 150-mil SOIC or 4.4-mm TSSOP packages (CY2309), and 8-pin, 150-mil SOIC package (CY2305)
- 3.3V operation
- Industrial temperature available

Functional Description

The CY2309 is a low-cost 3.3V zero delay buffer designed to distribute high-speed clocks and is available in a 16-pin SOIC or TSSOP package. The CY2305 is an 8-pin version of the CY2309. It accepts one reference input, and drives out five low-skew clocks. The -1H versions of each device operate at up to 100-/133 MHz frequencies, and have higher drive than the -1 devices. All parts have on-chip PLLs which lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

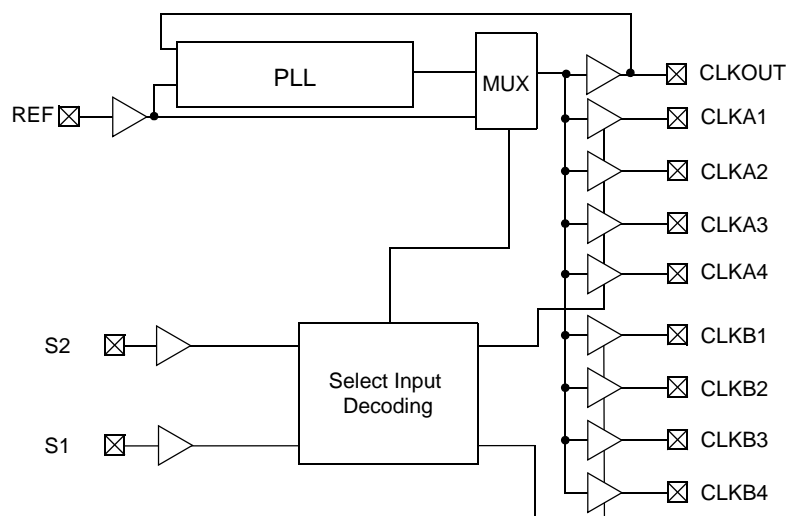
The CY2309 has two banks of four outputs each, which can be controlled by the Select inputs as shown in the "Select Input Decoding" table on page 3. If all output clocks are not required, BankB can be three-stated. The select inputs also allow the input clock to be directly applied to the outputs for chip and system testing purposes.

The CY2305 and CY2309 PLLs enter a power down mode when there are no rising edges on the REF input. In this state, the outputs are three-stated and the PLL is turned off, resulting in less than 25.0 μ A current draw for these parts. The CY2309 PLL shuts down in one additional case as shown in the table below.

Multiple CY2305 and CY2309 devices can accept the same input clock and distribute it. In this case, the skew between the outputs of two devices is guaranteed to be less than 700 ps.

The CY2305/CY2309 is available in two/three different configurations, as shown in the ordering information (page 10). The CY2305-1/CY2309-1 is the base part. The CY2305-1H/CY2309-1H is the high-drive version of the -1, and its rise and fall times are much faster than the -1s.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - CY2305

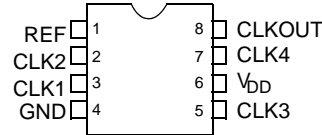


Table 1. Pin Description for CY2305

| Pin | Signal | Description |
|-----|-----------------------|--|
| 1 | REF ^[1] | Input reference frequency, 5V-tolerant input |
| 2 | CLK2 ^[2] | Buffered clock output |
| 3 | CLK1 ^[2] | Buffered clock output |
| 4 | GND | Ground |
| 5 | CLK3 ^[2] | Buffered clock output |
| 6 | V _{DD} | 3.3V supply |
| 7 | CLK4 ^[2] | Buffered clock output |
| 8 | CLKOUT ^[2] | Buffered clock output, internal feedback on this pin |

Figure 2. Pin Diagram - CY2309

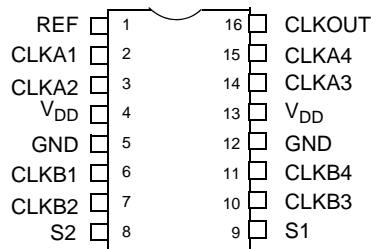


Table 2. Pin Description for CY2309

| Pin | Signal | Description |
|-----|----------------------|--|
| 1 | REF ^[1] | Input reference frequency, 5V-tolerant input |
| 2 | CLKA1 ^[2] | Buffered clock output, Bank A |
| 3 | CLKA2 ^[2] | Buffered clock output, Bank A |
| 4 | V _{DD} | 3.3V supply |
| 5 | GND | Ground |
| 6 | CLKB1 ^[2] | Buffered clock output, Bank B |
| 7 | CLKB2 ^[2] | Buffered clock output, Bank B |
| 8 | S2 ^[3] | Select input, bit 2 |
| 9 | S1 ^[3] | Select input, bit 1 |
| 10 | CLKB3 ^[2] | Buffered clock output, Bank B |
| 11 | CLKB4 ^[2] | Buffered clock output, Bank B |
| 12 | GND | Ground |

Notes

1. Weak pull down.
2. Weak pull down on all outputs.
3. Weak pull ups on these inputs.

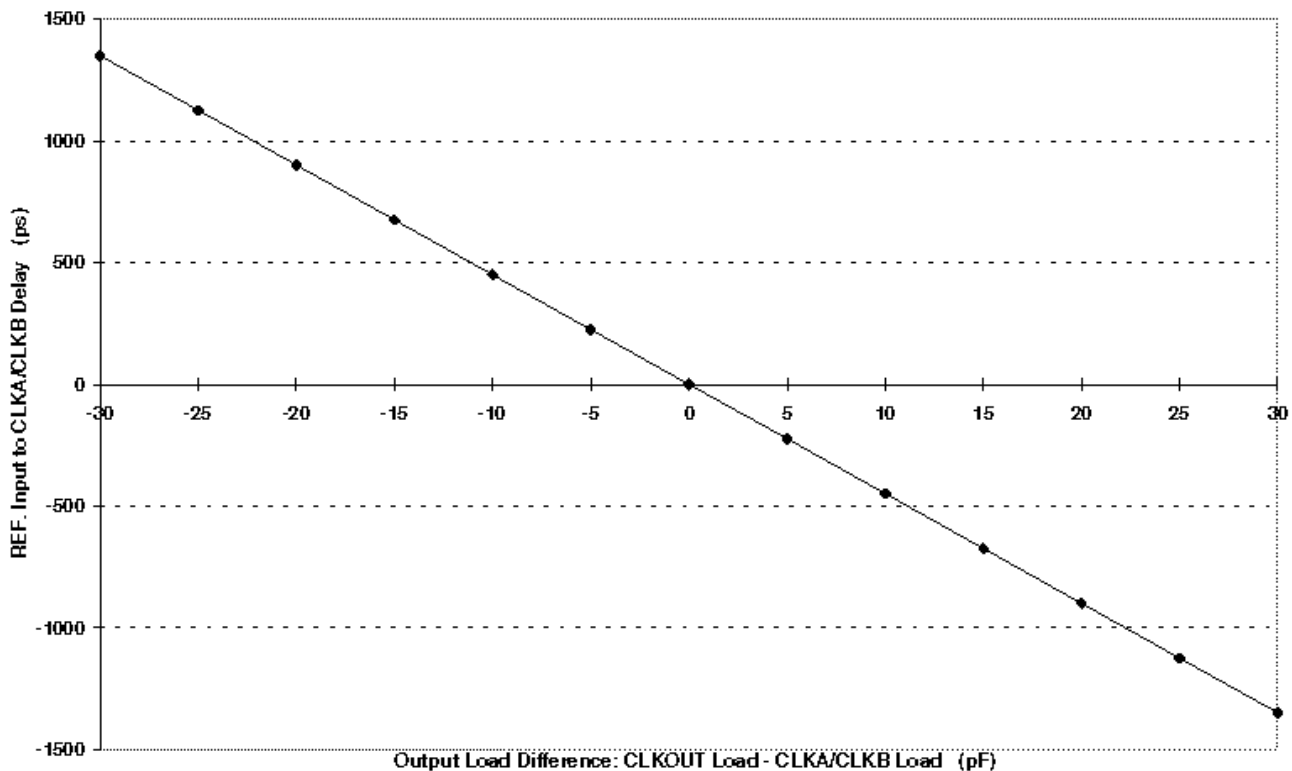
Table 2. Pin Description for CY2309

| Pin | Signal | Description |
|-----|-----------------------|--|
| 13 | V _{DD} | 3.3V supply |
| 14 | CLKA3 ^[2] | Buffered clock output, Bank A |
| 15 | CLKA4 ^[2] | Buffered clock output, Bank A |
| 16 | CLKOUT ^[2] | Buffered output, internal feedback on this pin |

Select Input Decoding for CY2309

| S2 | S1 | CLOCK A1–A4 | CLOCK B1–B4 | CLKOUT ^[4] | Output Source | PLL Shutdown |
|----|----|-------------|-------------|-----------------------|---------------|--------------|
| 0 | 0 | Three-state | Three-state | Driven | PLL | N |
| 0 | 1 | Driven | Three-state | Driven | PLL | N |
| 1 | 0 | Driven | Driven | Driven | Reference | Y |
| 1 | 1 | Driven | Driven | Driven | PLL | N |

Figure 3. REF. Input to CLKA/CLKB Delay vs. Loading Difference between CLKOUT and CLKA/CLKB Pins



Zero Delay and Skew Control

All outputs must be uniformly loaded to achieve Zero Delay between the input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay. This is shown in the above graph.

For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load, equal to that on other outputs, for obtaining zero input-output delay. If input to output delay adjustments are required, use the above graph to calculate loading differences between the CLKOUT pin and other outputs.

For zero output-output skew, be sure to load all outputs equally. For further information refer to the application note entitled “CY2305 and CY2309 as PCI and SDRAM Buffers.”

Notes

- This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

Absolute Maximum Conditions

| | | | |
|---|--------------------------|--------------------------------------|----------|
| Supply Voltage to Ground Potential..... | -0.5V to +7.0V | Junction Temperature..... | 150°C |
| DC Input Voltage (Except REF) | -0.5V to $V_{DD} + 0.5V$ | Static Discharge Voltage | |
| DC Input Voltage REF | -0.5V to 7V | (per MIL-STD-883, Method 3015) | > 2,000V |
| Storage Temperature | -65°C to +150°C | | |

Operating Conditions for CY2305SC-XX and CY2309SC-XX Commercial Temperature Devices

| Parameter | Description | Min | Max | Unit |
|-----------|---|------|-----|------|
| V_{DD} | Supply Voltage | 3.0 | 3.6 | V |
| T_A | Operating Temperature (Ambient Temperature) | 0 | 70 | °C |
| C_L | Load Capacitance, below 100 MHz | - | 30 | pF |
| C_L | Load Capacitance, from 100 MHz to 133 MHz | - | 10 | pF |
| C_{IN} | Input Capacitance | - | 7 | pF |
| t_{PU} | Power up time for all V_{DD} s to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | 50 | ms |

Electrical Characteristics for CY2305SC-XX and CY2309SC-XX Commercial Temperature Devices

| Parameter | Description | Test Conditions | Min | Max | Unit |
|--------------------|------------------------------------|--|-----|-------|------|
| V_{IL} | Input LOW Voltage ^[5] | | - | 0.8 | V |
| V_{IH} | Input HIGH Voltage ^[5] | | 2.0 | - | V |
| I_{IL} | Input LOW Current | $V_{IN} = 0V$ | - | 50.0 | μA |
| I_{IH} | Input HIGH Current | $V_{IN} = V_{DD}$ | - | 100.0 | μA |
| V_{OL} | Output LOW Voltage ^[6] | $I_{OL} = 8\text{ mA} (-1)$ $I_{OH} = 12\text{ mA} (-1H)$ | - | 0.4 | V |
| V_{OH} | Output HIGH Voltage ^[6] | $I_{OH} = -8\text{ mA} (-1)$ $I_{OL} = -12\text{ mA} (-1H)$ | 2.4 | - | V |
| I_{DD} (PD mode) | Power Down Supply Current | REF = 0 MHz | - | 25.0 | μA |
| I_{DD} | Supply Current | Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD} | - | 32.0 | mA |

Switching Characteristics for CY2305SC-1 and CY2309SC-1 Commercial Temperature Devices

| Parameter ^[7] | Name | Test Conditions | Min | Typ. | Max | Unit |
|--------------------------|---|---|----------|------|---------------|------------|
| t_1 | Output Frequency | 30-pF load 10 pF load | 10 10 | - | 100 133.33 | MHz MHz |
| t_{DC} | Duty Cycle ^[6] = $t_2 \div t_1$ | Measured at 1.4V, $F_{out} = 66.67$ MHz | 40.0 | 50.0 | 60.0 | % |
| t_3 | Rise Time ^[6] | Measured between 0.8V and 2.0V | - | - | 2.50 | ns |
| t_4 | Fall Time ^[6] | Measured between 0.8V and 2.0V | - | - | 2.50 | ns |
| t_5 | Output to Output Skew ^[6] | All outputs equally loaded | - | 85 | 250 | ps |
| t_{6A} | Delay, REF Rising Edge to CLKOUT Rising Edge ^[6] | Measured at $V_{DD}/2$ | - | 0 | ±350 | ps |

Notes

- 5. REF input has a threshold voltage of $V_{DD}/2$.
- 6. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics for CY2305SC-1 and CY2309SC-1 Commercial Temperature Devices

| Parameter ^[7] | Name | Test Conditions | Min | Typ. | Max | Unit |
|--------------------------|---|--|-----|------|-----|------|
| t _{6B} | Delay, REF Rising Edge to CLKOUT Rising Edge ^[6] | Measured at V _{DD} /2. Measured in PLL Bypass Mode, CY2309 device only. | 1 | 5 | 8.7 | ns |
| t ₇ | Device to Device Skew ^[6] | Measured at V _{DD} /2 on the CLKOUT pins of devices | – | – | 700 | ps |
| t _J | Cycle to Cycle Jitter ^[6] | Measured at 66.67 MHz, loaded outputs | – | 70 | 200 | ps |
| t _{LOCK} | PLL Lock Time ^[6] | Stable power supply, valid clock presented on REF pin | – | – | 1.0 | ms |

Switching Characteristics for CY2305SC-1H and CY2309SC-1H Commercial Temperature Devices

| Parameter ^[7] | Name | Description | Min | Typ. | Max | Unit |
|--------------------------|---|--|----------|------|---------------|------------|
| t ₁ | Output Frequency | 30 pF load 10 pF load | 10 10 | – | 100 133.33 | MHz MHz |
| t _{DC} | Duty Cycle ^[6] = t ₂ ÷ t ₁ | Measured at 1.4V, F _{out} = 66.67 MHz | 40.0 | 50.0 | 60.0 | % |
| t ₃ | Rise Time ^[6] | Measured between 0.8V and 2.0V | – | – | 1.50 | ns |
| t ₄ | Fall Time ^[6] | Measured between 0.8V and 2.0V | – | – | 1.50 | ns |
| t ₅ | Output to Output Skew ^[6] | All outputs equally loaded | – | 85 | 250 | ps |
| t _{6A} | Delay, REF Rising Edge to CLKOUT Rising Edge ^[6] | Measured at V _{DD} /2 | – | – | ±350 | ps |
| t _{6B} | Delay, REF Rising Edge to CLKOUT Rising Edge ^[6] | Measured at V _{DD} /2. Measured in PLL Bypass Mode, CY2309 device only. | 1 | 5 | 8.7 | ns |
| t ₇ | Device to Device Skew ^[6] | Measured at V _{DD} /2 on the CLKOUT pins of devices | – | – | 700 | ps |
| t ₈ | Output Slew Rate ^[6] | Measured between 0.8V and 2.0V using Test Circuit #2 | 1 | – | | V/ns |
| t _J | Cycle to Cycle Jitter ^[6] | Measured at 66.67 MHz, loaded outputs | – | 60 | 200 | ps |
| t _{LOCK} | PLL Lock Time ^[6] | Stable power supply, valid clock presented on REF pin | – | – | 1.0 | ms |

Operating Conditions for CY2305SI-XX and CY2309SI-XX Industrial Temperature Devices

| Parameter | Description | Min | Max | Unit |
|-----------------|---|-----|-----|------|
| V _{DD} | Supply Voltage | 3.0 | 3.6 | V |
| T _A | Operating Temperature (Ambient Temperature) | –40 | 85 | °C |
| C _L | Load Capacitance, below 100 MHz | – | 30 | pF |
| C _L | Load Capacitance, from 100 MHz to 133 MHz | – | 10 | pF |
| C _{IN} | Input Capacitance | – | 7 | pF |

Note

7. All parameters specified with loaded outputs.

Electrical Characteristics for CY2305SI-XX and CY2309SI-XX Industrial Temperature Devices

| Parameter | Description | Test Conditions | Min | Max | Unit |
|---------------------------|------------------------------------|--|-----|-------|------|
| V _{IL} | Input LOW Voltage ^[5] | | – | 0.8 | V |
| V _{IH} | Input HIGH Voltage ^[5] | | 2.0 | – | V |
| I _{IL} | Input LOW Current | V _{IN} = 0V | – | 50.0 | μA |
| I _{IH} | Input HIGH Current | V _{IN} = V _{DD} | – | 100.0 | μA |
| V _{OL} | Output LOW Voltage ^[6] | I _{OL} = 8 mA (–1) I _{OH} = 12 mA (–1H) | – | 0.4 | V |
| V _{OH} | Output HIGH Voltage ^[6] | I _{OH} = –8 mA (–1) I _{OL} = –12 mA (–1H) | 2.4 | – | V |
| I _{DD} (PD mode) | Power down Supply Current | REF = 0 MHz | – | 25.0 | μA |
| I _{DD} | Supply Current | Unloaded outputs at 66.67 MHz, SEL inputs at V _{DD} | – | 35.0 | mA |

Switching Characteristics for CY2305SI-1 and CY2309SI-1 Industrial Temperature Devices

| Parameter ^[7] | Name | Test Conditions | Min | Typ. | Max | Unit |
|--------------------------|---|--|----------|------|---------------|------------|
| t ₁ | Output Frequency | 30 pF load 10 pF load | 10 10 | – | 100 133.33 | MHz MHz |
| t _{DC} | Duty Cycle ^[6] = t ₂ ÷ t ₁ | Measured at 1.4V, F _{out} = 66.67 MHz | 40.0 | 50.0 | 60.0 | % |
| t ₃ | Rise Time ^[6] | Measured between 0.8V and 2.0V | – | – | 2.50 | ns |
| t ₄ | Fall Time ^[6] | Measured between 0.8V and 2.0V | – | – | 2.50 | ns |
| t ₅ | Output to Output Skew ^[6] | All outputs equally loaded | – | 85 | 250 | ps |
| t _{6A} | Delay, REF Rising Edge to CLKOUT Rising Edge ^[6] | Measured at V _{DD} /2 | – | – | ±350 | ps |
| t _{6B} | Delay, REF Rising Edge to CLKOUT Rising Edge ^[6] | Measured at V _{DD} /2. Measured in PLL Bypass Mode, CY2309 device only. | 1 | 5 | 8.7 | ns |
| t ₇ | Device to Device Skew ^[6] | Measured at V _{DD} /2 on the CLKOUT pins of devices | – | – | 700 | ps |
| t _J | Cycle to Cycle Jitter ^[6] | Measured at 66.67 MHz, loaded outputs | – | 70 | 200 | ps |
| t _{LOCK} | PLL Lock Time ^[6] | Stable power supply, valid clock presented on REF pin | – | – | 1.0 | ms |

Switching Characteristics for CY2305SI-1H and CY2309SI-1H Industrial Temperature Devices

| Parameter ^[7] | Name | Description | Min | Typ. | Max | Unit |
|--------------------------|---|--|----------|------|---------------|------------|
| t ₁ | Output Frequency | 30 pF load 10 pF load | 10 10 | – | 100 133.33 | MHz MHz |
| t _{DC} | Duty Cycle ^[6] = t ₂ ÷ t ₁ | Measured at 1.4V, F _{out} = 66.67 MHz | 40.0 | 50.0 | 60.0 | % |
| t ₃ | Rise Time ^[6] | Measured between 0.8V and 2.0V | – | – | 1.50 | ns |
| t ₄ | Fall Time ^[6] | Measured between 0.8V and 2.0V | – | – | 1.50 | ns |
| t ₅ | Output to Output Skew ^[6] | All outputs equally loaded | – | 85 | 250 | ps |
| t _{6A} | Delay, REF Rising Edge to CLKOUT Rising Edge ^[6] | Measured at V _{DD} /2 | – | – | ±350 | ps |
| t _{6B} | Delay, REF Rising Edge to CLKOUT Rising Edge ^[6] | Measured at V _{DD} /2. Measured in PLL Bypass Mode, CY2309 device only. | 1 | 5 | 8.7 | ns |
| t ₇ | Device to Device Skew ^[6] | Measured at V _{DD} /2 on the CLKOUT pins of devices | – | – | 700 | ps |

Switching Characteristics for CY2305SI-1H and CY2309SI-1H Industrial Temperature Devices

| Parameter ^[7] | Name | Description | Min | Typ. | Max | Unit |
|--------------------------|--------------------------------------|---|-----|------|-----|------|
| t_8 | Output Slew Rate ^[6] | Measured between 0.8V and 2.0V using Test Circuit #2 | 1 | – | – | V/ns |
| t_J | Cycle to Cycle Jitter ^[6] | Measured at 66.67 MHz, loaded outputs | – | 60 | 200 | ps |
| t_{LOCK} | PLL Lock Time ^[6] | Stable power supply, valid clock presented on REF pin | – | – | 1.0 | ms |

Switching Waveforms

Figure 4. Duty Cycle Timing

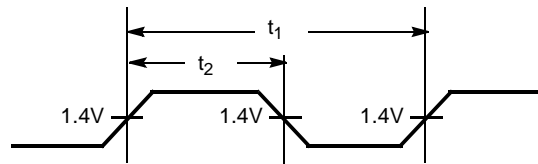


Figure 5. All Outputs Rise/Fall Time

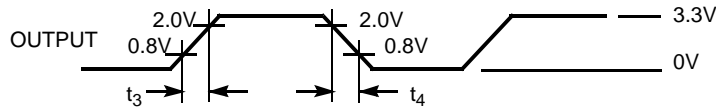


Figure 6. Output-Output Skew

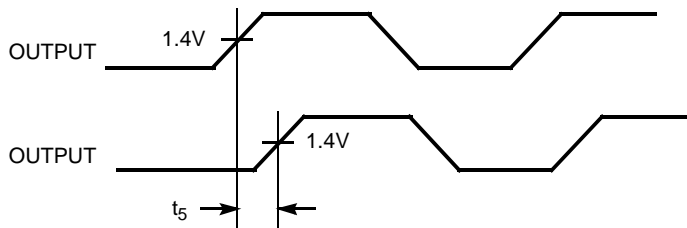


Figure 7. Input-Output Propagation Delay

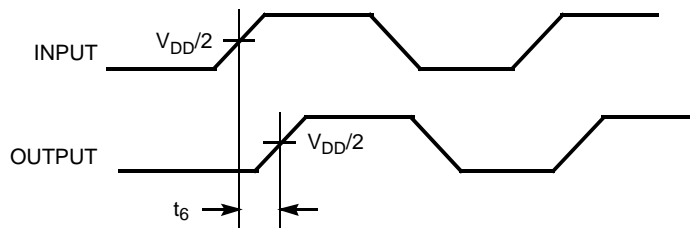
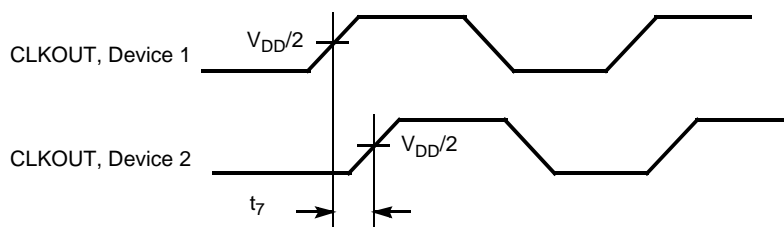
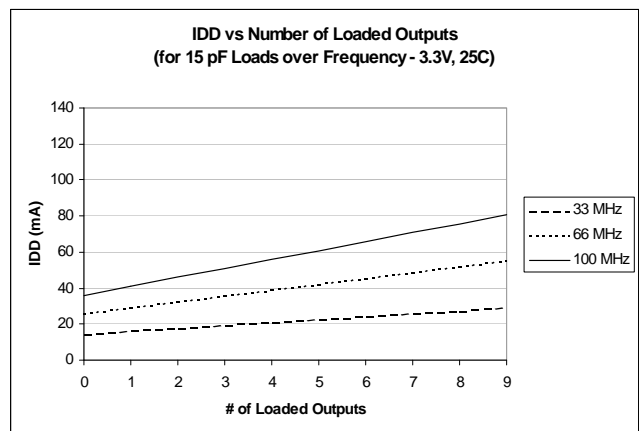
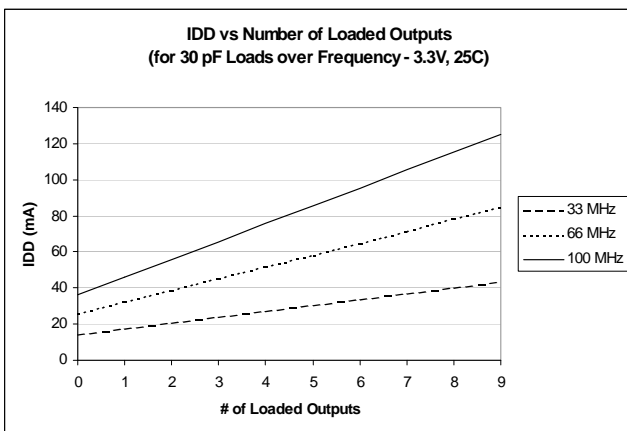
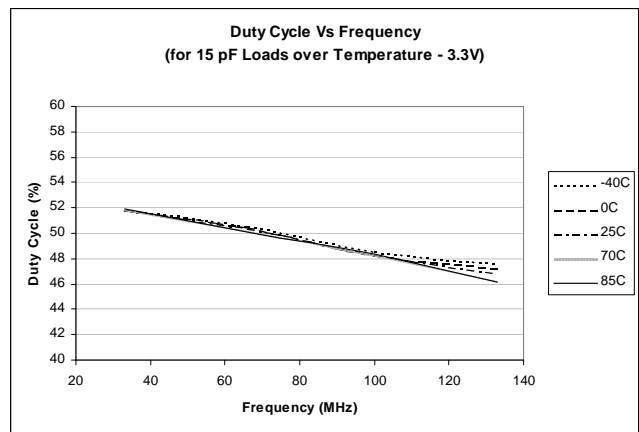
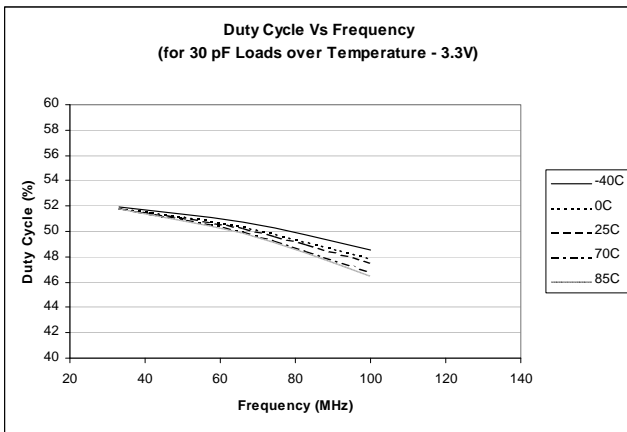
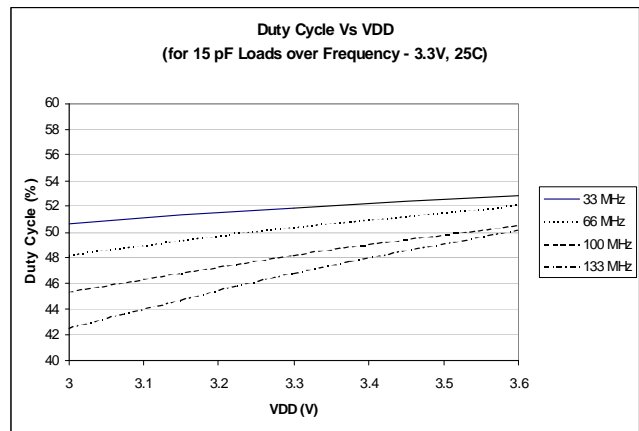
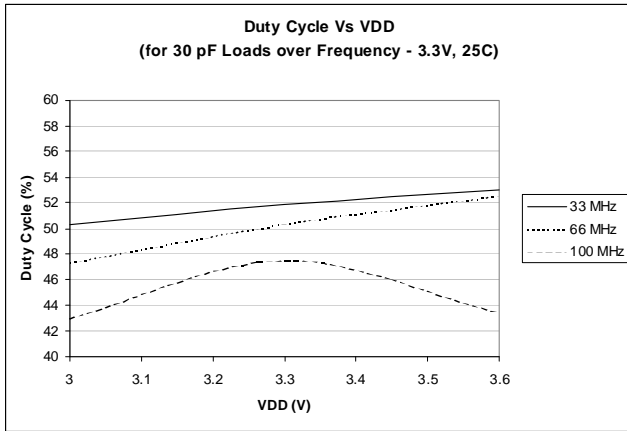


Figure 8. Device-Device Skew



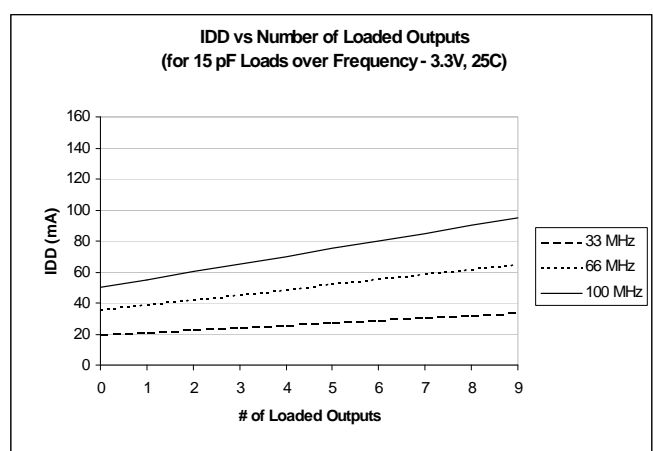
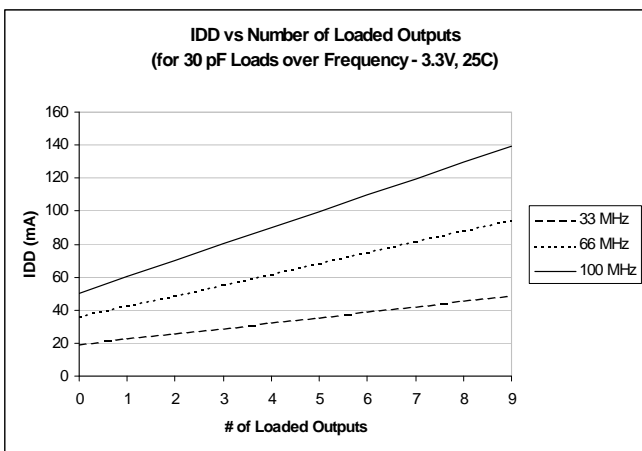
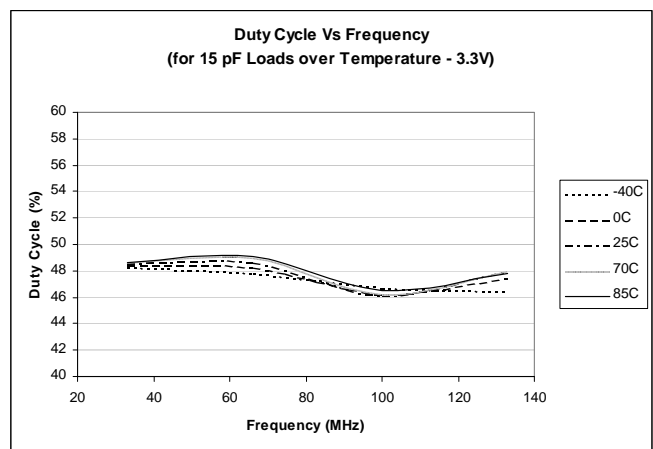
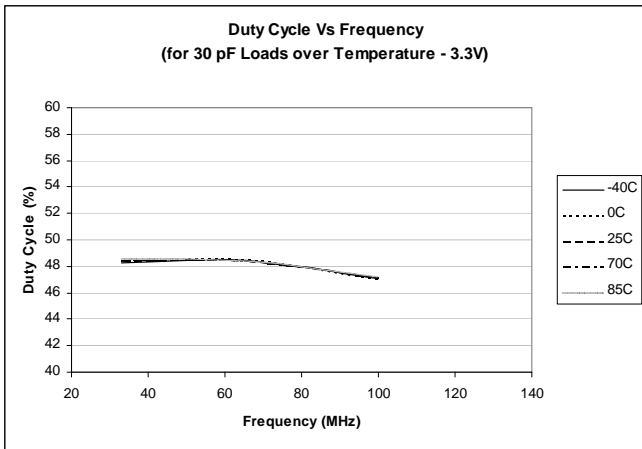
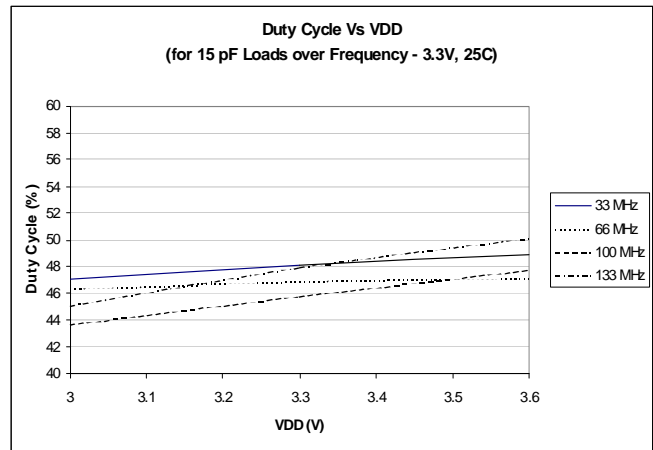
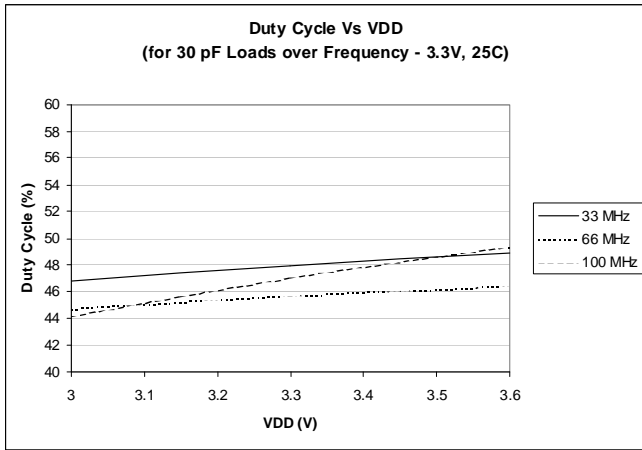
Typical Duty Cycle^[8] and I_{DD} Trends^[9] for CY2305-1 and CY2309-1



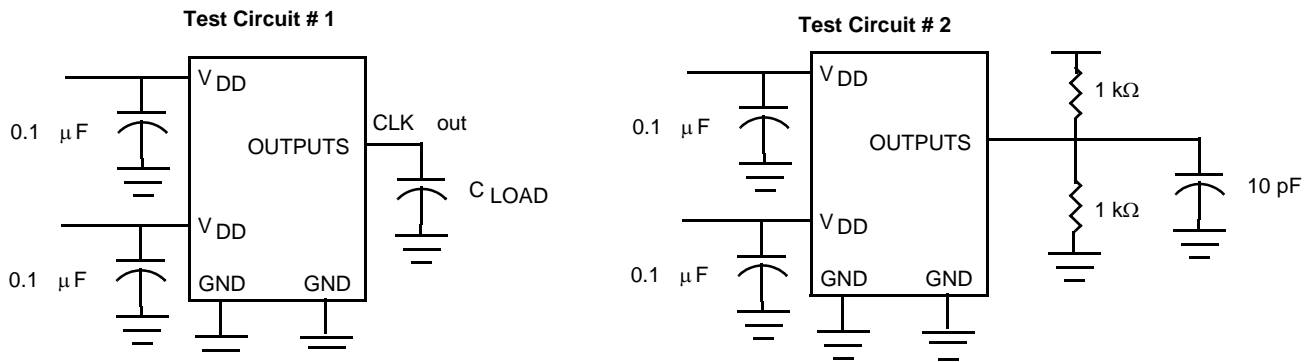
Notes

- 8. Duty Cycle is taken from typical chip measured at 1.4V.
- 9. I_{DD} data is calculated from $I_{DD} = I_{CORE} + nCVf$, where I_{CORE} is the unloaded current. (n = # of outputs; C = Capacitance load per output (F); V = Supply Voltage (V); f = frequency (Hz)).

Typical Duty Cycle^[8] and IDD Trends^[9] for CY2305-1H and CY2309-1H



Test Circuits



For parameter t_8 (output slew rate) on -1H devices

Ordering Information for CY2305

| Ordering Code | Package Type | Operating Range |
|------------------------------|------------------------------------|-----------------|
| CY2305SC-1 ^[10] | 8-pin 150-mil SOIC | Commercial |
| CY2305SC-1T ^[10] | 8-pin 150-mil SOIC – Tape and Reel | Commercial |
| CY2305SI-1 ^[10] | 8-pin 150-mil SOIC | Industrial |
| CY2305SI-1T ^[10] | 8-pin 150-mil SOIC – Tape and Reel | Industrial |
| CY2305SC-1H ^[10] | 8-pin 150-mil SOIC | Commercial |
| CY2305SC-1HT ^[10] | 8-pin 150-mil SOIC – Tape and Reel | Commercial |
| CY2305SI-1H ^[10] | 8-pin 150-mil SOIC | Industrial |
| CY2305SI-1HT ^[10] | 8-pin 150-mil SOIC – Tape and Reel | Industrial |
| Pb-Free | | |
| CY2305SXC-1 | 8-pin 150-mil SOIC | Commercial |
| CY2305SXC-1T | 8-pin 150-mil SOIC – Tape and Reel | Commercial |
| CY2305SXI-1 | 8-pin 150-mil SOIC | Industrial |
| CY2305SXI-1T | 8-pin 150-mil SOIC – Tape and Reel | Industrial |
| CY2305SXC-1H | 8-pin 150-mil SOIC | Commercial |
| CY2305SXC-1HT | 8-pin 150-mil SOIC – Tape and Reel | Commercial |
| CY2305SXI-1H | 8-pin 150-mil SOIC | Industrial |
| CY2305SXI-1HT | 8-pin 150-mil SOIC – Tape and Reel | Industrial |

Ordering Information for CY2309

| Ordering Code | Package Type | Operating Range |
|-----------------------------|-------------------------------------|-----------------|
| CY2309SC-1 ^[10] | 16-pin 150-mil SOIC | Commercial |
| CY2309SC-1T ^[10] | 16-pin 150-mil SOIC – Tape and Reel | Commercial |
| CY2309SI-1 ^[10] | 16-pin 150-mil SOIC | Industrial |
| CY2309SI-1T ^[10] | 16-pin 150-mil SOIC – Tape and Reel | Industrial |
| CY2309SC-1H ^[10] | 16-pin 150-mil SOIC | Commercial |

Note

10. Not recommended for new designs.

Ordering Information for CY2309 (continued)

| Ordering Code | Package Type | Operating Range |
|------------------------------|-------------------------------------|-----------------|
| CY2309SC-1HT ^[10] | 16-pin 150-mil SOIC – Tape and Reel | Commercial |
| CY2309ZC-1H ^[10] | 16-pin 4.4-mm TSSOP | Commercial |
| CY2309ZC-1HT ^[10] | 16-pin 4.4-mm TSSOP – Tape and Reel | Commercial |
| CY2309SI-1H ^[10] | 16-pin 150-mil SOIC | Industrial |
| CY2309SI-1HT ^[10] | 16-pin 150-mil SOIC – Tape and Reel | Industrial |
| Pb-Free | | |
| CY2309SXC-1 | 16-pin 150-mil SOIC | Commercial |
| CY2309SXC-1T | 16-pin 150-mil SOIC – Tape and Reel | Commercial |
| CY2309SXI-1 | 16-pin 150-mil SOIC | Industrial |
| CY2309SXI-1T | 16-pin 150-mil SOIC – Tape and Reel | Industrial |
| CY2309SXC-1H | 16-pin 150-mil SOIC | Commercial |
| CY2309SXC-1HT | 16-pin 150-mil SOIC – Tape and Reel | Commercial |
| CY2309SXI-1H | 16-pin 150-mil SOIC | Industrial |
| CY2309SXI-1HT | 16-pin 150-mil SOIC – Tape and Reel | Industrial |
| CY2309ZXC-1H | 16-pin 4.4-mm TSSOP | Commercial |
| CY2309ZXC-1HT | 16-pin 4.4-mm TSSOP – Tape and Reel | Commercial |
| CY2309ZXI-1H | 16-pin 4.4-mm TSSOP | Industrial |
| CY2309ZXI-1HT | 16-pin 4.4-mm TSSOP – Tape and Reel | Industrial |

Package Drawing and Dimensions

Figure 8. 8-Pin (150-Mil) SOIC S8

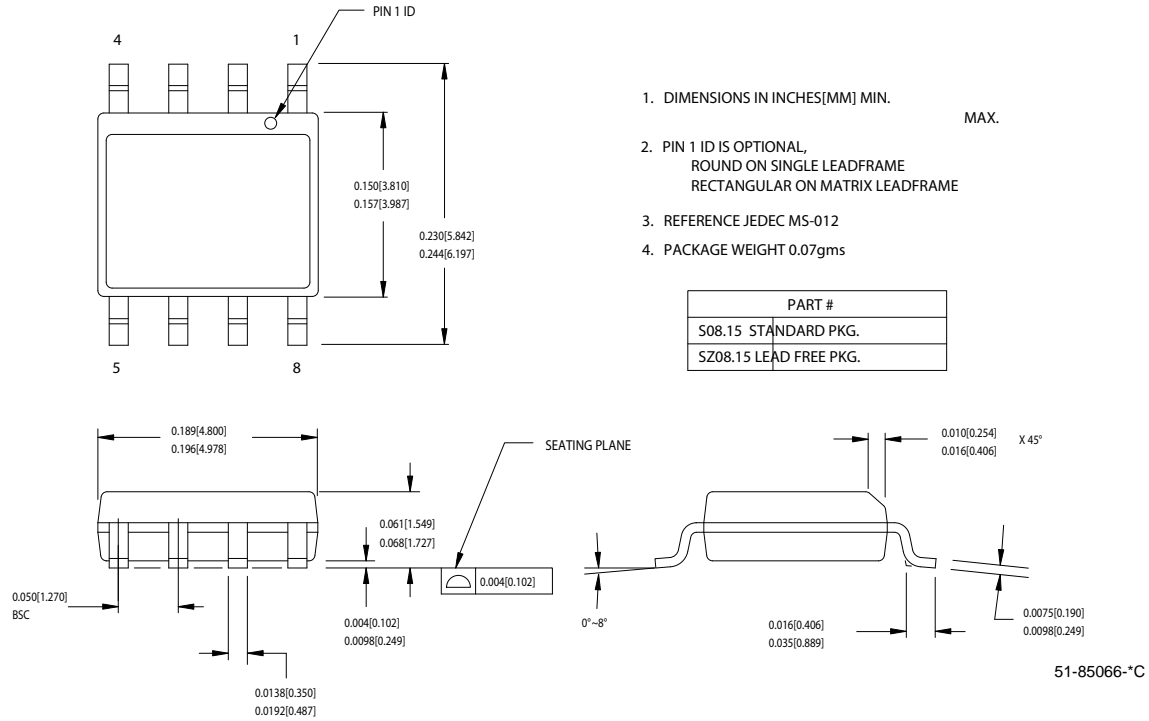
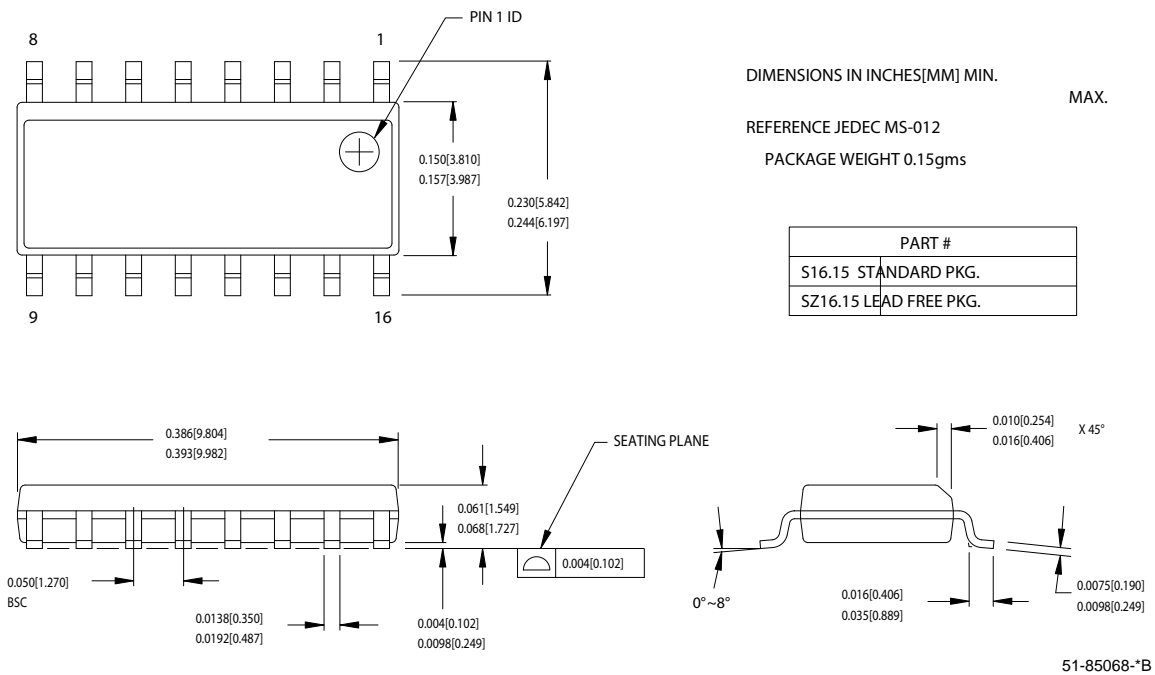
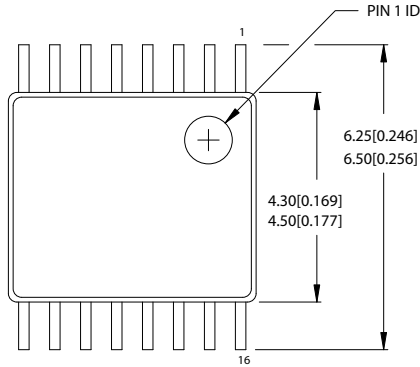


Figure 9. 16-Pin (150-Mil) SOIC S16



Package Drawing and Dimensions (continued)

Figure 10. 16-Pin TSSOP 4.40 MM Body Z16.173

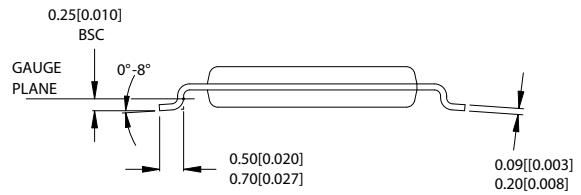
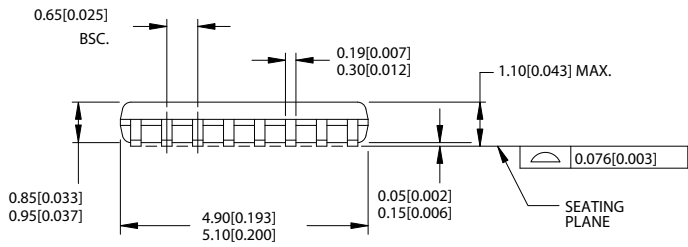


DIMENSIONS IN MM[INCHES] MIN.

MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05gms



51-85091-*A

Document History Page

| Document Title: CY2305/CY2309 Low-Cost 3.3V Zero Delay Buffer | | | | |
|---|---------|-----------------|-----------------|---|
| Document Number: 38-07140 | | | | |
| REV. | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 110249 | SZV | 10/19/01 | Change from Spec number: 38-00530 to 38-07140 |
| *A | 111117 | CKN | 03/01/02 | Added t6B row to the Switching Characteristics Table; also added the letter "A" to the t6A row Corrected the table title from CY2305SC-IH and CY2309SC-IH to CY2305SI-IH and CY2309SI-IH |
| *B | 117625 | HWT | 10/21/02 | Added eight-pin TSSOP packages (CY2305ZC-1 and CY2305ZC-1T) to the ordering information table. Added the Tape and Reel option to all the existing packages: CY2305SC-1T, CY2305SI-1T, CY2305SC-1HT, CY2305SI-1HT, CY2305ZC-1T, CY2309SC-1T, CY2309SI-1T, CY2309SC-1HT, CY2309SI-1HT, CY2309ZC-1HT, CY2309ZI-1HT |
| *C | 121828 | RBI | 12/14/02 | Power up requirements added to Operating Conditions information |
| *D | 131503 | RGL | 12/12/03 | Added Lead-free for all the devices in the ordering information table |
| *E | 214083 | RGL | See ECN | Added a Lead-free with the new coding for all SOIC devices in the ordering information table |
| *F | 291099 | RGL | See ECN | Added TSSOP Lead-free devices |
| *G | 390582 | RGL | See ECN | Added typical values for jitter |
| *H | 2542461 | AESA | 07/23/08 | Updated template. Added Note "Not recommended for new designs." Added part number CY2305ESXC-1, CY2305ESXC-1T, CY2305ESXI-1, CY2305ESXI-1T, CY2305ESXC-1H, CY2305ESXC-1HT, CY2305ESXI-1H, CY2305ESXI-1HT, CY2309ESXC-1, CY2309ESXC-1T, CY2309ESXI-1, CY2309ESXI-1T, CY2309ESXC-1H, CY2309ESXC-1HT, CY2309ESXI-1H, CY2309ESXI-1HT, CY2309EZXC-1H, CY2309EZXC-1HT, CY2309EZXI-1H, and CY2309EZXI-1HT in ordering information table. Removed part number CY2305SZC-1, CY2305SZC-1T, CY2305SZI-1, CY2305SZI-1T, CY2305SZC-1H, CY2305SZC-1HT, CY2305SZI-1H, CY2305SZI-1HT, CY2309SZC-1, CY2309SZC-1T, CY2309SZI-1, CY2309SZI-1T, CY2309SZC-1H, CY2309SZC-1HT, CY2309SZI-1H, CY2309SZI-1HT, CY2309ZZC-1H, CY2309ZZC-1HT, CY2309ZI-1H, CY2309ZI-1HT, CY2309ZZI-1H, and CY2309ZZI-1HT in Ordering Information table. Changed Lead-Free to Pb-Free. |
| *I | 2565153 | AESA | 09/18/08 | Removed part number CY2305ESXC-1, CY2305ESXC-1T, CY2305ESXI-1, CY2305ESXI-1T, CY2305ESXC-1H, CY2305ESXC-1HT, CY2305ESXI-1H, CY2305ESXI-1HT, CY2309ESXC-1, CY2309ESXC-1T, CY2309ESXI-1, CY2309ESXI-1T, CY2309ESXC-1H, CY2309ESXC-1HT, CY2309ESXI-1H, CY2309ESXI-1HT, CY2309EZXC-1H, CY2309EZXC-1HT, CY2309EZXI-1H, and CY2309EZXI-1HT in ordering information table. Removed note references to note 10 in Pb-Free sections of ordering information table. Changed IDD (PD mode) from 12.0 to 25.0 μ A for commercial temperature devices Deleted Duty Cycle parameters for $F_{out} < 50$ MHz commercial and industrial devices. |

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