



**THE DATASHEET OF
CY25814SXIT**



Spread Spectrum Clock Generator

Features

- 4 to 32 MHz input frequency range
- 4 to 128 MHz output frequency range
- Accepts clock, crystal, and resonator inputs
- 1x, 2x, and 4x frequency multiplication:
 - CY25811: 1x; CY25812: 2x; CY25814: 4x
- Center and Down Spread modulation
- Low power dissipation:
 - 3.3V = 52 mW - typ at 6 MHz
 - 3.3V = 60 mW - typ at 12 MHz
 - 3.3V = 72 mW - typ at 24 MHz
- Low cycle-to-cycle jitter:
 - 8 MHz = 480 ps-max
 - 16 MHz = 400 ps-max
 - 32 MHz = 450 ps-max
- Available in 8-pin SOIC and TSSOP packages
- Commercial and industrial temperature ranges

Applications

- Printers and MFPs
- LCD panels
- Digital copiers
- PDAs
- CD-ROM, VCD, and DVD
- Networking, LAN, and WAN
- Scanners
- Modems
- Embedded digital systems

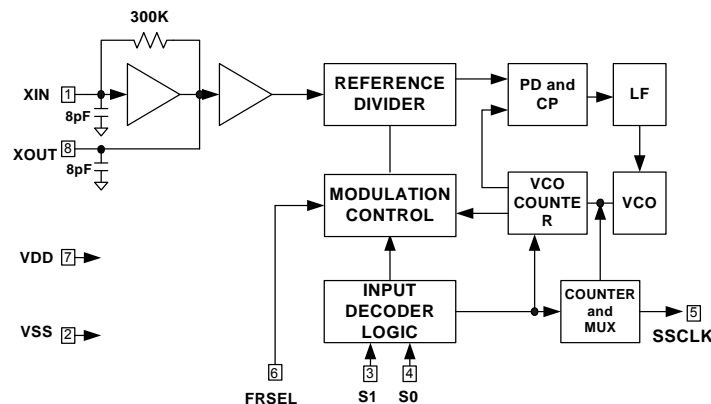
Benefits

- Peak EMI reduction by 8 to 16 dB
- Fast time to market
- Cost reduction

Functional Description

For a complete list of related documentation, click [here](#).

Logic Block Diagram

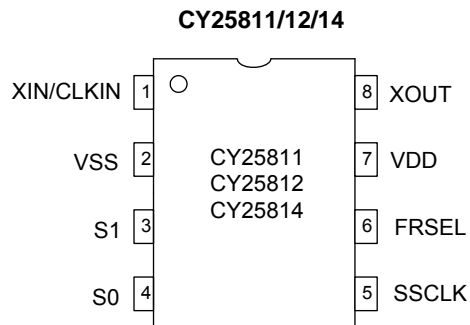


Contents

| | | | |
|--|-----------|--|-----------|
| Pin Configuration | 3 | Ordering Information | 13 |
| Pin Definitions | 3 | Ordering Code Definitions | 13 |
| Functional Overview | 3 | Package Drawing and Dimensions | 14 |
| Input Frequency Range and Selection | 3 | Acronyms | 16 |
| Spread Percentage Selection | 4 | Document Conventions | 16 |
| Input and Output Frequency Selection | 5 | Units of Measure | 16 |
| Absolute Maximum Conditions | 6 | Document History Page | 17 |
| DC Electrical Specifications | 6 | Sales, Solutions, and Legal Information | 19 |
| DC Electrical Specifications | 7 | Worldwide Sales and Design Support | 19 |
| Thermal Resistance | 7 | Products | 19 |
| AC Electrical Specifications | 8 | PSoC@Solutions | 19 |
| AC Electrical Specifications | 9 | Cypress Developer Community | 19 |
| Characteristic Curves | 10 | Technical Support | 19 |
| SSCG Profiles | 11 | | |
| Application Schematic | 12 | | |

Pin Configuration

Figure 1. 8-pin SOIC/TSSOP pinout



Pin Definitions

| Pin No. | Name | Type | Description |
|---------|-----------|--------|---|
| 1 | XIN/CLKIN | Input | Crystal, Ceramic Resonator or Clock Input Pin. |
| 2 | VSS | Power | Power Supply Ground. |
| 3 | S1 | Input | Digital Spread% Control Pin. 3-Level input (H-M-L). Default = M. |
| 4 | S0 | Input | Digital Spread% Control Pin. 3-Level input (H-M-L). Default = M. |
| 5 | SSCLK | Output | Spread Spectrum Output Clock. |
| 6 | FRSEL | Input | Input Frequency Range Selection Digital Control Input. 3-Level input (H-M-L). Default = M. |
| 7 | VDD | Power | Positive Power Supply. |
| 8 | XOUT | Output | Crystal or Ceramic Resonator Output Pin. |

Functional Overview

The CY25811/12/14 products are Spread Spectrum Clock Generator (SSCG) ICs used for the purpose of reducing electromagnetic interference (EMI) found in today's high-speed digital electronic systems.

The devices use a Cypress proprietary phase-locked loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the input clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies is greatly reduced.

This reduction in radiated energy significantly reduces the cost of complying with regulatory agency requirements and improves time to market without degrading system performance.

The input frequency range is 4 to 32 MHz and accepts clock, crystal and ceramic resonator inputs. The output clock can be selected to produce 1x, 2x, or 4x multiplication of the input frequency with Spread Spectrum Frequency Modulation.

The use of 2x or 4x frequency multiplication eliminates the need for higher order crystals and enables you to generate up to 128 MHz Spread Spectrum Clock (SSC) by using only first-order crystals. This reduces the cost while improving the system clock accuracy, performance, and complexity.

Select the Center Spread or Down Spread frequency modulation based on four discrete values of Spread % for each Spread mode with the option of a Non Spread mode for system test and verification purposes.

The CY25811/12/14 products are available in an 8-pin SOIC (150 mils) package with a commercial operating temperature range of 0 °C to 70 °C and industrial temperature range of -40 °C to 85 °C. Refer to [CY25568](#) for multiple clock output options such as modulated and unmodulated clock outputs or power down function.

Input Frequency Range and Selection

The CY25811/12/14 input frequency range is 4 to 32 MHz. This range is divided into three segments and controlled by a 3-level FRSEL pin as given in [Table 1](#).

Table 1. Input Frequency Selection

| FRSEL | Input Frequency Range |
|-------|-----------------------|
| 0 | 4.0 to 8.0 MHz |
| 1 | 8.0 to 16.0 MHz |
| M | 16.0 to 32.0 MHz |

Spread Percentage Selection

The CY25811/12/14 SSCG products provide Center Spread, Down Spread, and No Spread functions. The amount of Spread percentage is selected using 3-level. S0 and S1 digital inputs and Spread percent values are given in Table 2.

Table 2. Spread Percent Selection

| XIN (MHz) | FRSEL | S1 = 0 S0 = 0 | S1 = 0 S0 = M | S1 = 0 S0 = 1 | S1 = M S0 = 0 | S1 = 1 S0 = 1 | S1 = 1 S0 = 0 | S1 = M S0 = 1 | S1 = 1 S0 = M | S1 = M S0 = M |
|-----------|-------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| | | Center (%) | Center (%) | Center (%) | Center (%) | Down (%) | Down (%) | Down (%) | Down (%) | No Spread |
| 4-5 | 0 | ±1.4 | ±1.2 | ±0.6 | ±0.5 | -3.0 | -2.2 | -1.9 | -0.7 | 0 |
| 5-6 | 0 | ±1.3 | ±1.1 | ±0.5 | ±0.4 | -2.7 | -1.9 | -1.7 | -0.6 | 0 |
| 6-7 | 0 | ±1.2 | ±0.9 | ±0.5 | ±0.4 | -2.5 | -1.8 | -1.5 | -0.6 | 0 |
| 7-8 | 0 | ±1.1 | ±0.9 | ±0.4 | ±0.3 | -2.3 | -1.7 | -1.4 | -0.5 | 0 |
| 8-10 | 1 | ±1.4 | ±1.2 | ±0.6 | ±0.5 | -3.0 | -2.2 | -1.9 | -0.7 | 0 |
| 10-12 | 1 | ±1.3 | ±1.1 | ±0.5 | ±0.4 | -2.7 | -1.9 | -1.7 | -0.6 | 0 |
| 12-14 | 1 | ±1.2 | ±0.9 | ±0.5 | ±0.4 | -2.5 | -1.8 | -1.5 | -0.6 | 0 |
| 14-16 | 1 | ±1.1 | ±0.9 | ±0.4 | ±0.3 | -2.3 | -1.7 | -1.4 | -0.5 | 0 |
| 16-20 | M | ±1.4 | ±1.2 | ±0.6 | ±0.5 | -3.0 | -2.2 | -1.9 | -0.7 | 0 |
| 20-24 | M | ±1.3 | ±1.1 | ±0.5 | ±0.4 | -2.7 | -1.9 | -1.7 | -0.6 | 0 |
| 24-28 | M | ±1.2 | ±0.9 | ±0.5 | ±0.4 | -2.5 | -1.8 | -1.5 | -0.6 | 0 |
| 28-32 | M | ±1.1 | ±0.9 | ±0.4 | ±0.3 | -2.3 | -1.7 | -1.4 | -0.5 | 0 |

3-Level Digital Inputs

S0, S1, and FRSEL digital inputs are designed to sense three different logic levels designated as High “1”, Low “0”, and Middle “M”. With this 3-Level digital input logic, the 3-Level Logic detects nine different logic states.

S0, S1, and FRSEL pins include an on chip 20K (10K and 10K) resistor divider. No external application resistors are needed to implement the 3-level logic levels as shown here:

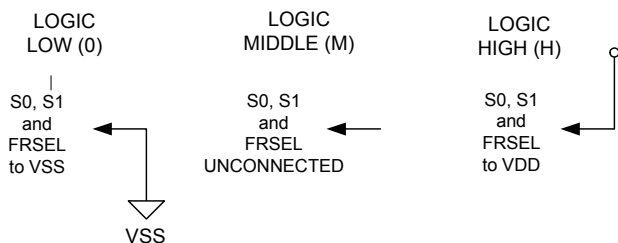
Logic Level “0”: 3-Level logic pin connected to GND.

Logic Level “M”: 3-Level logic pin left floating (no connection).

Logic Level “1”: 3-Level logic pin connected to V_{DD}.

Figure 2 illustrates how to implement 3-Level Logic.

Figure 2. 3-Level Logic



Modulation Rate

SSCGs use frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (f_{max}) and minimum frequency of the clock (f_{min}) determine this band of frequencies. The time required to transition from f_{min} to f_{max} and back to f_{min} is the period of the Modulation Rate. The Modulation Rate of SSCG clocks are generally referred to in terms of frequency, or:

$$f_{mod} = 1/T_{mod}$$

The input clock frequency, f_{in}, and the internal divider determine the Modulation Rate.

In CY25811/12/14 devices, the (Spread Spectrum) modulation rate, f_{mod}, is given by the following formula:

$$f_{mod} = f_{in}/DR$$

Here f_{mod} is the Modulation Rate, f_{in} is the Input Frequency, and DR is the Divider Ratio as given in Table 3. Note that Input Frequency Range is set by FRSEL.

Table 3. Modulation Rate Divider Ratios

| FRSEL | Input Frequency Range (MHz) | Divider Ratio (DR) |
|-------|-----------------------------|--------------------|
| 0 | 4 to 8 | 128 |
| 1 | 8 to 16 | 256 |
| M | 16 to 32 | 512 |

Input and Output Frequency Selection

The relationship between input frequency and output frequency in device selection and FRSEL setting is given in [Table 4](#). As shown, the input frequency range is selected by FRSEL and is the same for CY25811, CY25812, and CY25814. The selection of CY25811 (1x), CY25812 (2x), or CY25814 (4x) determines the frequency multiplication at the output (SSCLK, Pin 5) with respect to input frequency (XIN, Pin-1).

Table 4. Input and Output Frequency Selection

| Input Frequency Range (MHz) | FRSEL | Product | Multiplication | Output Frequency Range (MHz) |
|-----------------------------|-------|---------|----------------|------------------------------|
| 4 to 8 | 0 | CY25811 | 1x | 4 to 8 |
| 8 to 16 | 1 | CY25811 | 1x | 8 to 16 |
| 16 to 32 | M | CY25811 | 1x | 16 to 32 |
| 4 to 8 | 0 | CY25812 | 2x | 8 to 16 |
| 8 to 16 | 1 | CY25812 | 2x | 16 to 32 |
| 16 to 32 | M | CY25812 | 2x | 32 to 64 |
| 4 to 8 | 0 | CY25814 | 4x | 16 to 32 |
| 8 to 16 | 1 | CY25814 | 4x | 32 to 64 |
| 16 to 32 | M | CY25814 | 4x | 64 to 128 |

Absolute Maximum Conditions

Both Commercial and Industrial Grades

| Parameter ^[1, 2] | Description | Condition | Min | Max | Unit |
|-----------------------------|-----------------------------------|-----------------------------|------|-----------------------|------|
| V _{DD} | Supply Voltage | | -0.5 | 4.6 | V |
| V _{IN} | Input Voltage | Relative to V _{SS} | -0.5 | V _{DD} + 0.5 | V |
| T _S | Temperature, Storage | Non Functional | -65 | 150 | °C |
| T _{A1} | Temperature, Operating Ambient | Functional, C-Grade | 0 | 70 | °C |
| T _{A2} | Temperature, Operating Ambient | Functional, I-Grade | -40 | 85 | °C |
| T _J | Temperature, Junction | Functional | - | 150 | °C |
| ESD _{HBM} | ESD Protection (Human Body Model) | MIL-STD-883, Method 3015 | 2000 | - | V |
| UL-94 | Flammability Rating | at 1/8 in. | V-0 | | |
| MSL | Moisture Sensitivity Level | | 3 | | |

DC Electrical Specifications

Commercial Grade

| Parameter | Description | Condition | Min | Max | Unit |
|------------------|-------------------------|---------------------------------------|------------------------|------------------------|------|
| V _{DD} | 3.3 V Operating Voltage | 3.3 V ± 10% | 2.97 | 3.63 | V |
| V _{IL} | Input Low Voltage | S0, S1 and FRSEL Inputs | 0 | 0.15 × V _{DD} | V |
| V _{IM} | Input Middle Voltage | S0, S1 and FRSEL Inputs | 0.40 × V _{DD} | 0.60 × V _{DD} | V |
| V _{IH} | Input High Voltage | S0, S1 and FRSEL Inputs | 0.85 × V _{DD} | V _{DD} | V |
| V _{OL1} | Output Low Voltage | I _{OL} = 4 mA, SSCLK Output | - | 0.4 | V |
| V _{OL2} | Output Low Voltage | I _{OL} = 10 mA, SSCLK Output | - | 1.2 | V |
| V _{OH1} | Output High Voltage | I _{OH} = 4 mA, SSCLK Output | 2.4 | - | V |
| V _{OH2} | Output High Voltage | I _{OH} = 6 mA, SSCLK Output | 2.0 | - | V |
| C _{IN1} | Input Pin Capacitance | XIN (Pin 1) and XOUT (Pin 8) | 3.5 | 9.0 | pF |
| C _{IN2} | Input Pin Capacitance | All Digital Inputs | 2.8 | 6.0 | pF |
| C _L | Output Load Capacitor | SSCLK Output | - | 15 | pF |
| I _{DD1} | Dynamic Supply Current | F _{in} = 12 MHz, no load | - | 28 | mA |
| I _{DD2} | Dynamic Supply Current | F _{in} = 24 MHz, no load | - | 33 | mA |
| I _{DD3} | Dynamic Supply Current | F _{in} = 32 MHz, no load | - | 40 | mA |

Notes

1. Operation at any Absolute Maximum Rating is not implied.
2. Single Power Supply: The voltage on any input or I/O pin cannot exceed the power pin during power up.

DC Electrical Specifications

Industrial Grade

| Parameter | Description | Condition | Min | Max | Unit |
|------------------|-------------------------|---------------------------------------|------------------------|------------------------|------|
| V _{DD} | 3.3 V Operating Voltage | 3.3 V ± 5% | 3.135 | 3.465 | V |
| V _{IL} | Input Low Voltage | S0, S1 and FRSEL Inputs | 0 | 0.13 × V _{DD} | V |
| V _{IM} | Input Middle Voltage | S0, S1 and FRSEL Inputs | 0.40 × V _{DD} | 0.60 × V _{DD} | V |
| V _{IH} | Input High Voltage | S0, S1 and FRSEL Inputs | 0.85 × V _{DD} | V _{DD} | V |
| V _{OL1} | Output Low Voltage | I _{OL} = 4 mA, SSCLK Output | – | 0.4 | V |
| V _{OL2} | Output Low Voltage | I _{OL} = 10 mA, SSCLK Output | – | 1.2 | V |
| V _{OH1} | Output High Voltage | I _{OH} = 4 mA, SSCLK Output | 2.4 | – | V |
| V _{OH2} | Output High Voltage | I _{OH} = 6 mA, SSCLK Output | 2.0 | – | V |
| C _{IN1} | Input Pin Capacitance | XIN (Pin 1) and XOUT (Pin 8) | 3.5 | 9.0 | pF |
| C _{IN2} | Input Pin Capacitance | All Digital Inputs | 2.8 | 6.0 | pF |
| C _L | Output Load Capacitor | SSCLK Output | – | 15 | pF |
| I _{DD1} | Dynamic Supply Current | F _{in} = 12 MHz, no load | – | 28 | mA |
| I _{DD2} | Dynamic Supply Current | F _{in} = 24 MHz, no load | – | 33 | mA |
| I _{DD3} | Dynamic Supply Current | F _{in} = 32 MHz, no load | – | 41 | mA |

Thermal Resistance

| Parameter ^[3] | Description | Test Conditions | 8-pin SOIC | 8-pin TSSOP | Unit |
|--------------------------|--|---|------------|-------------|------|
| θ _{JA} | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51. | 139 | 159 | °C/W |
| θ _{JC} | Thermal resistance (junction to case) | | 54 | 32 | °C/W |

Note

3. These parameters are guaranteed by design and are not tested.

AC Electrical Specifications

Commercial Grade

| Parameter | Description | Condition | Min | Max | Unit |
|--------------------|----------------------------------|---|-----|-----|------|
| F _{IN} | Input Frequency Range | Clock, Crystal, or Ceramic Resonator Input | 4 | 32 | MHz |
| T _{R1} | Clock Rise Time | SSCLK, CY25811 and CY25812 | 2.0 | 5.0 | ns |
| T _{F1} | Clock Fall Time | SSCLK, CY25811 and CY25812 | 1.6 | 4.4 | ns |
| T _{R2} | Clock Rise Time | SSCLK, only CY25814 when FRSEL = M | 1.0 | 2.2 | ns |
| T _{F2} | Clock Fall Time | SSCLK, only CY25814 when FRSEL = M | 0.8 | 2.2 | ns |
| T _{DCIN} | Input Clock Duty Cycle | XIN | 40 | 60 | % |
| T _{DCOUT} | Output Clock Duty Cycle | SSCLK | 40 | 60 | % |
| T _{CCJ1} | Cycle to Cycle Jitter, Spread on | F _{in} = 4 MHz, F _{out} = 4 MHz, CY25811 | – | 800 | ps |
| T _{CCJ2} | Cycle to Cycle Jitter, Spread on | F _{in} = 8 MHz, F _{out} = 8 MHz, CY25811 | – | 480 | ps |
| T _{CCJ3} | Cycle to Cycle Jitter, Spread on | F _{in} = 8 MHz, F _{out} = 16 MHz, CY25812 | – | 400 | ps |
| T _{CCJ4} | Cycle to Cycle Jitter, Spread on | F _{in} = 16 MHz, F _{out} = 32 MHz, CY25812 | – | 450 | ps |
| T _{CCJ5} | Cycle to Cycle Jitter, Spread on | F _{in} = 16 MHz, F _{out} = 64 MHz, CY25814 | – | 550 | ps |
| T _{CCJ6} | Cycle to Cycle Jitter, Spread on | F _{in} = 32 MHz, F _{out} = 128 MHz, CY25814 | – | 380 | ps |
| T _{SU} | PLL Lock Time | From V _{DD} = 3.0 V to valid SSCLK | – | 3 | ms |

AC Electrical Specifications

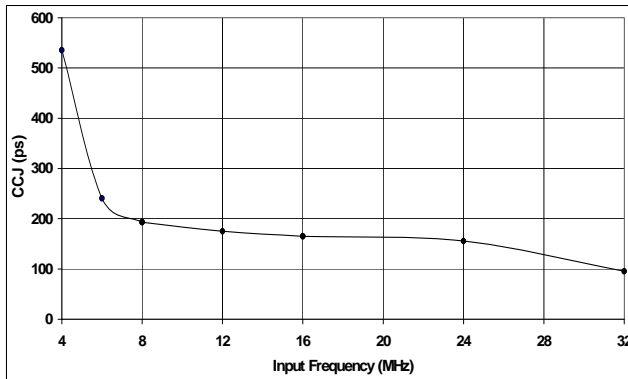
Industrial Grade

| Parameter | Description | Condition | Min | Max | Unit |
|--------------------|----------------------------------|---|-----|-----|------|
| F _{IN} | Input Frequency Range | Clock, Crystal or Ceramic Resonator Input | 4 | 32 | MHz |
| T _{R1} | Clock Rise Time | SSCLK, CY25811, and CY25812 | 2.0 | 5.0 | ns |
| T _{F1} | Clock Fall Time | SSCLK, CY25811, and CY25812 | 1.6 | 4.4 | ns |
| T _{R2} | Clock Rise Time | SSCLK, only CY25814 when FRSEL = M | 1.0 | 2.2 | ns |
| T _{F2} | Clock Fall Time | SSCLK, only CY25814 when FRSEL = M | 0.8 | 2.2 | ns |
| T _{DCIN} | Input Clock Duty Cycle | XIN | 40 | 60 | % |
| T _{DCOUT} | Output Clock Duty Cycle | SSCLK | 40 | 60 | % |
| T _{CCJ1} | Cycle to Cycle Jitter, Spread on | Fin = 6 MHz, CY25811/12/14 | – | 650 | ps |
| T _{CCJ2} | Cycle to Cycle Jitter, Spread on | Fin = 12 MHz, CY25811/12/14 | – | 630 | ps |
| T _{CCJ3} | Cycle to Cycle Jitter, Spread on | Fin = 24 MHz, CY25811/12/14 | – | 520 | ps |
| T _{SU} | PLL Lock Time | From V _{DD} = 3.0 V to valid SSCLK | – | 4 | ms |

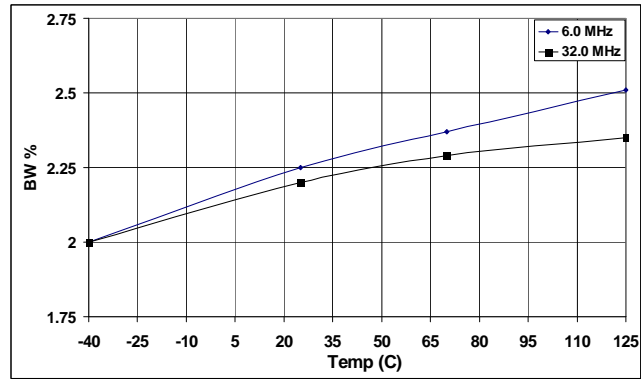
Characteristic Curves

The following curves demonstrate the characteristic behavior of CY25811/12/14 when tested over a number of environmental and application specific parameters. These are typical performance curves and are not meant to replace any parameter specified in DC and AC Specification tables.

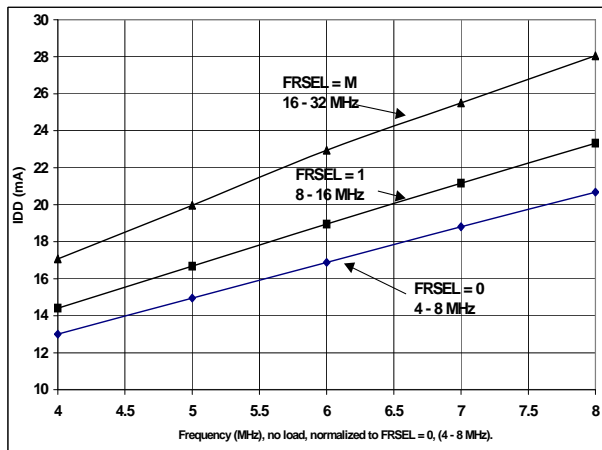
Figure 3. Characteristic Curves



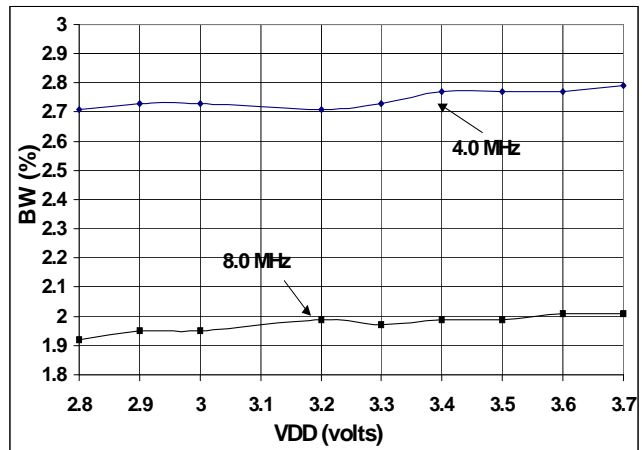
Jitter vs. Input Frequency (No Load)



Bandwidth % vs. Temperature



IDD vs. Frequency (FRSEL = 0, 1, M)

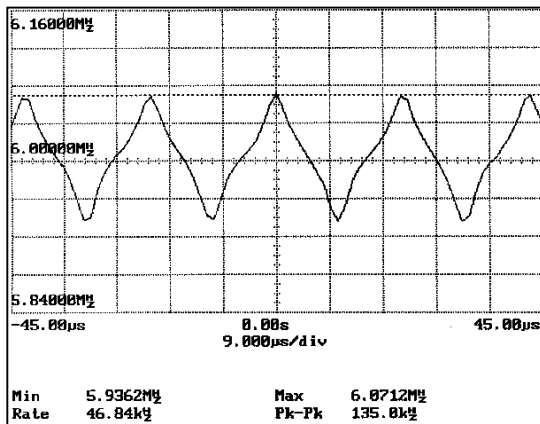


Bandwidth % vs. VDD

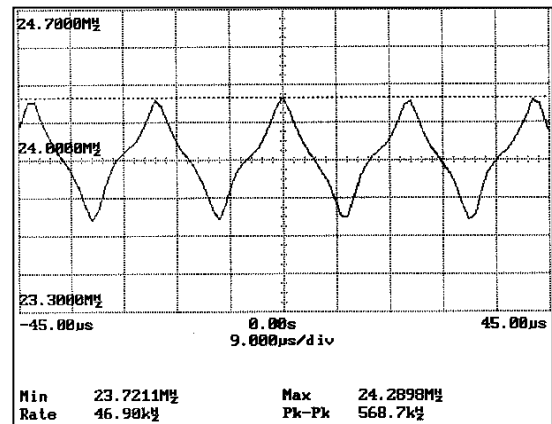
SSCG Profiles

CY25811/12/14 SSCG products use a non-linear “optimized” frequency profile as shown in Figure 4. The use of Cypress proprietary “optimized” frequency profile maintains flat energy distribution over the fundamental and higher order harmonics. This results in additional EMI reduction in electronic systems.

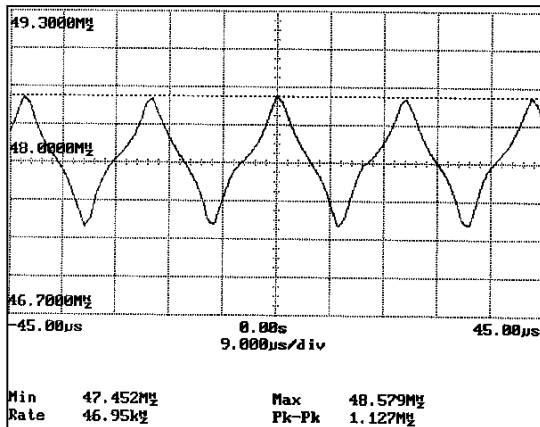
Figure 4. Spread Spectrum Profiles (Frequency versus Time)



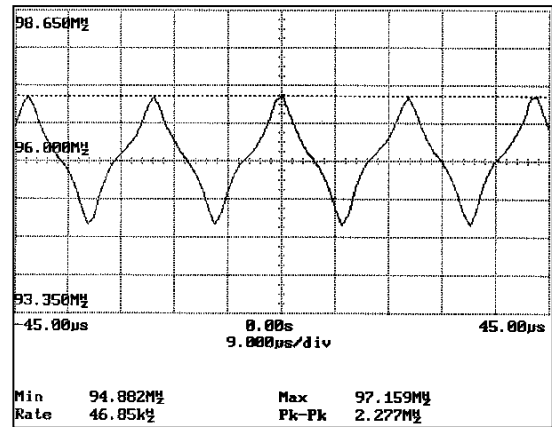
Xin = 6.0 MHz SSCLK1 = 6.0 MHz
 S1, S0 = 0
 FRSEL = 0 P/N = CY25811



Xin = 24.0 MHz SSCLK1 = 24.0 MHz
 S1, S0 = 0
 FRSEL = M P/N = CY25811

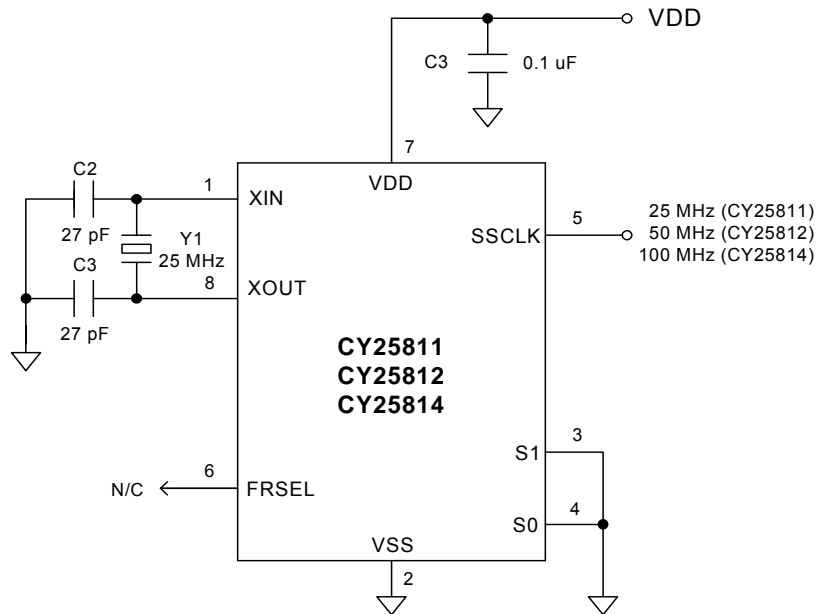


Xin = 12.0 MHz SSCLK1 = 48.0 MHz
 S1, S0 = 0
 FRSEL = 1 P/N = CY25814



Xin = 24.0 MHz SSCLK1 = 96.0 MHz
 S1, S0 = 0
 FRSEL = M P/N = CY25814

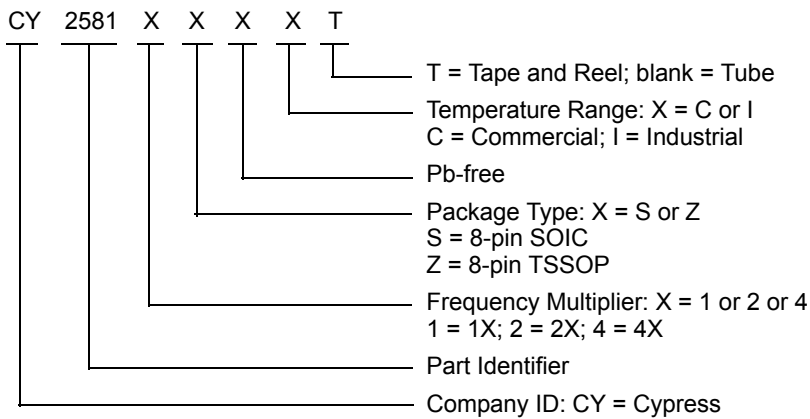
Application Schematic



Ordering Information

| Part Number | Package Type | Product Flow |
|------------------------|-----------------------------|-----------------------------|
| Pb-free Devices | | |
| CY25811SXC | 8-pin SOIC | Commercial, 0 °C to 70 °C |
| CY25811SXCT | 8-pin SOIC – Tape and Reel | Commercial, 0 °C to 70 °C |
| CY25811SXI | 8-pin SOIC | Industrial, –40 °C to 85 °C |
| CY25811SXIT | 8-pin SOIC – Tape and Reel | Industrial, –40 °C to 85 °C |
| CY25812SXC | 8-pin SOIC | Commercial, 0 °C to 70 °C |
| CY25812SXCT | 8-pin SOIC – Tape and Reel | Commercial, 0 °C to 70 °C |
| CY25812ZXC | 8-pin TSSOP | Commercial, 0 °C to 70 °C |
| CY25812ZXCT | 8-pin TSSOP – Tape and Reel | Commercial, 0 °C to 70 °C |
| CY25814SXC | 8-pin SOIC | Commercial, 0 °C to 70 °C |
| CY25814SXCT | 8-pin SOIC – Tape and Reel | Commercial, 0 °C to 70 °C |
| CY25814SXI | 8-pin SOIC | Industrial, –40 °C to 85 °C |
| CY25814SXIT | 8-pin SOIC – Tape and Reel | Industrial, –40 °C to 85 °C |

Ordering Code Definitions

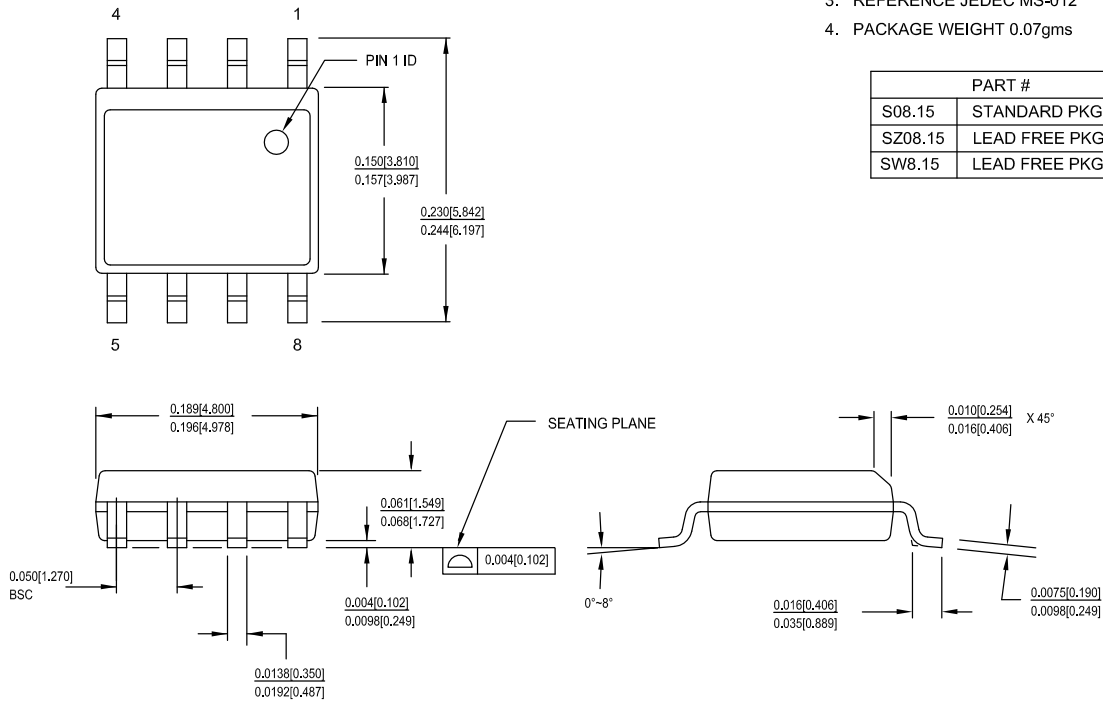


Package Drawing and Dimensions

Figure 5. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066

1. DIMENSIONS IN INCHES[MM] MIN. MAX.
2. PIN 1 ID IS OPTIONAL, ROUND ON SINGLE LEADFRAME RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

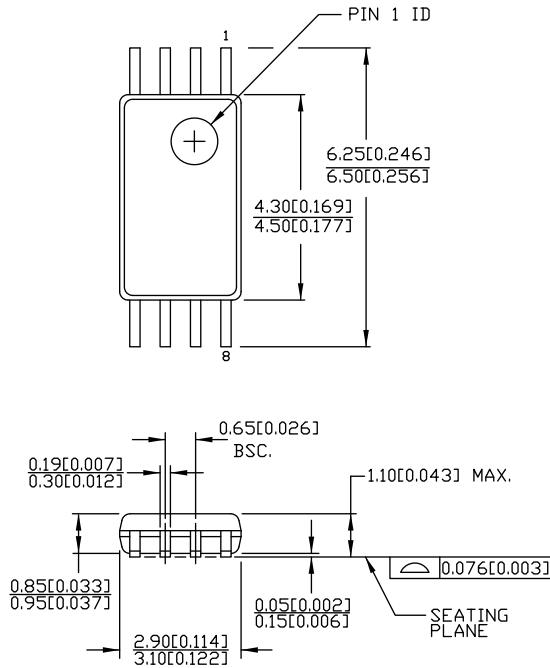
| PART # | |
|---------|---------------|
| S08.15 | STANDARD PKG |
| SZ08.15 | LEAD FREE PKG |
| SW8.15 | LEAD FREE PKG |



51-85066 *H

Package Drawing and Dimensions (continued)

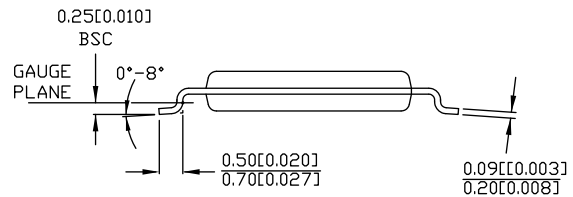
Figure 6. 8-pin TSSOP (4.40 mm Body) Z08.173/ZZ08.173 Package Outline, 51-85093



DIMENSIONS IN MM [INCHES] MIN.
MAX.

REFERENCE JEDEC MO-153

| PART # | |
|----------|----------------|
| Z08.173 | STANDARD PKG. |
| ZZ08.173 | LEAD FREE PKG. |



51-85093 *E

Acronyms

| Acronym | Description |
|---------|-----------------------------------|
| CD-ROM | compact disc, read only memory |
| DVD | digital versatile/video disc |
| EMI | Electromagnetic Interference |
| ESD | electrostatic discharge |
| FM | frequency modulation |
| LAN | local area network |
| LCD | liquid crystal display |
| PLL | phase locked loop |
| SOIC | small outline integrated circuit |
| SSC | spread spectrum clock |
| SSCG | spread spectrum clock generator |
| TSSOP | thin shrink small outline package |
| VCD | video compact disc |
| VCO | voltage controlled oscillator |
| WAN | wide area network |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| dB | decibel |
| MHz | megahertz |
| μF | microfarad |
| mA | milliampere |
| mm | millimeter |
| ms | millisecond |
| mW | milliwatt |
| ns | nanosecond |
| % | percent |
| pF | picofarad |
| ps | picosecond |
| V | volt |

Document History Page

| Document Title: CY25811/12/14, Spread Spectrum Clock Generator Document Number: 38-07112 | | | | |
|---|---------|-----------------|-----------------|--|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 107516 | NDP | 06/14/02 | Converted from IMI to Cypress |
| *A | 108002 | NDP | 06/29/02 | Deleted Junction Temp. in Absolute Maximum Ratings |
| *B | 121578 | RGL | 01/29/03 | Converted from Word to FrameMaker Added 8-pin TSSOP package in Commercial Temp. only Added an Industrial Temperature Range to all existing 8-pin SOIC packages |
| *C | 125550 | RGL | 05/14/03 | Changed IDD values from 19.6/22/27.2 to 25/30/35 in Commercial Grade DC Specs table Changed IDD values from 24/26.5/33 to 26/32/37 in Industrial grade DC Specs table Changed T _{CCJ1/2} values from 675/260 to 800/450 in Commercial grade AC Specs table Changed T _{CCJ1} value from 350 to 650 in Industrial grade AC Specs table |
| *D | 131941 | RGL | 12/24/03 | Removed automotive in the Applications section Changed the Output Clock Duty Cycle (T _{DCOUT}) from min. 45 and max. 55 to 40 and 60% respectively for both industrial and commercial grade Changed the min. Input Low Voltage (V _{IL}) from 0.15V _{DD} to 0.13V _{DD} Removed preliminary from the industrial AC/DC Electrical Specifications table |
| *E | 231057 | RGL | See ECN | Added Pb Free Devices |
| *F | 1499165 | KVM | See ECN | Updated Ordering Information table Corrected jitter values in features section on page 1 Changed:VDD from ±5% to ±10%, CIN1 min from 6 to 3.5 pF, CIN2 min from 3.5 to 2.8 pF, TF1 min from 2 to 1.6 ns, and TF2 min from 1.0 to 0.8 ns. Commercial grade: IDD1 max from 25 to 28 mA, IDD2 max from 30 to 33 mA, IDD3 max from 35 to 40 mA, TCCJ2 from 450 to 480 ps, TCCJ4 from 380 to 450 ps, and TCCJ5 from 380 to 550 ps Industrial grade: IDD1 max from 26 to 28 mA, IDD2 max from 32 to 33 mA, IDD3 max from 37 to 41 mA, TCCJ2 from 400 to 630 ps, and TCCJ3 from 400 to 520 ps |
| *G | 2592288 | CXQ / PYRS | 10/23/08 | Removed Pb package devices from Ordering Table |
| *H | 2761988 | CXQ | 09/10/09 | Removed reference to non-existent "Automotive" version. Fixed typo in DC spec table for VDD from min of 3.97 to 2.97. Fixed typo for PLL Lock time conditions. Removed CY25812SXI, CY25812SXIT, CY25814ZXC, and CY25814ZXT from Ordering Information. |
| *I | 2887509 | CXQ | 03/04/2010 | Updated MSL value in Absolute Maximum Conditions Added Contents Updated 8-pin SOIC and 8-pin TSSOP package drawings. Updated URLs in Sales, Solutions, and Legal Information |
| *J | 3339686 | PURU | 08/08/2011 | Added Ordering Code Definitions . Updated Package Drawing and Dimensions . Added Acronyms and Units of Measure . Updated to new template. |
| *K | 4499792 | TAVA | 09/11/2014 | Updated Package Drawing and Dimensions : spec 51-85066 – Changed revision from *E to *F. spec 51-85093 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review. |

Document History Page (continued)

| Document Title: CY25811/12/14, Spread Spectrum Clock Generator Document Number: 38-07112 | | | | |
|---|---------|-----------------|-----------------|---|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *L | 4587350 | TAVA | 12/05/2014 | Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end. Updated Package Drawing and Dimensions : spec 51-85093 – Changed revision from *D to *E. |
| *M | 5279207 | PSR | 05/26/2016 | Added Thermal Resistance . Updated Package Drawing and Dimensions : spec 51-85066 – Changed revision from *F to *H. Updated to new template. |
| *N | 5747567 | PSR | 05/24/2017 | Added the pin type column in Pin Definitions . Corrected unit for the V_{IN} parameter. Updated the Cypress logo, copyright information, Sales, Solutions, and Legal Information based on the new template. |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

| | |
|---|--|
| ARM [®] Cortex [®] Microcontrollers | cypress.com/arm |
| Automotive | cypress.com/automotive |
| Clocks & Buffers | cypress.com/clocks |
| Interface | cypress.com/interface |
| Internet of Things | cypress.com/iot |
| Memory | cypress.com/memory |
| Microcontrollers | cypress.com/mcu |
| PSoC | cypress.com/psoc |
| Power Management ICs | cypress.com/pmic |
| Touch Sensing | cypress.com/touch |
| USB Controllers | cypress.com/usb |
| Wireless Connectivity | cypress.com/wireless |

PSoC[®] Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6](#)

Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support



© Cypress Semiconductor Corporation, 2001-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, WICED, Spansion, the Spansion logo, and combinations thereof, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View CY25814SXIT on WIN SOURCE](#)
-  [Cypress Semiconductor Corp Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management