THE DATASHEET OF

CY62168DV30LL-55BVI

www.win-source.net 0086-755-83957316

CY62168DV30 MoBL®

16-Mbit (2 M × 8) Static RAM

Features

- Very high speed
  - 55 ns
- Wide voltage range
  - 2.2 V–3.6 V
- Ultra-low active power
  - Typical active current: 2 mA at f = 1 MHz
  - Typical active current: 15 mA at f = f_{Max} (55 ns Speed)
- Ultra-low standby power
- Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- Available in non Pb-free 48-ball very fine ball grid array (VFBGA) package.

Functional Description

The CY62168DV30 is a high-performance CMOS static RAMs organized as 2048Kbit words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can be put into standby mode reducing power consumption by 90% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected Chip Enable 1 ($\overline{CE}_1$) HIGH or Chip Enable 2 (CE_2) LOW. The input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when: deselected Chip Enable 1 ($\overline{CE}_1$) HIGH or Chip Enable 2 (CE_2) LOW, outputs are disabled ($\overline{OE}$ HIGH), or during a write operation (Chip Enable 1 ($\overline{CE}_1$) LOW and Chip Enable 2 (CE_2) HIGH and $\overline{WE}$ LOW).

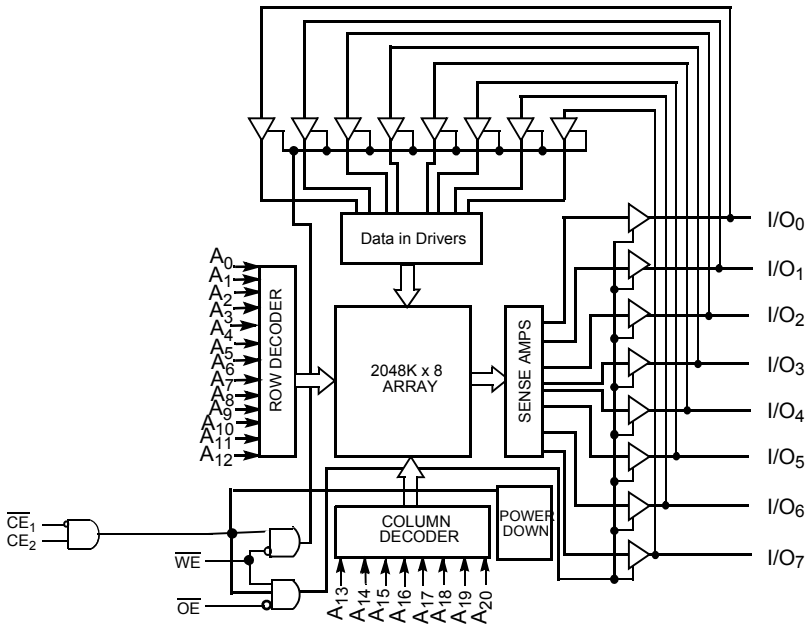
Writing to the device is accomplished by taking Chip Enable 1 ($\overline{CE}_1$) LOW and Chip Enable 2 (CE_2) HIGH and Write Enable ($\overline{WE}$) input LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins(A_0 through A_{20}).

Reading from the device is accomplished by taking Chip Enable 1 ($\overline{CE}_1$) and Output Enable ($\overline{OE}$) LOW and Chip Enable 2 (CE_2) HIGH while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ LOW and CE_2 HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW). See the Truth Table on page 10 for a complete description of read and write modes.

For a complete list of related documentation, click here.

Logic Block Diagram



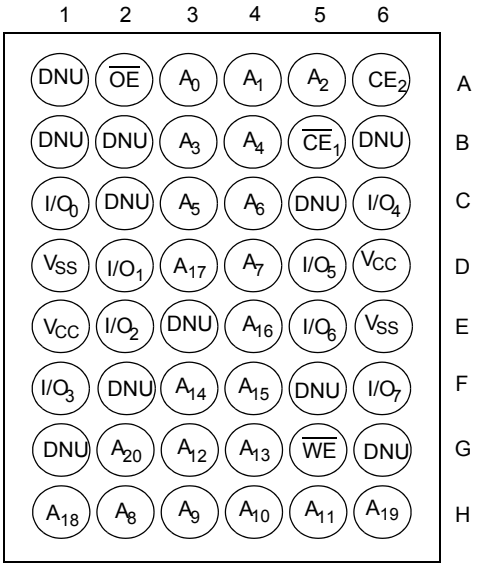
Contents

Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (μA)	
					f = 1 MHz		f = f_{Max}			
	Min	Typ [1]	Max		Typ [1]	Max	Typ [1]	Max	Typ [1]	Max
CY62168DV30LL	2.2	3.0	3.6	55	2	4	15	30	2.5	22

Pin Configuration

Figure 1. 48-ball VFBGA pinout (Top View) [2]



Notes
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25 °C.
2. DNU pins have to be left floating or tied to V_{SS} to ensure proper operation.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential ..... –0.3 V to $V_{CC(max)}$ + 0.3 V

DC voltage applied to outputs in High-Z state [3, 4] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC input voltage [3, 4] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature (T_A) [5]	V_{CC} [6]
Industrial	–40 °C to +85 °C	2.2 V–3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		CY62168DV30-55			Unit
				Min	Typ [7]	Max	
V_{OH}	Output HIGH voltage	2.2 V ≤ V_{CC} ≤ 2.7 V	I_{OH} = –0.1 mA	2.0	–	–	V
		2.7 V ≤ V_{CC} ≤ 3.6 V	I_{OH} = –1.0 mA	2.4	–	–	
V_{OL}	Output LOW voltage	2.2 V ≤ V_{CC} ≤ 2.7 V	I_{OL} = 0.1 mA	–	–	0.4	V
		2.7 V ≤ V_{CC} ≤ 3.6 V	I_{OL} = 2.1 mA	–	–	0.4	
V_{IH}	Input HIGH voltage	2.2 V ≤ V_{CC} ≤ 2.7 V		1.8	–	V_{CC} + 0.3	V
		2.7 V ≤ V_{CC} ≤ 3.6 V		2.2	–	V_{CC} + 0.3	
V_{IL}	Input LOW voltage	2.2 V ≤ V_{CC} ≤ 2.7 V		–0.3	–	0.6	V
		2.7 V ≤ V_{CC} ≤ 3.6 V		–0.3	–	0.8	
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, Output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{Max} = $1/t_{RC}$	V_{CC} = 3.6 V, I_{OUT} = 0 mA, CMOS level	–	15	30	mA
		f = 1 MHz		–	2	4	
I_{SB1}	Automatic CE power-down current – CMOS inputs	$\overline{CE}_1$ ≥ V_{CC} – 0.2 V, CE_2 ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = f_{Max} (Address and data only), f = 0 ($\overline{OE}$, $\overline{WE}$)		–	2.5	22	µA
I_{SB2}	Automatic CE power-down current – CMOS inputs	$\overline{CE}_1$ ≥ V_{CC} – 0.2 V, CE_2 ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = 3.6 V		–	2.5	22	µA

Notes
3. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
4. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
5. T_A is the “Instant-On” case temperature.
6. Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min) and 100 µs wait time after V_{CC} stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ.)}$, T_A = 25 °C.

Capacitance

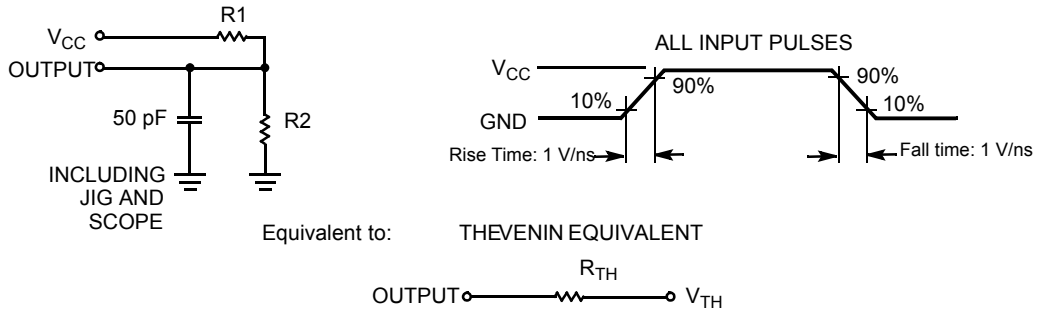
Parameter [8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ.)}$	8	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	VFBGA	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	55	°C/W
θ_{JC}	Thermal resistance (junction to case)		16	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	2.5 V	3.0 V	Unit
R1	16600	1103	Ω
R2	15400	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.2	1.75	V

Note
8. Tested initially and after any design or process changes that may affect these parameters.

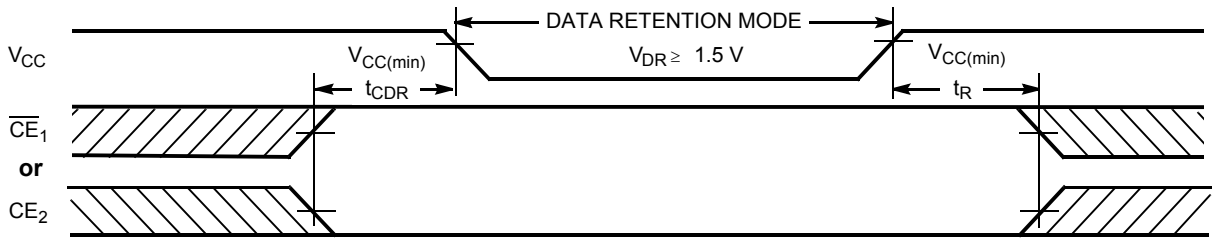
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [10]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	3.6	V
I_{CCDR}	Data retention current	V_{CC} = 1.5 V, $\overline{CE}_1 > V_{CC} - 0.2$ V or $CE_2 \le 0.2$ V, $V_{IN} > V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V	–	–	10	µA
t_{CDR}[9]	Chip deselect to data retention time		0	–	–	ns
t_R[11]	Operation recovery time		55	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes
9. Tested initially and after any design or process changes that may affect these parameters.
10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
11. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ > 100 µs or stable at $V_{CC(min)}$ > 100 µs.

Switching Characteristics

Over the Operating Range

Parameter [12]	Description	55 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	55	–	ns
t_{AA}	Address to data valid	–	55	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [13]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [13, 14]	–	20	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to low Z [13]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH or CE_2 LOW to high Z [13, 14]	–	20	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH or CE_2 LOW to power-down	–	55	ns
Write Cycle [15, 16]				
t_{WC}	Write cycle time	55	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	40	–	ns
t_{AW}	Address setup to write end	40	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse width	40	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [13, 14]	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [13]	10	–	ns

Notes

12. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3ns or less (1V/ns), timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the “AC Test Loads and Waveforms” section.
13. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
14. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
15. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
16. The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [17, 18]

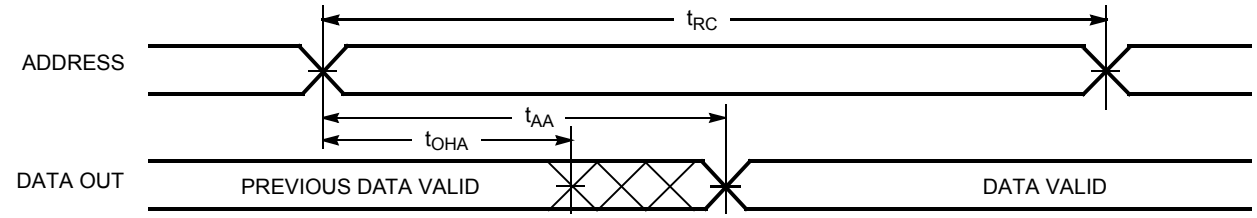


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [18, 19]

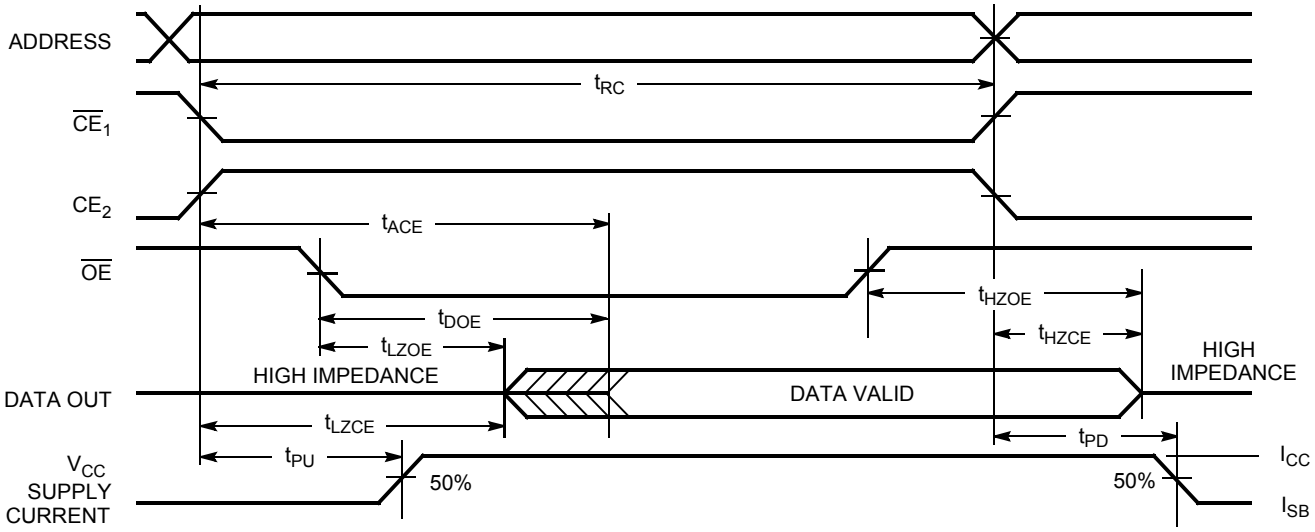
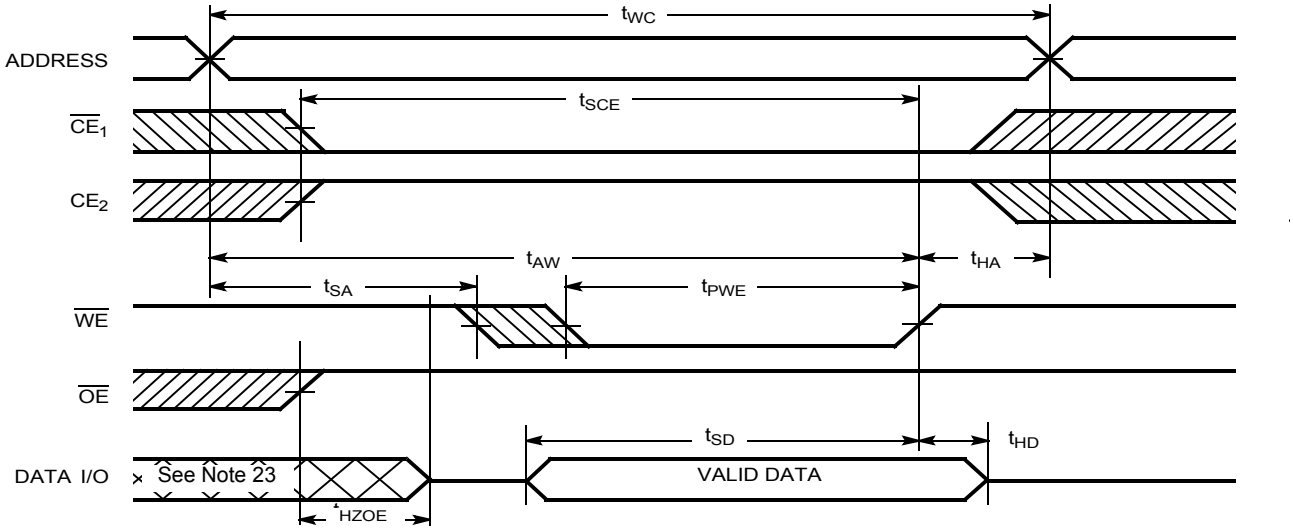


Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled) [20, 21, 22]



Notes

17. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}.
18. $\overline{WE}$ is HIGH for read cycle.
19. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.
20. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1}$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
21. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
22. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high-impedance state.
23. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{CE_1}$ or CE_2 Controlled) [24, 25, 26]

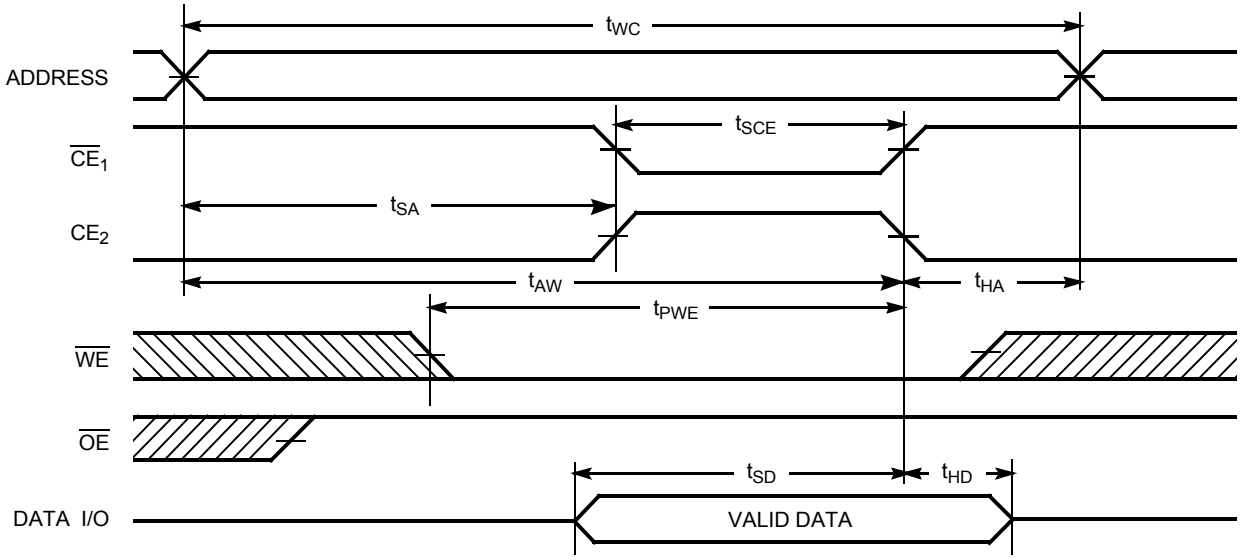
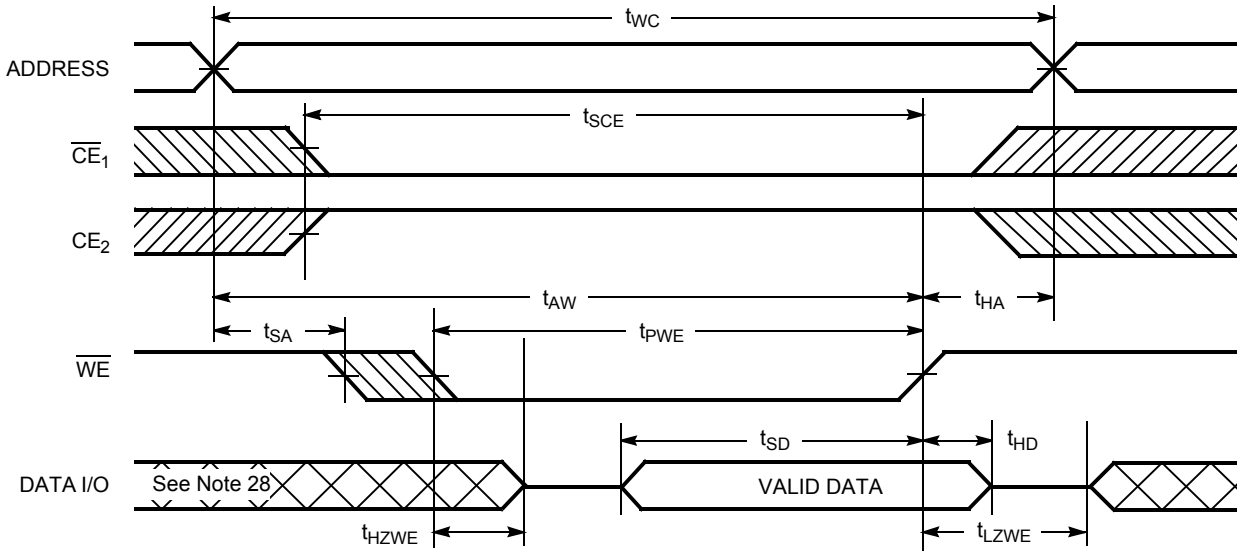


Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [27]



Notes
24. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1}$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
25. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
26. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high-impedance state.
27. The minimum write cycle pulse width should be equal to sum of t_{SD} and t_{HZWE}.
28. During this period, the I/Os are in output state and input signals should not be applied.

Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X	L	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	Data out (I/O_0–I/O_7)	Read	Active (I_{CC})
L	H	L	X	Data in (I/O_0–I/O_7)	Write	Active (I_{CC})
L	H	H	H	High Z	Output disabled	Active (I_{CC})

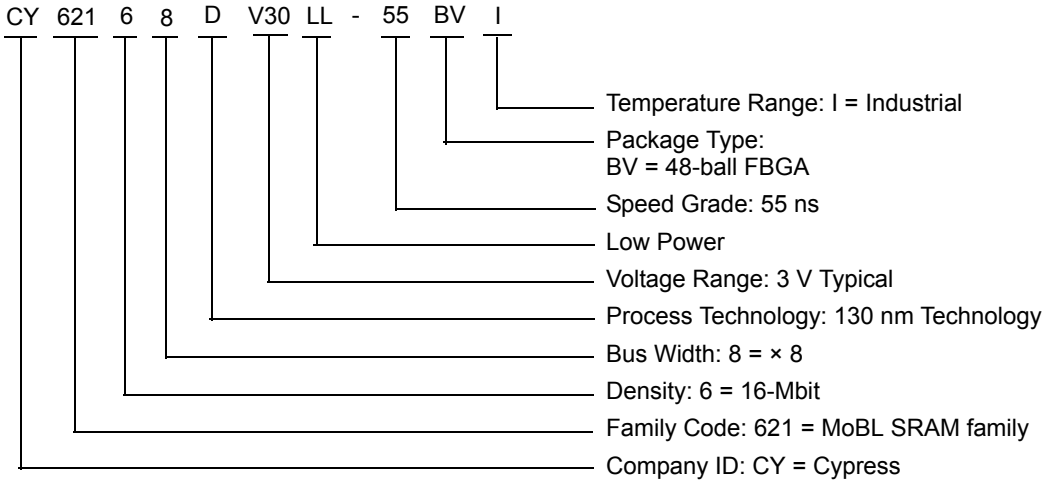
Ordering Information

The following table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at http://www.cypress.com and see product summary page at http://www.cypress.com/products. Cypress maintains a worldwide network of offices, solution centers, manufacturers representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62168DV30LL-55BVI	51-85178	48-ball FBGA (8 × 9.5 × 1 mm)	Industrial

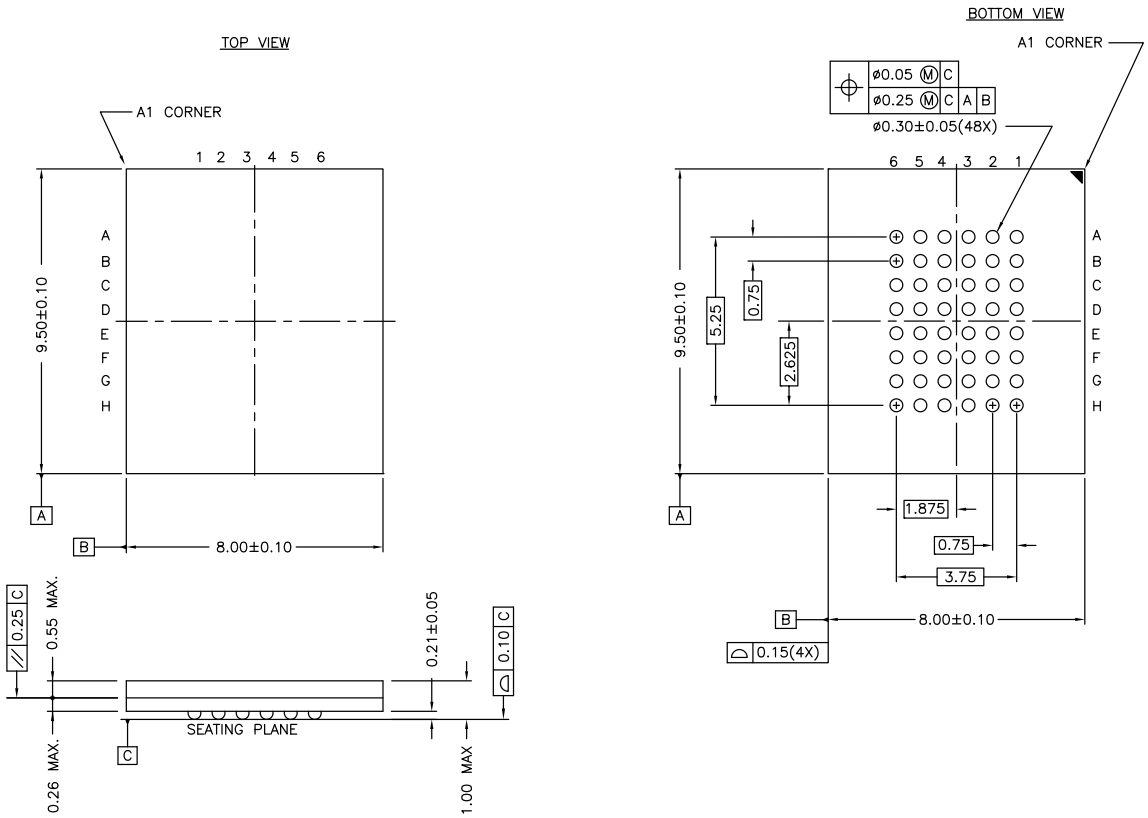
Please contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagram

Figure 9. 48-ball VFBGA (8 × 9.5 × 1.0 mm) BV48B Package Outline, 51-85178



51-85178 *C

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
SRAM	Static Random Access Memory
VFBGA	Very Fine-Pitch Ball Grid Array
TSOP	Thin Small Outline Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62168DV30 MoBL®, 16-Mbit (2 M × 8) Static RAM Document Number: 38-05329				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	118409	GUG	09/30/02	New data sheet.
*A	123693	DPM	02/05/03	Changed status from Advance Information to Preliminary. Added Package Diagram.
*B	126556	DPM	04/24/03	Minor change: Change sunset owner from DPM to HRT
*C	132869	XRJ	01/15/04	Changed status from Preliminary to Final.
*D	272589	PCI	See ECN	Added Pb-free package related information in all instances across the document. Updated Ordering Information.
*E	335864	PCI	See ECN	Updated Pin Configuration: Updated Figure 1 (Added Address A_{20} to ball G2). Updated Ordering Information: Removed redundant packages.
*F	492895	VKN	See ECN	Changed address of Cypress Semiconductor Corporation on Page 1 from “3901 North First Street” to “198 Champion Court” Removed 70 ns speed bin related information in all instances across the document. Removed Low Power parts related information in all instances across the document. Updated Ordering Information.
*G	2914085	NIKM	04/15/10	Updated Ordering Information: Removed inactive parts. Updated Package Diagram.
*H	3070774	RAME	10/27/10	Changed all table notes to footnotes in all instances across the document. Added Ordering Code Definitions. Added Acronyms and Units of Measure. Updated to new template.
*I	3090588	AJU	11/19/10	Post to external web.
*J	3329789	RAME	07/27/11	Updated Functional Description: Removed Note “For best-practice recommendations, please refer to the Cypress application note entitled System Design Guidelines, available at http://www.cypress.com website” and its reference. Updated to new template.
*K	4192919	VINI	11/15/2013	Updated Package Diagram: spec 51-85178 – Changed revision from *A to *C. Updated to new template. Completing Sunset Review.
*L	4574377	VINI	11/19/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*M	5036233	VINI	12/03/2015	Updated Switching Characteristics: Added Note 16 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 27 and referred the same note in Figure 8. Updated to new template. Completing Sunset Review.

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