

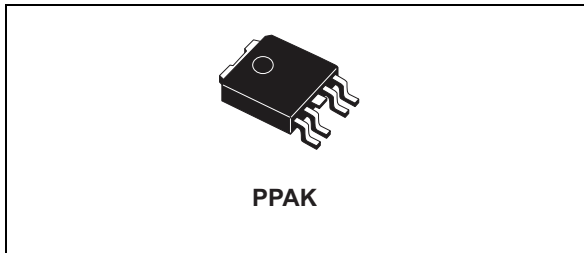


# THE DATASHEET OF ST1L04PT



## Low quiescent current voltage regulator

Datasheet - production data



### Description

The ST1L04 is a low drop adjustable linear voltage regulator, which supplies up to 1 A output current. The output voltage can be as low as 0.8 V. The quiescent current is controlled and maintained well below 3 mA over the whole allowed junction temperature range. The ST1L04 is stable with low ESR output ceramic capacitors only. Internal protection circuitry includes thermal protection with hysteresis and overcurrent limiting. The ST1L04 is especially suitable for applications requiring low voltage outputs from low voltage inputs. Typical applications for this product are: notebook PCs, low voltage ASIC, VID power supplies and low cost post regulation for 3.3 V output voltage switching regulators.

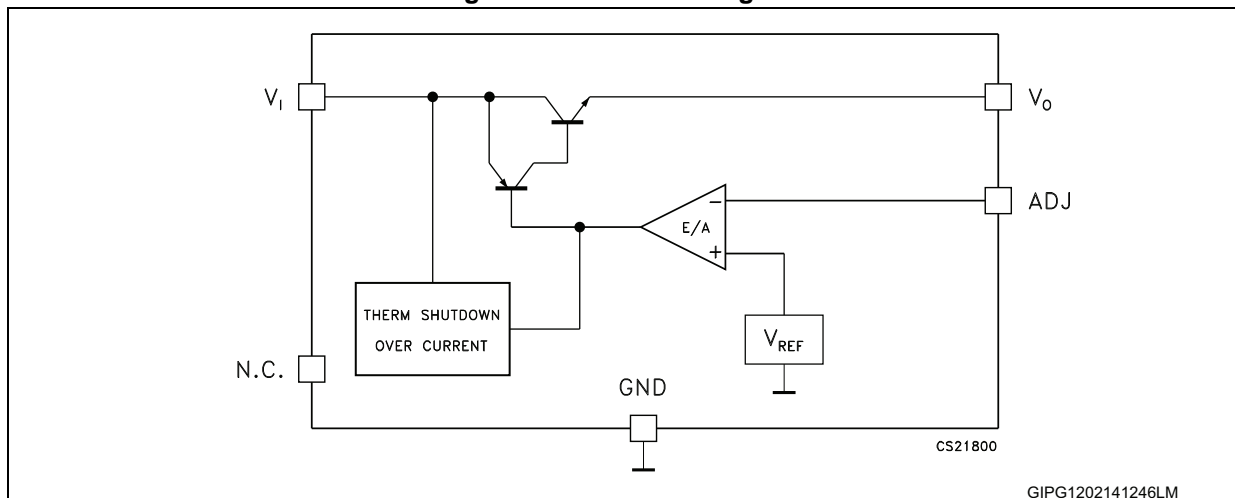
### Features

- Adjustable output voltage from 0.8 V to  $V_I - V_D$
- Internal reference voltage
- Accuracy  $\pm 2\%$  at 25 °C
- Output current capability: 1 A minimum
- Very low quiescent current: max. 3 mA over the whole temperature range
- Maximum dropout 1 V @  $I_O = 1$  A
- Stable with low ESR ceramic capacitors only
- Thermal shutdown protection with hysteresis
- Overcurrent protection
- Operating junction temperature range: from 0 to 125 °C

Table 1. Device summary

Order code	Package
ST1L04PT	PPAK

Figure 1. Schematic diagram



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# 1 Pin description

Figure 2. Pin connection (top view)

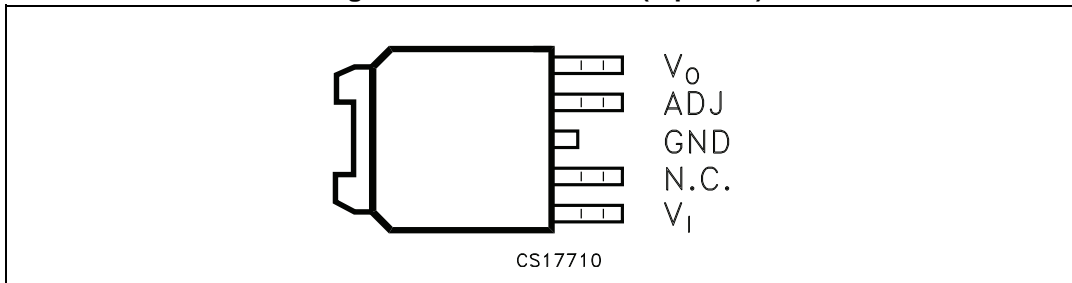
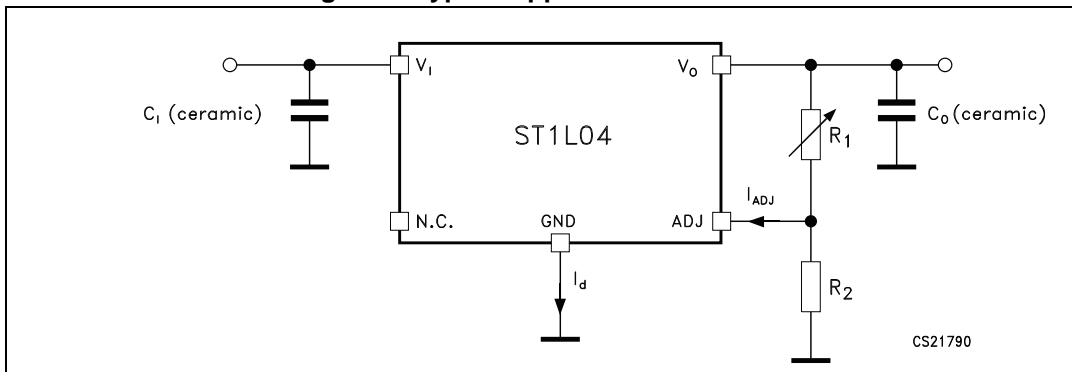


Table 2. Pin description

Pin	Name	Function
1	V <sub>I</sub>	Supply voltage input pin. Bypass with a ceramic capacitor to GND
2	N.C.	Not connected
3	GND	Ground. The exposed metallic pad of the package is connected to GND
4	ADJ	Adjust voltage pin. External resistor divider connection
5	V <sub>O</sub>	Output voltage pin. Bypass with a ceramic capacitor to GND

Figure 3. Typical application schematic



The adjustable output voltage is set by a resistor divider connected between V<sub>O</sub> and GND with its centre tap connected to ADJ. The voltage divider resistors are: R<sub>1</sub> connected between V<sub>O</sub> and ADJ and R<sub>2</sub> connected between ADJ and GND. V<sub>O</sub> is given by V<sub>REF</sub>, R<sub>1</sub>, R<sub>2</sub>, I<sub>ADJ</sub>, as follows:

$$V_O = V_{REF}(1 + R_1/R_2) + I_{ADJ}R_1$$

since I<sub>ADJ</sub> is very small and stable, it can be ignored and the output voltage can be simply calculated as follows:

$$V_O = V_{REF}(1 + R_1/R_2)$$

## 2 Maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_I$	DC supply voltage	From GND -0.3 to 10	V
$P_{TOT}$	Power dissipation	Internally limited	W
$I_O$	Output current	Internally limited	A
$T_{OP}$	Operating junction temperature range	0 to + 125	°C
$T_{STG}$	Storage temperature range	-40 to +150	°C

*Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.*

**Table 4. Thermal data**

Symbol	Parameter	PPAK	Unit
$R_{thj-case}$	Thermal resistance junction-case	8	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	100	°C/W

### 3 Electrical characteristics

Refer to the typical application schematic,  $V_{IN}$  from 2.9 to 5.5 V,  $I_O$  from 10 mA to 1 A,  $C_{IN} = 4.7 \mu\text{F}$ ,  $C_{OUT} = 4.7 \mu\text{F}$ ,  $T_J = 0$  to  $125 \text{ }^\circ\text{C}$ , unless otherwise specified.  $T_J = 25 \text{ }^\circ\text{C}$  unless otherwise specified.

**Table 5. Electrical characteristics**

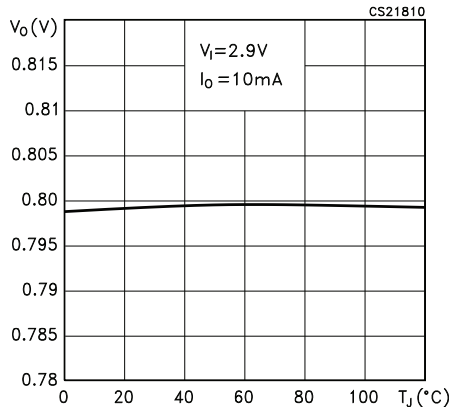
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_I$	Operating input voltage		2.8			V
$I_d$	Quiescent current				3	mA
$V_{REF}$	Reference voltage	$T_J = 25 \text{ }^\circ\text{C}$	0.784	0.8	0.816	V
			0.776	0.8	0.824	
$\Delta V_O$	Line regulation	$I_O = 10 \text{ mA}$			0.8	%
	Load regulation	$V_I = 3.3 \text{ V}$			0.8	%
$I_{ADJ}$	Adjustment current	$I_O = 10 \text{ mA}$			1	$\mu\text{A}$
$I_{\Delta ADJ}$	Adjustment current change				200	nA
$I_{Omin}$	Minimum output current for regulation				100	$\mu\text{A}$
$I_O$	Output current limit		1		1.4	A
$V_d$	Dropout voltage <sup>(1) (2)</sup>	$I_O = 1 \text{ A}$ , $V_O = \text{from } 1.8 \text{ to } 3.3 \text{ V}$			1	V
SVR	Supply voltage rejection <sup>(2)</sup>	$V_I = 3.3 \pm 0.5 \text{ V}$ , $I_O = 10 \text{ mA}$ , $T_J = 25 \text{ }^\circ\text{C}$	$f = 120 \text{ Hz}$	50		dB
			$f = 100 \text{ kHz}$	20		
$C_O$	Ceramic output capacitor value		2.2			$\mu\text{F}$
$C_{ESR}$	Output capacitor ESR value				200	m $\Omega$
eN	Output noise voltage <sup>(2)</sup>	$B = \text{from } 10 \text{ Hz to } 10 \text{ kHz}$ , $V_I = 3.3 \text{ V}$ , $I_O = 10 \text{ mA}$ , $T_J = 25 \text{ }^\circ\text{C}$		0.003		% $V_O$
$T_{SH}$	Thermal shutdown trip point <sup>(2)</sup>	$V_I = 3.3 \text{ V}$		165		$^\circ\text{C}$
$T_{HY}$	Thermal shutdown hysteresis <sup>(2)</sup>	$V_I = 3.3 \text{ V}$		5		$^\circ\text{C}$

1. This parameter is the minimum input-to-output differential voltage required to maintain 1% regulation with respect to the  $V_O$  nominal value. As to  $V_O$  between 0.8 V and 1.8 V included, the  $V_d$  value is overridden by the minimum operating input voltage.

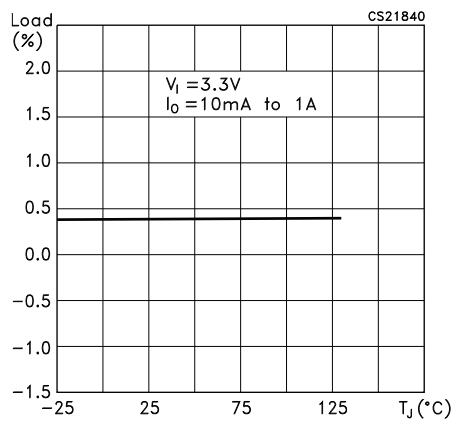
2. Guaranteed by design. Not tested in production.

# 4 Typical characteristics

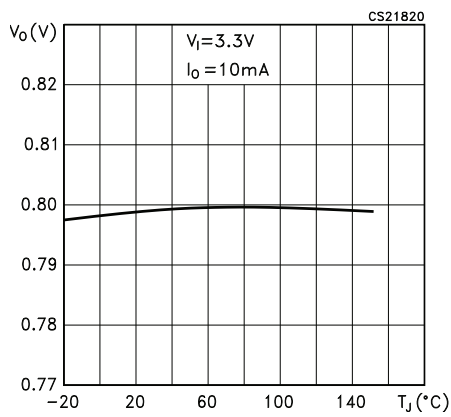
**Figure 4. Output voltage vs. temperature**  
 $V_I = 2.9\text{ V}$



**Figure 5. Load regulation vs. temperature**



**Figure 6. Output voltage vs. temperature**  
 $V_I = 3.3\text{ V}$



**Figure 7. Quiescent current vs. temperature**  
 $I_O = 1\text{ A}$

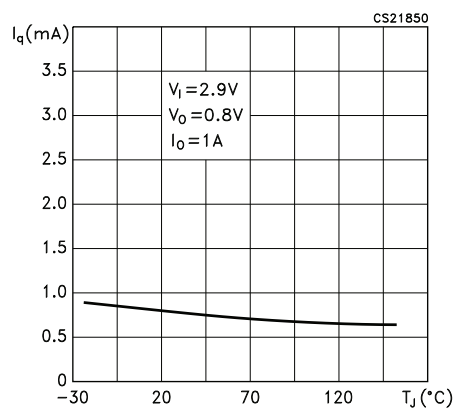


Figure 8. Line regulation vs. temperature

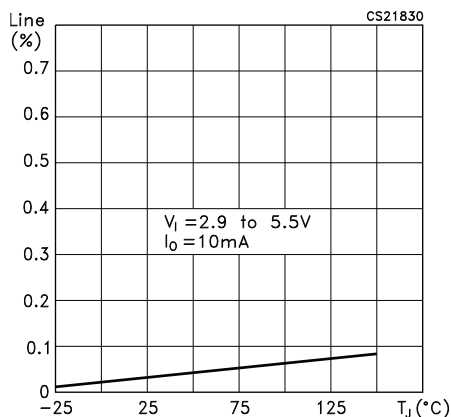


Figure 9. Quiescent current vs. temperature  
 $I_O = 10\text{ mA}$

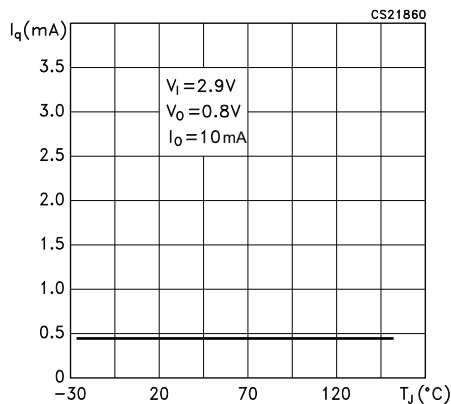


Figure 10. Quiescent current vs. output current

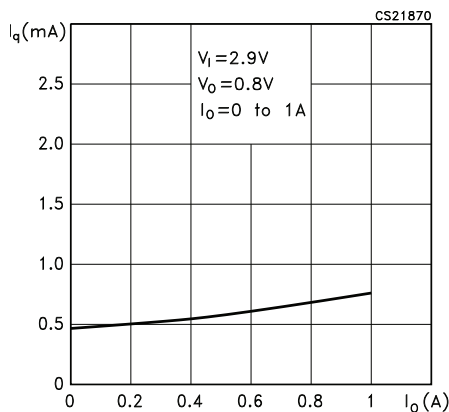


Figure 11. Dropout voltage vs. output current

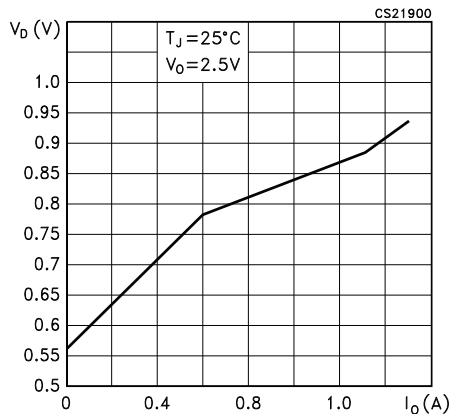


Figure 12. Quiescent current vs. input voltage

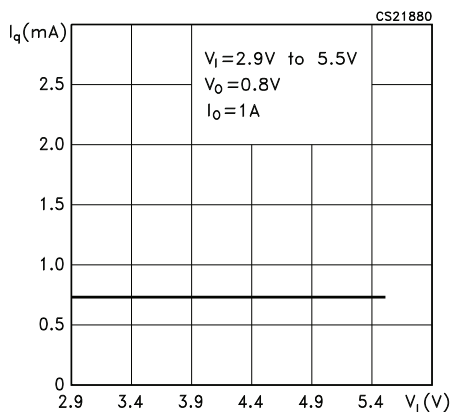


Figure 13. Supply ripple rejection vs. temperature  
 $f = 100\text{ kHz}$

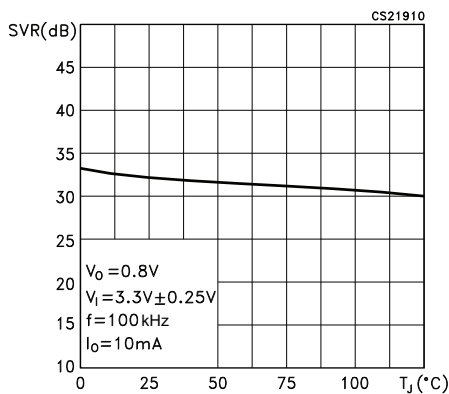


Figure 14. Dropout voltage vs. temperature

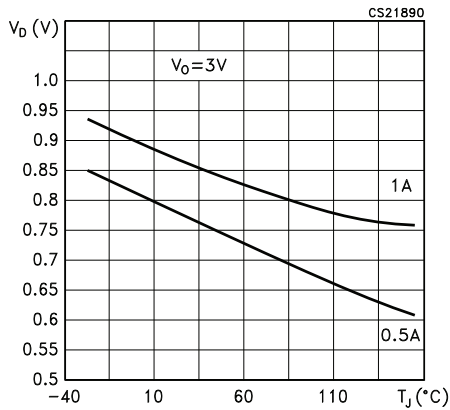


Figure 15. Supply ripple rejection vs. temperature  $f=102$  Hz

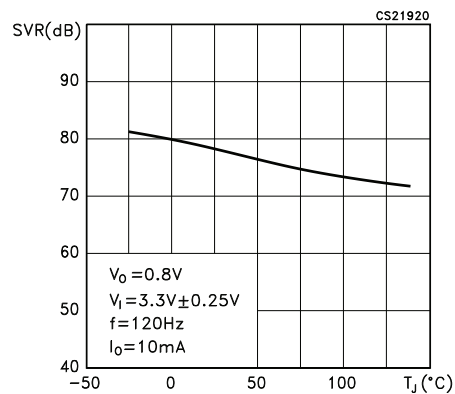


Figure 16. Supply ripple rejection vs. output current

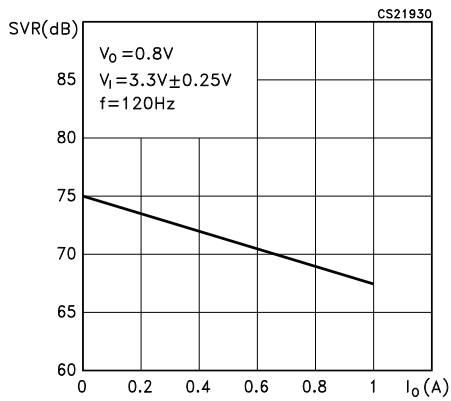


Figure 17. Adjustment current change vs. temperature

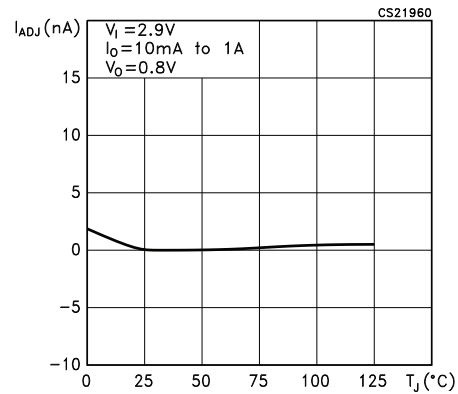


Figure 18. Supply ripple rejection vs. frequency

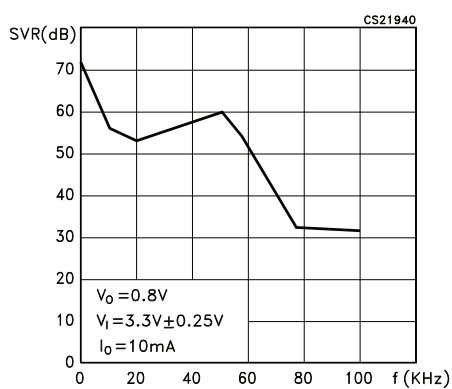


Figure 19. Minimum output current for regulation vs. temperature  $V_I = 5.5$  V

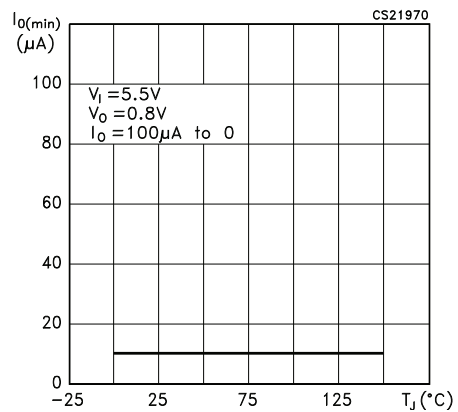


Figure 20. Adjustment current vs. temperature

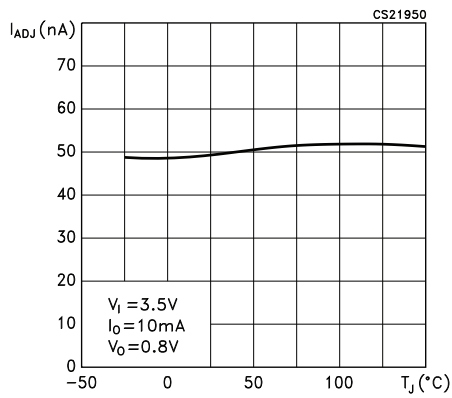


Figure 21. Minimum output current for regulation vs. temperature  $V_I = 2.6V$

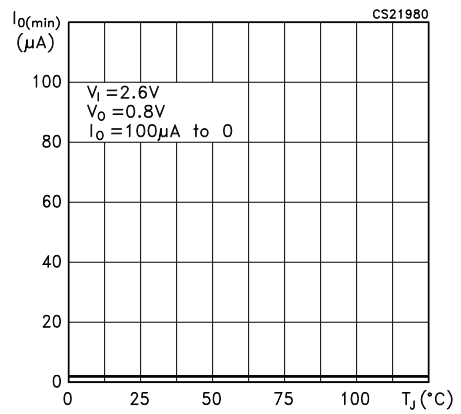


Figure 22. Load transient

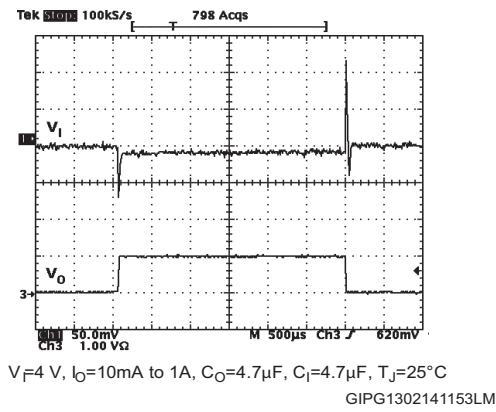
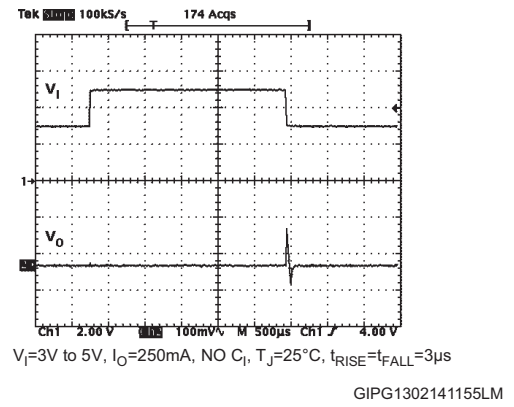


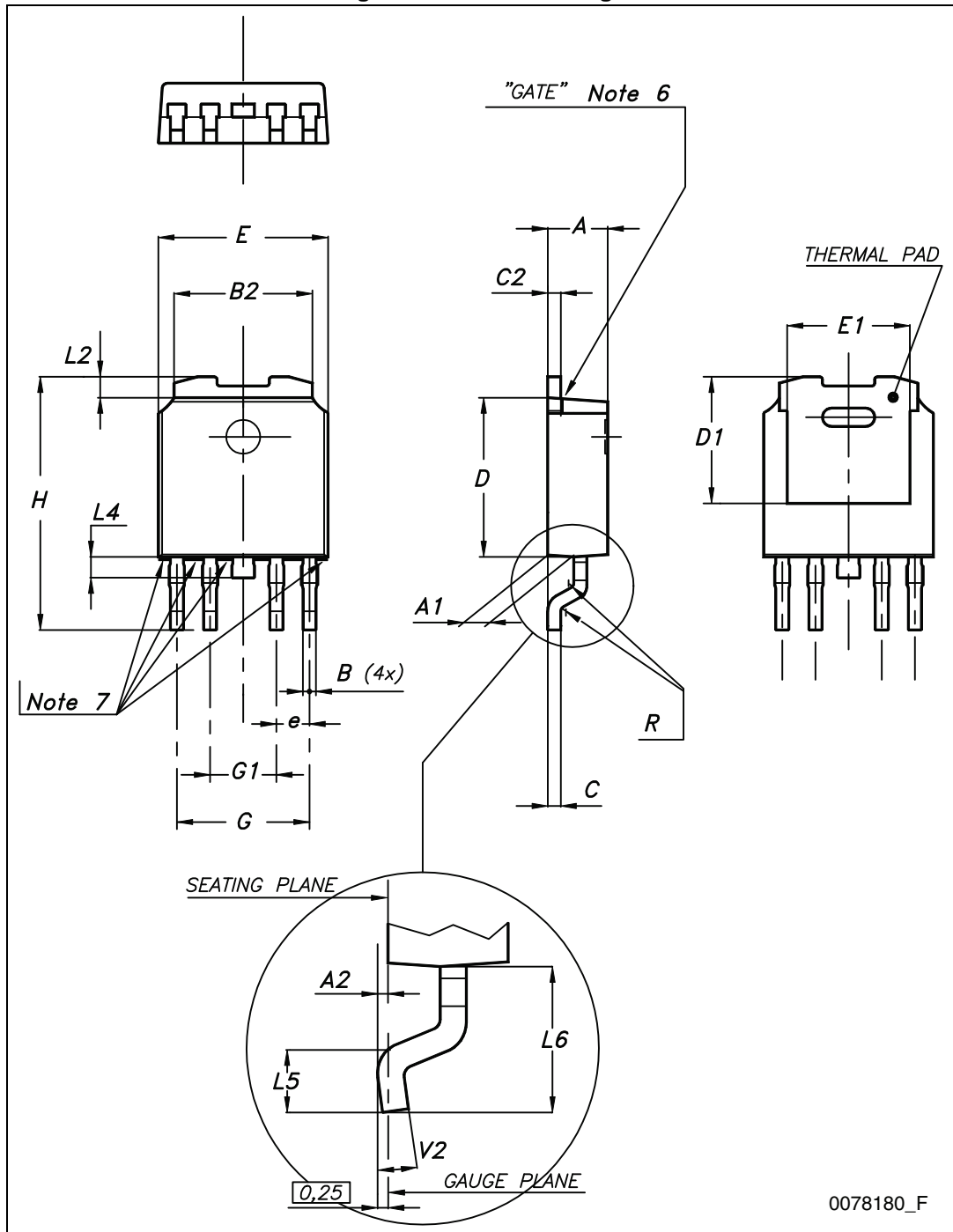
Figure 23. Line transient



## 5 ECOPACK®

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Figure 24. PPAK drawings



0078180\_F

Table 6. PPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.2		2.4
A1	0.9		1.1
A2	0.03		0.23
B	0.4		0.6
B2	5.2		5.4
C	0.45		0.6
C2	0.48		0.6
D	6		6.2
D1		5.1	
E	6.4		6.6
E1		4.7	
e		1.27	
G	4.9		5.25
G1	2.38		2.7
H	9.35		10.1
L2		0.8	1
L4	0.6		1
L5	1		
L6		2.8	
R		0.20	
V2	0°		8°

# 6 Packaging mechanical data

Figure 25. Tape for PPAK

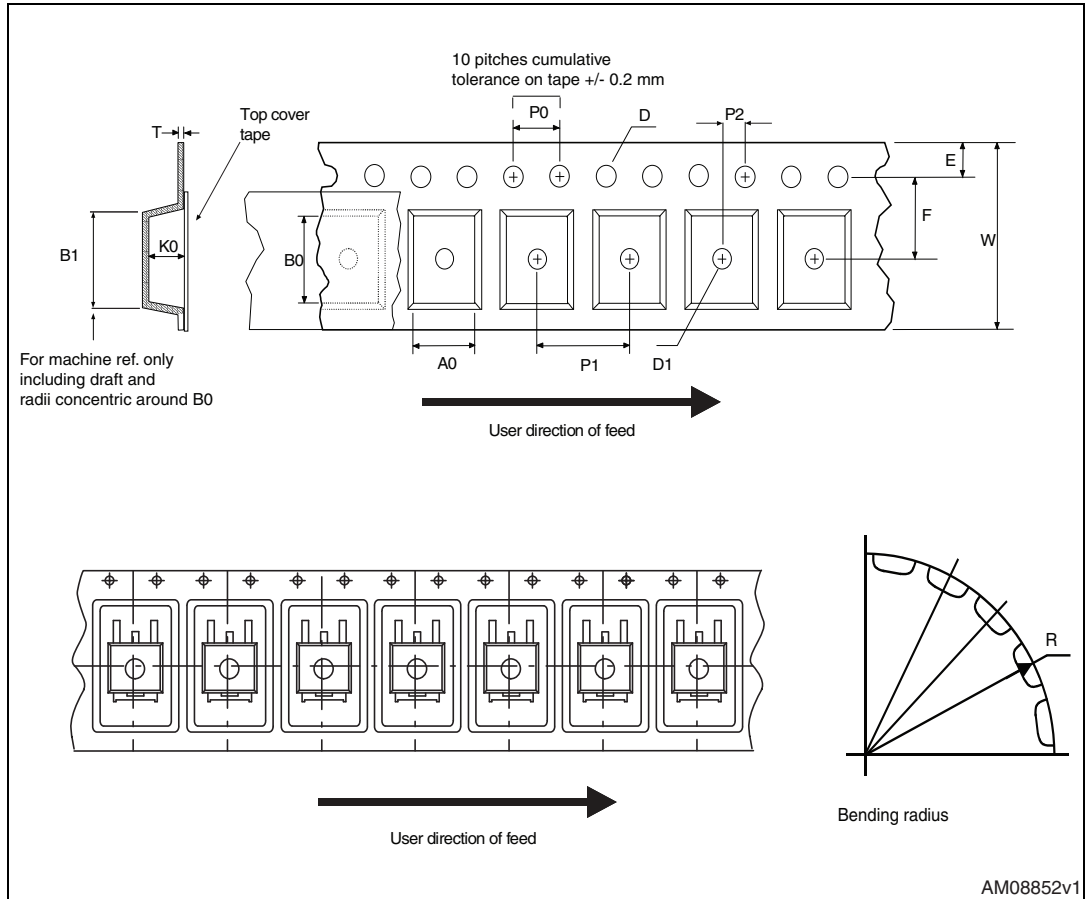


Figure 26. Reel for PPAK

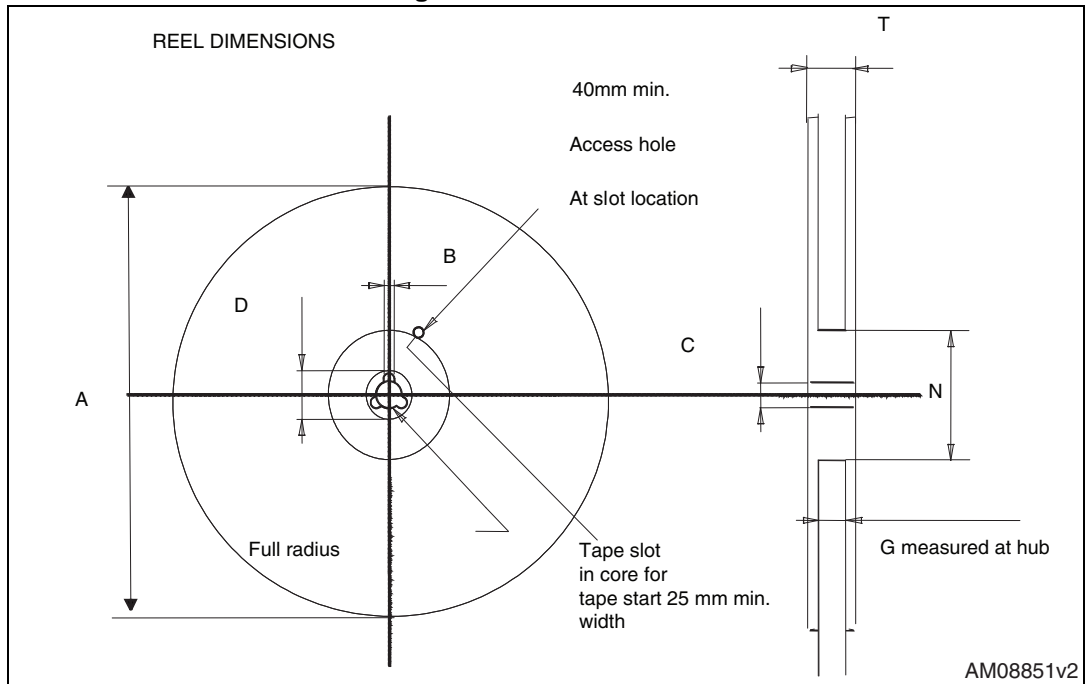


Table 7. PPAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base quantity		2500
P1	7.9	8.1	Bulk quantity		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 7 Revision history

Table 8. Document revision history

Date	Revision	Changes
10-Feb-2005	1	Initial release.
05-Mar-2014	2	Updated <i>Features</i> . Updated <i>Table 5</i> . Changed title of <i>Figure 4</i> , <i>Figure 6</i> , <i>Figure 7</i> , <i>Figure 15</i> , <i>Figure 19</i> and <i>Figure 21</i> . Updated <i>Figure 9</i> and <i>Figure 13</i> . Minor text changes.

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