



**THE DATASHEET OF
SG723T-883B**



Precision Voltage Regulator

Description

This monolithic voltage regulator is designed for use with either positive or negative supplies as a series, shunt, switching, or floating regulator with currents up to 150 mA. Higher current requirements may be accommodated through the use of external NPN or PNP power transistors. This device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor, current limit, and remote shutdown circuitry.

The SG723 will operate over the full military ambient temperature range of -55°C to 125°C.

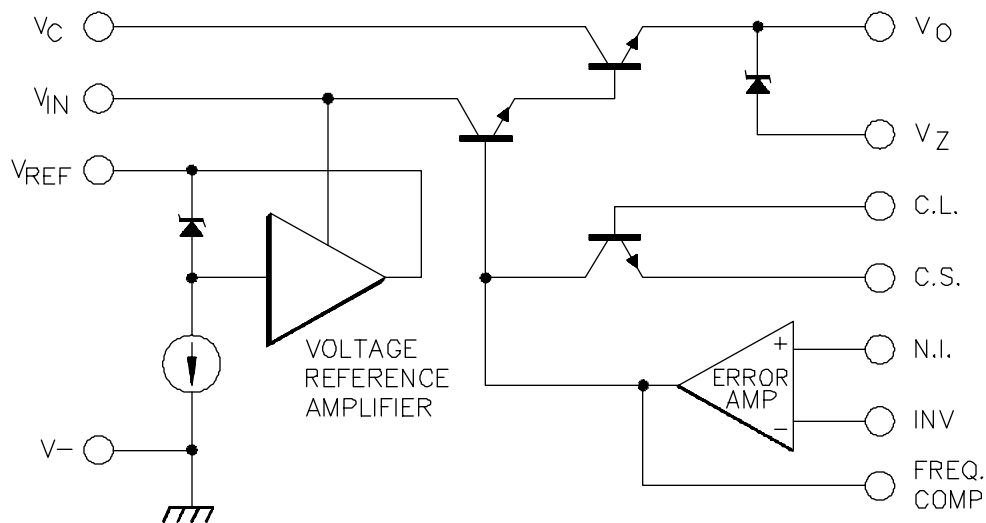
Features

- Positive or Negative Supply Operation
- Series, Shunt, Switching or Floating Operation
- Low Line and Load Regulation
- Output Adjustable from 2 V to 37 V
- Output Current to 150 mA
- Low Standby Current Drain
- 0.002%/°C Average Temperature Variation

High Reliability Features

- MIL-M38510/10201BHA - SG723F-JAN
- MIL-M38510/10201BIA - SG723T-JAN
- MIL-M38510/10201BCA - SG723J-JAN
- MSC-AMS Level "S" Processing Available

Block Diagram



Absolute Maximum Ratings (Note 1)

| | | | |
|--|--------|---|----------------|
| Pulse (50 ms) Input Voltage from V_{IN} to V_- | 50 V | Current from V_{REF} | 15 mA |
| Continuous Input Voltage from V_{IN} to V_- | 40 V | Operating Junction Temperature | |
| Input to Output Voltage Differential | 40 V | Hermetic (T, J, F - Packages)..... | 150°C |
| Maximum Output Current | 150 mA | Storage Temperature Range | -65°C to 150°C |
| Current from V_Z (J-Package only)..... | 25 mA | Lead Temperature (Soldering, 10 s)..... | 300°C |

Note 1. Exceeding these ratings could cause damage to the device.

Thermal Data

J Package:

| | |
|---|--------|
| Thermal Resistance-Junction to Case, θ_{JC} | 30°C/W |
| Thermal Resistance-Junction to Ambient, θ_{JA} | 80°C/W |

T Package:

| | |
|---|---------|
| Thermal Resistance-Junction to Case, θ_{JC} | 25°C/W |
| Thermal Resistance-Junction to Ambient, θ_{JA} | 130°C/W |

F Package:

| | |
|---|---------|
| Thermal Resistance-Junction to Case, θ_{JC} | 80°C/W |
| Thermal Resistance-Junction to Ambient, θ_{JA} | 145°C/W |

Note A. Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.

Note B. The above numbers for θ_{JC} are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

Recommended Operating Conditions (Note 2)

| | | | |
|----------------------------|-------------------------------|-------------------------------------|----------------|
| Input Voltage Range | ($V_{OUT} + 4.5 V$) to 38 V | Zener Current (J-Package only)..... | 5 mA |
| Output Current Range | 5 mA to 45 mA | Operating Ambient Temperature Range | |
| Reference Current..... | 5 mA | SG723 | -55°C to 125°C |

Note 2. Range over which the device is functional.

Electrical Characteristics

(Unless otherwise specified, these specifications apply for the operating ambient temperature of $T_A = 25^\circ\text{C}$, $V_{IN} = V_C = 12\text{ V}$, $V_- = 0\text{ V}$, $V_{OUT} = 5\text{ V}$, $I_L = 1\text{ mA}$, $R_{SC} = 0\ \Omega$, $C_1 = 100\text{ pF}$, and divider impedance as seen by error amplifier $\leq 10\text{ k}\Omega$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

| Parameter | Test Conditions | SG723 | | | Units |
|--------------------------------|---|-------|-------|-------|---------------------|
| | | Min. | Typ. | Max. | |
| Input Voltage Range | | 9.5 | | 40 | V |
| Output Voltage Range | | 2.0 | | 37 | V |
| Input to Output Differential | | 3.0 | | 38 | V |
| Line Regulation (Note 3) | $V_{IN} = 12\text{ V to }15\text{ V}$ $T_A = T_{MIN} \text{ to } T_{MAX}$ $V_{IN} = 12\text{ V to }40\text{ V}$ | | 0.01 | 0.1 | % V_{OUT} |
| | | | | 0.3 | % V_{OUT} |
| Load Regulation (Note 3) | $I_L = 1 \text{ to } 50\text{ mA}$ $T_A = T_{MIN} \text{ to } T_{MAX}$ | | 0.02 | 0.2 | % V_{OUT} |
| | | | 0.03 | 0.15 | % V_{OUT} |
| Ripple Rejection | $f = 50\text{ Hz to }10\text{ kHz}$ $C_{REF} = 0$ | | | 0.6 | % V_{OUT} |
| | $C_{REF} = 5\ \mu\text{F}$ | | 74 | | dB |
| Temperature Stability (Note 4) | $T_A = T_{MIN} \text{ to } T_{MAX}$ | | 86 | | dB |
| Short Circuit Current Limit | $R_{SC} = 10\ \Omega$ | | 0.002 | 0.015 | %/°C |
| Reference Voltage | | 6.95 | 65 | | mA |
| Output Noise Voltage | $BW = 100\text{ Hz to }10\text{ kHz}$ | | 7.15 | 7.35 | V |
| | $C_{REF} = 0$ | | 20 | | μV_{rms} |
| | $C_{REF} = 5\ \mu\text{F}$ | | 2.5 | | μV_{rms} |
| Standby Current Drain | $I_L = 0, V_{IN} = 30\text{ V}$ | | 2.3 | 3.5 | mA |
| Long Term Stability | | | 0.1 | | %/khr |

Note 3. Applies for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

Note 4. These parameters, although guaranteed, are not tested in production.

Characteristic Curves

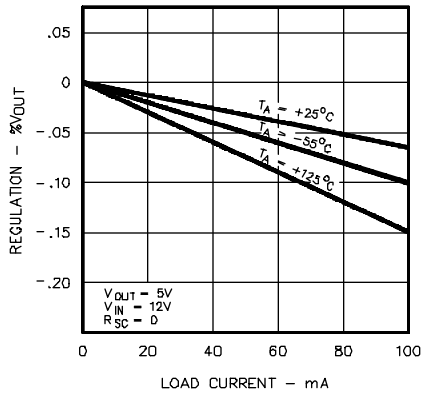


Figure 1. Load Regulation

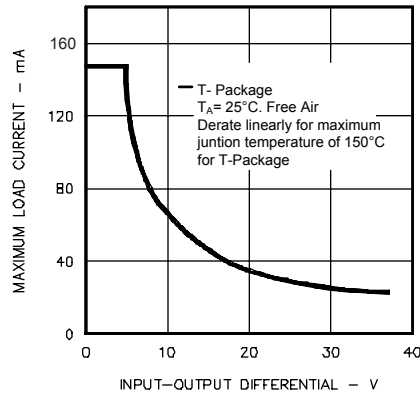


Figure 2. Maximum Load Current

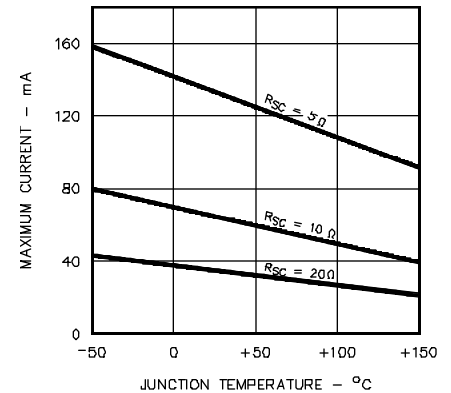


Figure 3. Current Limiting Characteristics

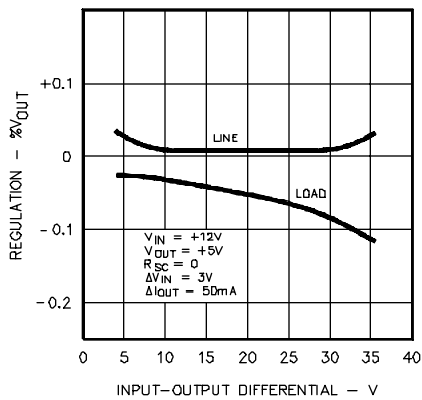


Figure 4. Regulations vs. Input-Output Voltage Regulation

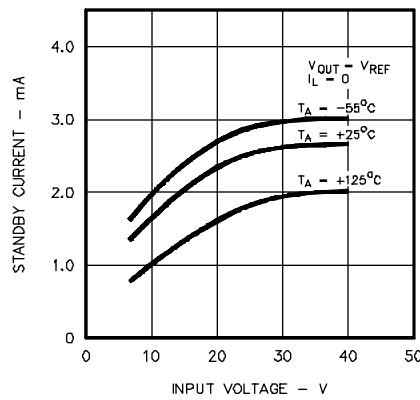


Figure 5. Standby Current Drain

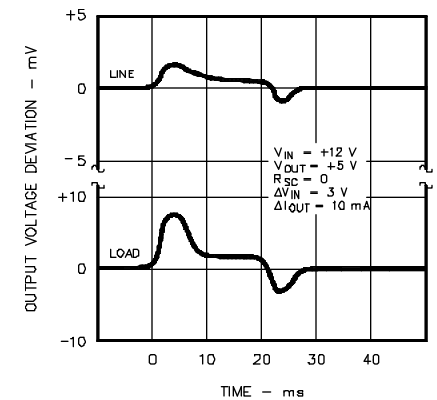


Figure 6. Transient Response

Application Information

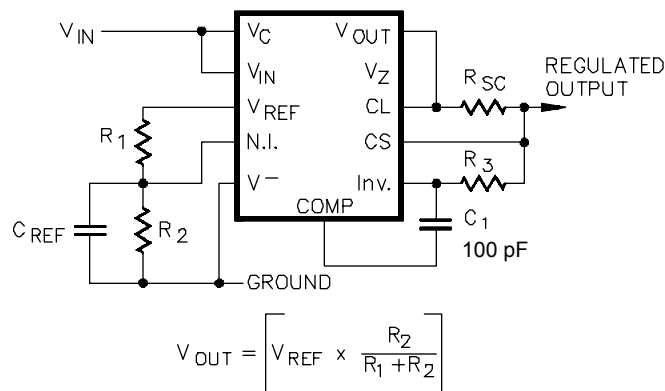


Figure 7 - Basic Low Voltage Regulator $V_{OUT} = 2 \text{ V TO } 7 \text{ V}$

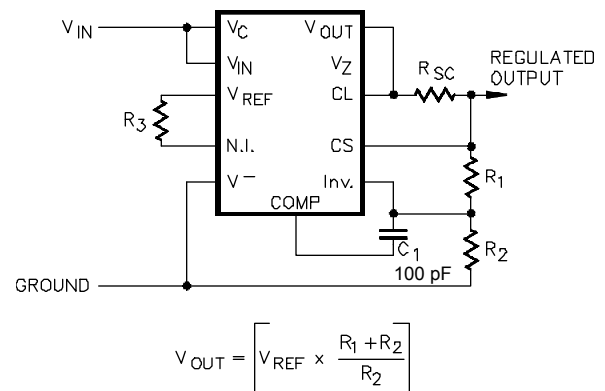


Figure 8 - Basic High Voltage Regulator $V_{OUT} = 7 \text{ V TO } 37 \text{ V}$

Application Information (Continued)

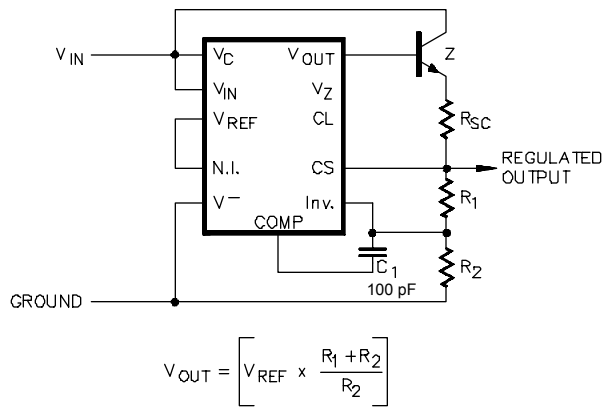


Figure 9 - High Current Regulator External NPN Transistor $I_L = 1.0 \text{ A}$

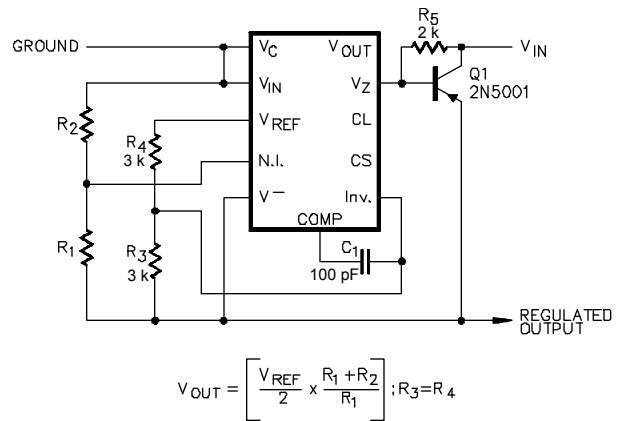


Figure 10 - Negative Voltage Regulator

Connection Diagrams and Ordering Information (See Notes Below)

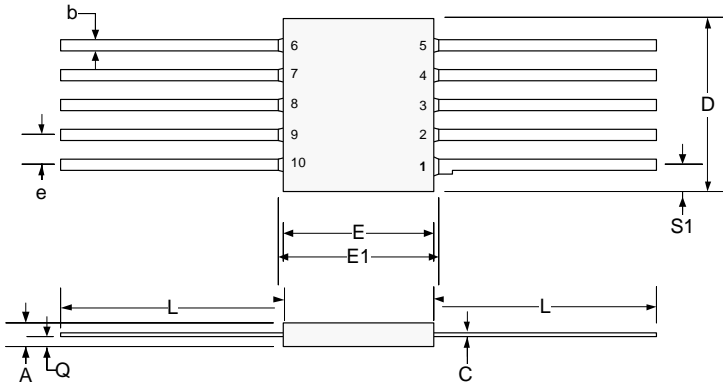
| Package | Part Number | Ambient Temperature Range | Connection Diagram |
|--------------------------------------|----------------------|----------------------------------|--------------------|
| 10-PIN CERAMIC FLAT PACK F - PACKAGE | SG723F-JAN | -55°C to 125°C | (Note 3) |
| 14-PIN CERAMIC DIP J - PACKAGE | SG723J-JAN | -55°C to 125°C | |
| 10-PIN METAL CAN T - PACKAGE | SG723T-JAN SG723T | -55°C to 125°C -55°C to 125°C | (Notes 3 & 4) |

Note 1. Contact factory for JAN product availability.
 Note 2. All packages are viewed from the top. Lead finish is Sn63/Pb37 for RoHS compliant version contact factory.

Note 3. V_Z output is not available in T, F-packages.
 Note 4. Pin 5 is connected to case.

Package Outline Dimensions

Controlling dimensions are in inches, metric equivalents are shown for general information.

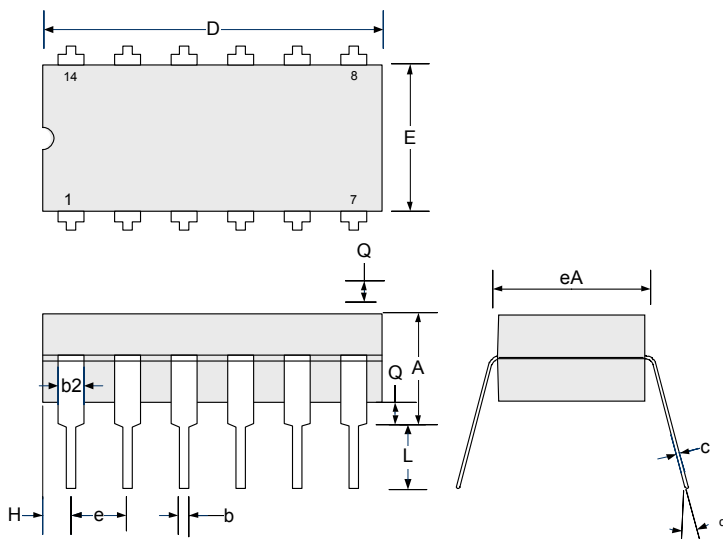


| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.45 | 1.90 | 0.057 | 0.075 |
| b | 0.25 | 0.483 | 0.010 | 0.019 |
| c | 0.102 | 0.152 | 0.004 | 0.006 |
| D | - | 7.37 | - | 0.290 |
| E | 6.04 | 6.40 | 0.238 | 0.252 |
| E1 | - | 6.91 | - | 0.272 |
| e | 1.27 BSC | | 0.050 BSC | |
| L | 6.35 | 9.40 | 0.250 | 0.370 |
| Q | 0.51 | 1.02 | 0.020 | 0.040 |
| S1 | 0.20 | 0.38 | 0.008 | 0.015 |

Note:

1. Lead No. 1 is identified by tab on lead or dot on cover.
2. Leads are within 0.13 mm (.0005") radius of the true position (TP) at maximum material condition.
3. Dimension "e" determines a zone within which all body and lead irregularities lie.
4. Dimensions are in mm, inches are for reference only.

Figure 11 · F 10-Pin Ceramic Flat-pack Package Outline Dimensions



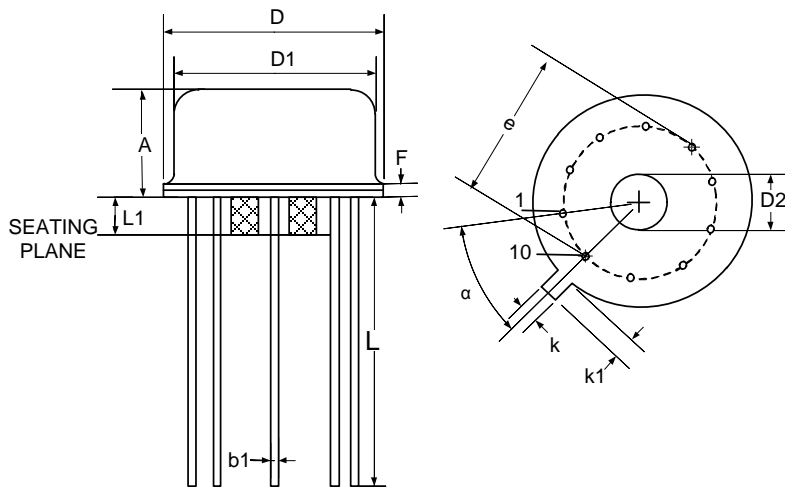
| DIM | MILLIMETERS | | INCHES | |
|-------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | - | 5.08 | - | 0.200 |
| b | 0.38 | 0.51 | 0.015 | 0.020 |
| b2 | 1.04 | 1.65 | 0.045 | 0.065 |
| c | 0.20 | 0.38 | 0.008 | 0.015 |
| D | 19.30 | 19.94 | 0.760 | 0.785 |
| E | 5.59 | 7.11 | 0.220 | 0.280 |
| e | 2.54 BSC | | 0.100 BSC | |
| eA | 7.37 | 7.87 | 0.290 | 0.310 |
| H | 0.63 | 1.78 | 0.025 | 0.070 |
| L | 3.18 | 5.08 | 0.125 | 0.200 |
| alpha | - | 15° | - | 15° |
| Q | 0.51 | 1.02 | 0.020 | 0.040 |

Note:

Dimensions do not include protrusions; these shall not exceed 0.155 mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 12 · J 14-Pin Ceramic Dip Package Dimensions

Package Outline Dimensions (Continued)



| DIM | MILLIMETERS | | INCHES | |
|----------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| D | 8.890 | 9.398 | 0.350 | 0.370 |
| D1 | 8.00 | 8.51 | 0.315 | 0.335 |
| A | 4.191 | 4.699 | 0.165 | 0.185 |
| b1 | 0.406 | 0.533 | 0.016 | 0.021 |
| F | - | 1.016 | - | 0.040 |
| e | 5.842 TYP | | 0.230 TYP | |
| k | 0.711 | 0.864 | 0.028 | 0.034 |
| k1 | 0.737 | 1.143 | 0.029 | 0.045 |
| L | 12.70 | 14.48 | 0.500 | 0.570 |
| α | 36° TYP | | 36° TYP | |
| D2 | 3.556 | 4.064 | 0.140 | 0.160 |
| L1 | 0.254 | 1.016 | 0.010 | 0.040 |

Note:

Dimensions do not include protrusions; these shall not exceed 0.155 mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 13 · T 10-Pin Metal Can Package Dimensions



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