THE DATASHEET OF

SC185HULTRT-A0

SC185

4A Synchronous Step-Down Regulator

Features

- V_{IN} Range: 2.9 – 5.5V
- V_{OUT} Options: 1.0V to 3.3V
- Up to 4A Output Current
- Ultra-Small Footprint, <1mm Height Solution
- 1.5MHz Switching Frequency
- Optional Power Save Mode Operation
- Efficiency Up to 95%
- Low Output Noise Across Load Range
- Excellent Transient Response
- Start Up into Pre-Bias Output
- 100% Duty-Cycle Low Dropout Operation
- <1µA Shutdown Current
- Externally Programmable Soft Start Time
- Power Good indicator
- Input Under-Voltage Lockout
- Output Over-Voltage, Current Limit Protection
- Over-Temperature Protection
- 3mm x 3mm x 0.6mm thermally enhanced MLPQ-UT16 package
- -40 to +85°C Temperature Range
- Pb-free, Halogen free, and RoHS/WEEE compliant

Applications

- Desktop Computing
- Set-Top Box
- LCD TV
- Network Cards
- Printer

Description

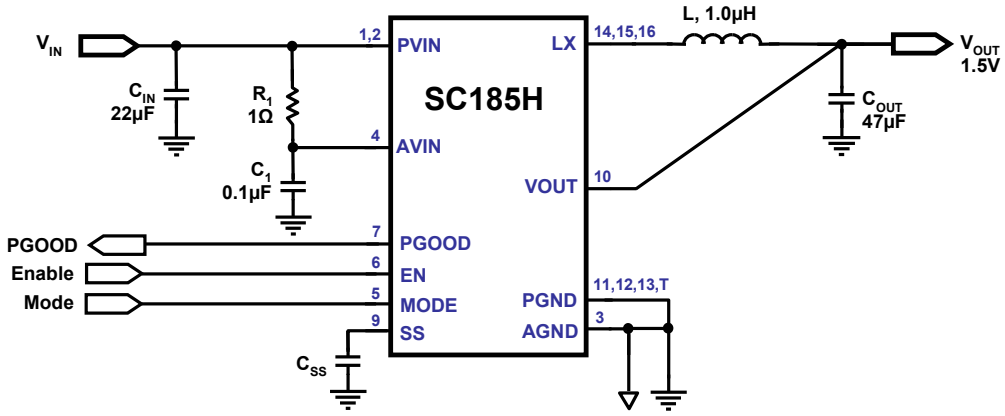
The SC185 is a 4A synchronous step-down regulator designed to operate with an input voltage range of 2.9V to 5.5V. The device requires only three external filter components for a complete a step down regulator solution. The output voltage is factory predetermined with an available range of 1.0V to 3.3V.

The SC185 is optimized for maximum efficiency over a wide range of load currents. During full load operation, the SC185 operates in PWM mode with fixed 1.5MHz oscillator frequency, allowing the use of small surface mount external components. As the load decreases, the regulator has the option to transition into Power Save mode maintaining high efficiency or stay in forced PWM mode operation.

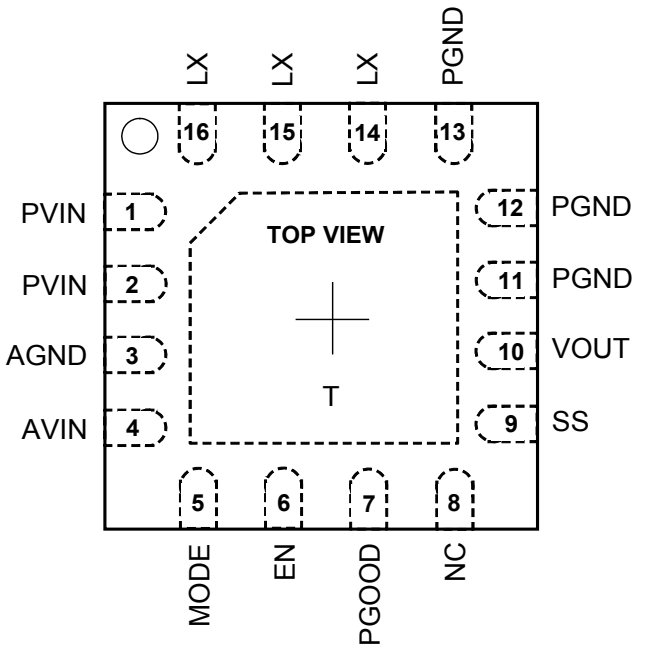
The SC185 offers output short circuit and thermal protection to safe guard the device under extreme operating conditions. The enable pin provides on/off control of the regulator. When connected to logic low, the device enters shutdown and consumes less than 1uA of current. Other protection features include programmable soft start with Power Good indicator, over voltage protection and under voltage lockout.

The SC185 is available in a thermally-enhanced, 3mm x 3mm x 0.6mm MLPQ-UT16 package and has a rated temperature range of -40 to +85°C.

Typical Application Circuit



Pin Configuration



3mm x 3mm x 0.6mm MLPQ-UT16

θ_{JA} = 40°C/W (1); θ_{JC} = 7°C/W

Ordering Information

Device	Package
SC185xULTRT(2)(3)(4)	3mm x 3mm x 0.6mm MLPQ-UT16
SC185xEVB(5)	Evaluation Board

Notes:

(1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

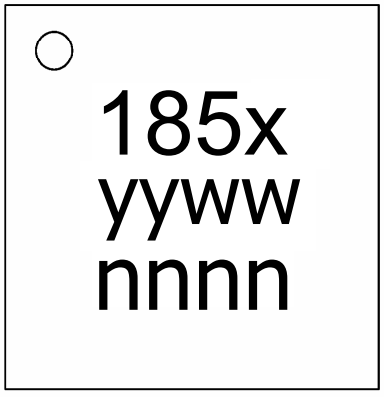
(2) Available in tape and reel only. A reel contains 3,000 devices.

(3) Device is Pb-free, Halogen free, and RoHS/WEEE compliant.

(4) "x" is the code of the output voltage. See Table 1 for the code. For example, the device number for VOUT= 1.50V is SC185HULTRT.

(5) "x" is the code of the output voltage. See Table 1 for the code. For example, the EVB with VOUT= 1.50V is SC185HEVB.

Marking Information



Marking for 3mm x 3mm MLPQ-UT 16 Lead Package:
x = Code of the output voltage (Example: H for VOUT=1.50V)
yyww = Datecode (Example: 0852)
nnnn = Semtech Lot number (Example: E901)

Table 1: Available Output Voltages

Code	VOUT(6)
B	1.00
E	1.20
H	1.50
J	1.80
L	2.50
Q	3.30

Notes:

(6) Contact factory for alternative output voltage options.

Absolute Maximum Ratings

PVIN and AVIN Supply Voltages ..... -0.3 to 6.0V
LX Voltage[9] ..... -0.3 to PVIN+0.3V, 6V Max
VOUT Voltage ..... -0.3 to AVIN+0.3V
CTLx pins Voltages ..... -0.3 to AVIN+0.3V
Peak IR Reflow Temperature ..... 260°C
ESD Protection Level[8] 3kV

Recommended Operating Conditions

Supply Voltage PVIN and AVIN ..... 2.9 to 5.5V
Maximum Output Current 4.0A
Temperature Range ..... -40 to +85°C
Input Capacitor 22uF
Output Capacitor ..... 47uF (or 2 x 22uF)
Output Inductor 1.0uH

Thermal Information

Thermal Resistance, Junction to Ambient[7] ..... 40 °C/W
Thermal Resistance, Junction to Case ..... 7 °C/W
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65 to +150 °C

Exceeding the absolute maximum ratings may result in permanent damage to the device and/or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

Notes:
(7) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.
(8) Tested according to JEDEC standard JESD22-A114-B.
(9) Due to parasitic board inductance, the transient LX pin voltage at the point of measurement may appear larger than that which exists on silicon. The device is designed to tolerate the short duration transient voltages that will appear on the LX pin due to the deadtime diode conduction, for inductor currents up to the current limit setting of the device.

Electrical Characteristics

Unless specified: PVIN= AVIN= 5.0V, VOUT= 1.50V, C_{IN}= 22µF, C_{OUT}= 2 x 22µF; L= 1.0µH; -40°C≤ T_J ≤ +125 °C; Unless otherwise noted typical values are T_A= +25 °C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Under-Voltage Lockout	UVLO	Rising AVIN, PVIN=AVIN	2.70	2.80	2.90	V
		Hysteresis		300		mV
Output Voltage Tolerance[10]	ΔV_{OUT}	PVIN= AVIN= 2.9 – 5.5V; I_{OUT}=0A	-1.25		+1.25	%
Current Limit	I_{LIMIT}	Peak LX current	5.0	6.0	7.0	A
Supply Current	I_Q	No load, MODE= High		12		mA
		No load, MODE= Low		100		µA
Shutdown Current	I_{SHDN}	EN= AGND		1	10	µA
High Side Switch Resistance[11]	R_{DSON_P}	I_{LX}= 100mA, T_J= 25 °C		50		mΩ
Low Side Switch Resistance[11]	R_{DSON_N}	I_{LX}= -100mA, T_J= 25 °C		35		
L_X Leakage Current[11]	$I_{LK(LX)}$	PVIN= AVIN= 5.5V; LX= 0V; EN= AGND		1	10	µA
		PVIN= AVIN= 5.5V; LX= 5.0V; EN= AGND	-20	-1		
Load Regulation	$\Delta V_{LOAD-REG}$	PVIN= AVIN= 5.0V, MODE=Hi, I_{OUT}=1mA – 4A		±0.3		%
Oscillator Frequency	f_{OSC}		1.275	1.5	1.725	MHz
Soft-Start Charging Current[11]	I_{SS}			+5		µA
Foldback Holding Current	I_{CL_HOLD}	Average LX Current		1		A

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Impedence of PGOOD Low	R_{PGOOD_LO}			10		Ω
PGOOD Threshold	V_{PG_TH}	VOUT rising		90		%
PGOOD Delay	V_{PG_DLY}	Asserted		2		ms
		PGOOD= Low		20		µs
EN Delay	t_{EN_DLY}	From EN Input High to SS starts rising		50		µs
EN Input Current(11)	$I_{EN\_}$	EN =AVIN or AGND	-2.0		2.0	µA
EN Input High Threshold	V_{EN_HI}		1.2			V
EN Input Low Threshold	V_{EN_LO}				0.4	V
MODE Input Current(11)	$I_{MODE\_}$	MODE= AVIN or AGND	-2.0		2.0	µA
MODE Input High Threshold	V_{MODE_HI}		1.2			V
MODE Input Low Threshold	V_{MODE_LO}				0.4	V
V_{OUT} Over Voltage Protection	V_{OVP}		110	115	120	%
Thermal Shutdown Temperature	T_{SD}			160		°C
Thermal Shutdown Hysteresis	T_{SD_HYS}			10		°C

Notes:

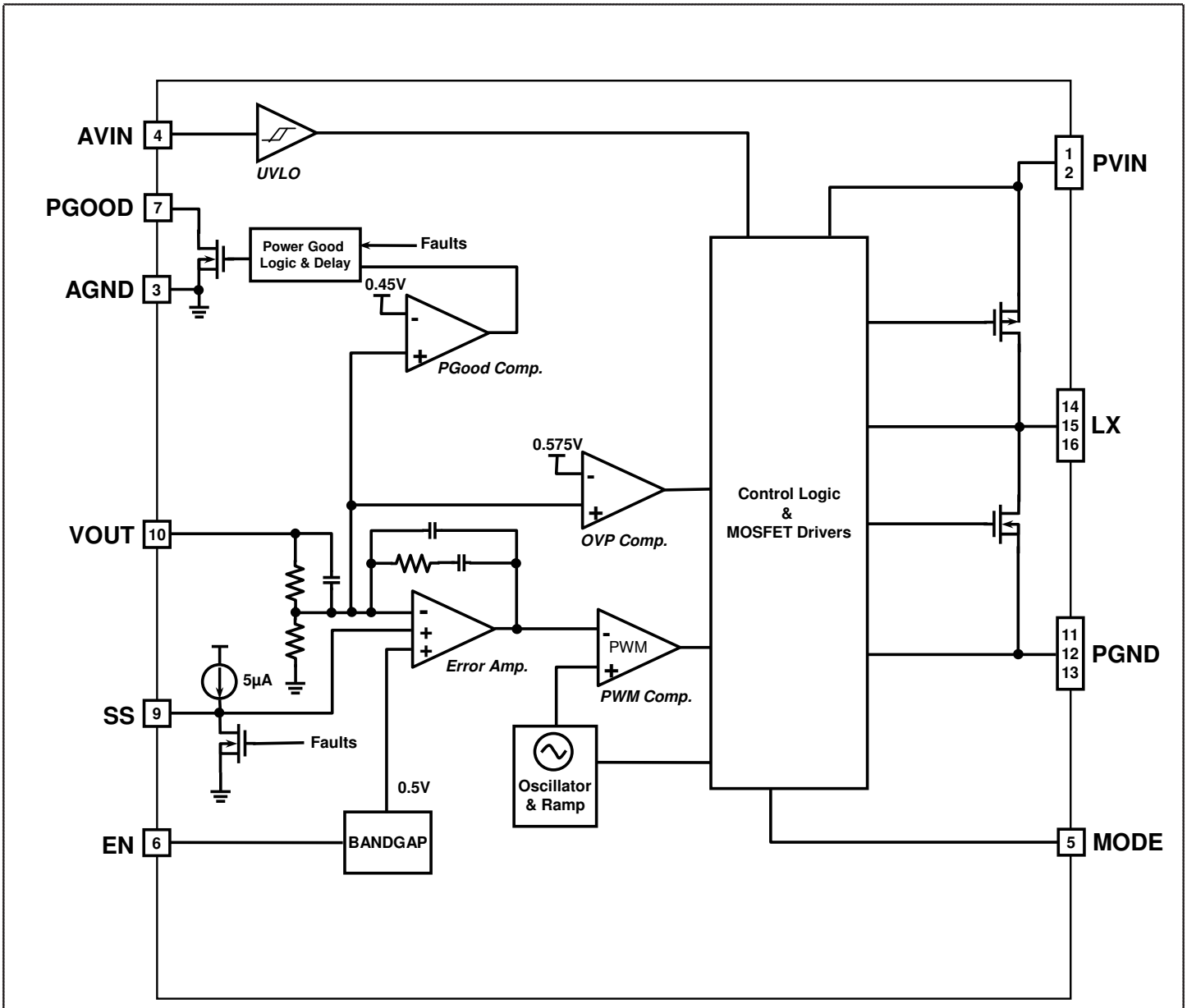
(10) The "Output Voltage Tolerance" includes output voltage accuracy, voltage drift over temperature and the line regulation.

(11) A negative current means the current flows into the pin and a positive current means the current flows out from the pin.

Pin Descriptions

Pin #	Pin Name	Pin Function
1,2	PVIN	Input supply voltage for the converter power stage.
3	AGND	Ground connection for the internal circuitry. AGND needs to be connected to PGND directly.
4	AVIN	Power supply for the internal circuitry. AVIN is required to be connected to PVIN through an R-C filter of 1Ω and 100nF.
5	MODE	MODE select pin. When connected to logic high, the device operates in forced PWM mode. When connected to logic low, it operates normally with PSAVE mode at light load. The enable pin has a 500kΩ internal pull-down resistor. This resistor is switched in circuit whenever the MODE pin is "Low" or when the part is in undervoltage lockout.
6	EN	Enable pin. When connected to logic high or tied to AVIN pin, the SC185 is on. When connected to logic low, the device enters shutdown and consumes less than 1µA current (typ.). The enable pin has a 500kΩ internal pulldown resistor. This resistor is switched in circuit whenever the EN is "Low" or when the part is in undervoltage lockout.
7	PGOOD	Power good indicator. When the output voltage reaches the PGOOD threshold, this pin will be open-drain (After the PGOOD delay), otherwise, it is pulled low internally.
8	NC	No connection.
9	SS	Soft Start. Connect a soft-start capacitor to program the soft start time. There is a 5µA charging current flowing out of the pin.
10	VOUT	Output voltage sense pin.
11,12,13	PGND	Ground connection for converter power stage.
14,15,16	LX	Switching node - connect an inductor between this pin and the output capacitor.
T	Thermal Pad	Thermal pad for heatsinking purposes. Recommend to connect it to PGND. It is not connected internally.

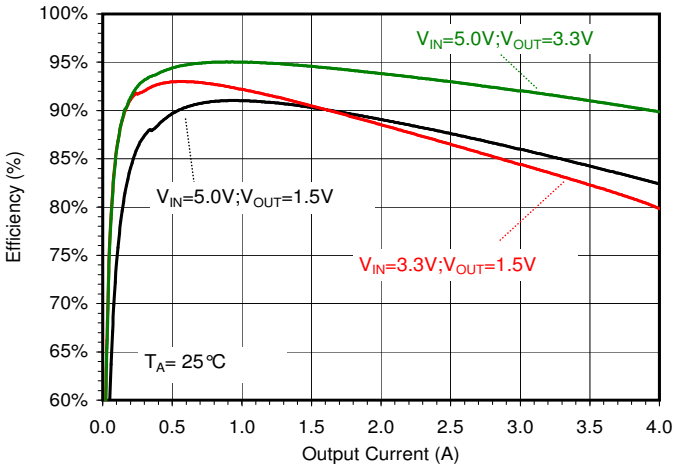
Block Diagram



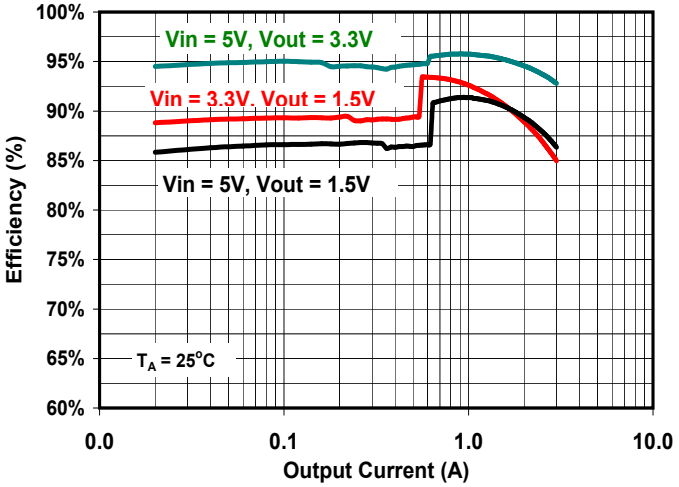
Typical Characteristics

Circuit Conditions: C_{IN}= 22uF/6.3V, C_{OUT}= 2 x 22uF/6.3V, C_{SS}= 10nF. Unless otherwise noted, L= 1.0uH (TOKO: FDV0530S-1R0).

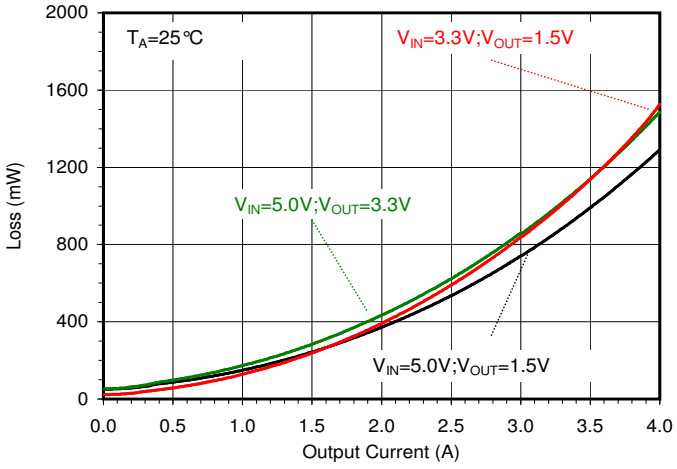
Efficiency (Forced PWM)



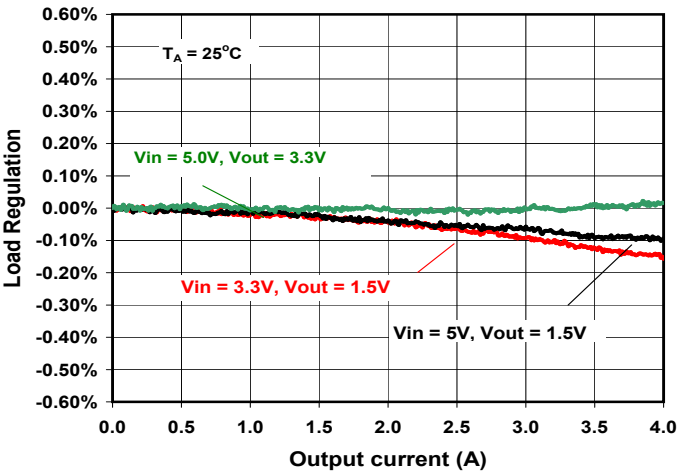
Efficiency (PSAVE Enabled)



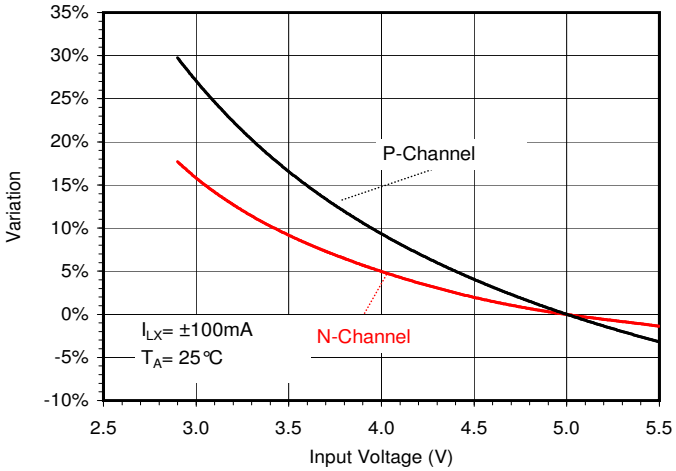
Total Loss (Forced PWM)



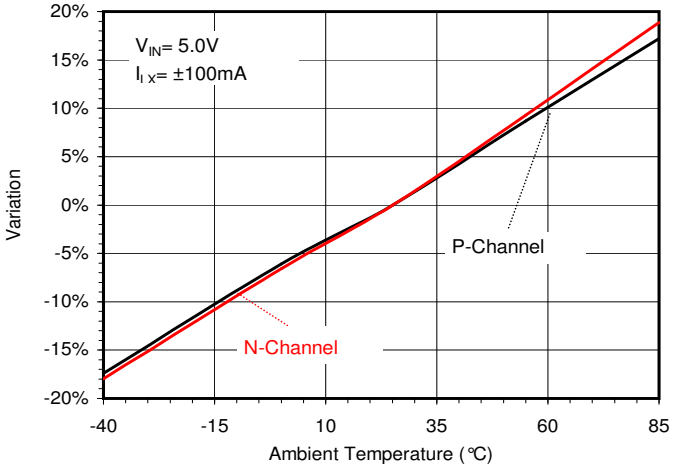
Load Regulation (Forced PWM)



$R_{DS(ON)}$ Variation vs. Input Voltage



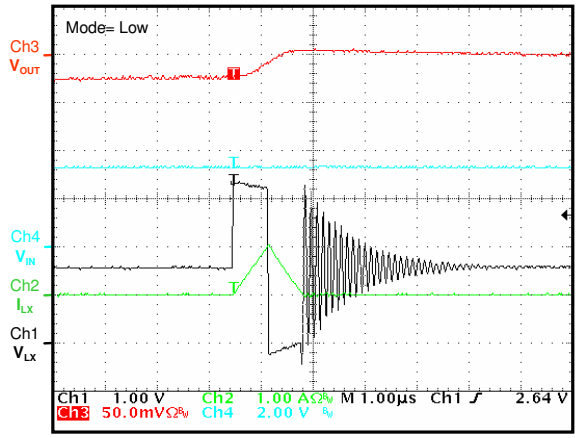
$R_{DS(ON)}$ Variation vs. Temperature



Typical Waveforms

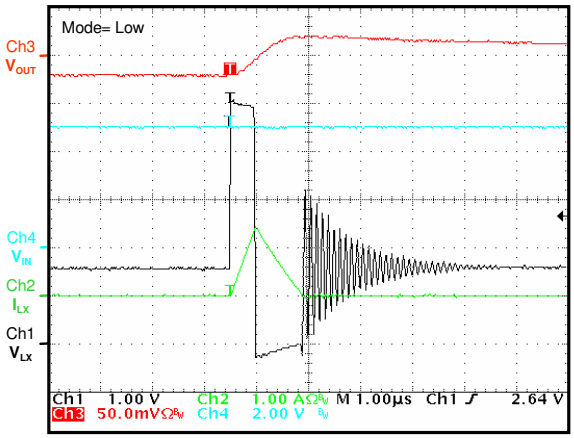
Circuit Conditions: C_{IN}= 22uF/6.3V, C_{OUT}= 2 x 22uF/6.3V, C_{SS}= 10nF. Unless otherwise noted, L= 1.0uH (TOKO: FDV0530S-1R0).

Output Voltage Ripple (V_{OUT}=1.5V), PSAVE Mode



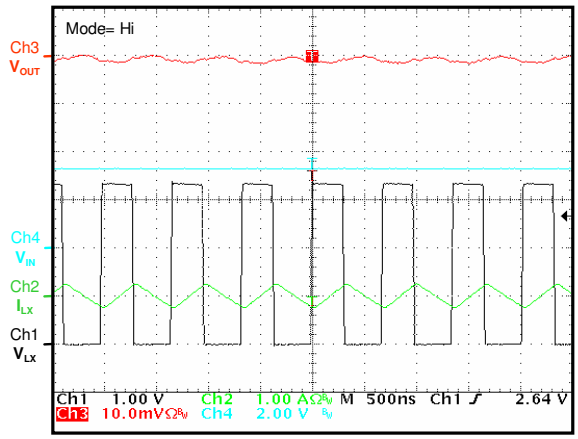
V_{IN} = 3.3V
I_{OUT} = 0A

Output Voltage Ripple (V_{OUT}=1.5V),PSAVE Mode



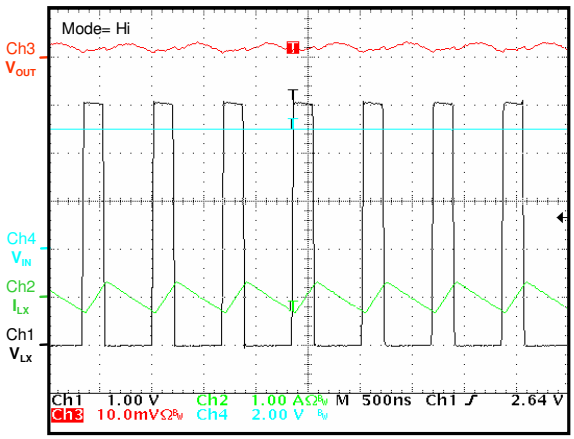
V_{IN} = 5.0V
I_{OUT} = 0A

Output Voltage Ripple (V_{OUT}=1.5V), Forced PWM



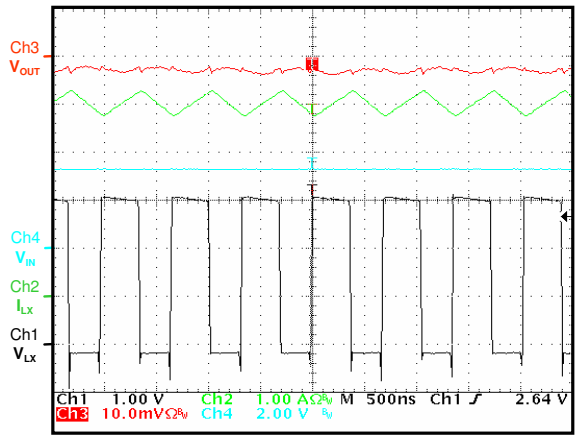
V_{IN} = 3.3V
I_{OUT} = 0A

Output Voltage Ripple (V_{OUT}=1.5V), Forced PWM



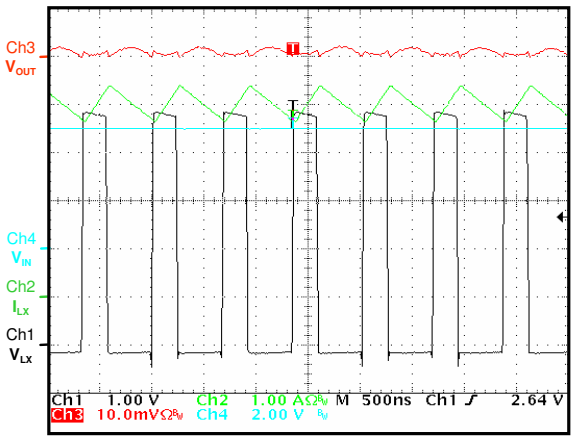
V_{IN} = 5.0V
I_{OUT} = 0A

Output Voltage Ripple (V_{OUT}=1.5V) @ Full Load



V_{IN} = 3.3V
I_{OUT} = 4A

Output Voltage Ripple (V_{OUT}=1.5V) @ Full Load

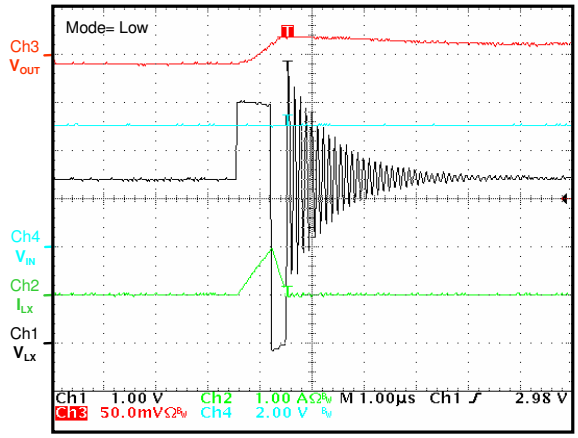


V_{IN} = 5.0V
I_{OUT} = 4A

Typical Waveforms (continued)

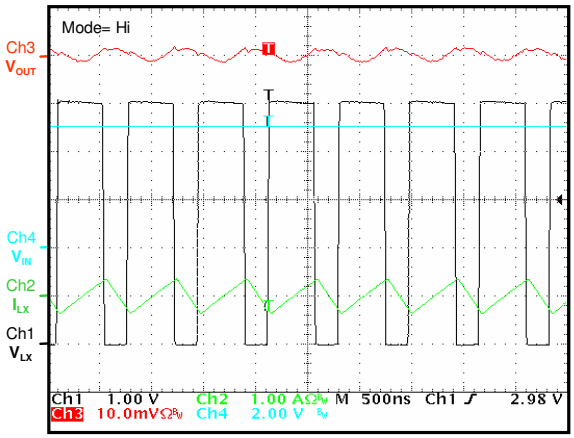
Circuit Conditions: C_{IN}= 22uF/6.3V, C_{OUT}= 2 x 22uF/6.3V, C_{SS}= 10nF. Unless otherwise noted, L= 1.0uH (TOKO: FDV0530S-1R0).

Output Voltage Ripple (V_{OUT}=3.3V), PSAVE Mode



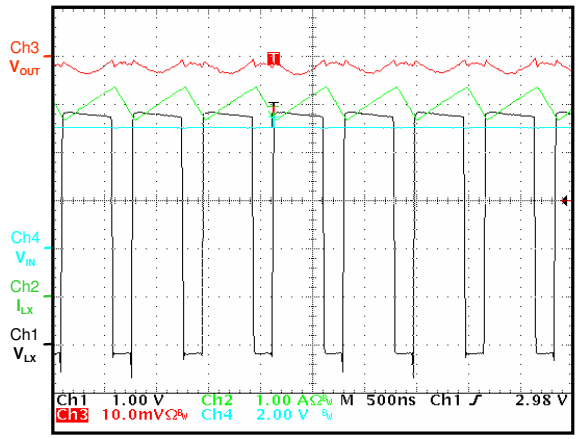
V_{IN} = 5.0V
I_{OUT} = 0A

Output Voltage Ripple (V_{OUT}=3.3V), forced PWM



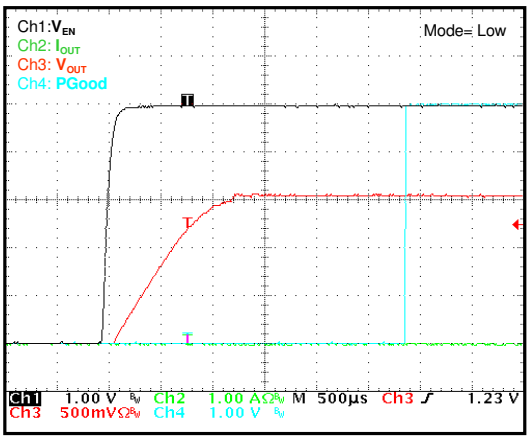
V_{IN} = 5.0V
I_{OUT} = 0A

Output Voltage Ripple (V_{OUT}=3.3V) @ Full Load



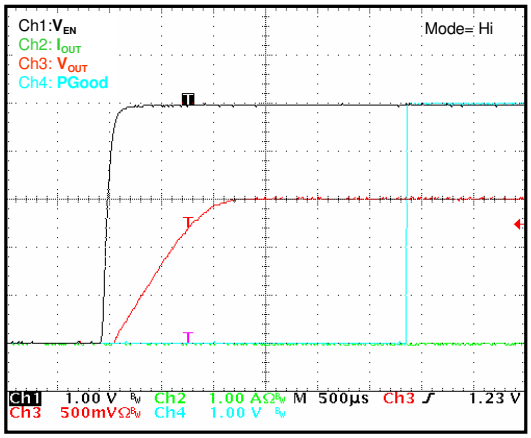
V_{IN} = 5.0V
I_{OUT} = 4A

Start Up (Enable) (V_{OUT}=1.5V), PSAVE Mode



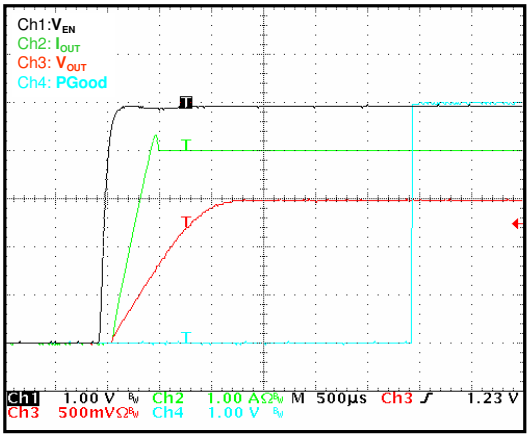
V_{IN} = 5.0V
I_{OUT} = 0A

Start Up (Enable) (V_{OUT}=1.5V), forced PWM



V_{IN} = 5.0V
I_{OUT} = 0A

Start Up (Enable) (V_{OUT}=1.5V) @Full Load

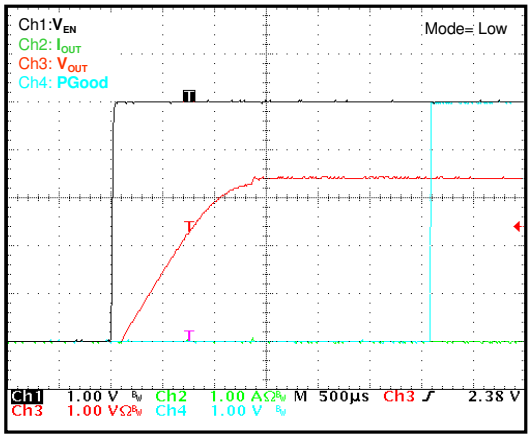


V_{IN} = 5.0V
I_{OUT} = 4A

Typical Waveforms (continued)

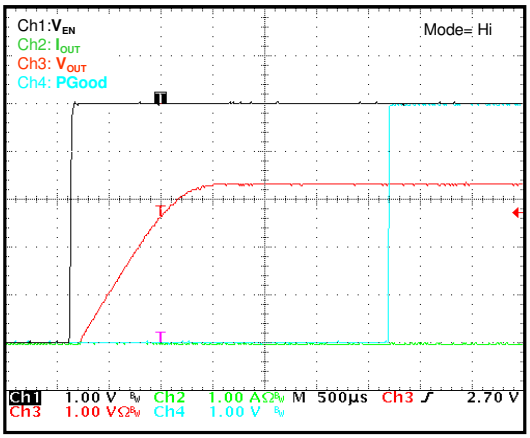
Circuit Conditions: C_{IN}= 22uF/6.3V, C_{OUT}= 2 x 22uF/6.3V, C_{SS}= 10nF. Unless otherwise noted, L= 1.0uH (TOKO: FDV0530S-1R0).

Start Up (Enable) (V_{OUT}=3.3V), PSAVE Mode



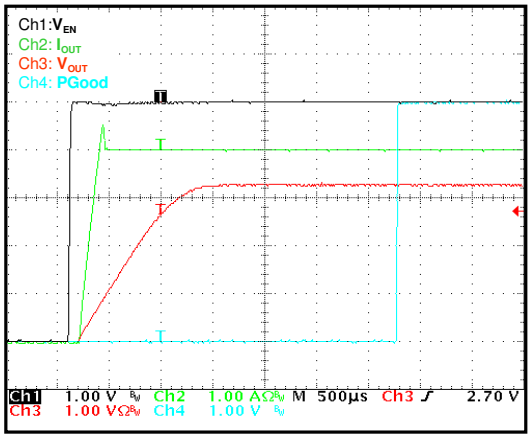
V_{IN} = 5.0V
I_{OUT} = 0A

Start Up (Enable) (V_{OUT}=3.3V), forced PWM



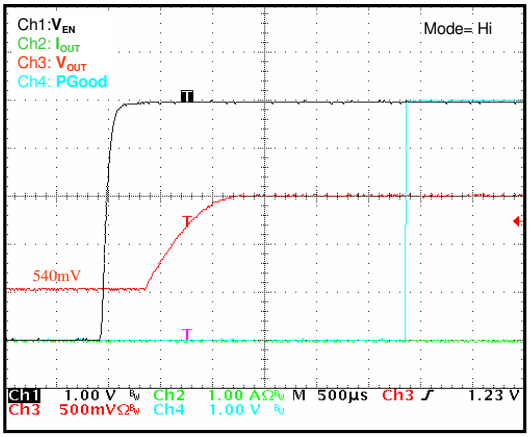
V_{IN} = 5.0V
I_{OUT} = 0A

Start Up (Enable) (V_{OUT}=3.3V) @Full Load



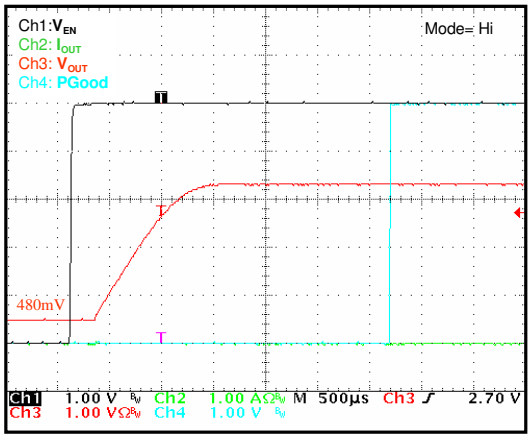
V_{IN} = 5.0V
I_{OUT} = 4A

Start Up into Pre-Biased Output (V_{OUT}=1.5V)



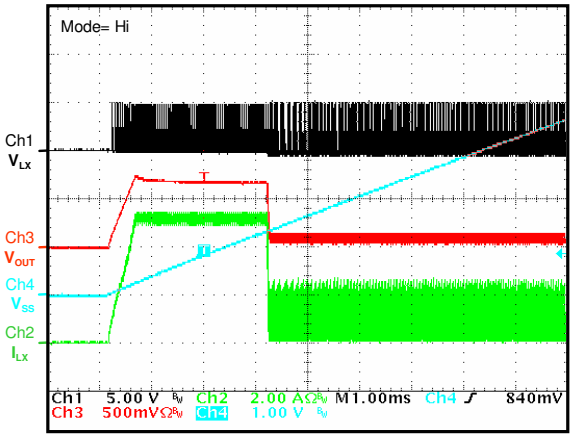
V_{IN} = 5.0V
I_{OUT} = 0A

Start Up into Pre-Biased Output (V_{OUT}=3.3V)



V_{IN} = 5.0V
I_{OUT} = 0A

Start Up (Enable) into Output Short Circuit

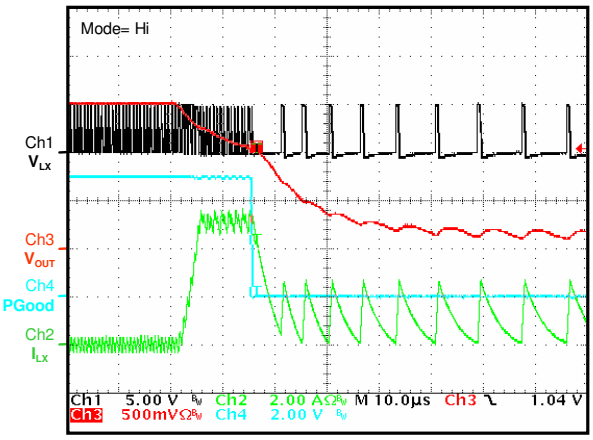


V_{IN} = 5.0V
R_{OUT} = 0Ω

Typical Waveforms (continued)

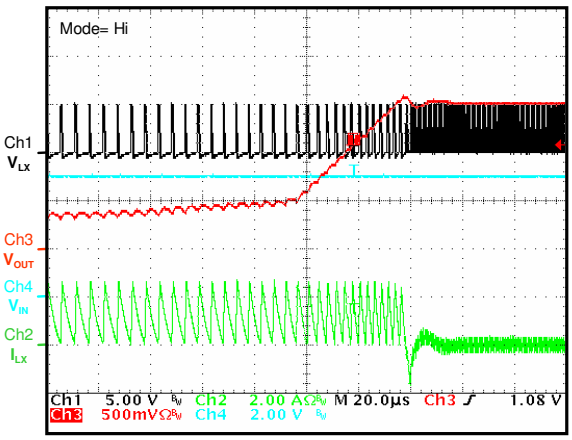
Circuit Conditions: C_{IN}= 22uF/6.3V, C_{OUT}= 2 x 22uF/6.3V, C_{SS}= 10nF. Unless otherwise noted, L= 1.0uH (TOKO: FDV0530S-1R0).

Output Short Circuit (V_{OUT}=1.5V)



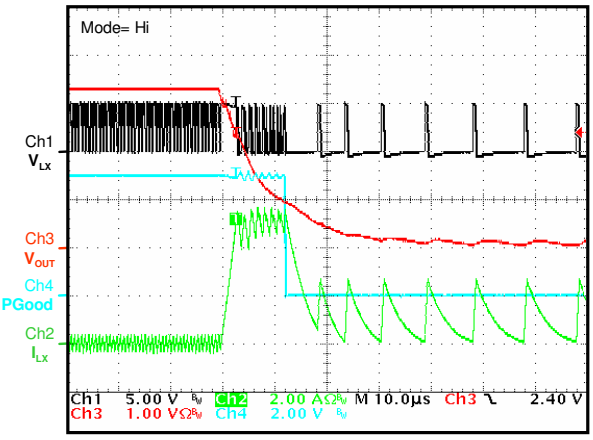
V_{IN} = 5.0V

Recovery from OCP (V_{OUT}=1.5V)



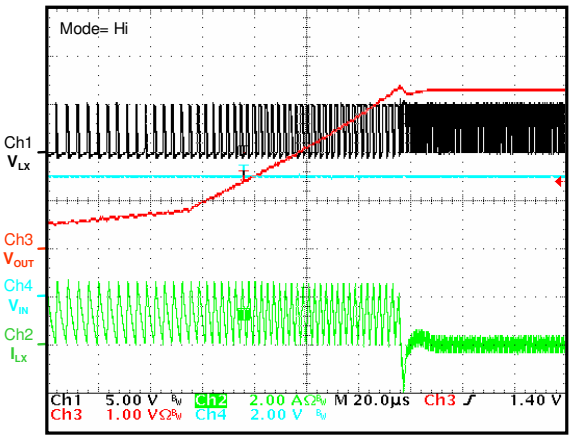
V_{IN} = 5.0V
I_{OUT} = 0A

Output Short Circuit (V_{OUT}=3.3V)



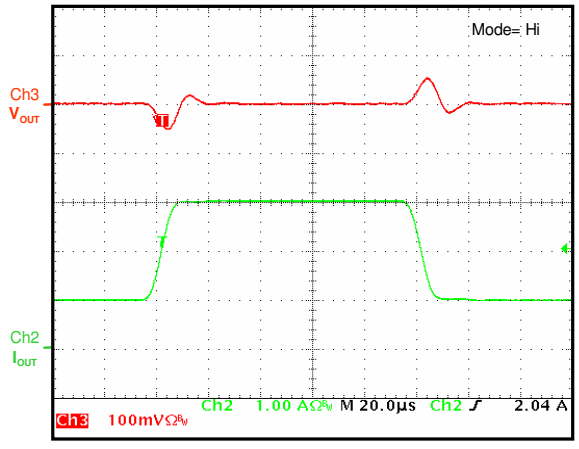
V_{IN} = 5.0V

Recovery from OCP (V_{OUT}=3.3V)



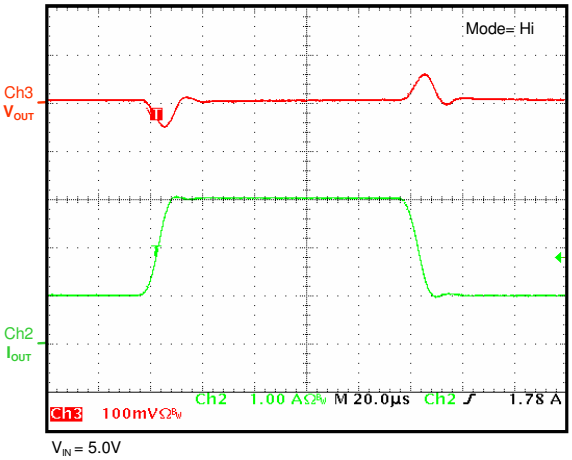
V_{IN} = 5.0V
I_{OUT} = 0A

Transient Response (V_{OUT}=1.5V, I_{STEP}=2A)



V_{IN} = 5.0V
I_{OUT} = 1A to 3A to 1A

Transient Response (V_{OUT}=3.3V, I_{STEP}=2A)

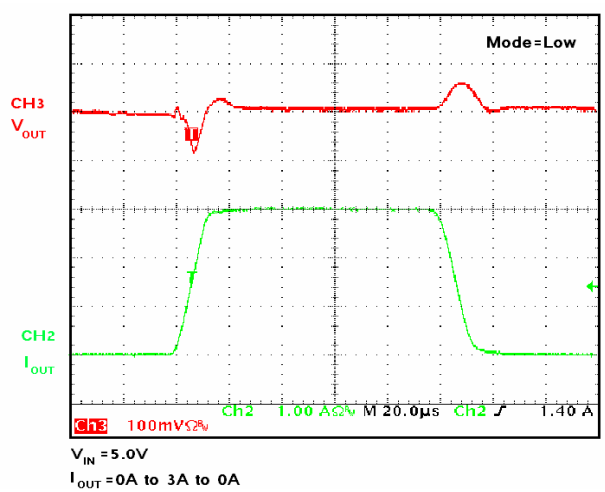


V_{IN} = 5.0V
I_{OUT} = 1A to 3A to 1A

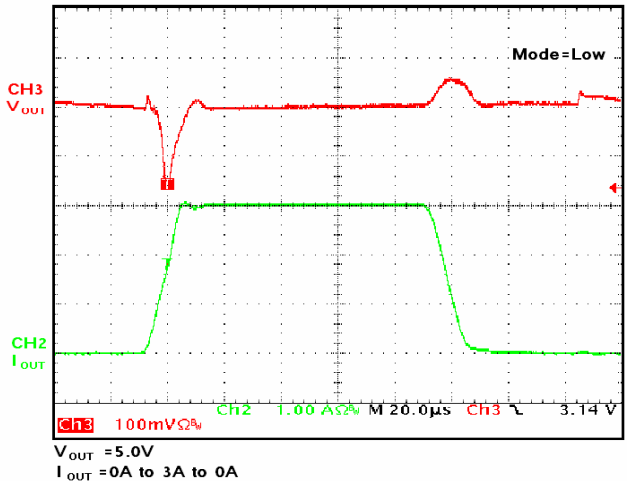
Typical Waveforms (continued)

Circuit Conditions: C_{IN}= 22uF/6.3V, C_{OUT}= 2 x 22uF/6.3V, C_{SS}= 10nF. Unless otherwise noted, L= 1.0uH (TOKO: FDV0530S-1R0).

Transient Response (V_{OUT}=1.5V, I_{STEP}=3A)-PSAVE Enabled



Transient Response (V_{OUT}=3.3V, I_{STEP}=3A)-PSAVE Enabled



Applications Information

Detailed Description

The SC185 is a synchronous step-down Pulse Width Modulated (PWM), DC-DC converter utilizing a 1.5MHz fixed-frequency voltage mode architecture. The device is designed to operate in fixed-frequency PWM mode and has the option to enter power save mode (PSAVE) at light loads to maximize efficiency. The switching frequency is chosen to minimize the size of the external inductor and capacitors while maintaining high efficiency.

Operation

During normal operation, the PMOS MOSFET is activated on each rising edge of the internal oscillator. The period is set by the onboard oscillator when in PWM mode. The device has an internal synchronous NMOS rectifier and does not require a Schottky diode on the LX pin. The device operates as a buck converter in PWM mode with a fixed frequency of 1.5MHz at medium to high loads. At light loads, depending on the MODE pin configuration, the part will either enter PSAVE mode to maximize efficiency or stay in forced PWM mode.

Power Save Mode Operation

Connect the MODE pin to ground to enable the PSAVE mode. When the load current decreases below the PSAVE threshold, PWM switching stops and the device automatically enters PSAVE mode. This threshold varies depending on the input voltage and output voltage setting, optimizing efficiency for all possible load currents - whether in PWM or PSAVE mode. While in PSAVE mode, output voltage regulation is controlled by a series of bursts in switching. During a burst, the inductor current is limited to a peak value which controls the on-time of the PMOS switch. After reaching this peak, the PMOS switch is disabled and the inductor current is forced to near 0mA. Switching bursts continue until the output voltage climbs to V_{OUT} +2% or until the PSAVE current limit is reached. Switching is then stopped to eliminate switching losses, enhancing overall efficiency. Switching resumes when the output voltage reaches the lower threshold of V_{OUT} and continues until the upper threshold again is reached. Note that the output voltage is regulated hysterically while in PSAVE mode between V_{OUT} and V_{OUT} + 2%. The period and duty cycle while in PSAVE mode are solely determined by V_{IN} and V_{OUT} until PWM mode resumes. This can result in the switching frequency being much lower than the PWM mode frequency.

If the output load current increases enough to cause V_{OUT} to decrease below the PSAVE exit threshold (V_{OUT} - 4%), the device automatically exits PSAVE and operates in continuous PWM mode. Note that the PSAVE high and low threshold levels are both set at or above V_{OUT} to minimize undershoot when the SC185 exits PSAVE. Figure 1 illustrates the transitions from PWM mode to PSAVE mode and back to PWM mode.

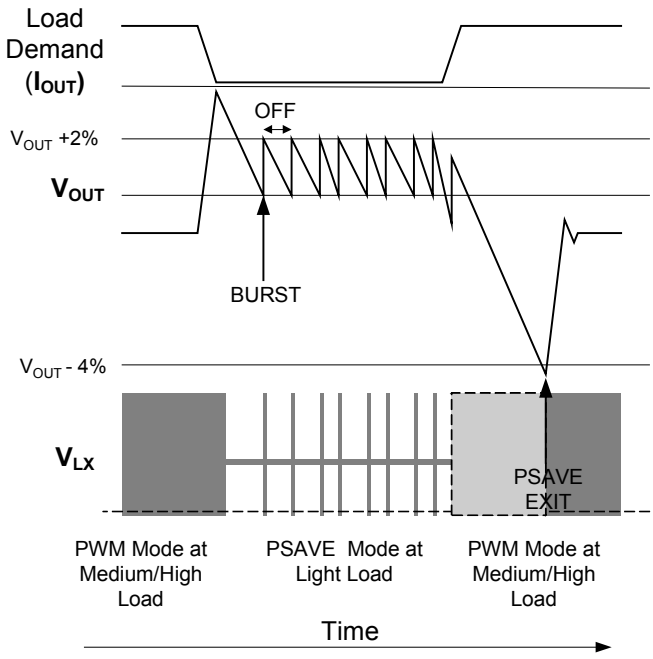


Figure 1 — Transitions between PWM and PSAVE Modes

Protection Features

The SC185 provides the following protection features:

- Current Limit
- Over-Voltage Protection
- Soft-Start Operation
- Thermal Shutdown

Applications Information (continued)

Current Limit & OCP

The internal PMOS power device in the switching stage is protected by a current limit feature. If the inductor current is above the PMOS current limit for 16 consecutive cycles, the part enters foldback current limit mode and the output current is limited to the current limit holding current (I_{CL_HOLD}) which is approximately 900mA. Under this condition, the output voltage will be the product of I_{CL_HOLD} and the load resistance. When the load presented falls below the current limit holding level, the output will charge to the upper PSAVE voltage threshold and return to normal operation. The SC185 is capable of sustaining an indefinite short circuit without damage. During the soft start, if current limit has occurred before the SS voltage has reached 400mV, the part enters foldback current limit mode. Foldback current limit mode will be disabled during soft-start after the SS voltage is higher than 400mV.

Over-Voltage Protection

In the event of a 15% over-voltage on the output, the PWM drive is disabled with the LX pin floating. Switching does not resume until the output voltage falls below the nominal Vout regulation voltage.

Soft-Start

The soft-start mode is activated after AVIN reaches it's UVLO voltage threshold and EN is set high to enable the part. A thermal shutdown event will also activate the soft start sequence. The Soft-start mode controls the slew-rate of the output voltage during startup thus limiting in-rush current on the input supply. During start up, the reference voltage for the error amplifier is clamped by the voltage on SS pin. The output voltage slew rate during soft start is determined by the value of the external capacitor connected to the SS pin and the internal 5µA charging current. The SC185 requires a minimum soft-start time from enable to final regulation in the order of 200µs, including the 50µs enable delay. As a result the soft start capacitor, Css, should be higher than 1.5nF. During start up, the chip operates in forced PWM mode. The value of Css for the desired soft-start time, tss, can be determined by Equation 1.

$$t_{SS} = C_{SS} \times \frac{0.5V}{5\mu A} \quad \text{(1)}$$

The SC185 is capable of starting up into a pre-biased output. When the output is pre-charged by another supply rail, the SC185 will not discharge the output during the soft start period.

Shut Down

When the EN pin is low, the SC185 will run in shutdown mode, drawing less than 1µA (typ.) from the input power supply. The internal switches and bandgap voltage will be immediately turned off.

Thermal Shutdown

The device has a thermal shutdown feature to protect the SC185 if the junction temperature exceeds 160°C. During thermal shutdown, the on-chip power devices are disabled, floating the LX output. When the temperature drops by 10°C, it will initial a soft start cycle to resume normal operation.

Under-Voltage Lockout

Under-Voltage Lockout (UVLO) is enabled when the input voltage drops below the UVLO threshold. This prevents the device from entering an ambiguous state in which regulation cannot be maintained. Hysteresis of approximately 300mV is included to prevent chattering near the threshold. When the AVIN voltage reaches back to the turn-on threshold and EN is high, the soft-start mode is resumed.

Power Good

The power good (PGOOD) is an open-drain output. When the output voltage drops below 10% of nominal voltage, the PGOOD pin is pulled low after a 20µs delay. During start-up, PGOOD will be asserted 1.8ms (typ.) after the output voltage reaches 90% of the final regulation voltage. The faults of over voltage, fold-back current limit mode and thermal shutdown will force PGOOD low after a 20µs delay. When recovering from a fault, PGOOD will be asserted 1.8ms (typ.) after Vout reaches 90% of the final regulation voltage.

Enable

The EN input is used to enable or disable the device when the device is not in UVLO. When EN is low (grounded), the device enters shutdown mode and consumes less than 1µA of current. In shutdown mode, the device tri-states the LX pin and pulls down the SS pin. The EN pin has a 500kΩ internal pull-down resistor. This resistor is switched

Applications Information (continued)

in circuit whenever the EN pin is below its threshold, or when the device is in under voltage lockout and AVIN exceeds 0.8V. When the device is enabled, it takes about 50µs for the internal circuitry wake up and begin the soft-start up sequence.

Operation Mode Selection

The MODE input is used to select between forced PWM and automatic PSAVE modes. When the MODE pin is held high, the device operates in forced continuous PWM mode regardless of the output load condition. When the MODE pin is held low (grounded), the device is permitted to operate in Power Save mode (PSAVE). The MODE pin can be changed on-the-fly. When the MODE pin is switched from low to high, the device will transition to forced continuous PWM mode immediately. When the MODE pin is switched from high to low, and the load current is below the PSAVE entry level, the device will transition to PSAVE mode after 64 clock cycles. The MODE pin has a 500kΩ internal pull-down resistor. This resistor is switched in circuit whenever the MODE pin is below its threshold, or when the device is in under voltage lockout but AVIN exceeds 0.8V.

100% Duty-Cycle Operation

SC185 is capable of operating at 100% duty-cycle. When the difference between input voltage to output voltage is less than the minimum dropout voltage, the PMOS switch is completely on, operating in 100% duty-cycle. The minimum dropout voltage is the output current multiplied by the on-resistance of the internal PMOS switch and the DC-resistance of the inductor when PMOS switch is on continuously.

Output L-C filter Selection

SC185 has fixed internal loop-gain compensation. It is optimized for X5R or X7R ceramic output capacitors and an output L-C filter corner frequency of less than 34KHz. The output L-C corner frequency can be determined by Equation 2.

$$f_C = \frac{1}{2\pi\sqrt{L \cdot C_{OUT}}} \quad \text{(2)}$$

In general, the inductor is chosen to set the inductor ripple current to approximately 30% of the maximum output current. It is recommended to use a typical inductor value of 1µH to 2.2µH with output ceramic capacitors of 44µF or higher capacitance. Lower inductance should be considered in applications where faster transient response is required. More output capacitance will reduce the output deviation for a particular load transient. When using low inductance, the maximum peak inductor current at any condition (normal operation and start up) can not exceed 5A which is the guaranteed minimum current limit. The saturation current rating of the inductor needs to be at least larger than the peak inductor current which is the maximum output current plus half of inductor ripple current.

Applications Information (continued)

PCB Layout Considerations

The layout diagram in Figure 2 shows a recommended top-layer PCB for the SC185 and supporting components. Figure 3 shows the bottom layer for this PCB. Fundamental layout rules must be followed since the layout is critical for achieving the performance specified in the Electrical Characteristics table. Poor layout can degrade the performance of the DC-DC converter and can contribute to EMI problems, ground bounce, and resistive voltage losses. Poor regulation and instability can result.

The following guidelines are recommended when developing a PCB layout:

1. The input capacitor, C_{IN} should be placed as close to the PVIN and PGND pins as possible. This capacitor provides a low impedance loop for the pulsed currents present at the buck converter's input. Use short wide traces to connect as closely to the IC as possible. This will minimize EMI and input voltage ripple by localizing the high frequency current pulses.
2. Keep the LX pin traces as short as possible to minimize pickup of high frequency switching edges to other parts of the circuit. C_{OUT} and L should be connected as close as possible between the LX and PGND pins, with a direct return to the PGND pin from C_{OUT}.
3. Route the output voltage feedback/sense path away from the inductor and LX node to minimize noise and magnetic interference.
4. Use a ground plane referenced to the SC185 PGND pin. Use several vias to connect to the component side ground to further reduce noise and interference on sensitive circuit nodes.
5. If possible, minimize the resistance from the VOUT and PGND pins to the load. This will reduce the voltage drop on the ground plane and improve the load regulation. And it will also improve the overall efficiency by reducing the copper losses on the output and ground planes.

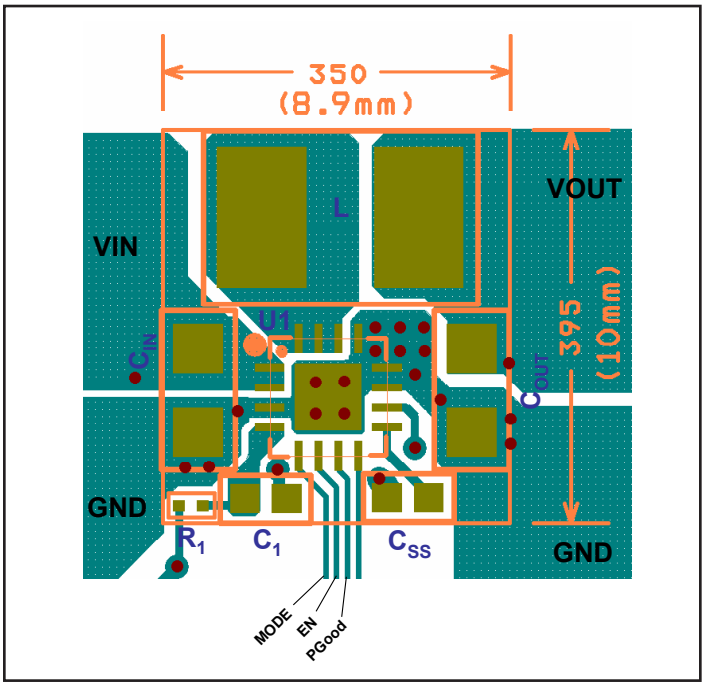


Figure 2 — Recommended PCB Layout (Top Layer)

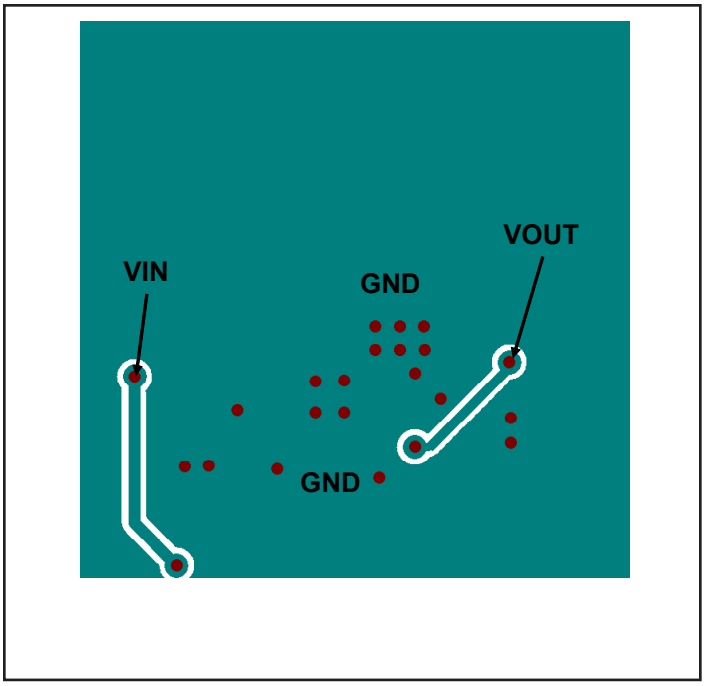
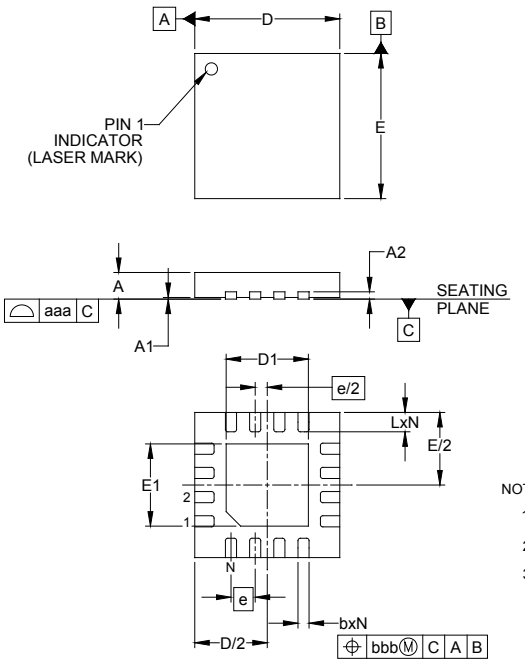


Figure 3 — Bottom Layer Detail

Outline Drawing – 3x3 MLPQ-UT16

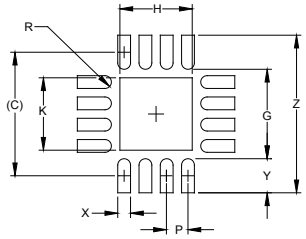


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.152)	
b	.007	.009	.012	0.18	0.23	0.30
D	.114	.118	.122	2.90	3.00	3.10
D1	.061	.067	.071	1.55	1.70	1.80
E	.114	.118	.122	2.90	3.00	3.10
E1	.061	.067	.071	1.55	1.70	1.80
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	16			16		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP IS 1.90 x 1.90mm.

Land Pattern – 3x3 MLPQ-UT16



DIM	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.083	2.10
H	.067	1.70
K	.067	1.70
P	.020	0.50
R	.006	0.15
X	.012	0.30
Y	.031	0.80
Z	.146	3.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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