THE DATASHEET OF

LTC3114IDHC-1#WPBF

40V, 1A Synchronous Buck-Boost DC/DC Converter with Programmable Output Current

FEATURES

- **Regulates V_{OUT} Above, Below or Equal to V_{IN}**
- **Single Inductor**
- **Wide V_{IN} Range: 2.2V to 40V**
- **Wide V_{OUT} Range: 2.7V to 40V**
- **1A Output Current in Buck Mode**
- **0.5A Output Current, V_{IN} = 3.6V, V_{OUT} = 5V**
- **Programmable Average Output Current**
- **Up to 96% Efficiency**
- Burst Mode® Operation, 30µA No-Load I_Q
- Current Mode Control
- 1.2MHz Ultralow Noise PWM
- Accurate RUN Pin Threshold
- Thermally Enhanced, 16-lead 3mm × 5mm DFN and TSSOP Packages
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

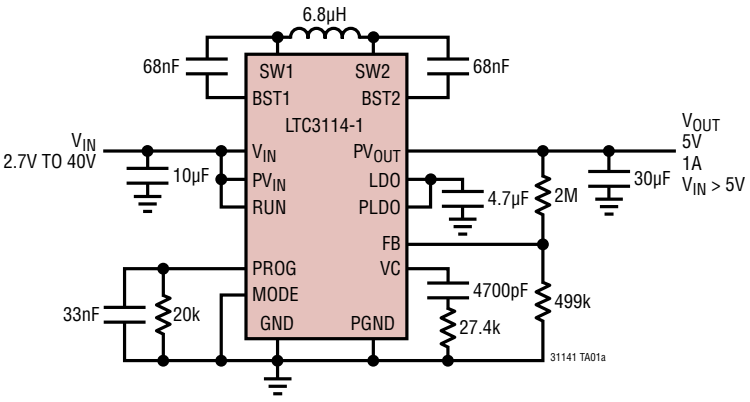
- 24V/28V Industrial Power Supply
- 12V Lead-Acid to 12V Regulator
- High Power LED Driver
- 12V/24V Solar Panel Battery Charging Systems
- Automotive Power Systems

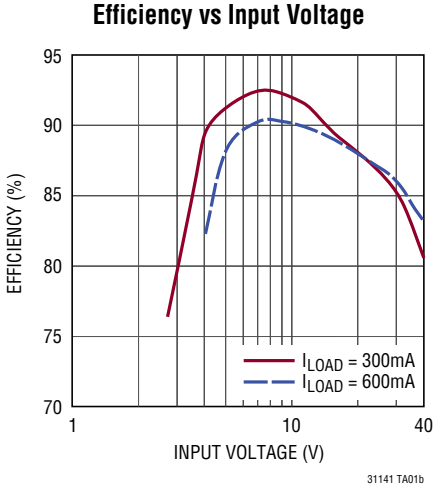
DESCRIPTION

The LTC®3114-1 is a versatile, wide operating voltage range synchronous monolithic buck-boost DC/DC converter with programmable average output current. The LTC3114-1's proprietary buck-boost PWM control circuitry delivers low noise operation across the entire operating voltage range. Current mode control ensures exceptional line and load transient responses.

Synchronous, internal MOSFET switches and pin selectable Burst Mode operation maintain high efficiency across the entire range of load current. Average output current is programmed with a standard resistor and provides the basis for wide input range, high efficiency charging systems or constant current, high efficiency LED drive. Regulator turn-on is programmable through the accurate RUN pin. Quiescent current is just 3µA in shutdown. Overtemperature protection, short-circuit protection and soft-start are integrated. The LTC3114-1 is offered in 16-lead 3mm × 5mm × 0.75mm DFN and 16 lead TSSOP (FE) packages.

TYPICAL APPLICATION

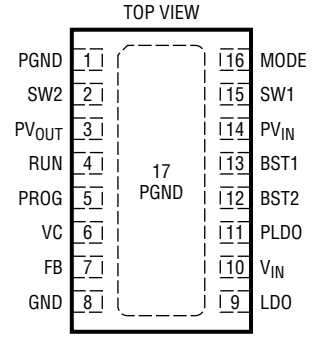




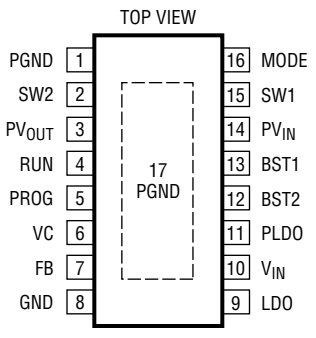
ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN}, PV_{IN}, PV_{OUT} ..... –0.3V to 45V
V_{BST1} ..... V_{SW1} – 0.3V to V_{SW1} + 6V
V_{BST2} ..... V_{SW2} – 0.3V to V_{SW2} + 6V
V_{RUN} ..... –0.3V to (V_{IN} + 0.3V)
Voltage, All Other Pins ..... –0.3V to 6V
Operating Junction Temperature Range (Notes 2, 4)
LTC3114E-1/LTC3114I-1 ..... –40°C to 125°C
LTC3114H-1 ..... –40°C to 150°C
LTC3114MP-1 ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 Sec)
FE Package ..... 300°C

PIN CONFIGURATION



DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W (4-LAYER BOARD), θ_{JC} = 4°C/W
EXPOSED PAD (PIN 17) IS PGND, MUST BE SOLDERED TO PCB
FOR RATED THERMAL PERFORMANCE



FE PACKAGE
16-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 17) IS PGND, MUST BE SOLDERED TO PCB
FOR RATED THERMAL PERFORMANCE

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3114EDHC-1#PBF	LTC3114EDHC-1#TRPBF	31141	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3114IDHC-1#PBF	LTC3114IDHC-1#TRPBF	31141	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3114HDHC-1#PBF	LTC3114HDHC-1#TRPBF	31141	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 150°C
LTC3114MPDHC-1#PBF	LTC3114MPDHC-1#TRPBF	31141	16-Lead (5mm × 3mm) Plastic DFN	–55°C to 150°C
LTC3114EFE-1#PBF	LTC3114EFE-1#TRPBF	3114FE-1	16-Lead Plastic TSSOP	–40°C to 125°C
LTC3114IFE-1#PBF	LTC3114IFE-1#TRPBF	3114FE-1	16-Lead Plastic TSSOP	–40°C to 125°C
LTC3114HFE-1#PBF	LTC3114HFE-1#TRPBF	3114FE-1	16-Lead Plastic TSSOP	–40°C to 150°C
LTC3114MPFE-1#PBF	LTC3114MPFE-1#TRPBF	3114FE-1	16-Lead Plastic TSSOP	–55°C to 150°C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
AUTOMOTIVE PRODUCTS**				
LTC3114EDHC-1#WPBF	LTC3114EDHC-1#WTRPBF	31141	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3114IDHC-1#WPBF	LTC3114IDHC-1#WTRPBF	31141	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3114IFE-1#WPBF	LTC3114IFE-1#WTRPBF	3114FE-1	16-Lead Plastic TSSOP	–40°C to 125°C
LTC3114EFE-1#WPBF	LTC3114EFE-1#WTRPBF	3114FE-1	16-Lead Plastic TSSOP	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 24V, V_{OUT} = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage	V_{LDO} ≥ 2.7V, –55°C to 0°C V_{LDO} ≥ 2.7V, 0°C to 150°C	● ●	2.3 2.2		40 40	V V
Output Operating Voltage	(Note 5)	●	2.7		40	V
Undervoltage Lockout Threshold on LDO	V_{LDO} Rising	●	2.3	2.5	2.7	V
V_{IN} Quiescent Current in Shutdown				3		µA
V_{IN} Quiescent Current in Burst Mode Operation	FB = 1.4V, Non-Bootstrapped (Note 6)			50		µA
Oscillator Frequency		●	1000	1200	1400	kHz
Oscillator Frequency Variation	V_{IN} = 12V to 36V			0.1		%/V
Feedback Voltage	Measured on FB	●	0.98	1.0	1.02	V
Feedback Voltage Line Regulation	V_{IN} = 2.7V to 40V, Measured on FB			0.2		%
Error Amplifier Transconductance	VC Current = ±5µA			120		µS
FB Pin Input Current	FB = 1V			1	50	nA
VC Source Current	VC = 0.6V			–12		µA
VC Sink Current	VC = 0.6V			12		µA
RUN Pin Threshold—Accurate	RUN Pin Rising	●	1.185	1.205	1.29	V
RUN Pin Hysteresis				140		mV
Run Pin Threshold—Logic		●	0.3	0.7	1.1	V
PROG Current	Switch D Current = 1A Switch D Current = 500mA Switch D Current = 100mA (Note 3)		38 18 2	40 20 4	42 22 6	µA µA µA
PROG Current Gain	Ratio of PROG Current to SWD Current			40		µA/A
PROG Voltage Threshold			0.90	0.925	0.95	V
Inductor Current Limit	(Note 3)	●	1.3	1.7	2.3	A
Overload Current Limit	V_{OUT} = 0V (Note 3)			2.6		A
I_{ZERO} Inductor Current Limit	(Note 3)			100		mA
Maximum Duty Cycle	Percentage of Period SW2 is Low in Boost Mode Percentage of Period SW1 is High in Boost Mode	● ●	90 85	95 88		% %
Minimum Duty Cycle	Percentage of Period SW1 is High in Buck Mode	●			0	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 24V, V_{OUT} = 5V, unless otherwise noted.

N-Channel Switch Resistance	Switch A (from PV_{IN} to SW1) Switch B (from SW1 to PGND) Switch C (from SW2 to PGND) Switch D (from PV_{OUT} to SW2)			250 250 250 250		mΩ mΩ mΩ mΩ
N-Channel Switch Leakage				0.1	10	µA
LDO Output Voltage	I_{LDO} = 10mA	●	4.2	4.4	4.6	V
LDO Load Regulation	I_{LDO} = 1mA to 10mA			0.8		%
LDO Line Regulation	I_{LDO} = 1mA, V_{IN} = 10V to 40V			0.2		%
LDO Current Limit	V_{LDO} = 2.5V		40	65		mA
Soft-Start Time				2		ms
SW1 and SW2 Forced Low Time				100		ns
MODE Pin Logic Threshold	H = PWM Mode, L = Burst Mode Operation	●	0.5	0.9	1.3	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3114-1 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3114E-1 is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3114I-1 specifications are guaranteed over the –40°C to 125°C operating junction temperature range. The LTC3114H-1 specifications are guaranteed over the –40°C to 150°C operating junction temperature range. The LTC3114MP-1 specifications are guaranteed over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetime; operating lifetime is derated for junction temperatures greater than 125°C. The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

The junction temperature (T_J in degrees Celsius) is calculated from the ambient temperature (T_A in degrees Celsius) and the power dissipation (P_D in Watts) according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} is the thermal impedance of the package.

Note 3: Current measurements are performed when the LTC3114-1 is not switching. The current limit values measured in operation will be somewhat higher due to the propagation delay of the comparators. The LTC3114-1 is tested in a proprietary non-switching test mode.

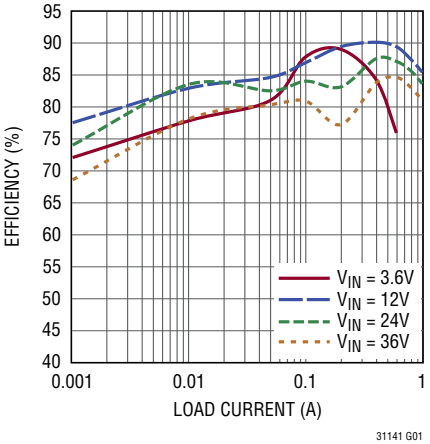
Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 5: Operating output voltage can be programmed as low as 1.0V nominal if the accurate programmable output current limit feature is not required.

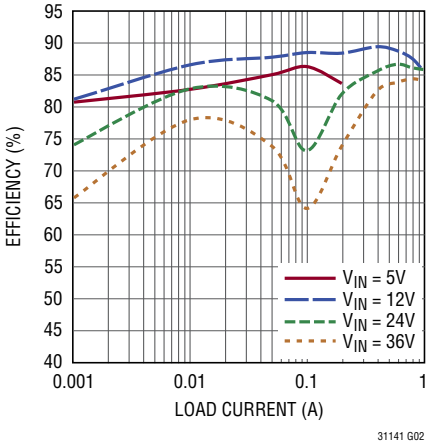
Note 6: Connecting LDO/PLDO to the regulated 5V output (bootstrapping), reduces quiescent current substantially. Typical no-load quiescent current for 12V V_{IN} to 5V V_{OUT} is 30µA, if boostrapped.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

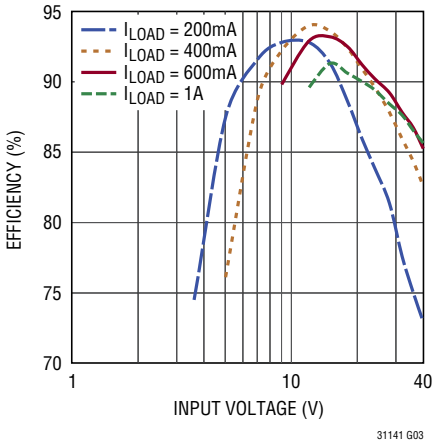
5V Output Efficiency vs Load



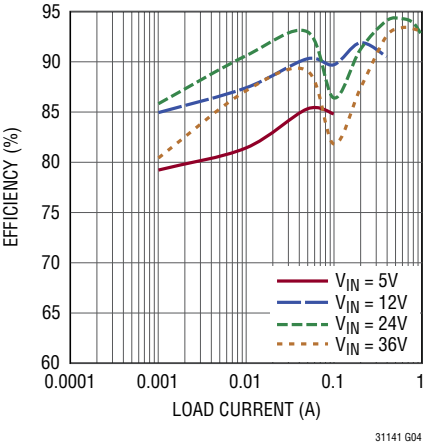
12V Output Efficiency vs Load



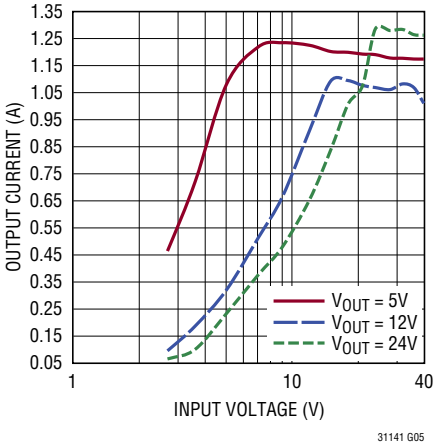
12V Output Efficiency vs V_{IN}



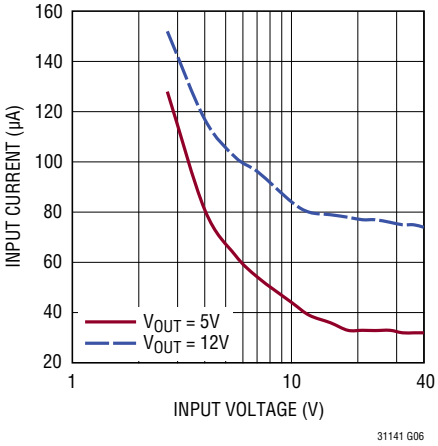
24V Output Efficiency vs Load



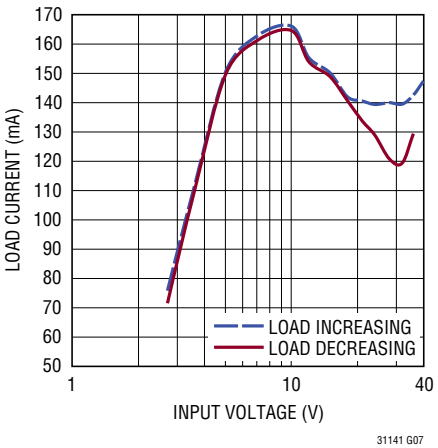
Maximum Load Current vs V_{IN}



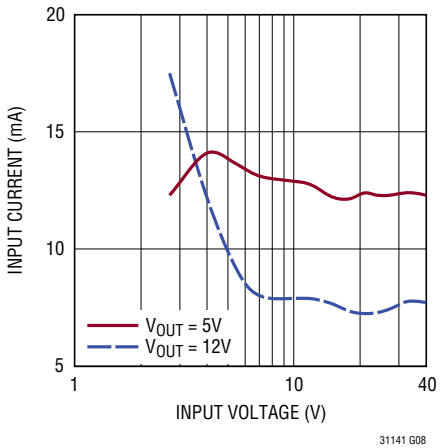
No-Load Input Current vs V_{IN}, Burst Mode Enabled



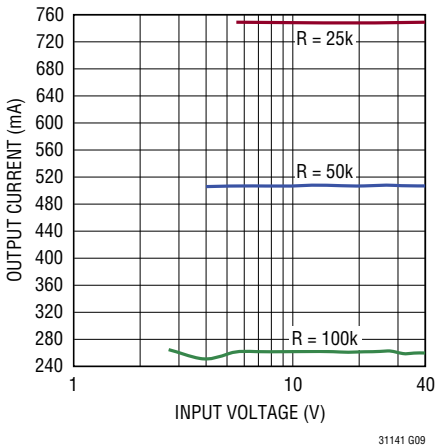
Burst Mode Operation Threshold vs V_{IN}



No-Load Input Current vs V_{IN}, PWM Mode

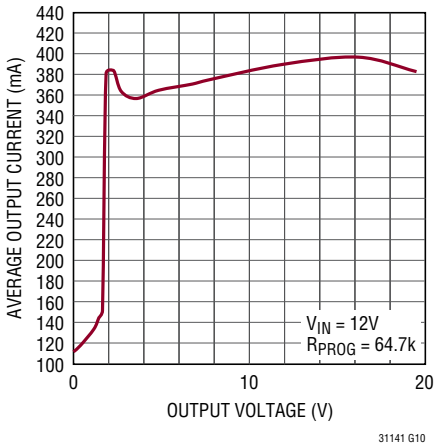


Average Output Current vs V_{IN}, R_{PROG}

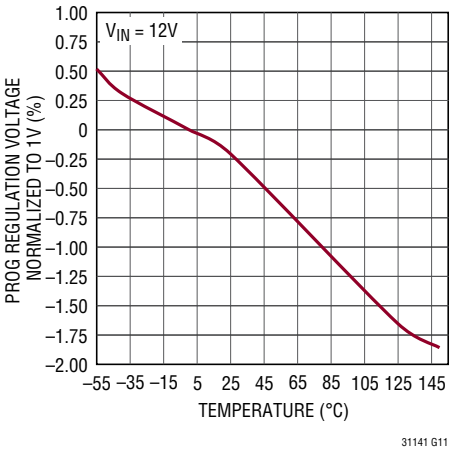


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

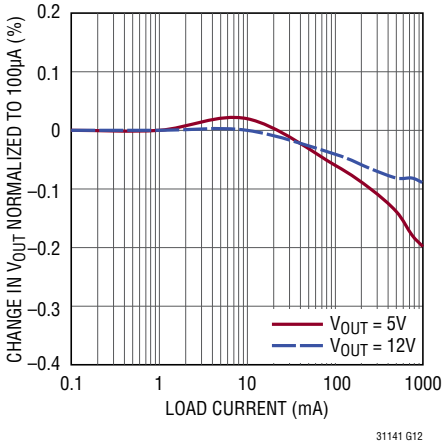
Average Output Current vs V_{OUT}



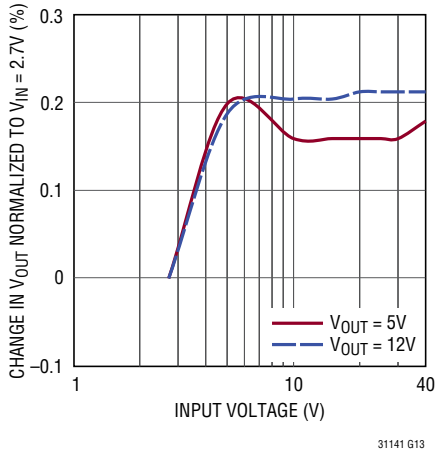
PROG Regulation Voltage vs Temperature



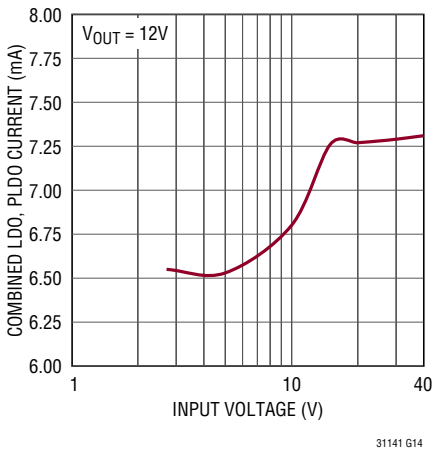
Output Voltage Load Regulation



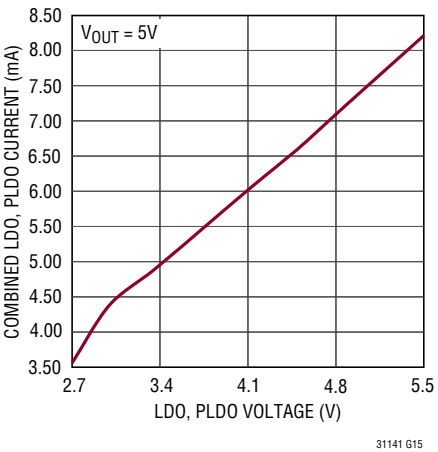
Output Voltage Line Regulation



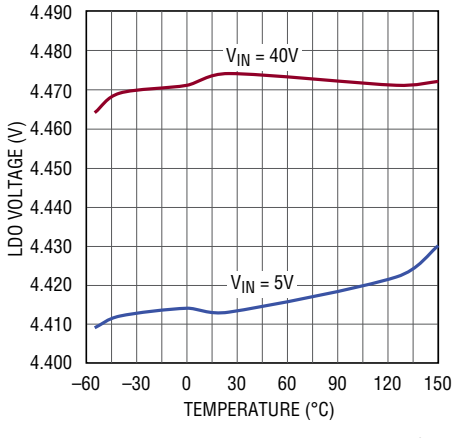
Combined LDO, PLDO Supply Current vs V_{IN}



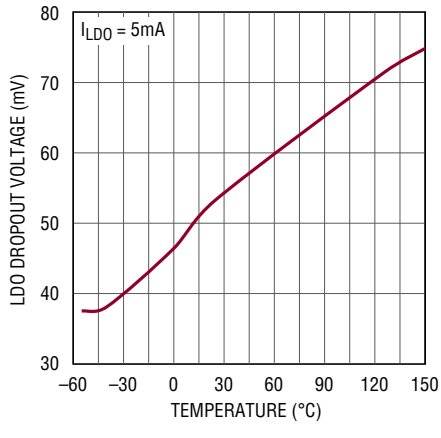
Combined LDO, PLDO Supply Current vs LDO



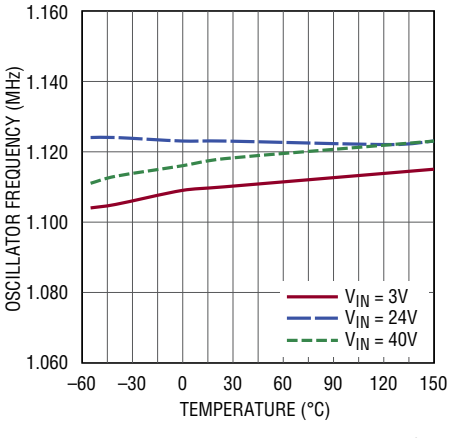
LDO Voltage vs Temperature



LDO Dropout Voltage vs Temperature



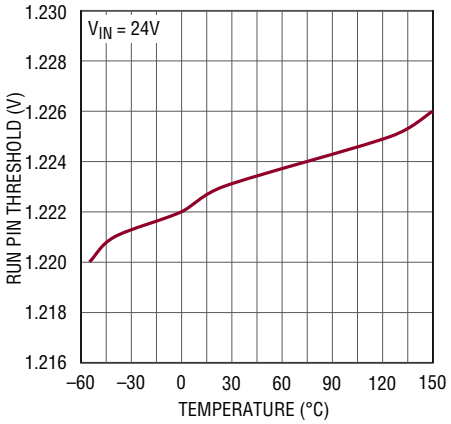
Oscillator Frequency vs Temperature



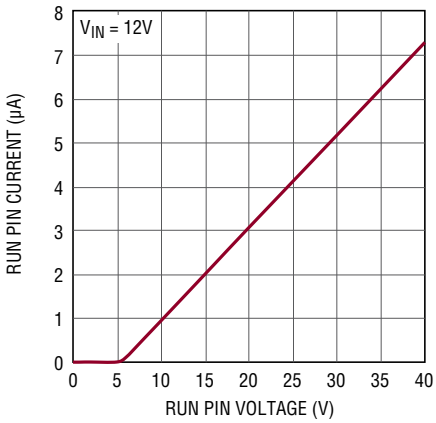
Rev. D

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

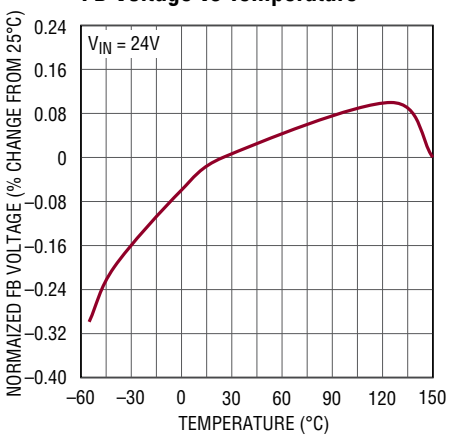
RUN Pin Threshold vs Temperature



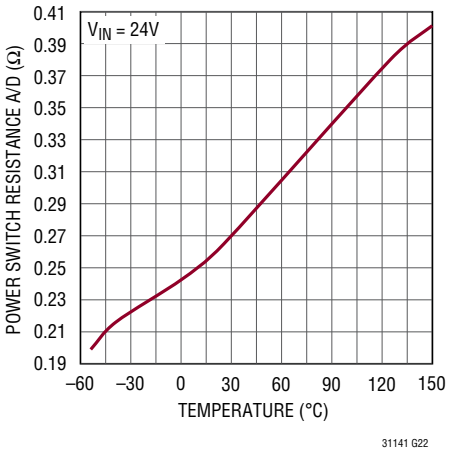
RUN Pin Current vs RUN Pin Voltage



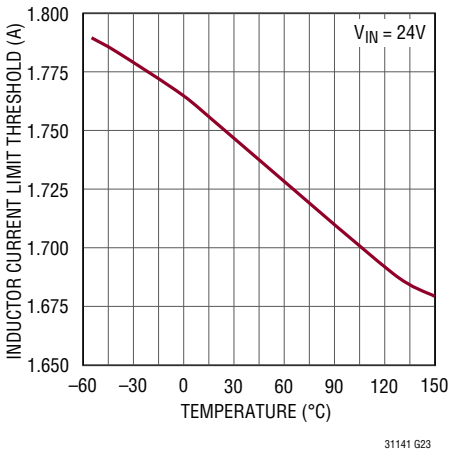
FB Voltage vs Temperature



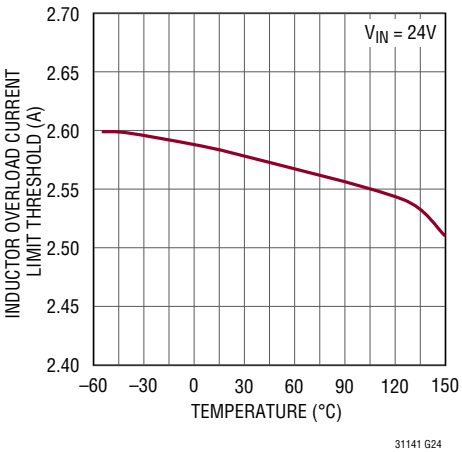
Power Switch Resistance vs Temperature



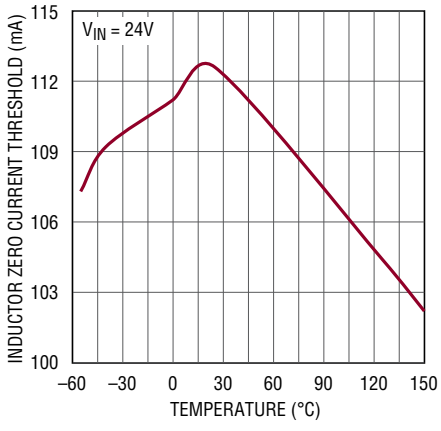
Inductor Current Limit Threshold vs Temperature



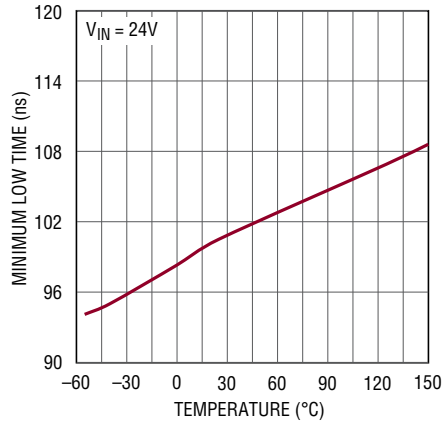
Inductor Overload Current Limit Threshold vs Temperature



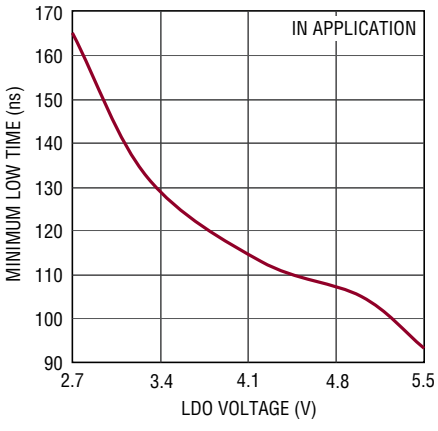
Inductor Zero Current Threshold vs Temperature



SW1/SW2 Minimum Low Times vs Temperature

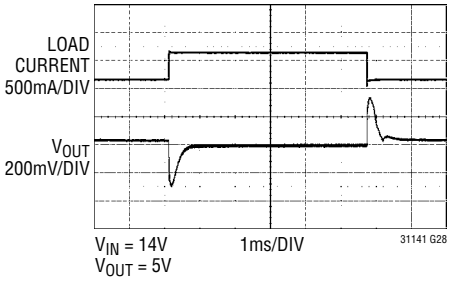


SW1/SW2 Minimum Low Times vs LDO

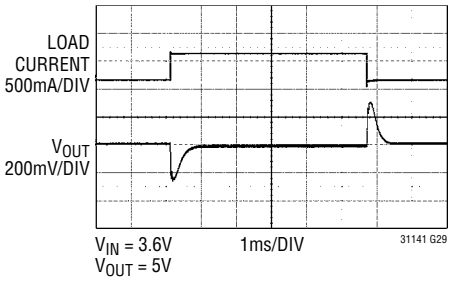


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

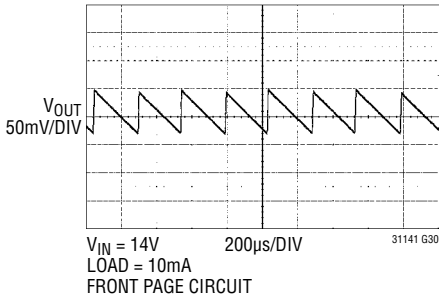
Load Transient in Buck Mode, 100mA to 600mA



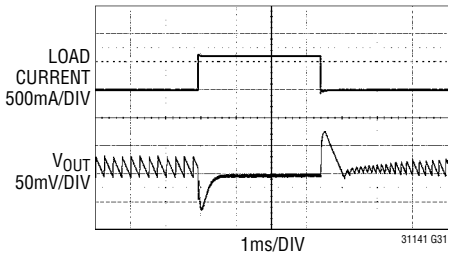
Load Transient in Boost Mode, 100mA to 600mA



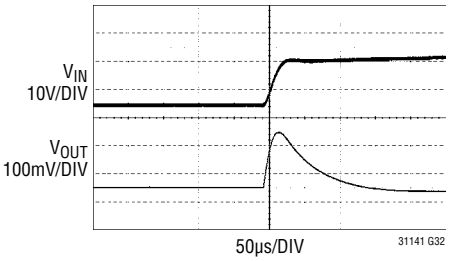
Output Voltage Ripple in Burst Mode Operation



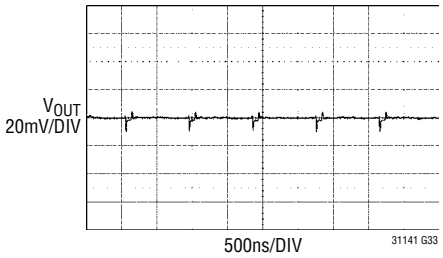
Burst Mode Operation to PWM Mode Output Voltage Response



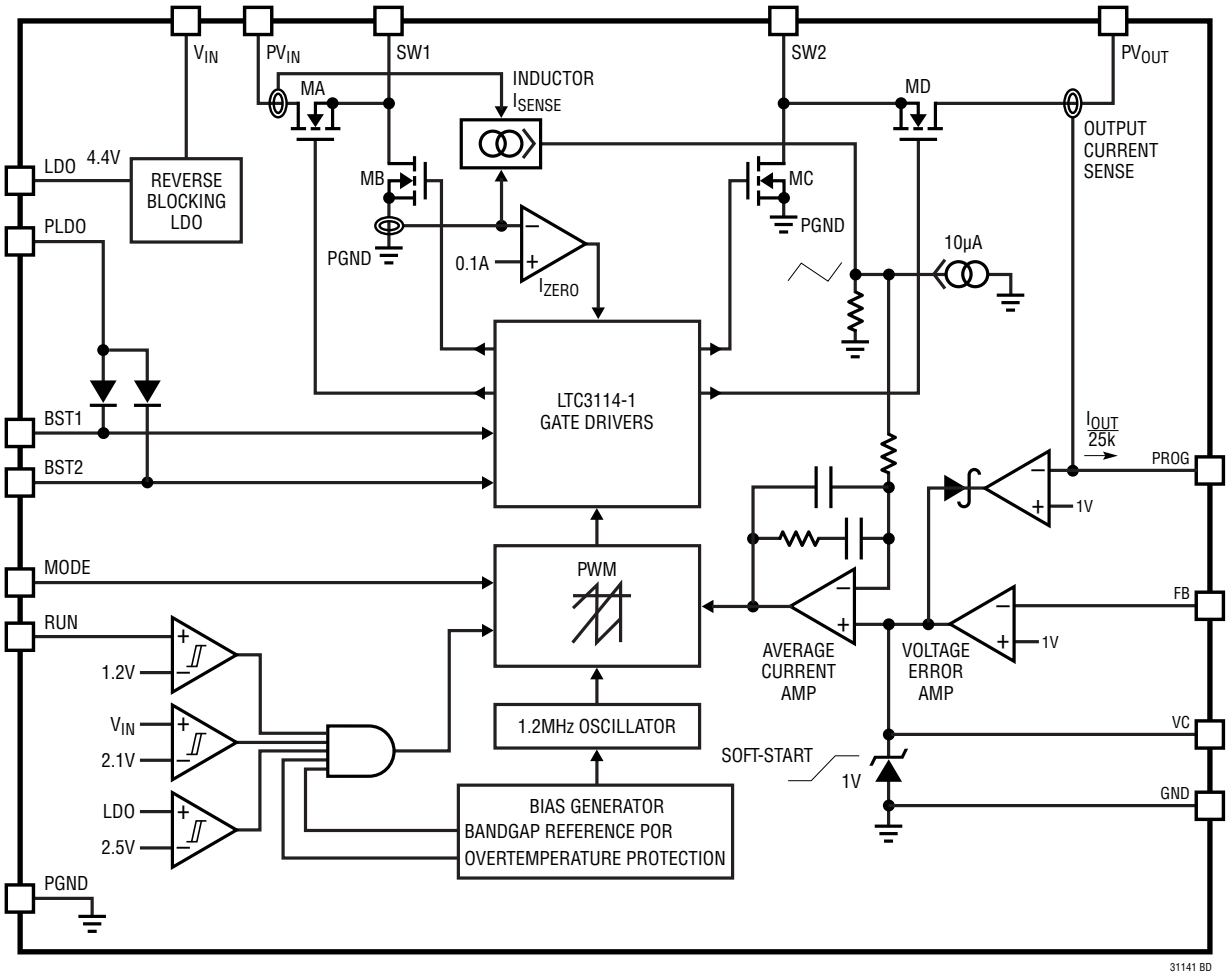
5V Output Voltage Response to Fast Line Transient (4V to 28V in 10µs)



Output Voltage Ripple in PWM Mode



BLOCK DIAGRAM



PIN FUNCTIONS

PGND (Pin 1, Exposed Pad Pin 17): Power Ground Connections. The PGND pin must be electrically connected to a power ground plane in the application. The exposed pad is an additional power ground connection in parallel with Pin 1. Optimal thermal performance requires that the exposed pad be soldered to the PC board and preferably to a ground plane.

SW2 (Pin 2): Buck-Boost Converter Power Switch Pin. This pin is connected to one side of the buck-boost inductor.

PV_{OUT} (Pin 3): Buck-Boost Converter Power Output. This pin should be connected to a low ESR capacitor of at least 10µF. The capacitor should be placed as close to the IC as possible and should have a short return path to PGND. In applications subject to output short circuits through an inductive load, it is recommended that a Schottky diode be installed from ground (anode) to PV_{OUT} (cathode) to limit the extent that PV_{OUT} is driven below ground during the short-circuit transient.

RUN (Pin 4): Input to Enable and Disable the IC and Set Custom Input Undervoltage Lockout (UVLO) Thresholds. The RUN pin can be driven by an external logic signal to enable and disable the IC. In addition, the voltage on this pin can be set by a resistive voltage divider connected to the input voltage in order to provide accurate turn-on and turn-off (UVLO) thresholds. The IC is enabled if RUN exceeds 1.2V nominally. Once enabled, the UVLO threshold has built-in hysteresis of approximately 100mV, so turn-off will occur when the voltage on RUN drops to below 1.1V nominally. To continuously enable the IC, RUN can be tied directly to the input voltage up to the absolute maximum rating.

PROG (Pin 5): Output Current Programming Pin and Output of the Switch D Current Sense Amplifier. A current proportional to the current in switch D, the buck-boost converter output current, is delivered from PROG. The PROG current magnitude is approximately $I_{SWD}/25000$. Connect a parallel resistor and capacitor from PROG to GND to generate a voltage proportional to output current. In applications where this voltage is used to control average output current, the resistor value should be set such that the desired average output current produces 1V on PROG and is given by:

$$R_{PROG}(\Omega) = \frac{1V \bullet 25000}{I_{OUT}(A)}$$

Alternatively, the voltage on PROG can be connected to an A/D converter and used for system diagnostic functions. Refer to the Applications Information section for complete details on how to select the proper values for R_{PROG} and C_{PROG}.

VC (Pin 6): Error Amplifier Output. A frequency compensation network must be connected between VC and GND to stabilize the buck-boost converter. Refer to the Applications Information section for details.

FB (Pin 7): Feedback Voltage Input. A resistor divider connected to this pin sets the output voltage for the buck-boost converter. The nominal FB voltage is 1V. Care should be taken in the routing of the connection to this pin to minimize the possibility of stray coupling from the SW pins. V_{OUT} is determined by the following relationship: V_{OUT} (V) = 1 + R_{TOP}/R_{BOT} where R_{TOP} is connected from PV_{OUT} to FB and R_{BOT} is connected from FB to GND

GND (Pin 8): Signal Ground. This pin is the ground connection for the control circuitry of the IC and must be tied to ground in the application.

LDO (Pin 9): Low Voltage Supply Input for the IC Control Circuitry. This pin powers internal IC control circuitry and must be connected to the LDO pin in the application. A 4.7µF or larger bypass capacitor must be connected between this pin and ground. **Pins LDO and PLDO must be connected together in the application.**

V_{IN} (Pin 10): LDO Supply Connection. This pin provides power to the internal V_{CC} regulator. **Pins V_{IN} and PV_{IN} must be connected together in the application.** If the trace connecting V_{IN} and PV_{IN} is of substantial length, a 1µF capacitor should be connected from V_{IN} to GND as close to the IC pins as possible.

PIN FUNCTIONS

PLDO (Pin 11): Internal LDO Regulator Output. PLDO is the output of the internal linear regulator that generates the LDO rail from V_{IN}. PLDO is also used as the supply connection to the power switch gate drivers. **Pins PLDO and LDO must be connected together in the application.**

BST2 (Pin 12): Flying Capacitor Pin for SW2. This pin must be connected to SW2 through a 68nF capacitor. BST2 is used to generate the gate driver rail for power switch D. Make the PCB trace from BST2 to the boost capacitor as short and direct as possible.

BST1 (Pin 13): Flying Capacitor Pin for SW1. This pin must be connected to SW1 through a 68nF capacitor. BST1 is used to generate the gate driver rail for power switch A. Make the PCB trace from BST2 to the boost capacitor as short and direct as possible.

PV_{IN} (Pin 14): Power Input for the Buck-Boost Converter. A 10µF or larger capacitor must be connected between PV_{IN} and GND as close to the IC as possible. The bypass capacitor ground connection should via directly down to the PCB ground plane. **Pins PV_{IN} and V_{IN} must be connected together in the application.**

SW1 (Pin 15): Buck-Boost Power Converter Switch Pin. This pin is connected to one side of the buck-boost inductor.

MODE (Pin 16): Burst Mode/PWM Mode Control Pin. Forcing MODE high causes the IC to operate in continuous fixed frequency PWM mode. The nominal switching frequency in PWM mode is 1.2MHz. Forcing MODE low enables Burst Mode operation. Burst Mode operation improves efficiency at light loads by only activating the buck-boost converter as needed to maintain the nominal regulated output voltage. If MODE is low, the converter will automatically transition to PWM mode if the load current increases.

OPERATION

INTRODUCTION

The LTC3114-1 is a monolithic, current mode, buck-boost DC/DC converter that can operate over a wide voltage range of 2.2V to 40V and provide up to 1A to the load. Internal, low $R_{DS(ON)}$ N-channel DMOS power switches reduce solution complexity and maximize efficiency. A proprietary switch control algorithm allows the buck-boost converter to maintain output voltage regulation with input voltages that are above, below or equal to the output voltage. Transitions between the step-up or step-down operating modes are seamless and free of transients and subharmonic switching, making this product ideal for noise sensitive applications. The LTC3114-1 operates at a fixed nominal switching frequency of 1.2MHz, which provides an ideal trade-off between small solution size and high efficiency. Current mode control provides inherent input line voltage rejection, simplified compensation and rapid response to load transients. Burst Mode capability is also included in the LTC3114-1 and is user selected via the MODE input pin. In Burst Mode operation, the LTC3114-1 provides exceptional efficiency at light output loading conditions by operating the converter only when necessary to maintain voltage regulation. At higher loads, the LTC3114-1 automatically switches to fixed frequency PWM mode when Burst Mode operation is selected. For 5V V_{OUT} applications, the quiescent current in Burst Mode operation can be as low as 20µA with the internal LDO regulator bootstrapped to the output voltage. If the application requires extremely low noise, continuous PWM operation can also be selected via the MODE pin. The LTC3114-1 also features an accurate RUN comparator threshold with hysteresis. This allows the buck-boost DC/DC converter to turn on and off at user-selected V_{IN} voltage thresholds. With a wide voltage range and programmable output current or monitoring capabilities, the LTC3114-1 is well suited for many demanding power conversion needs.

PROGRAMMABLE AVERAGE OUTPUT CURRENT

The LTC3114-1 includes the ability to program an accurate average output current from the buck-boost DC/DC converter. Whether the application is driving high power

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LEDs, charging batteries, a wide compliance range current source or just providing a well controlled current limit, the LTC3114-1 programmable average output current capability delivers high efficiency and maximum flexibility. The output current limit level is independent of operating mode, (buck or boost), and is active down to approximately 2V on V_{OUT}. Below 2V on V_{OUT}, a secondary foldback current limit circuit is activated to reduce power dissipation. The desired average output current level is programmed with a standard low wattage resistor from PROG to ground. A low loss current sense resistor and accurate current sense amplifier are integrated within the IC, greatly simplifying the PCB layout and design. Factory trimming of the output current limit offset and gain provide a high degree of accuracy, typically within ±5% of the setpoint. The applications section provides details on how to select the programming resistor, R_{PROG}, for the desired average output current level from the LTC3114-1.

PWM Mode Operation

If the MODE pin is high or if the load current on the converter is high enough to command PWM mode operation with MODE low, the LTC3114-1 operates in a fixed 1.2MHz PWM mode using a current mode control loop. PWM mode minimizes output voltage ripple and yields a low noise switching frequency spectrum. A proprietary switching algorithm provides seamless transitions between operating modes and eliminates discontinuities in the average inductor current, inductor ripple current and loop transfer function throughout all modes of operation. These advantages result in increased efficiency, improved loop stability and lower output voltage ripple in comparison to the traditional buck-boost converter.

Figure 1 shows the topology of the LTC3114-1 power stage which is comprised of four N-channel DMOS switches and their associated gate drivers. In PWM mode operation both switch pins transition on every cycle independent of the input and output voltages. In response to the internal control loop command, an internal pulse width modulator generates the appropriate switch duty cycle to maintain regulation of the output voltage.

When stepping down from a high input voltage to a lower output voltage, the converter operates in buck mode and switch D remains on for the entire switching cycle except for the minimum switch low duration (typically 50ns). During the switch low duration, switch C is turned on which forces SW2 low and charges the flying capacitor, C_{BST2}. This ensures that the switch D gate driver power supply rail on BST2 is maintained. The duty cycle of switches A and B are adjusted by the PWM to maintain output voltage regulation in buck mode.

If the input voltage is lower than the output voltage, the converter operates in boost mode. Switch A remains on for the entire switching cycle except for the minimum switch low duration (typically 100ns). During the switch low duration, switch B is turned on which forces SW1 low and charges the flying capacitor, C_{BST1}. This ensures that the switch A gate driver power supply rail on BST1 is maintained. The duty cycle of switches C and D are adjusted by the PWM to maintain output voltage regulation in boost mode.

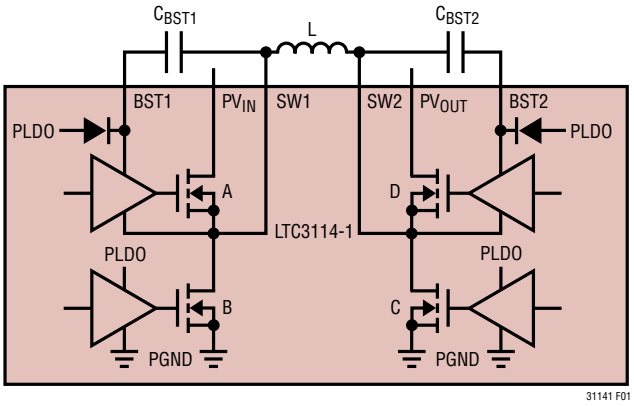


Figure 1. Power Stage Schematic

OPERATION

Oscillator

The LTC3114-1 operates from an internal oscillator with a nominal fixed frequency of 1.2MHz. This allows the DC/DC converter efficiency to be maximized while still using small external components.

Current Mode Control

The LTC3114-1 utilizes average current mode control for the pulse width modulator as shown in Figure 2. Current mode control, both average and the better known peak method, enjoy some benefits compared to other control methods including: simplified loop compensation, rapid response to load transients and improved rejection of line voltage transients.

Referring to Figure 2, an internal high gain transconductance error amplifier monitors V_{OUT} through a voltage divider connected to the FB pin and provides an output, VC, that is used by the current mode control loop to command the appropriate inductor current level. To ensure stability, external frequency compensation components (C_{P1}, C_{P2} and R_Z) must be installed between VC and ground. The procedure for determining these components is provided in the Applications Information section of this data sheet. VC is internally connected to the noninverting input of a high gain, integrating, operational amplifier, referred to in Figure 2, as the average current amp. The inverting input of the average current amplifier is connected to the inductor current sense circuit through a gain setting resistor (R_{CS1}) and to its output (VIA) through an internal frequency compensation network comprised of R_{CS2}, C_{CS1} and C_{CS2}. The average current amplifier's output provides the cycle-by-cycle duty cycle command into the buck-boost PWM circuitry.

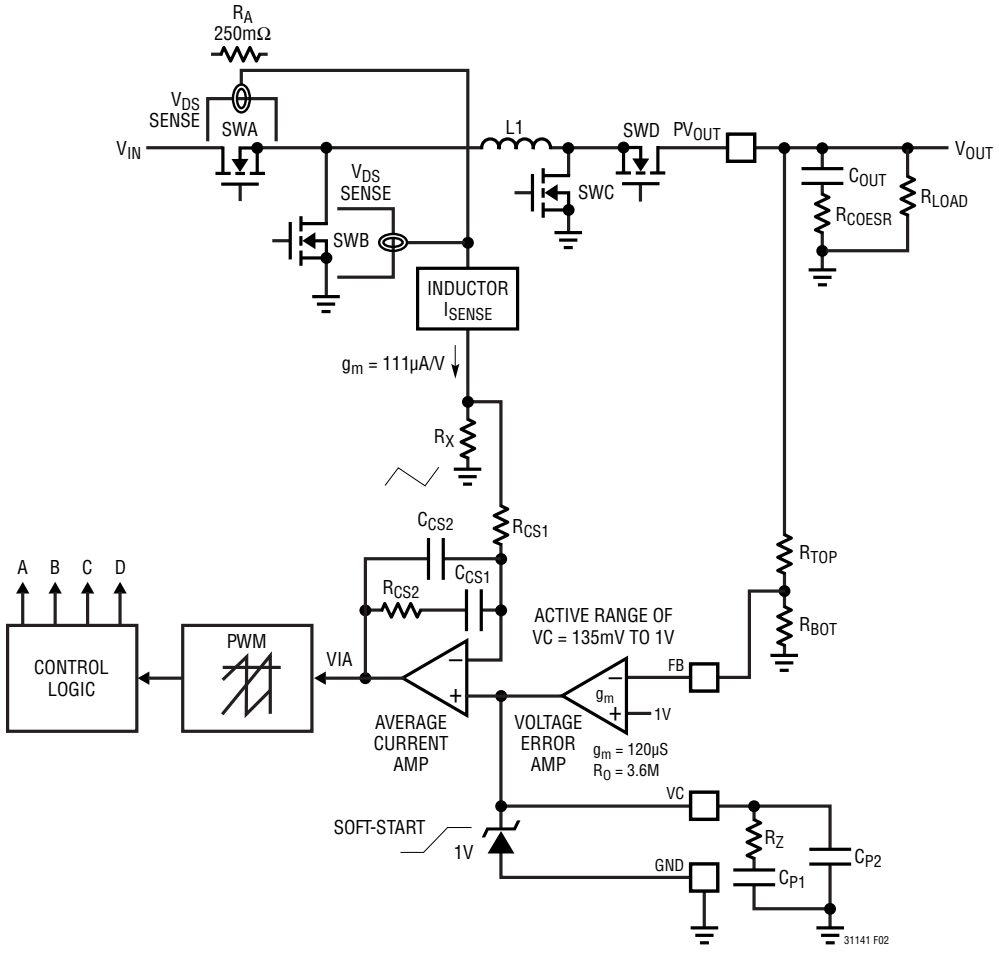


Figure 2. Average Current Mode Control Loop

OPERATION

The noninverting reference level input to the average current amplifier is VC and the feedback or inverting input is driven from the inductor current sensing circuitry. The inductor current sensing circuitry alternately measures the current through switches A and B. The output of the sensing circuitry produces a voltage across resistor R_X that resembles the inductor current waveform transformed to a voltage. If there is an increase in the power converter load on V_{OUT}, the instantaneous level of V_{OUT} will drop slightly, which will increase the voltage level on VC by the inverting action of the voltage error amplifier. When the increase on VC first occurs, the output of the current averaging amplifier, VIA, will also increase momentarily to command a larger duty cycle. This duty cycle increase will result in a higher inductor current level, ultimately raising the average voltage across R_X. Once the average value of the voltage on R_X is equivalent to the VC level, the voltage on VIA will revert very closely to its previous level into the PWM and force the correct duty cycle to maintain voltage regulation at this new higher inductor current level. The average current amplifier is configured as an integrator, so in steady state, the average value of the voltage applied to its inverting input (voltage across R_X) will be equivalent to the voltage on its noninverting, VC. As a result, the average value of the inductor current is controlled in order to maintain voltage regulation. The entire current amplifier and PWM can be simplified as a voltage controlled current source, with the driving voltage coming from VC. VC is commonly referred to as the current command for this reason and the voltage on VC is directly proportional to average inductor current, which can prove useful for many applications.

The voltage error amplifier monitors the output voltage, V_{OUT} through a voltage divider and makes adjustments to the current command as necessary to maintain regulation. The voltage error amplifier therefore controls the outer voltage regulation loop. The average current amplifier makes adjustments to the inductor current as directed by the voltage error amplifier output via VC and is commonly referred to as the inner current-loop amplifier.

The average current mode control technique is similar to peak current mode control except that the average current amplifier, by virtue of its configuration as an integrator, controls average current instead of the peak current. This difference eliminates the peak to average current error inherent to peak current mode control, while maintaining most of the advantages inherent to peak current mode control.

Average current mode control requires appropriate compensation for the inner current loop unlike peak current mode control. The compensation network must have high DC gain to minimize errors between the commanded average current level and actual, high bandwidth to quickly change the commanded current level following transient load steps and a controlled mid-band gain to provide a form of slope compensation unique to average current mode control. Fortunately, the compensation components required to ensure these sometimes conflicting requirements have been carefully selected and are integrated within the LTC3114-1. With the inner loop compensation fixed internally, compensation of the outer voltage loop as is detailed in the applications section, is similar to well known techniques used with peak current mode control.

Inductor Current Sense and Maximum Output Current

As part of the current control loop required for current mode control, the LTC3114-1 includes a pair of current sensing circuits that directly measure the buck-boost converter inductor current as shown in Figure 2. These circuits measure the voltage dropped across switches A and B separately and produce output currents proportional to the switches' voltage drop. By sensing current in this manner, there is no additional power loss incurred, which improves converter efficiency. The amplifier output terminals are summed together into a common resistor, R_X connected to ground. Since switches A and B are never conducting at the same time, the resultant waveform on R_X resembles the inductor current. This replica of the inductor current is used as one input to the current averaging amplifier as described in the previous section.

The voltage error amplifier output, VC, is internally clamped to a nominal level of 1V. Since the average inductor current is proportional to VC, the 1V clamp level sets the maximum average inductor current that can be programmed by the inner current loop. Taking into account the current sense amplifier's gain and the value of R_X, the

OPERATION

maximum average inductor current is approximately 1.7A (typical). In buck mode, the output current is approximately equal to the inductor current, I_L.

$$I_{OUT(BUCK)} \approx I_L \bullet 0.9$$

The SW1/SW2 forced low time on each switching cycle briefly disconnects the inductor from V_{OUT} and V_{IN} resulting in slightly less output current in either buck or boost mode for a given inductor current. In boost mode, the output current is related to average inductor current and duty cycle by:

$$I_{OUT(BOOST)} \approx I_L \bullet (1 – D)$$

where D is the converter duty cycle.

Since the output current in boost mode is reduced by the duty cycle (D), the output current rating in buck mode is always greater than in boost mode. Also, because boost mode operation requires a higher inductor current for a given output current compared to buck mode, the efficiency in boost mode will be lower due to higher $I_{INDUCTOR}^2 \bullet R_{DS(ON)}$ losses in the power switches. This will further reduce the output current capability in boost mode. In either operating mode, however, the inductor peak-to-peak ripple current does not play a major role in determining the output current capability, unlike peak current mode control.

With peak current mode control, the maximum output current capability is reduced by the magnitude of inductor ripple current because the peak inductor current level is the control variable, but the average inductor current is what determines the output current. The LTC3114 -1 measures and controls average inductor current, and therefore, the inductor ripple current magnitude has little effect on the maximum current capability in contrast to an equivalent peak current mode converter. Under most conditions in buck mode, the LTC3114 -1 is capable of providing 1A to the load. Under certain conditions, more output current is possible, refer to the Typical Performance Characteristics section for more details. In boost mode, as described previously, the output current capability is related to the boost ratio or duty cycle (D). For a 3.6V V_{IN} to 5V output application, the LTC3114-1 can provide up to 500mA to the load. Refer to the Typical Performance Characteristics section for more detail on output current capability.

At VC levels below 135mV, the LTC3114-1 will not command any current because the internal current sense signal has a built-in 135mV offset. Therefore, the active range of VC is between approximately 135mV (zero current) and 1V (full current). In some applications, an external circuit may be used to control the VC voltage level. Any such circuit needs to have the capability to sink or source the approximate 12µA provided by the internal error amplifier and to pull below 135mV to disable the current command, if necessary.

OVERLOAD CURRENT LIMIT AND ZERO CURRENT COMPARATOR

The internal current sense waveform is also used by the peak overload current (I_{PEAK}) and zero current (I_{ZERO}) comparators. The I_{PEAK} current comparator monitors I_{SENSE} and halts converter operation if the inductor current level exceeds its maximum internal threshold, which is approximately 50% above the normal maximum current level commanded by the current control loop. An inductor current level of this magnitude will only occur during a fault, such as an output short circuit or a fast V_{IN} (line) transient. If the I_{PEAK} comparator is engaged, the PWM is halted for the remainder of the switching cycle with SW1 and SW2 held low. If V_{OUT} is less than approximately 1.8V when the peak limit occurs, then a soft-start cycle is initiated. In the event that the current overload is the result of an output short-circuit condition, the LTC3114-1 will remain in a low frequency restart mode, keeping the on-chip power dissipation to very low levels. If the short circuit is removed, the LTC3114-1 will restart in the normal fashion.

The LTC3114-1 exhibits discontinuous inductor current operation at light output loads by virtue of the I_{ZERO} comparator circuit under most operating conditions. This improves efficiency at light output loads if PWM mode operation compared to continuous conduction mode. If the internal current sense waveform transitions below the internally set zero current threshold, the LTC3114-1 will disconnect the inductor from V_{OUT}, by shutting off switch D, to prevent discharge of the output capacitor. The I_{ZERO} circuitry is reset by the oscillator clock at the end of the switching cycle. The I_{ZERO} comparator threshold is set

OPERATION

slightly above zero current to compensate for comparator propagation delay. In some cases, the inductor current may reverse slightly if there is a very high voltage output or small inductor resulting in a small amount of residual energy left in the inductor following a zero current event. In this case the LTC3114-1 SW1 waveform will display a characteristic half sine wave between the time at which Izero is detected and when the next switching cycle commences. This is because SWC is the only active (on) switch following an I_{ZERO} event and this behavior is not harmful to the LTC3114-1.

Burst Mode Operation

When the MODE pin is held low, the LTC3114-1 is configured for Burst Mode operation. As a result, the buck-boost DC/DC converter will operate with normal continuous PWM switching above a predetermined minimum output load and will automatically transition to power saving Burst Mode operation below this output load level. Refer to the Typical Performance Characteristics section of this data sheet to determine the Burst Mode transition threshold for various combinations of V_{IN} and V_{OUT}. If MODE is low, at light output loads, the LTC3114-1 will go into a standby or sleep state when the output voltage achieves its nominal regulation level. The sleep state halts PWM switching and powers down all non-essential functions of the IC, significantly reducing the quiescent current of the LTC3114-1. This greatly improves overall power conversion efficiency when the output load is light. Since the converter is not operating in sleep, the output voltage will slowly decay at a rate determined by the output load resistance and the output capacitor value. When the output voltage has decayed by a small amount, typically 1%, the LTC3114-1 will wake and resume normal PWM switching operation until the voltage on V_{OUT} is restored to the previous level. If the load is very light, the LTC3114-1 may only need to switch for a few cycles to restore V_{OUT} and may sleep for extended periods of time, significantly improving efficiency.

Soft-Start

The LTC3114-1 soft-start circuit minimizes input current transients and output voltage overshoot on initial power up. The required timing components for soft-start are internal to the LTC3114-1 and produce a nominal soft-start duration of approximately 2ms. The internal soft-start circuit slowly ramps the error amplifier output, VC. In doing so, the current command of the IC is also slowly increased, starting from zero. It is unaffected by output loading or output capacitor value. Soft-start is reset by undervoltage lockout on both V_{IN} and LDO, the accurate RUN pin comparator, thermal shutdown and the overload current limit as described previously.

LDO REGULATOR

An internal low dropout regulator generates a nominal 4.4V rail from V_{IN}. The LDO rail powers the internal control circuitry and power device gate drivers of the LTC3114-1. The LDO regulator is disabled in shutdown to reduce quiescent current and is enabled by forcing the RUN pin above its logic threshold. The LDO regulator includes current-limit protection to safeguard against accidental short-circuiting of the LDO rail. In 5V V_{OUT} applications, the LDO can be driven by V_{OUT} through a Schottky diode, commonly referred to as bootstrapping. Bootstrapping can provide a significant efficiency improvement, particularly when V_{IN} is very high and also allows operation to the minimum rated input voltage of 2.2V.

UNDERVOLTAGE LOCKOUT

The LTC3114-1 undervoltage lockout (UVLO) circuit disables operation of the internal power switches and keeps other IC functions in a reset state if either the input voltage applied to V_{IN} or the LDO output voltage are below their respective UVLO thresholds. There are two UVLO circuits, one that monitors V_{IN} and another that monitors LDO. The V_{IN} UVLO comparator has a falling voltage threshold of 2.1V (typical). If V_{IN} falls below this level, IC operation is disabled until V_{IN} rises above 2.2V (typical), as long as the LDO voltage is above its UVLO threshold. The LDO UVLO has a falling voltage threshold of 2.4V (typical). If the LDO voltage falls below this threshold, IC operation is disabled until LDO rises above 2.5V (typical) as long as V_{IN} is above its nominal UVLO threshold level.

OPERATION

Depending on the particular application, either of these UVLO thresholds could be the limiting factor affecting the minimum input voltage required for operation. The LTC3114-1 LDO regulator uses V_{IN} for its power input. If LDO is not bootstrapped, then there exists a voltage drop or dropout voltage between V_{IN} and LDO. The dropout voltage is proportional to the loading on LDO, which is primarily due to the gate charge and capacitive charging currents inherent to the internal power switches. The loading on LDO and the LDO dropout voltage, therefore, are proportional to V_{IN} and V_{OUT}. For this reason, the minimum input voltage required for operation is limited by the LDO minimum voltage as input voltage (V_{IN}) will always be higher than LDO in the normal (non-bootstrapped) configuration. The Typical Performance Characteristics section of this data sheet provides guidance on the dropout voltage between V_{IN} and LDO over the range of V_{IN} and V_{OUT}.

In applications where LDO is bootstrapped (powered by V_{OUT} through a Schottky diode or auxiliary power rail), the minimum input voltage for operation (after start-up) will be limited only by the V_{IN} UVLO threshold (2.1V typical). *Please note that if the bootstrap voltage is derived from the LTC3114-1 V_{OUT} and not an independent power rail, then the minimum input voltage required for* ***initial start-up*** *is still limited by the minimum LDO voltage (2.6V typical).*

RUN PIN COMPARATOR

In addition to serving as a logic-level input to enable certain functions of the IC, the RUN pin includes an accurate internal comparator that allows it to be used to set custom rising and falling on/off thresholds with the addition of an external resistor divider. When RUN is driven above its logic threshold (0.7V typical), the LDO regulator is enabled, which provides power to the internal control circuitry of the IC. If the voltage on RUN is increased further so that it exceeds the RUN comparator accurate analog threshold (1.2V nominal), all functions of the buck-boost converter will be enabled and a startup sequence will ensue.

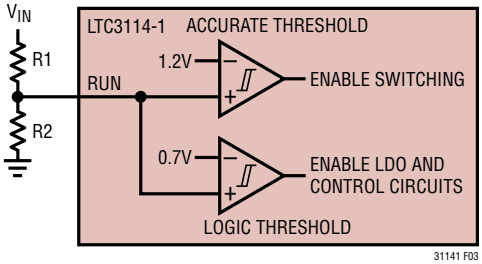


Figure 3. Accurate RUN Pin Comparator

If RUN is brought below the accurate comparator threshold, the buck-boost converter will inhibit switching, but the LDO regulator and control circuitry will remain powered unless RUN is brought below its logic threshold. Therefore, in order to completely shut down the IC and reduce the V_{IN} current to 3µA (typical), it is necessary to ensure that RUN is brought below its worst-case low-logic threshold of 0.3V. RUN is a high voltage input and can be tied directly to V_{IN} to continuously enable the IC when the input supply is present. Also note that RUN can be driven above V_{IN} or V_{OUT} as long as it stays within the operating range of the IC, that is, less than 40V. If RUN is forced above 5V, it will sink a small current as given by the following equation:

$$I_{RUN} \approx \frac{V_{RUN} - 5V}{5M\Omega}$$

With the addition of an optional resistor divider as shown in Figure 3, the RUN pin can be used to establish a user-programmable turn on and turn off threshold.

The buck-boost converter is enabled when the voltage on RUN reaches 1.205V (nominal). Therefore, the turn-on voltage threshold on V_{IN} is given by:

$$V_{TURNON} = 1.205V\left(1 + \frac{R1}{R2}\right)$$

Once the converter is enabled, the RUN comparator includes a built-in hysteresis of approximately 140mV, so that the turn-off threshold will be approximately 8.33% lower than the turn-on threshold. Put another way, the internal threshold level for the RUN comparator looks like 1.1V after the IC is enabled.

OPERATION

The RUN comparator is relatively noise insensitive, but there may be cases dues to PCB layout, very large value resistors for R1 and R2 or proximity to noisy components where noise pickup is unavoidable and may cause the turn on or turn off of the IC to be intermittent. In these cases, a filter capacitor can be added across R2 to ensure proper operation.

THERMAL CONSIDERATIONS

The power switches of the LTC3114-1 are designed to operate continuously with currents up to the internal current limit thresholds. However, when operating at high current levels, there may be significant heat generated within the IC. In addition, the LDO regulator can generate a significant amount of heat when V_{IN} is very high. This adds to the total power dissipation of the IC. As described elsewhere in this data sheet, bootstrapping of the LDO for 5V output applications can essentially eliminate the LDO power dissipation term and significantly improve efficiency. As a result, careful consideration must be given to the thermal environment of the IC in order to provide a means to remove heat from the IC and ensure that the LTC3114-1 is able to provide its full rated output current. Specifically, the exposed die attach pad of both the DHC and FE packages must be soldered to a copper layer on the PCB to maximize the conduction of heat out of the IC package. This can be accomplished by utilizing multiple vias from the die attach pad connection underneath the IC package to other PCB layer(s) containing a large copper plane. A typical board layout incorporating these concepts is shown in Figure 4.

If the IC die temperature exceeds approximately 165°C, overtemperature shutdown will be invoked and all switching will be inhibited. The part will remain disabled until the die temperature cools by approximately 10°C. The soft-start circuit is re-initialized in overtemperature shutdown to provide a smooth recovery when the IC die temperature cools enough to resume operation.

Start-Up Into a Pre-Biased V_{OUT}

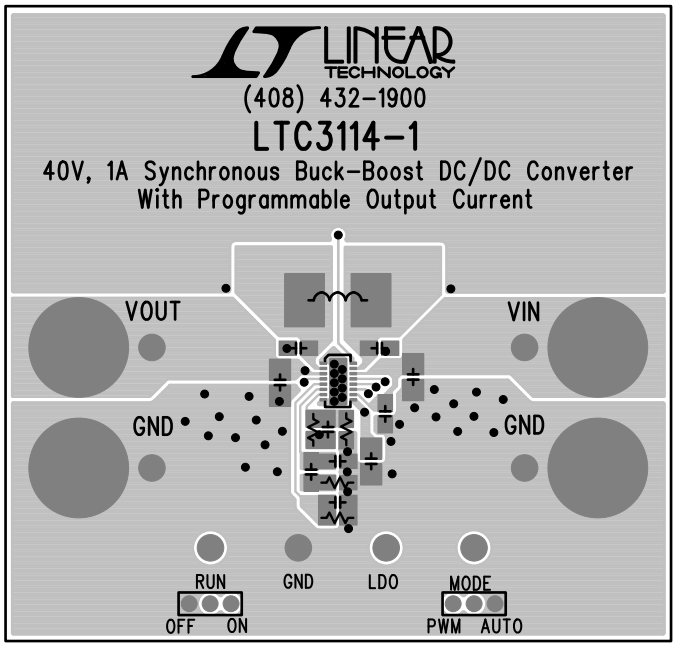
Some applications require the LTC3114-1 to start up into an output voltage (V_{OUT}), that is pre-biased by an external source to some level. It is desirable at LTC3114-1 start-up to minimize current taken from the pre-bias voltage source and V_{OUT} storage capacitor to prevent V_{OUT} glitches and currents fed backwards into the V_{IN} power source of the LTC3114-1.

If the LTC3114-1 V_{IN} voltage is higher than the pre-biased V_{OUT}, indicating buck mode operation, then there will be minimal reverse current at start-up. However, if the LTC3114-1 V_{IN} voltage is lower than the pre-biased V_{OUT}, indicating boost mode operation, then it is possible for a brief, but substantial reverse current to be taken by the LTC3114-1 from V_{OUT}. The duration of this reverse current is approximately 100µs to 200µs. The magnitude is inversely proportional to the V_{IN} voltage and dependent upon external component values.

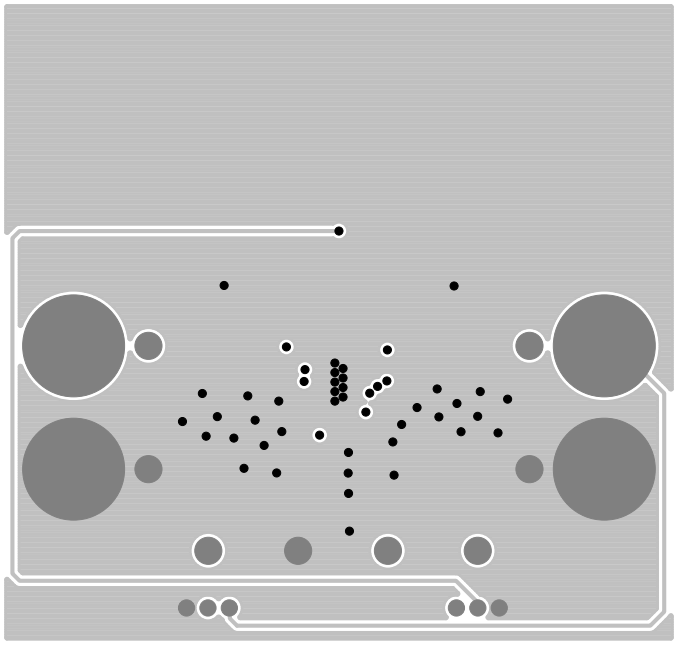
Prevention of pre-biased V_{OUT} reverse current in boost mode can be achieved in two ways. The preferred method is to ensure that the pre-biased V_{OUT} voltage level is set higher than the nominal V_{OUT} regulation level. For example, if V_{OUT} is pre-biased to 13V, then setting the V_{OUT} regulation voltage of the LTC3114-1 to less than 13V, taking into account error margins, will result in negligible or zero reverse current at start-up. If this is not possible, then a Schottky diode can be connected in series between V_{OUT} of the LTC3114-1 and the converter output to block reverse current .

OPERATION

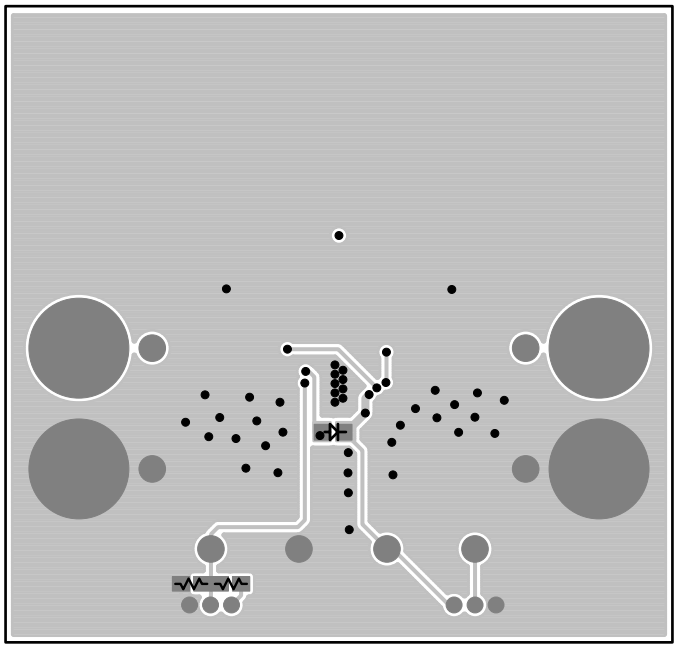
Top Layer



2nd Layer



Bottom Layer



3rd Layer

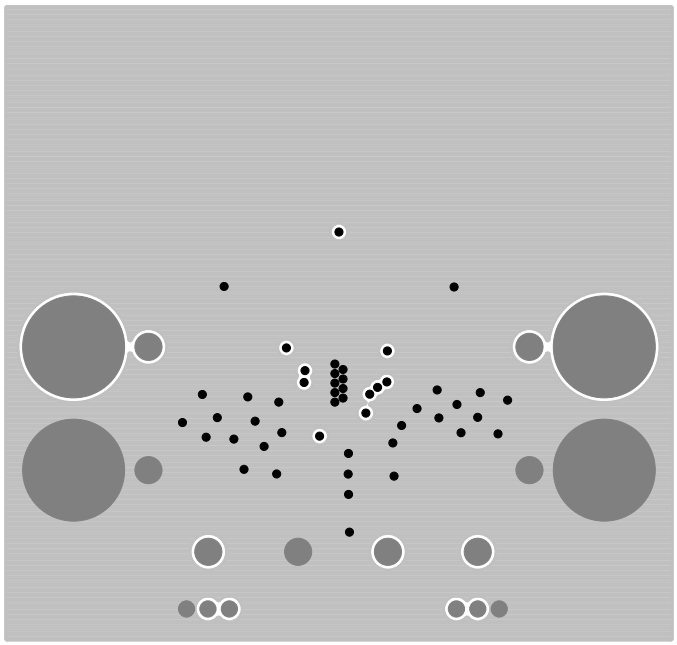


Figure 4. Typical 4 Layer PC Board Layout

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A standard application circuit for the LTC3114-1 is shown on the front page of this data sheet. The appropriate selection of external components is dependent upon the required performance of the IC in each particular application given considerations and trade-offs such as PCB area, input and output voltage range, output voltage ripple, required efficiency, thermal considerations and cost. This section of the data sheet provides some basic guidelines and considerations to aid in the selection of external components and the design of the applications circuit.

LDO Capacitor Selection

The LDO output of the LTC3114-1 is generated from V_{IN} by a low dropout linear regulator. The LDO regulator has been designed for stable operation with a wide range of output capacitors. For most applications, a low ESR capacitor of at least 4.7µF should be used. The capacitor should be located as close to the PLDO pin as possible and connected to the LDO pin and ground through the shortest traces possible. PLDO is the regulator output and is also the internal supply pin for the gate drivers and boost rail charging diodes. The LDO pin is the supply connection for the remainder of the control circuitry. The LDO and PLDO pins must be connected together on the PCB. If the connecting trace cannot be made short, an additional 0.1µF bypass capacitor should be connected between the LDO pin and ground as close to the package pins as possible.

Inductor Selection

The choice of inductor used in LTC3114-1 application circuits influences the maximum deliverable output current, the converter bandwidth, the magnitude of the inductor current ripple and the overall converter efficiency. The inductor must have a low DC series resistance or output current capability and efficiency will be compromised. Larger inductor values reduce inductor current ripple but will not increase output current capability as is the case with peak current mode control as described in the Maximum Output Current section of this data sheet. Larger value inductors also tend to have a higher DC series resistance for a given case size, which will have a negative impact on efficiency. Larger values of inductance will also lower the right half plane (RHP) zero frequency when operating in boost mode, which requires the converter bandwidth to be set lower in frequency, slowing the converter's response to load transients. Nearly all LTC3114-1 application circuits deliver the best performance with an inductor value between 4.7µH and 15µH. Buck mode-only applications can use the larger inductor values as they are unaffected by the RHP zero, while mostly boost applications generally require inductance on the low end of this range depending on how deep they will operate in boost mode.

Regardless of inductor value, the saturation current rating should be selected such that it is greater than the worst-case average inductor current plus half of the ripple current. The peak-to-peak inductor current ripple for each operational mode can be calculated from the following formula, where f is the switching frequency (1.2MHz), L is the inductance in µH and t_{LOW} is the switch pin minimum low time in µs. The switch pin minimum low time is typically 0.05µs.

$$\Delta I_{L(P-P)(BUCK)} = \frac{V_{OUT}}{L}\left(\frac{V_{IN}-V_{OUT}}{V_{IN}}\right)\left(\frac{1}{f}-t_{LOW}\right) \text{ Amps}$$

$$\Delta I_{L(P-P)(BOOST)} = \frac{V_{IN}}{L}\left(\frac{V_{OUT}-V_{IN}}{V_{OUT}}\right)\left(\frac{1}{f}-t_{LOW}\right) \text{ Amps}$$

It should be noted that the worst-case inductor peak-to-peak inductor ripple current occurs when the duty cycle in buck mode is maximum (highest V_{IN}) and in boost mode when the duty cycle is 50% ($V_{OUT} = 2 \bullet V_{IN}$). As an example, if V_{IN} (minimum) = 3.6V and V_{IN} (maximum) = 40V, V_{OUT} = 5V and L = 6.8µH, the peak-to-peak inductor ripples at the voltage extremes (40V V_{IN} for buck and 3.6V V_{IN} for boost) are:

Buck = 504mA peak-to-peak

Boost = 116mA peak-to-peak

One-half of this inductor ripple current must be added to the highest expected average inductor current in order to select the proper saturation current rating for the inductor.

In addition to its influence on power conversion efficiency, the inductor DC resistance can also impact the maximum output current capability of the buck-boost converter particularly at low input voltages. In buck mode, the output current of the buck-boost converter is primarily limited by the inductor current reaching the average current limit

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threshold defined by VC. However, in boost mode, especially at large step-up ratios, the output current capability can also be limited by the total resistive losses in the power stage. These losses include, switch resistances, inductor DC resistance and PCB trace resistance. Avoid inductors with a high DC resistance (DCR) as they can degrade the maximum output current capability from what is shown in the Typical Performance Characteristics section and from the Typical Application circuits. As a guideline, the inductor DCR should be significantly less than the typical power switch resistance of 250mΩ. The only exceptions are applications that have a maximum output current much less than what the LTC3114-1 is capable of delivering.

Different inductor core materials and styles have an impact on the size and price of an inductor at any given current rating. Shielded construction is generally preferred as it minimizes the chances of interference with other circuitry. The choice of inductor style depends upon the price, sizing, and EMI requirements of a particular application. Table 1 provides a small sampling of inductors that are well suited to many LTC3114-1 applications.

Table 1. Representative Surface Mount Inductors

PART NUMBER	VALUE (µH)	DCR (mΩ)	MAX DC CURRENT (A)	SIZE (mm) W × L × H
Coilcraft				
LPS6225	4.7	65	3.2	6.2 × 6.2 × 2.5
LPS6235	6.8	75	2.8	6.2 × 6.2 × 3.5
MSS1038	22	70	3.3	10.2 × 10.5 × 3.8
D03316P	15	50	3.0	12.9 × 9.4 × 5.2
Cooper-Bussmann				
CD1-150-R	15	50	3.6	10.5 × 10.4 × 4.0
DR1030-100-R	10	40	3.18	10.3 × 10.5 × 3.0
FP3-8R2-R	8.2	74	3.4	7.3 × 6.7 × 3.0
DR1040-220-R	22	54	2.9	10.3 × 10.5 × 4.0
Panasonic				
ELLCTV180M	18	30	3.0	12 × 12 × 4.2
ELLATV100M	10	23	3.3	10 × 10 × 4.2
Sumida				
CDRH8D28/HP	10	78	3.0	8.3 × 8.3 × 3
CDR10D48MNNP	39	105	3.0	10.3 × 10.3 × 5
CDRH8D28NP	4.7	24.7	3.4	8.3 × 8.3 × 3
Taiyo-Yuden				
NR10050T150M	15	46	3.6	9.8 × 9.8 × 5
TOKO				
B1047AS-6R8N	6.8	36	2.9	7.6 × 7.6 × 5
B1179BS-150M	15	56	3.3	10.3 × 10.3 × 4
892NAS-180M	18	42	3.0	12.3 × 12.3 × 4.5
Wurth				
7447789004	4.7	33	2.9	7.3 × 7.3 × 3.2
7440650068	6.8	33	3.6	10 × 10 × 3
744771133	33	49	2.7	12 × 12 × 6
744066150	15	40	3.2	10 × 10 × 3.8

Output Capacitor Selection

A low effective series resistance (ESR) output capacitor should be connected at the output of the buck-boost converter in order to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent option as they have low ESR and are available in small footprints. The capacitor value should be chosen large enough to reduce the output voltage ripple to acceptable levels. Neglecting the capacitor's ESR and ESL (effect series inductance), the peak-to-peak output voltage ripple can be calculated by the following formula, where f is the frequency in MHz (1.2MHz for the LTC3114-1), C_{OUT} is the capacitance in µF, t_{LOW} is the switch pin minimum low time in us (0.1µs for the LTC3114-1) and I_{LOAD} is the output current in Amps.

$$\Delta V_{P-P(BUCK)} = \frac{I_{LOAD} t_{LOW}}{C_{OUT}} \text{ Volts}$$

$$\Delta V_{P-P(BOOST)} = \frac{I_{LOAD}}{f C_{OUT}} \left(\frac{V_{OUT} - V_{IN} + t_{LOW} f V_{IN}}{V_{OUT}} \right) \text{ Volts}$$

Examining the previous equations reveal that the output voltage ripple increases with load current and is generally higher in boost mode than in buck mode. Note that these equations only take into account the voltage ripple that occurs from the inductor current to the output being discontinuous. They provide a good approximation to the ripple at any significant load current but underestimate the output voltage ripple at very light loads where the output voltage ripple is dominated by the inductor current ripple.

In addition to the output voltage ripple generated across the output capacitance, there is also output voltage ripple produced across the internal resistance of the output capacitor. The ESR-generated output voltage ripple is proportional to the series resistance of the output capacitor and is given by the following expressions where R_{ESR} is

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the series resistance of the output capacitor and all other terms as previously defined.

$$\Delta V_{P-P(BUCK)} = \frac{I_{LOAD}R_{ESR}}{1-t_{LOW}f} \cong I_{LOAD}R_{ESR} \text{ Volts}$$

$$\Delta V_{P-P(BOOST)} = \frac{I_{LOAD}R_{ESR}V_{OUT}}{V_{IN}(1-t_{LOW}f)} \cong I_{LOAD}R_{ESR}\left(\frac{V_{OUT}}{V_{IN}}\right) \text{ Volts}$$

In most LTC3114-1 applications, an output capacitor between 10µF and 22µF will work well.

Input Capacitor Selection

The PV_{IN} pin carries the full inductor current and provides power to internal control circuits in the IC. To minimize input voltage ripple and ensure proper operation of the IC, a low ESR bypass capacitor with a value of at least 6.8µF should be located as close to the pin as possible. The traces connecting this capacitor to PV_{IN} and the ground plane should be made as short as possible. The V_{IN} pin provides power to the LDO regulator and other internal circuitry. If the PCB trace connecting PV_{IN} to V_{IN} is long, it is recommended to add an additional small 0.1µF bypass capacitor near the V_{IN} pin.

When powered through long leads or from a high ESR power source, a larger value bulk input capacitor may be required. In such applications, a 47µF to 100µF electrolytic capacitor in parallel with a 1µF ceramic capacitor generally yields a high performance, low cost solution.

Recommended Input and Output Capacitors

The capacitors used to filter the input and output of the LTC3114-1 must have low ESR and must be rated to handle the large AC currents generated by the switching converters. This is important to maintain proper functioning of the IC and to reduce output voltage ripple. There are many capacitor types that are well suited to these applications including multilayer ceramic, low ESR tantalum, OS-CON and POSCAP technologies. In addition, there are certain types of electrolytic capacitors such as solid aluminum organic polymer capacitors that are designed for low ESR and high AC currents and these are also well suited to some LTC3114-1 applications. Table 2 provides a partial listing of appropriate capacitors to use with the LTC3114-1. The choice of capacitor technology is primarily dictated by a trade-off between size, leakage current and cost. In backup power applications, the input or output capacitor might be a super or ultra capacitor with a capacitance value measuring in the Farad range. The selection criteria in these

Table 2. Representative Bypass and Output Capacitors

MANUFACTURER, PART NUMBER	VALUE (µF)	VOLTAGE (V)	SIZE L × W × H (mm), TYPE, ESR
AVX			
12103D226MAT2A	22	25	3.2 × 2.5 × 2.79 X5R Ceramic
TPME226K050R0075	22	50	7.3 × 4.3 × 4.1 Tantalum, 75mΩ
Kemet			
C2220X226K3RACTU	22	25	5.7 × 5.0 × 2.4 X7R Ceramic
A700D226M016ATE030	22	16	7.3 × 4.3 × 2.8 Alum. Polymer, 30mΩ
Murata			
GRM32ER71E226KE15L	22	25	3.2 × 2.5 × 2.5 X7R Ceramic
Nichicon			
PLV1E121MDL1	82	25	8 × 8 × 12 Alum. Polymer, 25mΩ
Panasonic			
ECJ-4YB1E226M	22	25	3.2 × 2.5 × 2.5 X5R Ceramic
Sanyo			
25TQC22MV	22	25	7.3 × 4.3 × 3.1 POSCAP, 50mΩ
16TQC100M	100	16	7.3 × 4.3 × 1.9 POSCAP, 45mΩ
25SVPF47M	47	25	6.6 × 6.6 × 5.9 OS-CON, 30mΩ
Taiyo Yuden			
UMK325BJ106MM-T	10	50	3.2 × 2.5 × 2.5 X5R Ceramic
TMK325BJ226MM-T	22	25	3.2 × 2.5 × 2.5 X5R Ceramic
TDK			
KTJ500B226M55BFT00	22	50	6.0 × 5.3 × 5.5 X7R Ceramic
C5750X7R1H106M	10	50	5.7 × 5.0 × 2.0 X7R Ceramic
CKG57NX5R1E476M	47	25	6.5 × 5.5 × 5.5 X5R Ceramic
Vishay			
94SVPD476X0035F12	47	35	10.3 × 10.3 × 12.6 OS-CON, 30mΩ

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applications are generally similar except that voltage ripple is generally not a concern. Some capacitors exhibit a high DC leakage current which may preclude their consideration for applications that require a very low quiescent current in Burst Mode operation.

Ceramic capacitors are often utilized in switching converter applications due to their small size, low ESR and low leakage currents. However, many ceramic capacitors intended for power applications experience a significant loss in capacitance from their rated value as the DC bias voltage on the capacitor increases. It is not uncommon for a small surface mount capacitor to lose more than 50% of its rated capacitance when operated near its maximum rated voltage. This effect is generally reduced as the case size is increased for the same nominal value capacitor. As a result, it is often necessary to use a larger value capacitance or a higher voltage rated capacitor than would ordinarily be required to actually realize the intended capacitance at the operating voltage of the application. X5R and X7R dielectric types are recommended as they exhibit the best performance over the wide operating range and temperature of the LTC3114-1. To verify that the intended capacitance is achieved in the application circuit, be sure to consult the capacitor vendor's curve of capacitance versus DC bias voltage.

Programming Custom V_{IN} Turn-On and Turn-Off Thresholds

With the addition of an external resistor divider connected to the input voltage as shown in Figure 3, the RUN pin can be used to program the input voltage at which the LTC3114-1 is enabled and disabled.

For a rising input voltage, the LTC3114-1 is enabled when V_{IN} reaches the threshold given by the following equation, where R1 and R2 are the values of the resistor divider resistors specified in kΩ:

$$V_{TH(RISING)} = 1.2\left(\frac{R1+R2}{R2}\right) \text{ Volts}$$

Once the IC is enabled, it will remain so until the input voltage drops below the comparator threshold by the hysteresis voltage of approximately 100mV, measured on the RUN pin. Therefore, the amount of hysteresis is approximately 8.33% of the programmed turn-on threshold level given in the previous equation.

Bootstrapping the LDO Regulator

The high and low side gate drivers are powered through the PLDO rail, which is generated from the input voltage, V_{IN}, through an internal linear regulator. In some applications, especially at high input voltages, the power dissipation in the linear regulator can become a major contributor to thermal heating of the IC. The Typical Performance Characteristics section of this data sheet provides data on the LDO/PLDO current and resulting power loss versus V_{IN} and V_{OUT}. A significant performance advantage can be attained in applications where converter output voltage (V_{OUT}) is programmed to 5V, if V_{OUT} is used to power the LDO/PLDO rails. Powering the LDO/PLDO rails in this manner is referred to as bootstrapping. This can be done by connecting a Schottky diode from V_{OUT} to LDO/PLDO as shown in Figure 5. With the bootstrap diode installed, the gate driver currents are supplied by the buck-boost converter at high efficiency rather than through the internal linear regulator. The internal linear regulator contains reverse blocking circuitry that allows LDO/PLDO pins to be driven slightly above their nominal regulation level with only a very slight amount of reverse current. Please note that the bootstrapping supply (either V_{OUT} or a separate regulator) must be limited to less than 5.7V.

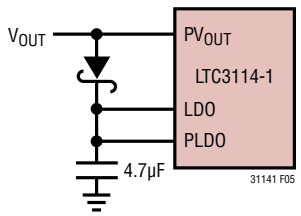

Figure 5. Bootstrapping PLDO and LDO

Average Output Current Limit Programming

The LTC3114-1 includes an average output current programming feature that transforms the LTC3114-1 into a wide voltage compliance range, high efficiency, constant current source. A resistor from PROG to ground programs the desired level of average output current up to 1A. Potential uses include high brightness LED driving and constant current battery or capacitor charging.

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A simplified diagram of the average output current programming circuitry is shown in the Block Diagram. An internal sense resistor, R_S, and low offset amplifier directly measure current in the V_{OUT} path and produce a small fraction of this current out of the PROG pin. Accordingly, a resistor and filtering capacitor connected from PROG to ground produce a voltage proportional to average output current on PROG. An internal transconductance amplifier compares the PROG voltage to the fixed 1V internal reference. If the PROG voltage tries to exceed the 1V reference level, this amplifier will pull down on VC and take command of the PWM. As described earlier, VC is the current command voltage, so limiting VC in this manner will also limit output current. The resulting average output current is given by the following equation:

$$I_{OUT(AVG)} \cong 25{,}000 \bullet \frac{1V}{R_{PROG}}$$

where: R_{PROG} = 24.9k to 100k.

The largest recommended PROG pin resistor is 100k. Values of R_{PROG} larger than 100k may latch-off the LTC3114-1 if V_{OUT} is forced to less than 2V by an external load. This is generally not an issue for battery charging applications, but may prevent the charging of very large capacitors. In some general purpose power supply applications, this latch-off behavior may be desirable and in these cases, values of R_{PROG} > 100k are acceptable to use.

The gain of 25,000 is generated internal to the LTC3114-1 and is factory trimmed to provide the best accuracy at 500mA of output current. The accuracy of the programmed output current is best at the high end of the range as the residual internal current sense amplifier offset becomes a smaller percentage of the total current sense signal amplitude with increasing current. The provided electrical specifications define the PROG pin current accuracy over a range of output currents.

Selecting the capacitor, C_{PROG}, to put in parallel with R_{PROG} is a trade-off between response time, output current ripple and interaction with the normal output voltage control loop. In general, if speed is not a concern as is the case for most current sourcing applications, then C_{PROG} should be made at least 3 times higher than the voltage error amplifier compensation capacitor, C_{P1}, described in the Compensation section of this data sheet. This will ensure minimal to no interaction when the transition occurs between voltage regulation mode and output current regulation mode.

In current sourcing applications, the maximum output compliance voltage of the LTC3114-1 is set by the voltage error amplifier dividers resistors as it is for standard voltage regulation applications. For LED drivIng applications, select the V_{OUT} divider resistors for a clamping level 1V to 2V higher than the expected forward voltage drop of the LED string. The average output current circuitry can also be used to monitor, rather than control the output current. To do this, select an R_{PROG} value that will limit the voltage on the PROG pin to 0.8V or less at the highest output current expected in the application.

Connect a 20k resistor and 33nF capacitor from PROG to ground if the function is not going to be used to provide a higher level of protection against inadvertent short-circuit conditions on V_{OUT}.

Compensation of the Buck-Boost Converter

The LTC3114-1 utilizes average current mode control to regulate the output voltage. Average current mode control has two loops that require frequency compensation, the inner average current loop and the outer voltage loop. The compensation for the inner average current loop is fixed within the LTC3114-1 in order to provide the highest possible bandwidth over the wide operating range of the LTC3114-1. Therefore, the only control loop that requires compensation design is the outer voltage loop. As will be shown, compensation design of the outer loop is similar to the techniques used in well known peak current mode control devices.

The LTC3114-1 utilizing average current mode control can be conceptualized in its simplest form as a voltage-controlled current source (V_{CCS}), driving the output load formed primarily by R_{LOAD} and C_{OUT}, as shown in Figure 6.

The error amplifier output (VC), provides the command input to the V_{CCS}. The full-scale range of VC is 0.865V (135mV to 1V). With a full-scale command on VC, the LTC3114-1 buck-boost converter will generate an average 1.7A of inductor current (typical) from the converter for a

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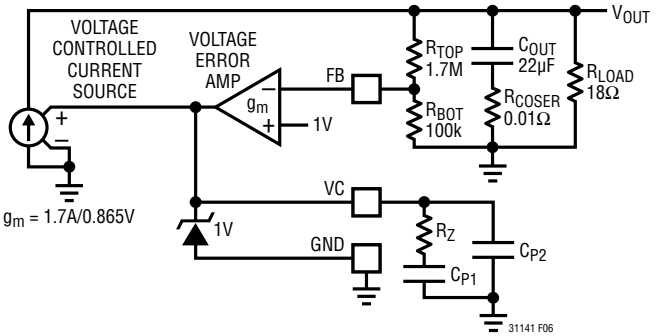

Figure 6. Simplified Representation of Average Current Mode Control Loop

transconductance gain of 1.97A/V. Similar to peak current mode control, the inner average current mode control loop effectively turns the inductor into a current source over the frequency range of interest, resulting in a frequency response from the power stage that exhibits a single pole (–20dB/decade) roll off. The output capacitor (C_{OUT}) and load resistance (R_{LOAD}) form the normally dominant low frequency pole and the effective series resistance of the output capacitor and its capacitance form a zero, usually at a high enough frequency to be ignored. A potentially troublesome right half plane zero (RHPZ) is also encountered if the LTC3114-1 is operated in boost mode. The RHPZ causes an increase in gain, like a zero, but a decrease in phase, like a pole. This will ultimately limit the maximum converter bandwidth that can be achieved with the LTC3114-1. The RHPZ is not present when operating in buck mode. The overall open loop gain at DC is the product of the following terms:

Voltage Error Amp Gain:

$g_m \bullet R_O = 120\mu s \bullet 3.6M = 432V/V$ (not adjustable)

Voltage Divider Gain:

$$\frac{V_{FB}}{V_{OUT}} = \frac{1V}{V_{OUT}}$$

(determined by the application, V_{FB} is the reference voltage for the voltage error amplifier)

Current Loop Transconductance:

$$G_C = \frac{1.7A}{0.865V} = 1.97A/V \text{ (not adjustable)}$$

Load Resistance (R_{LOAD}) (determined by the application)

The frequency dependent terms that affect the loop gain include:

Output Load Pole(P1):

$$\frac{1}{2\pi \bullet R_{LOAD} \bullet C_{OUT}} \text{ (application dependent)}$$

Error Amplifier Compensation (2 Poles and 1 Zero): These are the design variables available

Right Half Plane Zero (RHPZ): boost mode only (determined by maximum load, V_{IN}, V_{OUT} and inductor)

Current Amplifier Compensation Components (Fixed Internal to the LTC3114-1)

The internal current amplifier and inner current loop have a much higher bandwidth than the overall loop, however, unlike an ideal V_{CCS} with a flat gain versus frequency characteristic, the inner loop exhibits gain peaking in the range of approximately 2kHz to 20kHz that is an artifact of the fixed current amplifier compensation. This gain peaking has the effect of pushing out the overall loop crossover frequency, while providing some phase margin boost as well. As long as there is sufficient margin between the loop crossover frequency and the worst-case RHPZ frequency, then stable operation over all conditions is relatively easy to achieve.

The design parameters for compensation design will focus on the series resistor and capacitors connected from VC to ground (R_Z, C_{P1} and C_{P2}). The general goal is to provide a phase boost using the compensation network zero in order to maximize the bandwidth and phase margin of the converter. Being a buck-boost converter, the target loop crossover frequency for the compensation design will be dictated by the highest boost ratio and load current that is expected as this will result in the lowest RHPZ frequency. An illustrative example is provided next that will derive the compensation components for a typical LTC3114-1 application.

Compensation Example

This section will demonstrate how to derive and select the compensation components for a typical LTC3114-1 application. Designing compensation for other applications

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is simply a matter of substituting different values in the equations provided and reviewing the Bode plots, making minor adjustments as needed. Since the compensation design procedure uses a simplified model of the LTC3114-1, the results from the following compensation design should always be verified with time domain step load response tests to validate the effectiveness of the compensation design. It is assumed that the value and type of output capacitor will be selected based on the guidelines provided elsewhere in this data sheet. Particular attention needs to be paid to the voltage bias effect on ceramic capacitors typically used for output bypassing. Similarly, it is assumed that the inductor value and current rating has been selected as well based on the application requirements.

Example Application Details:

V_{IN} = 9V to 36V

V_{OUT} = 12V

Maximum I_{OUT} (boost mode) = 700mA, R_{LOAD} (min) = 12V/0.7A = 17.1Ω

Maximum I_{OUT} (buck mode) = 1A, R_{LOAD} (min) = 12Ω

C_{OUT} = 44µF

L = 10µH

Since this application includes boost mode operation, the first step is to calculate the worst-case RHPZ frequency as this will dictate the maximum loop bandwidth for the converter:

$$RHPZ(f) = \frac{V_{IN}^2 \bullet R_{LOAD}}{V_{OUT}^2 \bullet 2\pi \bullet L} (Hz)$$

substituting the values mentioned earlier yields:

$$RHPZ(f) = \frac{9V^2 \bullet 17.1\Omega}{12V^2 \bullet 2\pi \bullet 10\mu H} = 153.1kHz$$

In order to account for internal IC component variations, it is good practice to set the converter bandwidth or crossover frequency at least three times lower than the RHPZ frequency to avoid excessive phase loss from the RHPZ when operating in boost mode. In some instances such as higher output voltage applications, an even greater separation between the loop crossover frequency and the RHPZ frequency may be necessary. In this example design, we'll plan to achieve a loop bandwidth (f_{CC}) of 29kHz or approximately one-fifth the RHPZ frequency.

The system poles and zeros are as follows:

Output Load Pole (P1) = $\frac{1}{2\pi \bullet R_{LOAD} \bullet C_{OUT}}$;

buck mode, where R_{LOAD} = output resistance.

In boost mode this equation is slightly different:

$$\frac{2}{(2\pi \bullet R_{LOAD} \bullet C_{OUT})'},$$

but with the reduced output current capability in boost (higher R_{LOAD}), the load pole location is about the same.

Error Amp Pole (P2) = $\frac{1}{(2\pi \bullet R_{EA} \bullet C_C)}$;

this pole is very close to DC, R_{EA} = error amp output resistance, which is approximately 3.6MΩ. It has no impact on the compensation design, but is included here for completeness.

Compensation Zero (Z1) = $\frac{1}{(2\pi \bullet R_Z \bullet C_{P1})}$;

R_Z and C_{P1} are the error amp compensation components that will be selected.

Ignoring very high frequency output capacitor ESR zero and secondary high frequency error amp pole, the system has two poles and one zero. The error amp pole (P2) is always near DC and we have little influence on it. The output load pole (P1) will move depending on buck-boost converter load resistance. The highest frequency for P1, the output load pole, is at maximum load current (minimum R_{LOAD}). If we design the error amp zero (Z1) frequency so that it coincides with P1(max), then we will get the maximum phase benefit from the compensation network at full load and enough phase boost at lighter loads for stable operation and a single pole response where the loop crosses zero dB.

APPLICATIONS INFORMATION

Assuming the error amp zero is designed as just described, at frequencies above P2 (and Z1), the closed-loop gain of our system simplifies to:

$$G_{CL} = \frac{G_{CS} \bullet R_{LOAD} \bullet g_m \bullet R_Z}{V_{OUT}}$$

where:

G_{CS} is the inner current loop closed-loop transconductance = 1.97A/V

R_{LOAD} is the minimum load resistance in ohms

g_m is the transconductance of the error amplifier, 120µS

R_Z is the compensation zero setting resistor (one of our design variables)

V_{OUT} is the output voltage

Our desired closed-loop frequency (f_{CC}) defined earlier is 29kHz. Assuming that we have a single pole response in our system, we can express the ratio of the closed-loop crossover frequency to f_{P1} in the buck mode of operation as follows:

$$\frac{f_{CC}}{f_{P1}} = \frac{G_{CS} \bullet R_{LOAD} \bullet g_m \bullet R_z}{V_O}$$

We can now calculate R_Z by rearranging the previous equation:

$$R_Z = \frac{f_{CC} \bullet V_{OUT} \bullet 2\pi \bullet C_{OUT}}{G_{CS} \bullet g_m}$$

It's important to note that the value of R_Z is proportional to the overall crossover frequency, f_{CC}. If we later want to adjust f_{CC} lower, for example, R_Z can be lowered in value and C_{P1} increased proportionally to keep the compensation zero at the same frequency.

As mentioned previously, we will place the zero at frequency P1, yielding:

$$C_{P1} = \frac{1}{2\pi \bullet R_Z \bullet f_{P1}} \text{ or more simply, } \frac{R_{LOAD} \bullet C_{OUT}}{R_Z}$$

where R_l is the minimum load resistance in buck mode, 12Ω in this example.

Quickly substituting our values in the above equations yields:

R_Z = 407k, C_{P1} = 1.3nF,

but please continue reading as this is not the final answer.

If the inner current loop were an ideal V_{CCS}, then the previously derived compensation would be sufficient to stabilize the converter. However, the inner current loop utilizes an operational amplifier with an integral compensation network, which contributes an additional zero and pole in the power stage response, the gain peaking, as described previously. The effect of the additional zero/pole pair pushes out f_{CC}, our crossover frequency, beyond what was predicted by the previous calculations. A simplified approach to calculating our compensation components then is to re-use the previous equations but scale f_{CC}, the cross over frequency, by a scaling factor (α), which will account for the gain boost present in the system:

$$f_{CC'} = \frac{f_{CC}}{3} \bullet (\alpha), \text{ where } \alpha = 0.42$$

So, in our example, this results in:

$$f_{CC'} = \frac{29kHz}{3} \bullet (0.42) = 4.06kHz$$

Using the new value of $f_{CC'}$ in the previous equations for R_Z and C_C yields:

$$R_Z = \frac{4.06kHz \bullet 12V \bullet 2\pi \bullet 44\mu F}{\frac{1.97A}{V} \bullet \frac{120\mu A}{V}}$$

$R_Z = 56.9k\Omega$, use 56.2kΩ

$$C_{P1} = \frac{12\Omega \bullet 44\mu F}{56.2k}$$

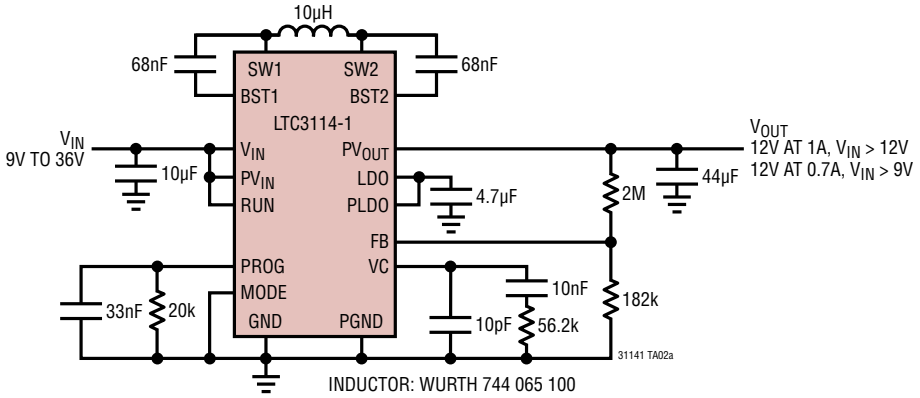
$C_{P1} = 9.4nF$, use 10nF

C_{P2} is usually chosen to be a small value around 10pF as it is meant to filter out high frequency switching frequency related components.

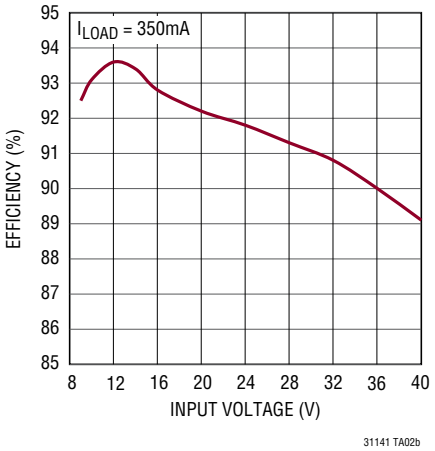
Keep in mind that this analysis assumes that the zero provided by the output capacitor and its ESR is at a frequency much higher than f_{CC}.

TYPICAL APPLICATIONS

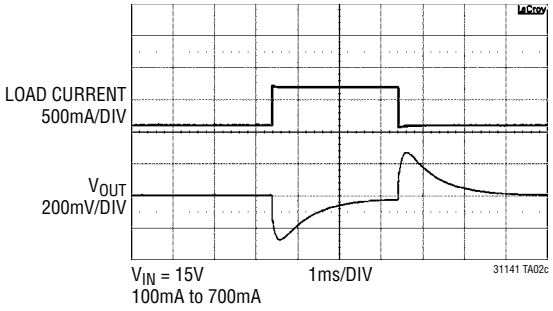
9V to 36V V_{IN} to 12V V_{OUT} Regulator



Efficiency vs Input Voltage

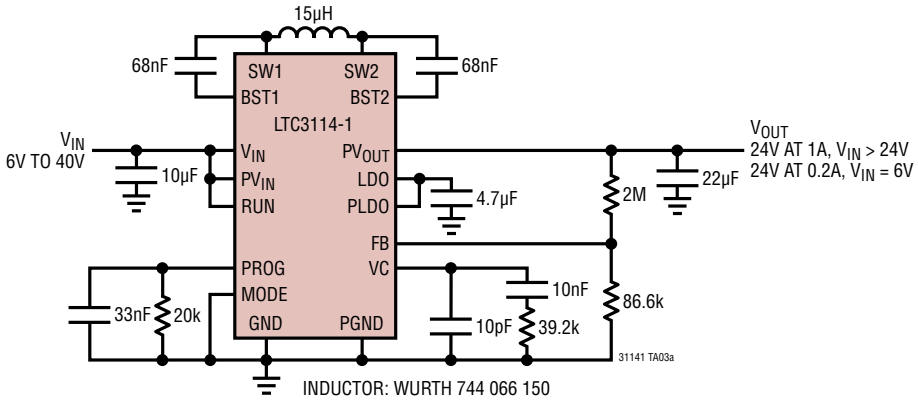


Load Step Response

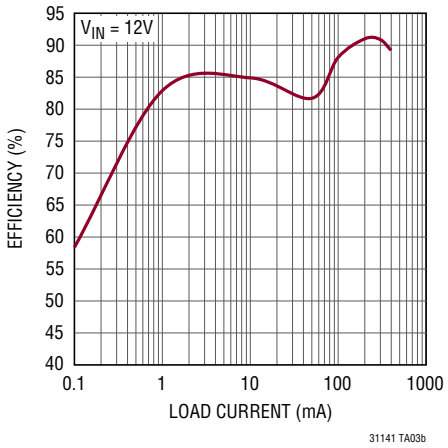


TYPICAL APPLICATIONS

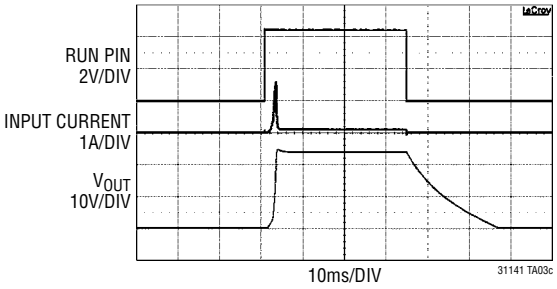
6V to 40V V_{IN} to 24V V_{OUT} Regulator



Efficiency vs Load Current

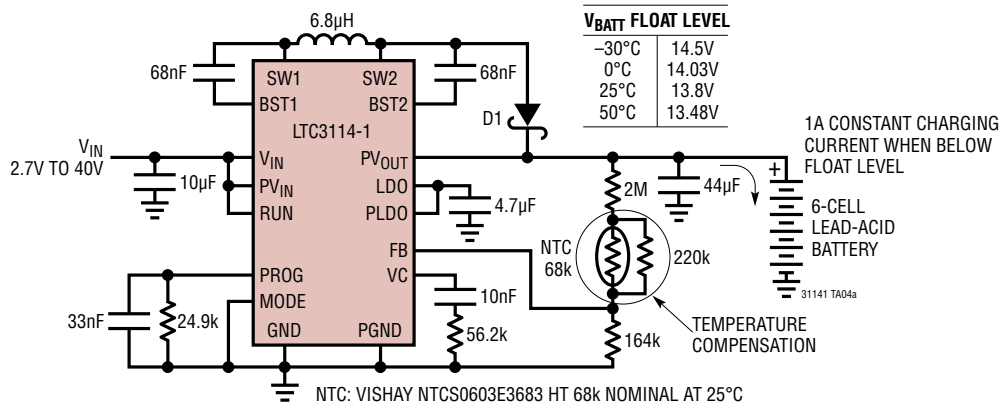


12V V_{IN} Synchronous Boost Operation with Inrush Current Limiting at Start-Up and Output Disconnect in Shutdown



TYPICAL APPLICATIONS

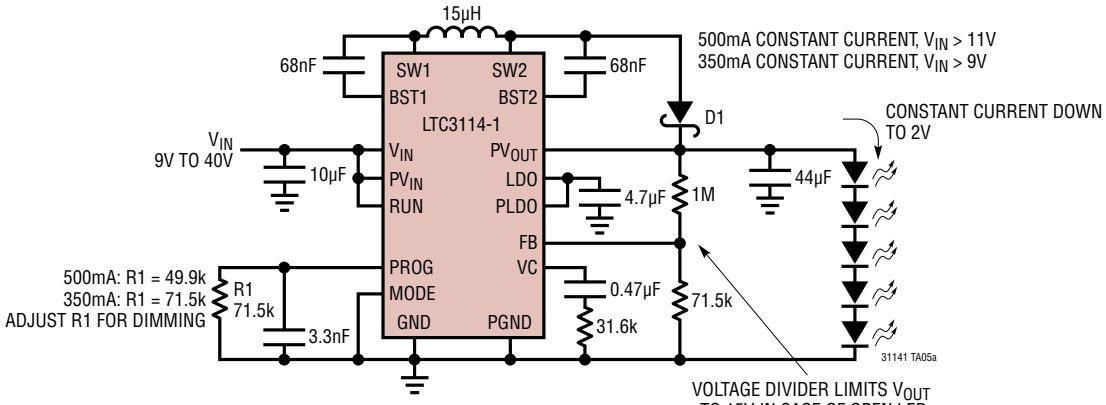
Constant Current/Constant Voltage Lead-Acid Battery Charger



V_{BATT} FLOAT LEVEL	
–30°C	14.5V
0°C	14.03V
25°C	13.8V
50°C	13.48V

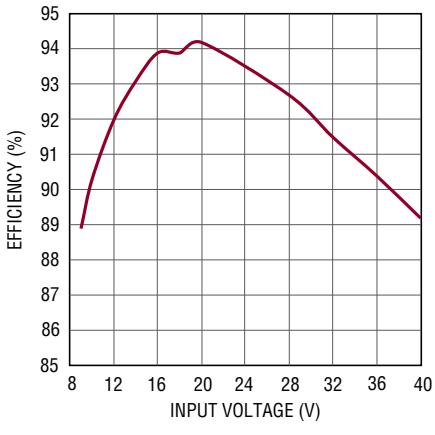
NTC: VISHAY NTCS0603E3683 HT 68k NOMINAL AT 25°C
INDUCTOR: COILCRAFT MSS1048-682NL
D1: ON SEMI MBRS260T3G

Constant Current High Brightness LED Driver



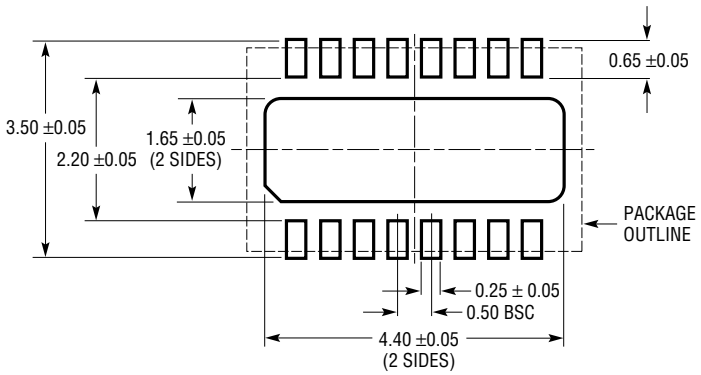
INDUCTOR: WURTH 744 066 150
D1: ON SEMI MBRS260T3G

Efficiency vs Input Voltage, 350mA Drive Current

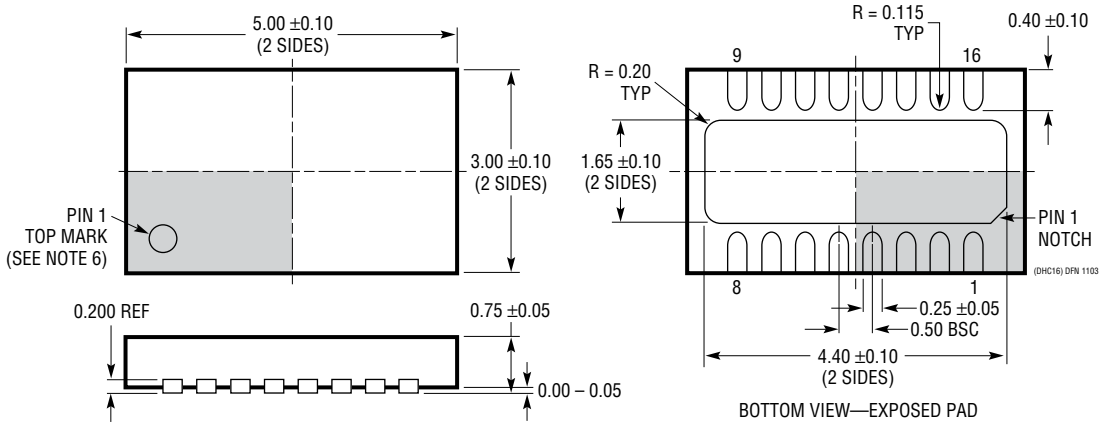


PACKAGE DESCRIPTION

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

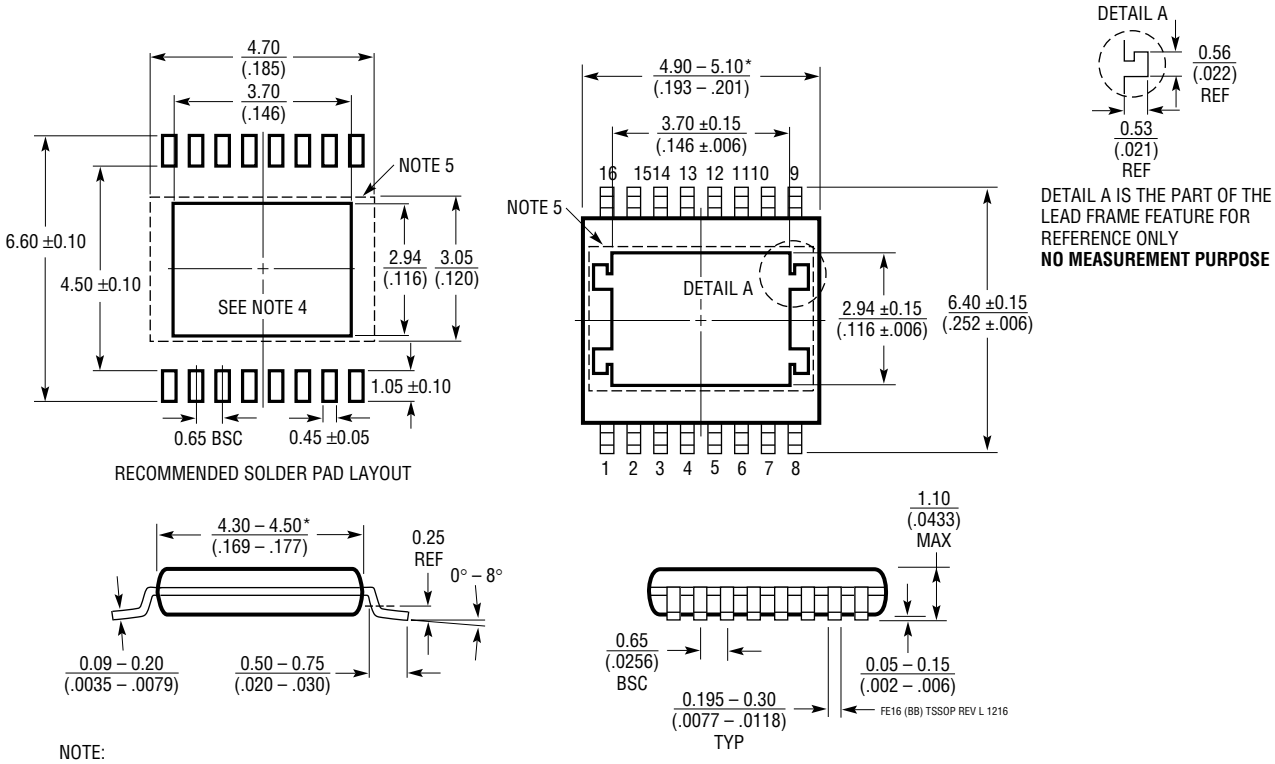


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev L)
Exposed Pad Variation BB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
5. BOTTOM EXPOSED PADDLE MAY HAVE METAL PROTRUSION IN THIS AREA. THIS REGION MUST BE FREE OF ANY EXPOSED TRACES OR VIAS ON PCB LAYOUT

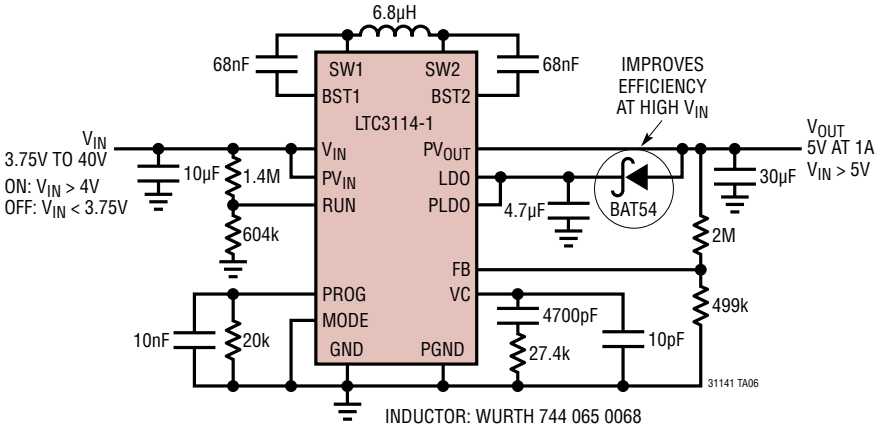
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/14	Corrected Part Marking Table for TSSOP Package Option.	2
B	03/16	Clarified Min V_{IN} on Electrical Characteristics.	3
		Clarified FB (Pin 7) description, BST2 (Pin 12) and BST1 (Pin 13) description.	9
		Added High Transient Input Voltage Applications section.	17
		Clarified Average Output Current Limit Programming section.	23
		Added optional diode to Typical Applications.	17-30
		Added LTC3118 to Related Parts.	34
C	07/19	Add AEC-Q100 Qualification and Orderable Part Numbers	1, 3
D	05/20	Added patent number to end of paragraph description.	1
		Added #W_FE temp grades to part list (I, E).	3
		Schottky diode recommendation to PV_{OUT}.	10
		Striked out “High transient Input Voltage Applications”.	18
		Removed D1 from schematic.	28
		Removed D1 part number description from schematic.	28
		Removed D1 from schematic.	29
		Removed D1 part number description from schematic.	29
		Removed D2 from schematics.	30
		Removed D2 part number description from schematics.	30
		Removed D1 from schematic.	34
		Removed D1 part number description from schematic.	34

TYPICAL APPLICATION

Wide V_{IN} Range 5V, 1A Regulator with Bootstrapped LDO and Custom UVLO Threshold



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3534	7V, 500mA (I_{OUT}), 1MHz Synchronous Buck-Boost DC/DC Converter	94% Efficiency, V_{IN}: 2.4V to 7V, V_{OUT}: 1.8V to 7V, I_Q = 25µA, I_{SD} < 1µA, DFN and GN Packages
LTC3112	2.5A (I_{OUT}), Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.7V to 15V, V_{OUT}: 2.5V to 14V, I_Q = 40µA, I_{SD} < 1µA, DFN and TSSOP Packages
LTC3115-1	40V, 2A Synchronous Buck-Boost DC/DC Converter	V_{IN}, V_{OUT}: 2.7V to 40V, I_Q = 30µA, I_{SD} = 3µA, DFN and TSSOP Packages
LTC3785	≤10A (I_{OUT}), High Efficiency, 1MHz Synchronous, No R_{SENSE}™ Buck-Boost DC/DC Controller	V_{IN}: 2.7V to 10V, V_{OUT}: 2.7V to 10V, I_Q = 86µA, I_{SD} < 15µA, QFN Package
LTC3789	Buck-Boost DC/DC Controller	96% Efficiency, V_{IN}: 4.5V to 38V, V_{OUT}: 0.8V to 38V, 4mm × 5mm QFN and SSOP Packages
LTM®4605	4.5V to 20V, 10A Buck-Boost µModule® Regulator	High Power Buck-Boost µModule Regulator
LTC3129	15.75V, 200mA Buck-Boost DC/DC Converter with 1.3µA I_Q	V_{IN}: 2.42V to 15.75V, V_{OUT}: 1.4V to 15V, I_Q = 1.3µA, I_{SD} = 10nA, DFN and MS Packages
LTC3129-1	15.75V, 200mA Buck-Boost DC/DC Converter with 1.3µA I_Q and Programmable Output Voltages	V_{IN}: 2.42V to 15.75V, V_{OUT}: Pin Programmable 2.5V to 15V, I_Q = 1.3µA, I_{SD} = 10nA, DFN and MS Packages
LTC3118	10V, 2A Synchronous Buck-Boost DC/DC Converter with Low Loss Dual Input PowerPath™	V_{IN}: 2.2V to 10V, V_{OUT}: 2.0V to 16V, I_Q = 50µA, I_{SD} < 1µA, 4mm × 5mm QFN and TSSOP Packages

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- Alternative Solution
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