THE DATASHEET OF

MAX15301AA02+CJK

MAX15301AA02

InTune Automatically Compensated Digital PoL Controller with Driver and PMBus Telemetry

General Description

The MAX15301AA02 is a full-featured, highly efficient, digital point-of-load (PoL) controller with advanced power management and telemetry features. Unlike PID-based digital power regulators, the MAX15301AA02 uses Maxim's patented InTune™ automatically compensated, state-space control algorithm. The InTune control law is valid for both the small- and large-signal response and accounts for duty-cycle saturation effects. These capabilities result in fast loop transient response and reduce the number of output capacitors compared to competing digital controllers.

The MAX15301AA02 includes multiple features to optimize efficiency. An internal switch BabyBuck™ regulator generates the gate drive and the internal bias supplies for the controller with low power loss. An advanced, high-efficiency MOSFET gate driver has adjustable nonoverlap timing and load-variable gate-drive voltage to minimize switching losses over the full range of voltage, current, and temperature.

The MAX15301AA02 was designed for end-customer's design environment. An on-board PMBus™-compliant serial bus interface enables communication with a supervisory controller for monitoring and fault management. A full suite of power management features eliminates the need for complicated and expensive sequencing and monitoring ICs. Basic DC-DC conversion operation can be set up via pin strapping and does not require user configuration firmware. This allows for rapid development of the power-supply subsystem before board-level systems engineering is completed. Maxim provides support hardware and software for configuring the IC.

The MAX15301AA02 is available in a 32-lead, 5mm x 5mm TQFN package and operates over the -40°C to +85°C temperature range.

Benefits and Features

- InTune Automatic Compensation Ensures Stability While Optimizing Transient Performance
- State-Space Compensation Results in Fast Transient Response with Reduced Output Capacitance
- Differential Remote Voltage Sensing Enables ±1% V_{OUT} Accuracy over Temperature (-40°C to +85°C)
- PMBus Interface for Configuration, Control, and Monitoring
- Supports Voltage Positioning
- High Output 2A/4A MOSFET Driver
  - Adjustable Nonoverlap Timing
  - Variable Gate-Drive Voltage
- Wide Input Range of 4.5V to 14V
- Efficient On-Chip BabyBuck Regulator for Self-Bias
- Output Voltage Range from 0.5V to 5.25V
- Startup into a Prebiased Output
- Configurable Soft-Start and Soft-Stop Time
- Fixed-Frequency Operation and Synchronization
- Flexible Sequencing and Fault Management
- Pin-Strappable Configuration
  - Output Voltage, SMBus Address, Switching Frequency, Current Limit
- Out-of-the-Box Operation Enables Fast Prototyping

Applications

- Servers
- Storage Systems
- Routers/Switches
- Base-Station Equipment
- Power Modules

***Ordering Information* and *Typical Operating Circuit* appear at end of data sheet.**

19-7508; Rev 0; 2/15

maxim integrated™

Absolute Maximum Ratings

INSNS to SGND .....-0.3V to +14V
LXSNS to SGND .....-2V to +14V
LXSNS (pulse < 10ns) to SGND .....-2V to +20V
OUTP, OUTN, DCRP, DCRN to SGND .....-0.3V to +5.5V
PWR to PGND .....-0.3V to +18V
3P3 to SGND ..... -0.3V to the minimum of +4V or (V_{GDRV} + 0.3V)
GDRV to SGND ..... -0.3V to the minimum of +12V or (V_{PWR} + 0.3V)
LX to PGND .....-2V to the minimum of +26V or (V_{BST} + 0.3V)
DL to PGND ..... -0.3V to (V_{GDRV} + 0.3V)
LBI to PGND .....-0.3V to (V_{PWR} + 0.3V)
LBO to PGND .....(V_{3P3} - 0.3V) to (V_{GDRV} + 0.3V)
DH to PGND ..... (V_{LX} - 0.3V) to (V_{BST} + 0.3V)
BST to LX .....-0.3V to +12V
BST to PGND .....-0.3V to +26V
BST to GDRV .....-0.3V to +26V
1P8 to DGND .....-0.3V to +2.2V
CIO, SET, PG, ADDR0, ADDR1, SYNC, TEMPX, $\overline{SALRT}$ to DGND .....-0.3V to +4V
EN, SCL, SDA to DGND .....-0.3V to +4V
PGND to SGND .....-0.3V to +0.3V
DGND to SGND .....-0.3V to +0.3V
Electrostatic Discharge (ESD) Rating
  Human Body Model (HBM) .....±3500V
  Machine Model .....±200V
Junction Temperature .....+125°C
Operating Temperature Range ..... -40°C to +85°C
Continuous Power Dissipation (T_A = +70°C)
  TQFN (derate 34.5mW/°C above +70°C).....2758mW
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....29°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1.7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(All settings = factory default, V_{PWR} = V_{INSNS} = 12V, V_{SGND} = V_{DGND} = V_{PGND} = 0V, V_{OUT} = 1.2V, f_{SW} = 600kHz. Specifications are for T_A = T_J = -40°C to +85°C, typical values are at T_A = T_J = +25°C. See the *Typical Operating Circuit*, unless otherwise noted.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage Range	V_{PWR}		4.5		14	V
Input Supply Current	I_{PWR}	BabyBuck bias supply, driver not switching		10		mA
		Linear mode bias supply, driver not switching		24	50	
Input Overvoltage Lockout Threshold	$V_{OVLO(PWR)}$	Input rising	14.3	15.2	16.0	V
Input Undervoltage Lockout Threshold	$V_{UVLO(PWR)}$	Rising edge	3.8	4.1	4.4	V
		Hysteresis		0.24		
BIAS REGULATORS						
3P3 Output Voltage	V_{3P3}	$I_{LOAD(3P3)}$ = 0mA		3.3		V
1P8 Output Voltage	V_{1P8}	$I_{LOAD(1P8)}$ = 0mA		1.80		V

Electrical Characteristics (continued)

(All settings = factory default, V_{PWR} = V_{INSNS} = 12V, V_{SGND} = V_{DGND} = V_{PGND} = 0V, V_{OUT} = 1.2V, f_{SW} = 600kHz. Specifications are for T_A = T_J = -40°C to +85°C, typical values are at T_A = T_J = +25°C. See the *Typical Operating Circuit*, unless otherwise noted.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STARTUP/SHUTDOWN TIMING						
Firmware Initialization	t_1	From V_{IN} > $V_{UVLO(PWR)}$, until ready to enable (Figure 2)		25		ms
Minimum Programmable t_{ON_DELAY}	t_2	(Figure 2, Note 10)	1			ms
Minimum Programmable t_{ON_RISE}	t_3	(Figure 2, Note 10)	1			ms
Adaptive Tuning Time	t_4	From V_{OUT} = V_{OUT} command to assertion of power good (PG) (Figure 2)		12		ms
OUTPUT VOLTAGE						
Output Voltage Range	V_{OUT}	Measured from OUTP to OUTN (Notes 5 and 10)	0.5		5.25	V
LX Bias Current	I_{LX}	Not switching, current out of device pin		200		µA
Duty-Cycle Range		(Notes 3 and 4)	5		95	%
Regulation Set-Point Accuracy (Note 4)		T_A = +25°C, I_{OUT} ≤ 20A (Notes 4, 8, 9)	-0.5		+0.5	%
		-40°C ≤ T_A ≤ +85°C (Notes 4, 8, 9)	-1		+1	
V_{OUT} Sense Bias Current	I_{OUTP}	Current flowing into OUTP		50		µA
	I_{OUTN}	Current flowing out of OUTN		35		µA
DCR Sense Bias Current	I_{DCRP}	Current flowing into DCR, V_{DCRP} - V_{DCRN} = 150mV		120		nA
	I_{DCRN}			4		µA
PWM CLOCK (Note 4)						
Switching Frequency Range	f_{SW}	(Note 10)	300		1000	kHz
Switching Frequency Set-Point Accuracy			-5		+5	%
External Clock-to-SYNC Frequency Range	f_{SYNC}		300		1000	kHz
Minimum Allowable SYNC Duty-Cycle Range				40		%
Maximum Allowable SYNC Duty Cycle				60		%
PROTECTION (Note 4)						
Overcurrent Fault Threshold Accuracy		T_A = +25°C, exclusive of sensor error		±3		%
Output Overvoltage-Fault Threshold		Output rising		115		% V_{OUT}
Output Undervoltage-Fault Threshold		Output falling		85		% V_{OUT}
Thermal-Shutdown Threshold Accuracy				±20		°C

Electrical Characteristics (continued)

(All settings = factory default, V_{PWR} = V_{INSNS} = 12V, V_{SGND} = V_{DGND} = V_{PGND} = 0V, V_{OUT} = 1.2V, f_{SW} = 600kHz. Specifications are for T_A = T_J = -40°C to +85°C, typical values are at T_A = T_J = +25°C. See the *Typical Operating Circuit*, unless otherwise noted.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal-Shutdown Hysteresis				20		°C
Power-Good Threshold		V_{OUT} rising		90		% V_{OUT}
		V_{OUT} falling		85		
STARTUP/SHUTDOWN TIMING						
Firmware Initialization	t_1	From V_{IN} > $V_{UVLO(PWR)}$, until ready to enable (Figure 2)		25		ms
TON_DELAY, TOFF_DELAY Range	t_2	Minimum delay (Figure 2, Note 4)		1		ms
		Maximum delay (Figure 2, Note 4)		145		
TON_DELAY, TOFF DELAY Resolution		Delay timing step size		0.6		ms
TON_DELAY, TOFF DELAY Command Accuracy	(Note 10)	Command value sent vs. readback			±0.3	ms
TON_DELAY, TOFF DELAY Timing Accuracy		Command readback value vs. actual delay time		±0.8		ms
TON_RISE, TOFF_FALL Range	t_3	Minimum (Figure 2, Note 4)		1		ms
		Maximum (Figure 2, Note 4)		255 x t_{RR}		
TON_RISE, TOFF_FALL Resolution	t_{RR}	Ramp timing step size (varies with VOUT_COMMAND)		0.4 -1.0		ms
TON_RISE, TOFF_FALL Command Accuracy	(Note 10)	Command value sent vs. readback			±0.5	ms
TON_RISE, TOFF_FALL Timing Accuracy		Command readback value vs. actual ramp duration		±10		µs
Adaptive Tuning Time	t_4	From end of soft-start ramp to PG assertion (varies with FREQUENCY_SWITCH (Figure 2)		12		ms
Temperature-Measurement Accuracy		External		±5		°C
		Internal		±5		
DIGITAL I/O						
Power-Good Logic-High Leakage Current		Open-drain output mode, open-drain connected to 5.5V, V_{3P3} = 3.3V			10	µA
Output Logic-High		CMOS mode, I_{SOURCE} = 4mA	V_{3P3} - 0.4		V_{3P3}	V
Output Logic-Low		I_{SINK} = 4mA			0.4	V
Input Bias Current			-1		+1	µA
Rise/Fall Slew Rate		C_{LOAD} = 15pF		2		ns
EN, SYNC Input Logic-Low Voltage		Input voltage falling			0.8	V

Electrical Characteristics (continued)

(All settings = factory default, V_{PWR} = V_{INSNS} = 12V, V_{SGND} = V_{DGND} = V_{PGND} = 0V, V_{OUT} = 1.2V, f_{SW} = 600kHz. Specifications are for T_A = T_J = -40°C to +85°C, typical values are at T_A = T_J = +25°C. See the *Typical Operating Circuit*, unless otherwise noted.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN, SYNC Input Logic- High Voltage		Input voltage rising	2			V
EN, SYNC Input Leakage Current			-10		+10	µA
SMBus (Note 4)						
SDA, SCL Input Logic-Low Voltage		Input voltage falling			0.8	V
SDA, SCL Input Logic-High Voltage		Input voltage rising	2			V
SDA, SCL, SALRT Logic-High Leakage Current		V_{SCL}, V_{SDA} = 0V, and V_{SALRT} tested at 0V and 3.3V			10	µA
SDA, SCL, SALRT Logic-Low Output Voltage		I_{SINK} = 4mA			0.4	V
PMBus Operating Frequency	f_{SMB}			400		kHz
Bus Free Time (STOP - START)	t_{BUF}		1.3			µs
START Condition Hold Time from SCL	$t_{HD:STA}$		0.6			µs
START Condition Setup Time from SCL	$t_{SU:STA}$		0.6			µs
STOP Condition Setup Time from SCL	$t_{SU:STO}$		0.6			µs
SDA Hold Time from SCL	$t_{HD:DAT}$		300			ns
SDA Setup Time from SCL	$t_{SU:DAT}$		100			ns
SCL Low Period	t_{LOW}		1.3			µs
SCL High Period	t_{HIGH}		0.6			µs
DRIVER BIAS REGULATOR						
GDRV Output Voltage Range	V_{GDRV}	GCTRLDAC = 0		5.2		V
		GCTRLDAC = 15		8.7		
GDRV Undervoltage Lockout	$V_{GDRVUVLO}$	GDRV falling, 200mV (typ) hysteresis	3.5	3.75		V
LBI, LBO Current Limit				0.7		A
HIGH-SIDE DRIVER						
Driver Source Current	I_{DH_SOURCE}	V_{PWR} = 12V, V_{DH} = 0V, 3.0nF load		2		A
Driver Sink Current	I_{DH_SINK}	V_{PWR} = 12V, V_{DH} = 0V, 3.0nF load		4		A
DH Driver On-Resistance (Sourcing)	$R_{ON(DH)}$	V_{PWR} = 12V, V_{BST} - V_{LX} forced to 5V		1		Ω
DH Driver On-Resistance (Sinking)	$R_{ON(DH)}$	V_{PWR} = 12V, V_{BST} - V_{LX} forced to 5V		0.4		Ω

Electrical Characteristics (continued)

(All settings = factory default, V_{PWR} = V_{INSNS} = 12V, V_{SGND} = V_{DGND} = V_{PGND} = 0V, V_{OUT} = 1.2V, f_{SW} = 600kHz. Specifications are for T_A = T_J = -40°C to +85°C, typical values are at T_A = T_J = +25°C. See the *Typical Operating Circuit*, unless otherwise noted.)(Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOW-SIDE DRIVER						
Driver Source Current	I_{DL_SOURCE}	V_{PWR} = 12V, V_{DL} = 0V, 5.0nF load		2		A
Driver Sink Current	I_{DL_SINK}	V_{PWR} = 12V, V_{DL} = 5V, 5.0nF load		4		A
DL Driver On-Resistance (Sourcing)	$R_{ON(DL)}$	V_{PWR} = 12V, V_{LX} - V_{PGND} forced to 5V		1		Ω
DL Driver On-Resistance (Sinking)	$R_{ON(DL)}$	V_{PWR} = 12V, V_{LX} - V_{PGND} forced to 5V		0.4		Ω
DRIVER TIMING AND RESISTANCE						
DL Transition Time	t_{F_DL}	Falling, 5.0nF load, V_{GDRV} = 5V		10		ns
	t_{R_DL}	Rising, 5.0nF load, V_{GDRV} = 5V		15		
DH Transition Time	t_{F_DH}	Falling, 3.0nF load, V_{GDRV} = 5V		8		ns
	t_{R_DH}	Rising, 3.0nF load, V_{GDRV} = 5V		10		
DH Driver Pulldown Resistance	$R_{PD(DH)}$	Not switching, V_{EN} = 0V	100		300	kΩ
DL Driver Pulldown Resistance	$R_{PD(DL)}$	Not switching, V_{EN} = 0V	100		300	kΩ
Boost On-Resistance	$R_{ON(BST)}$	V_{GDRV} = 5V, V_{DH} = V_{LX} = V_{PGND} (pulldown state), I_{BST} = 10mA		1.5		Ω
THERMAL PROTECTION						
Gate-Driver Thermal Shutdown Threshold	T_{SHDN}	Hysteresis = 20°C		150		°C

Note 2: Limits are 100% production tested at T_A = +25°C. Maximum and minimum limits over temperature are guaranteed through correlation using statistical quality control (SQC) methods. Typical values are expressed as factory-default values also for configurable specifications within a range.

Note 3: Can go to 100% during a transient.

Note 4: Design guaranteed by bench characterization. Limits are not production tested.

Note 5: The settable output voltage range is 0.6V to 5.0V. This range expands to 0.5V to 5.25V when the voltage margining function is enabled.

Note 6: Once the MAX15301AA02 locks onto an external synchronizing clock, the tolerance on the capture range is ±10%.

Note 7: See the *Voltage Tracking* section.

Note 8: Excluding tracking mode.

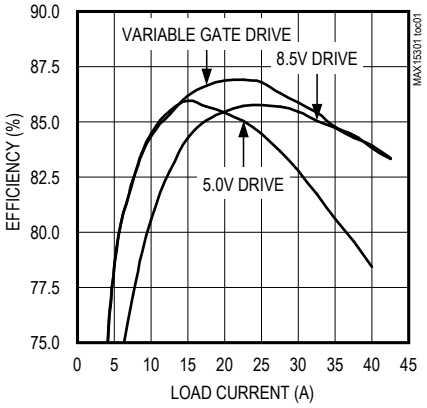
Note 9: Voltage regulation accuracy is power-stage dependent; adherence to all data sheet design recommendations is required to achieve specified accuracy.

Note 10: Customer-programmable parameters.

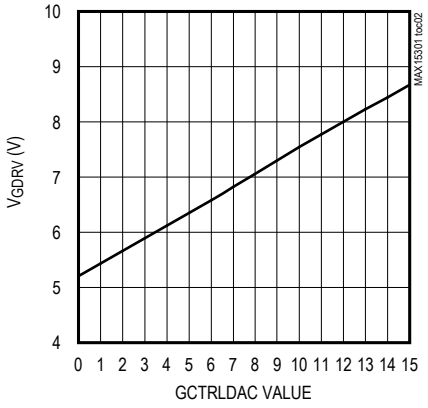
Typical Operating Characteristics

(T_A = +25°C, V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 600kHz, unless otherwise noted. See the Typical Operating Circuit and Application 1 in Table 8).

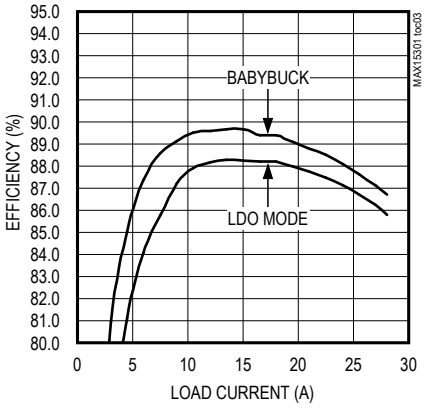
VARIABLE GATE-DRIVE EFFICIENCY GAIN



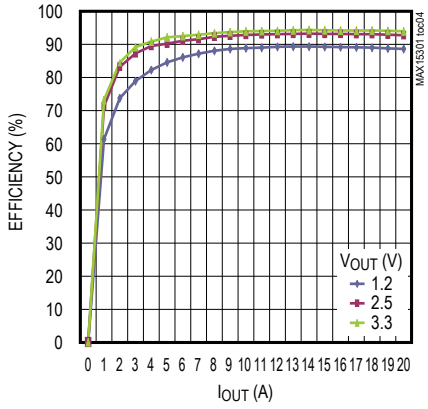
GDRV VOLTAGE vs. GCTRLDAC SETTING



BABYBUCK EFFICIENCY GAIN (V_{IN} = 12V, V_{OUT} = 1.2V, 500kHz)



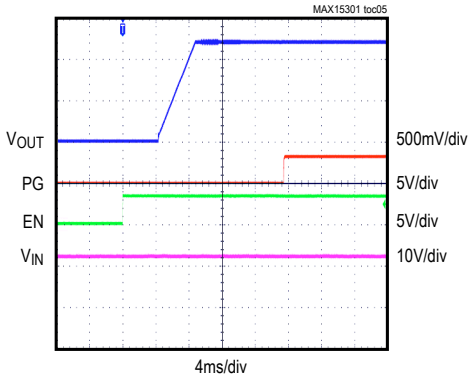
EFFICIENCY vs. LOAD (V_{IN} = 12V, 600kHz)



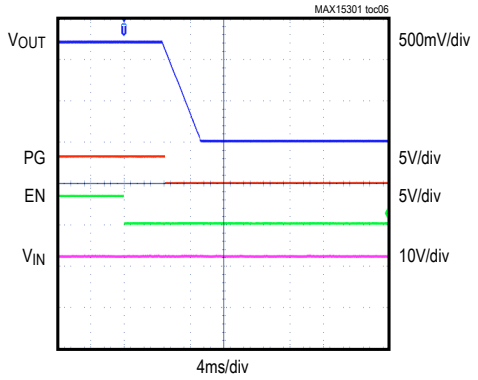
Typical Operating Characteristics (continued)

(T_A = +25°C, V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 600kHz, unless otherwise noted. See the Typical Operating Circuit and Application 1 in Table 8).

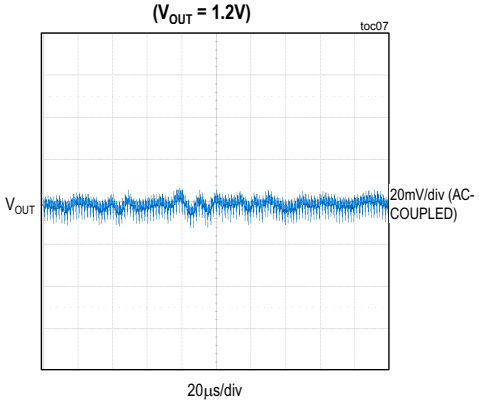
STARTUP



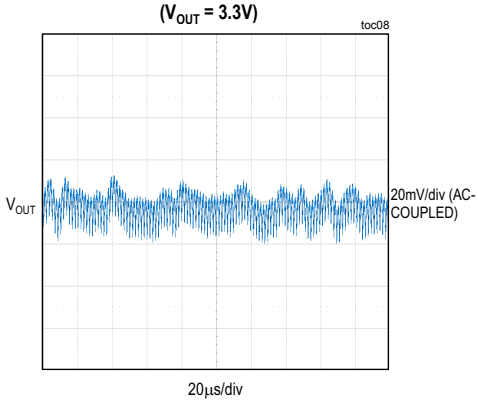
SHUTDOWN



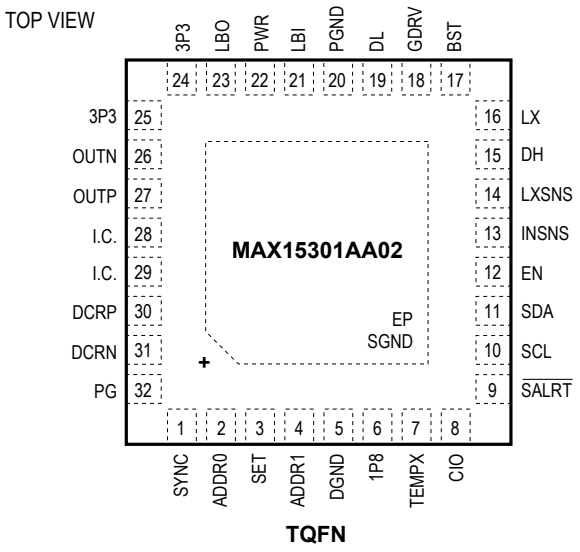
OUTPUT-VOLTAGE RIPPLE (V_{OUT} = 1.2V)



OUTPUT-VOLTAGE RIPPLE (V_{OUT} = 3.3V)



Pin Configuration



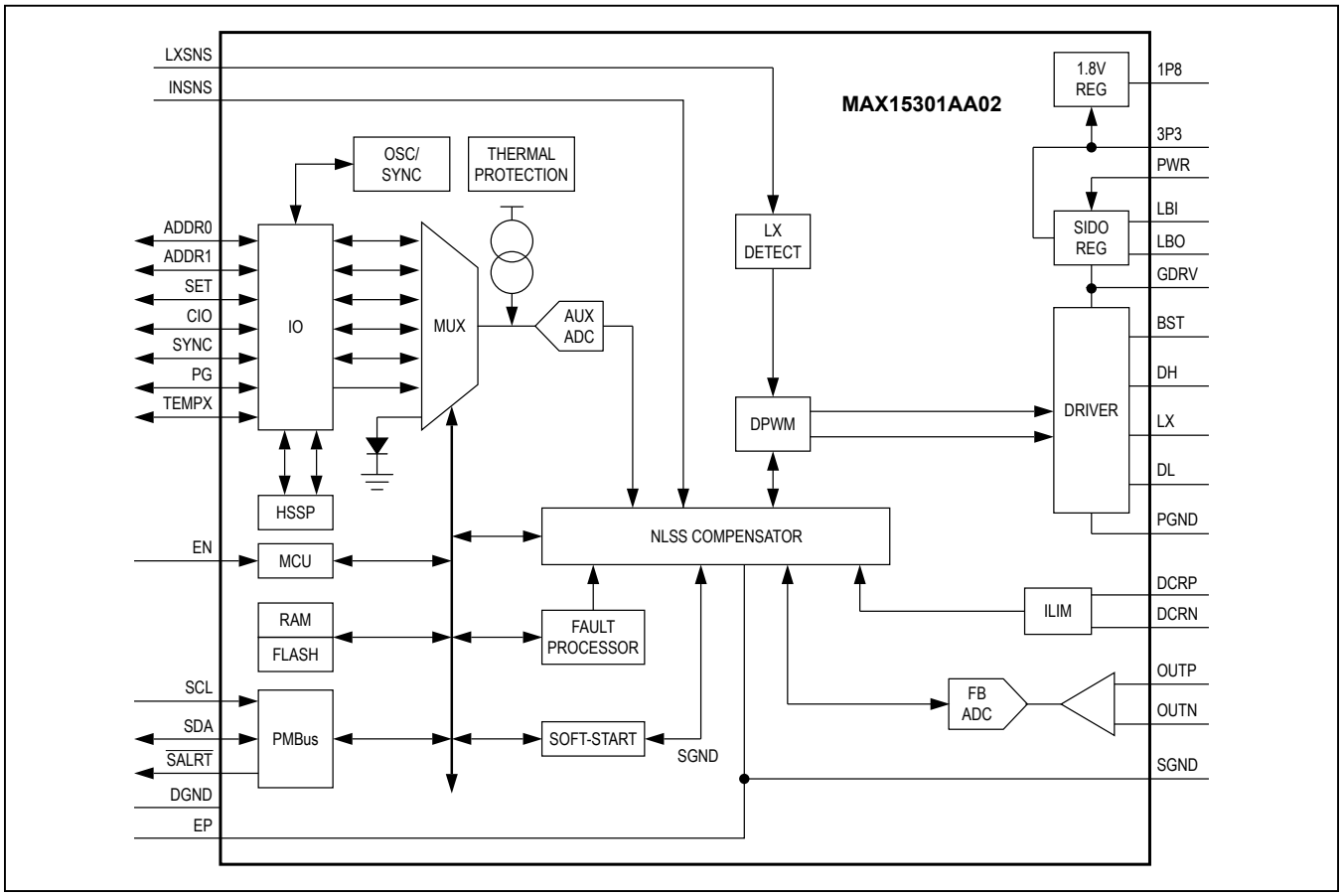
Pin Description

PIN	NAME	FUNCTION
1	SYNC	External Switching Frequency Synchronization Input. Connect a resistor between SYNC and SGND to set the switching frequency of the DC-DC converter (see Table 2). The MAX15301 can also synchronize with an external clock applied at SYNC.
2	ADDR0	SMBus Address Select Input 0. Used with ADDR1 to assign a unique SMBus address to the device.
3	SET	Output Voltage Set Input. Connect a resistor between SET and SGND to set the output voltage. Shorting this pin to ground selects tracking mode (see Table 1).
4	ADDR1	SMBus Address Select Input 1. Used with ADDR0 to assign a unique SMBus address to the device and set the current limit for MAX15301.
5	DGND	Digital Ground. Connect to DGND and PGND using short, wide PCB traces.
6	1P8	Internal 1.8V Regulator Output. 1P8 is the supply rail for the internal digital circuitry. Bypass 1P8 to DGND with a 10µF ceramic capacitor. This pin may not be used to power any circuitry external to the MAX15301.
7	TEMPX	Connection for the External Temperature Sensor. Connect an npn transistor junction from TEMPX to SGND to measure the temperature at any point on the PCB. Place a 100pF ceramic capacitor in parallel with the temperature sense junction.
8	CIO	Configurable Input/Output Pin. This is a voltage-tracking input when SET is connected to SGND to select tracking mode. CIO must be grounded when not in tracking mode.

Pin Description (continued)

PIN	NAME	FUNCTION
9	$\overline{\text{SALRT}}$	SMBus Alert. Interrupt to the SMBus master. Open-drain output that pulls low when SMBus interaction is required.
10	SCL	SMBus Clock Input
11	SDA	SMBus Data Input/Output
12	EN	Enable Input. Do not leave unconnected. By default, driving EN high enables output regulation, and driving EN low disables output regulation.
13	INSNS	Powertrain Input Rail Sense. Monitors the input supply of the DC-DC converter. Connect a series 2kΩ resistor between input rail and INSNS pin.
14	LXSNS	Connect to SGND
15	DH	High-Side MOSFET Gate Drive
16	LX	Switching Node. Connect directly to the high-side of the output inductor.
17	BST	Bootstrap Capacitor Connection. Connect a 0.22µF ceramic capacitor between BST and the switching node.
18	GDRV	Gate-Driver Supply. Bypass GDRV to PGND with a 2.2µF ceramic capacitor.
19	DL	Low-Side MOSFET Gate Drive
20	PGND	Power Ground. Connect to SGND and DGND using short wide PCB traces.
21	LBI	BabyBuck Switching Node 1. See the *BabyBuck Regulator* section for configurations.
22	PWR	Power-Supply Input. Connect to a power-supply input. Bypass to ground with a 1µF ceramic capacitor.
23	LBO	BabyBuck Switching Node 2. See the *BabyBuck Regulator* section for configurations.
24, 25	3P3	Internal 3.3V Regulator Output. 3P3 is the supply rail for the internal analog circuitry. Bypass 3P3 to SGND with a 4.7µF ceramic capacitor. This pin may not be used to power any circuitry external to the MAX15301.
26	OUTN	Output Voltage Differential Sense Negative Input. Connect to ground at the load.
27	OUTP	Output Voltage Differential Sense Positive Input. Connect to the output at the load.
28, 29	I.C.	Internally Connected. Connect directly to ground near the MAX15301.
30	DCRP	Output Current Differential Sense Positive Input. Connect to the inductor or current-sense element positive side through an appropriate filter network.
31	DCRN	Output Current Differential Sense Negative Input. Connect to the inductor or current-sense element negative side.
32	PG	Open-Drain Power-Good Indicator. PG asserts high when soft-start is complete, the voltage has reached regulation, after a successful InTune calibration is completed.
EP	SGND	Exposed Pad and Analog Ground. The EP serves two purposes: it is both the analog ground of the device and a conduit for heat transfer. Connect to a large ground plane to maximize thermal performance. See the *PCB Layout Guidelines* section.

Functional Diagram



Detailed Description

The MAX15301AA02 is an innovative, PMBus-compliant, mixed-signal power-management IC with a built-in high-performance digital PWM controller for POL applications. The IC is based on Maxim's InTune automatically compensated digital PWM control loop. The MAX15301AA02 has optimal partitioning of the digital power-management and the digital power-conversion domains to minimize startup times and reduce bias current. The MAX15301AA02 supports over 80 standard and manufacturer-specific PMBus commands.

The IC uses adaptive compensation techniques to handle a broad range of timing, voltage, current, temperature, and external component parameter variations. Efficiency-optimization techniques further enhance the performance of the MAX15301AA02, including adjustable nonoverlap timing, load-variable gate-drive voltage, and switch-mode BabyBuck bias regulators for biasing the internal circuit blocks and the MOSFET gate drive.

The MAX15301AA02 features integrated power conversion to self-bias its digital, analog, and driver blocks from a single input supply (V_{PWR}). The IC relies on mixed-signal design techniques to control the power system efficiently and precisely. It does not require any software to configure or initialize the device. In addition, functions can be monitored and configured through the SMBus interface using standard PMBus commands resulting in ease of design and flexibility.

The control loop is separated from the housekeeping, power monitoring, and fault management blocks. Control loop parameters are stored in an on-chip nonvolatile flash memory. An internal microcontroller enables monitoring operating conditions using the SMBus interface. The DPWM control loop is implemented using dedicated state machines, there is no DSP or MCU in the control loop. This partition allows for architecture that minimizes power consumption while optimizing performance.

The *Functional Diagram* shows the controller implementation using a digital state space compensator (model predictive) controller, a microcontroller unit (MCU), a digital pulse-width modulator (DPWM), a PLL-based master timing generator, and a PMBus serial communication port.

State-Space Controller and DPWM

The MAX15301AA02 uses a digital pulse-width modulation (DPWM) control scheme to regulate the output voltage. Traditional PWM regulators (both analog and digital) use classical control methods for DC-DC converters based on linear models of a discrete time nature and root locus, Bode and Nyquist plots. These linear time-invariant approximations work well for small signals. However, when large transients cause duty-cycle saturation, the performance of the closed loop can be degraded (larger overshoots) and the output transients will be “slower” (large settling times). Tighter regulation performance during these disturbances is becoming a requirement. The IC addresses the issue by using model-predictive-based feedback design to compensate the DPWM.

The IC automatically constructs a state-space model (state estimator) of the control plant (Figure 1). The internal model gives access to state control variables that are otherwise unavailable. The state control variables are used to set the proper control values. For a given input to output step-down ratio and PWM switching frequency the IC sets the compensation coefficients for that application. Upon output enable, or in response to a PMBus command, the IC will perform the InTune calibration. During this calibration several powertrain parameter values are measured and the extracted parameters are used to create the internal model to optimize the bandwidth and transient response of the converter.

The state-space compensator block generates the duty-cycle command for the DPWM block. The DPWM block generates the required PWM outputs for the driver. The state-space controller block also contains a digital-to-analog converter that adjusts the gate-drive voltage. The gate-drive voltage can be set using a PMBus command (manufacturer specific) to a value between 5V and 8.5V to improve the power-supply efficiency.

BabyBuck Regulator

The MAX15301AA02 has an internal BabyBuck bias regulator circuit to generate both the gate-drive voltage supply and the internal digital supply to power the controller. The BabyBuck bias regulator is an internal two output switching regulator that uses a small (1008-size), low-cost inductor. If the user is not concerned with optimizing operating efficiency, the inductor can be omitted from the designs (connect the LBI pin to the PWR pin through a 100kΩ resistor). In this configuration, the bias regulator operates as a linear regulator (LDO). If an external gate-drive voltage is available, the LBI pin can be connected to V_{IN} through a 2kΩ resistor and the GDRV pin can be connected to the external source.

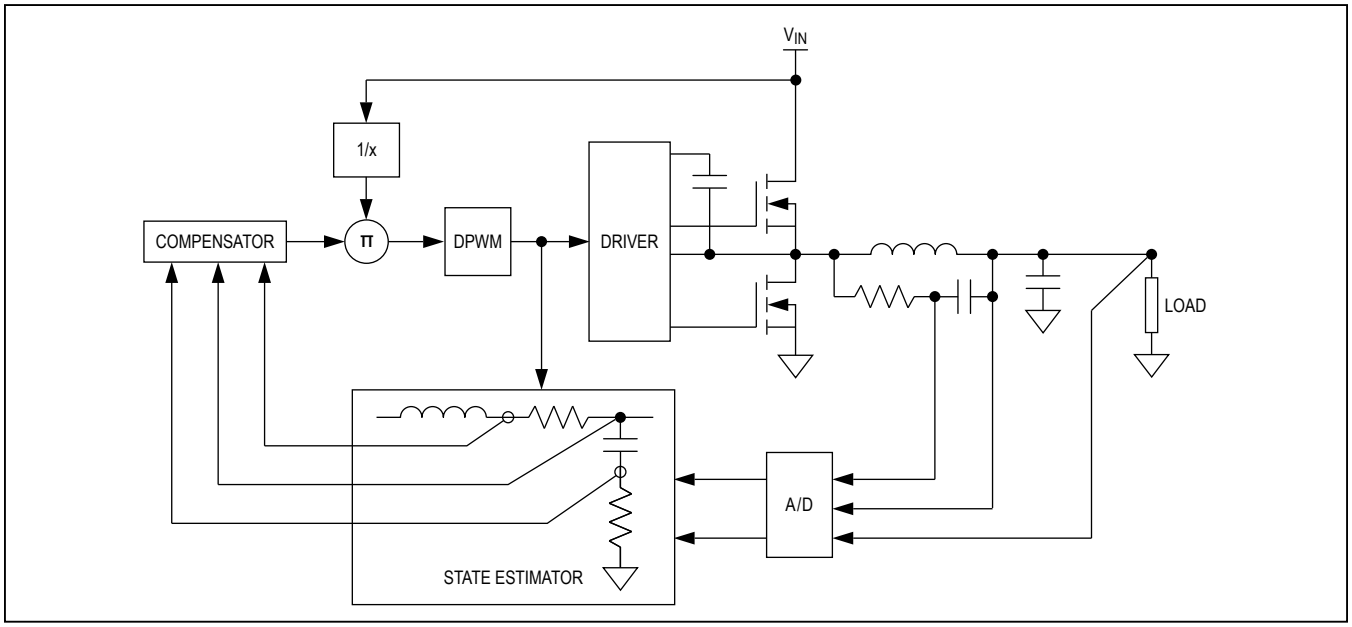


Figure 1. State-Space Controller Concept

External Temperature Sense

The MAX15301AA02 provides both an internal and external temperature measurement. Both the internal and external temperatures are reported to the user through the PMBus READ_TEMPERATURE_1 and READ_TEMPERATURE_2 commands, respectively. The internal temperature is measured directly at the device silicon junction. The external temperature is measured through the TEMPX pin using the base-emitter junction of a standard 2N3904 transistor. This technique is widely employed because it requires no calibration of the sensor; any PN junction can be used as a temperature sensor. The 2N3904 and 2N2222 transistors and integrated thermal diodes found in microprocessors, FPGAs, and ASICs are commonly used temperature sensors. Connect a 100pF filter capacitor, as shown in Figure 7, to ensure accurate temperature measurements. When the 2N3904 is connected to the TEMPX pin, the device uses the external temperature information for temperature-fault and current-measurement temperature compensation (tempco). If the external temperature measurement is not used or measures out of range, the device uses the internal temperature for temperature compensation and thermal-fault protection. Disable the external temperature measurement by connecting TEMPX to ground. The device's temperature-fault thresholds are programmed through the PMBus interface. The default value for the thermal-shutdown threshold is +115°C. The default overtemperature response is to shut down and restart when the fault is no longer present. Note that a rising temperature faults when it crosses the OT_FAULT_LIMIT and clears when it falls below the OT_WARN_LIMIT. The OT_WARN_LIMIT should always be set below the OT_FAULT_LIMIT. The device shuts down and pulls PG low when it acts on a temperature fault.

Regulation and Monitoring Functions

The MAX15301AA02 improves the reliability of the system it powers with multiple circuits that protect the regulator and the load from unexpected system faults. The IC continuously monitors the input voltage, output voltage and current, and internal/external temperatures. The IC can be configured to provide alerts for specific conditions of the monitored parameters. The thresholds and responses for these parameters have factory-default values, but can also be configured through the PMBus interface. The status of the power supply can be queried any time by a PMBus master.

Regulator Parameters

Key operating parameters in the MAX15301AA02, such as output voltage, switching frequency, and current-sense resistance, can be configured using resistors. This provides flexibility for the user while ensuring that the device has a well-defined "out-of-the-box" operational state. The pin configurations are only sampled when power is first applied (the IC ignores changes to resistor settings after power-up). From this initial operating state, it is possible for the user to change the parameters using PMBus commands. These changes can be stored in nonvolatile memory, and the device subsequently powers up in the newly stored configuration state; however, it is recommended that the pin-strap or resistor settings always be applied with values chosen to provide a safe initial behavior prior to PMBus configuration.

Pin-strap settings are programmed by connecting a resistor from the appropriate IC pins to SGND. The IC reads the resistance at startup and sets command parameters per the tables in the following detail sections. Note that the external parts count can be reduced in some cases by unconnecting or grounding the configuration pins.

Table 1. Output Voltage Setting Using Pin-Resistor Setting

R_{SET} (kΩ)	OUTPUT VOLTAGE (V)
0 to 4.3	Track mode
5 to 5.2	0.6
6.1 to 6.3	0.7
7 to 7.3	0.75
8.1 to 8.4	0.8
9.4 to 9.7	0.85
10.8 to 11.2	0.9
12.5 to 12.9	0.95
14.5 to 14.9	1
17.6 to 18	1.05
21.2 to 21.8	1.1
25.8 to 26.4	1.2
31.2 to 32	1.5
37.9 to 38.7	1.8
43.7 to 44.7	2.5
50.5 to 51.7	3.3
58.4 to 59.6	5
67.4 to Open	0

Table 2. Interleave Settings

SMBus ADDRESS	PHASE DELAY (°)
xxxx000b	0
xxxx001b	60
xxxx010b	120
xxxx011b	180
xxxx100b	240
xxxx101b	300
xxxx110b	90
xxxx111b	270

Output-Voltage Selection

The SET pin is used to establish the initial output voltage; it can be pin strapped high or low, or connected to SGND through a resistor to select the output voltage, as shown in Table 1. Note that the SET pin is read once at power-up and cannot be used to change the output voltage after that time.

If the desired output voltage is not included in Table 1, use a resistor to set the initial approximate output voltage, and then send VOUT_COMMAND to set the exact desired output voltage.

The output voltage can be set to any voltage between 0.5V and 5.25V, including margining, provided the input voltage to the DC-DC converter (V_{PWR}) is higher than the output voltage by an amount that conforms to the maximum duty-cycle specification.

The device's output voltage can be dynamically changed during operation through several PMBus commands. The output voltage can be decreased during operation without limit. The output voltage can be increased to 20% above the upper end of the allowable voltage determined by the RDIV setting. The RDIV setting is determined by the programmed output voltage when the output is enabled. Table 5 shows the voltage ranges that set each RDIV setting. As an example, if the output voltage is pin strapped to 1.4V, the RDIV is set to 0.65572 at startup. The output voltage can be increased to 15% above the upper end of the 0.65572 RDIV range, or 1.723V. The output voltage can be programmed higher than 1.723V, but the actual power-supply output can be clamped to a lower voltage.

Setting the Switching Frequency

The switching frequency can be adjusted from 300kHz to 1MHz with an external resistor from SYNC to SGND per Table 3, or by sending the PMBus FREQUENCY_SWITCH command. Note that the SYNC pin is read once at power-up and cannot be used to change the switching frequency after that time. The device considers open circuit on SYNC to be a fault condition so it sets the switching frequency to 575kHz in an attempt to pick a switching frequency typical of most applications; 575kHz is not a normal pin-strappable frequency, so if the user reads back a switching frequency of 575kHz, they know the SYNC resistor is open circuited. The switching frequency can be changed on-the-fly for frequencies between 300kHz to 475kHz and for frequencies between 476kHz to 1000kHz. The switching frequency during operation must stay either above or below 475kHz and should never cross this frequency. Doing so may result in unexpected operation. The user can cross the 475kHz switching boundary by disabling the device, changing the switching frequency, and then reenabling the device. As a guideline, lower frequencies can be used to improve efficiency, while higher frequencies can be selected to reduce the physical size and value of the external filter inductor and capacitors.

Table 3. Switching Frequency Resistor Settings (SYNC)

R_{SYNC} (kΩ)	SWITCHING FREQUENCY (kHz)
0 to 4.3	575
5 to 5.2	300
6.1 to 6.3	350
7 to 7.3	400
8.1 to 8.4	450
9.4 to 9.7	500
10.8 to 11.2	550
12.5 to 12.9	600
14.5 to 14.9	650
17.6 to 18	700
21.2 to 21.8	750
25.8 to 26.4	800
31.2 to 32	850
37.9 to 38.7	900
43.7 to 44.7	950
50.5 to 51.7	1000
58.4 to Open	575

External Synchronization

The device can be synchronized with an external clock to eliminate beat noise on the input- and output-voltage lines or to minimize input-voltage ripple. Synchronization is achieved by connecting a clock source to the SYNC pin. The incoming clock signal must be in the 300kHz to 1MHz range and must be stable with less than 10% variation. The device synchronizes to the rising edge of the clock after the device is enabled. In the event of a loss of the external clock signal during normal operation after successful synchronization with the external clock, the device automatically switches at the frequency programmed into the PMBus command's FREQUENCY_SWITCH variable. If an external clock is present at power-on when the device is trying to read the SYNC pin-strap resistance, the device cannot detect the synchronization frequency and does not write the proper frequency into FREQUENCY_SWITCH. However, if the clock is still present at enable, the device reads the proper frequency and overwrites FREQUENCY_SWITCH with the actual clock frequency. If a clock is not present at power-on, the device reads the pin-strap resistor value and writes the frequency into FREQUENCY_SWITCH per Table 3. If an external clock is applied to SYNC after power-on but before enable, the device overwrites FREQUENCY_SWITCH with the external clock frequency when the device is enabled. If an external clock is not applied prior to the device being enabled, the device keeps the originally programmed FREQUENCY_SWITCH value. Applying a clock to SYNC after the device is enabled causes the IC to synchronize to the clock; however, the FREQUENCY_SWITCH value is not updated. For proper synchronization, the external clock can be applied prior to applying power to the device, but must be applied prior to enabling the device. The external clock frequency should not be changed after the device is enabled. The device supports interleaving with an external SYNC input. The default phase delay is pin strappable and is determined by the 7-bit SMBus address, as shown in Table 2. The phase delay can also be changed by sending the PMBus INTERLEAVE command while the output is disabled. The phase delay should not be changed during operation. The programmed phase delay is between the rising edge of the SYNC clock signal and the center of the device's PWM pulse. The center of the PWM pulse is used for a reference point because the device's PWM pulse is dual-edge modulated.

IOUT_CAL_GAIN Selection

The device allows the user to set a default pin-strapped IOUT_CAL_GAIN at startup. IOUT_CAL_GAIN is the resistance of the current-sense element, which can be either the power inductor's DCR or a discrete current-sense resistor. The device's actual overcurrent trip point is a function of IOUT_CAL_GAIN, the current-sense element's actual resistance, and the value of the IOUT_OC_FAULT_LIMIT. See the output-overcurrent protection paragraph for more information on setting the overcurrent trip point. Setting IOUT_CAL_GAIN is accomplished by pin strapping, connecting a resistor from ADDR1 to SGND, as listed in Table 4b. The user can achieve a more accurate value of IOUT_CAL_GAIN by setting this parameter through the PMBus. Note that ADDR1 is used to set both the PMBus address and IOUT_CAL_GAIN. The user should first determine the desired PMBus address and then choose the appropriate ADDR1 resistor per Table 4a and Table 4b.

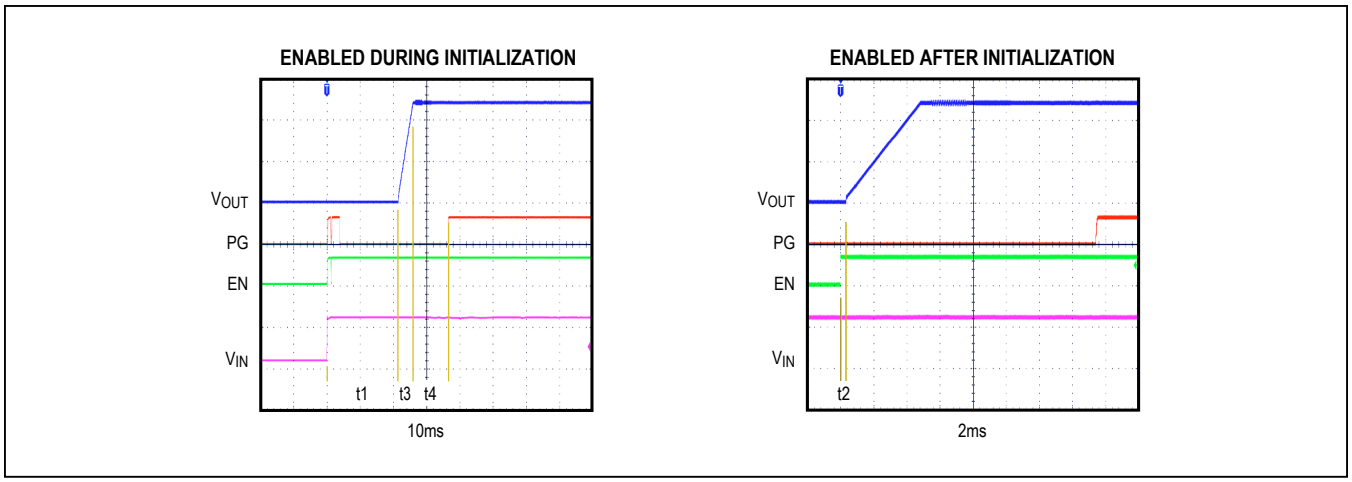


Figure 2. Startup Timing Diagrams

Table 4a. SMBus Address Set by ADDR0, ADDR1 Resistor Connections

DCR	R_{ADDR1} (kΩ)				
0.4mΩ →	0 to 4.3	5 to 5.2	6.1 to 6.3	7 to 7.3	8.1 to 8.4
0.8mΩ →	9.4 to 9.7	10.8 to 11.2	12.5 to 12.9	14.5 to 14.9	17.6 to 18
1.2mΩ →	21.2 to 21.8	25.8 to 26.4	31.2 to 32	37.9 to 38.7	43.7 to 44.7
1.6mΩ →	50.5 to 51.7	58.4 to 59.6	67.4 to 68.8	85.7 to 87.5	113.8 to 116.2
2.0mΩ →	138.6 to 141.4	167.3 to 170.7	202.9 to 207.1	234.6 to 239.4	271.2 to Open
R_{ADDR0} (kΩ)	SMBus 7-BIT DEVICE ADDRESS				
0 to 4.3	0x0A	0x22	0x3A	0x52	0x6A
5 to 5.2	0x0B	0x23	0x3B	0x53	0x6B
6.1 to 6.3	0x0C	0x24	0x3C	0x54	0x6C
7 to 7.3	0x0D	0x25	0x3D	0x55	0x6D
8.1 to 8.4	0x0E	0x26	0x3E	0x56	0x6E
9.4 to 9.7	0x0F	0x27	0x3F	0x57	0x6F
10.8 to 11.2	0x10	0x28	0x40	0x58	0x70
12.5 to 12.9	0x11	0x29	0x41	0x59	0x71
14.5 to 14.9	0x12	0x2A	0x42	0x5A	0x72
17.6 to 18	0x13	0x2B	0x43	0x5B	0x73
21.2 to 21.8	0x14	0x2C	0x44	0x5C	0x74
25.8 to 26.4	0x15	0x2D	0x45	0x5D	0x75
31.2 to 32	0x16	0x2E	0x46	0x5E	0x76
37.9 to 38.7	0x17	0x2F	0x47	0x5F	0x77
43.7 to 44.7	0x18	0x30	0x48	0x60	0x78
50.5 to 51.7	0x19	0x31	0x49	0x61	0x79
58.4 to 59.6	0x1A	0x32	0x4A	0x62	0x7A
67.4 to 68.8	0x1B	0x33	0x4B	0x63	0x7B
85.7 to 87.5	0x1C	0x34	0x4C	0x64	0x7C
113.8 to 116.2	0x1D	0x35	0x4D	0x65	0x7D
138.6 to 141.4	0x1E	0x36	0x4E	0x66	0x7E
167.3 to 170.7	0x1F	0x37	0x4F	0x67	0x7F
202.9 to 207.1	0x20	0x38	0x50	0x68	0x7F
234.6 to Open	0x21	0x39	0x51	0x69	0x7F

Note: *The SMBus specification recommends against using the shaded addresses.*

Table 4b. IOUT_CAL_GAIN Set by ADDR1 Resistor Connection

R_{ADDR1} (kΩ)	IOUT_CAL_GAIN (mΩ)
0 to 8.4	0.4
9.4 to 18	0.8
21.2 to 44.7	1.2
50.5 to 116.2	1.6
138.6 to Open	2.0

Internal Bias Regulators

The MAX15301AA02 analog circuitry is powered by an internal 3.3V regulator (3P3). The IC also has an internal bias regulator to generate a 1.8V rail (1P8) to power internal digital circuitry. Bypass the 3P3 pin to SGND with a 4.7µF ceramic (X5R or better) capacitor. Bypass 1P8 to DGND with a 10µF ceramic (X5R or better) capacitor. These internal regulators are not designed to power external circuitry.

Input Voltage Feed-Forward

The MAX15301AA02 uses input voltage feed-forward techniques to provide excellent line regulation. Connect the INSNS pin to the powertrain input voltage through a 2kΩ series resistor for input voltage feed-forward and telemetry. The voltage at INSNS is sampled every 4µs.

The IC does not enable DC-DC conversion if the voltage at INSNS is below the PMBus VIN_UV_FAULT_LIMIT threshold (default 4V) or below the VIN_ON, VIN_OFF limits (default 6V rising and 5.5V falling, respectively.) The user can read back the measured input voltage value using the PMBus READ_VIN command.

Output On/Off Control

The MAX15301AA02 features both a hardware enable input (EN pin) and a PMBus enable function. The factory default for the enable functions is that the IC can be enabled by either an assertion of the hardware EN pin to a logic-high level or by issuing a PMBus enable command. The enable functionality can be changed using the PMBus ON_OFF_CONFIG PMBus command (see the PMBus specification for details).

The default configuration of the IC allows the output to be enabled either by driving the EN input to a logic-high level, or by sending the PMBus OPERATION command. The enable criteria can be changed using the PMBus ON_OFF_CONFIG command.

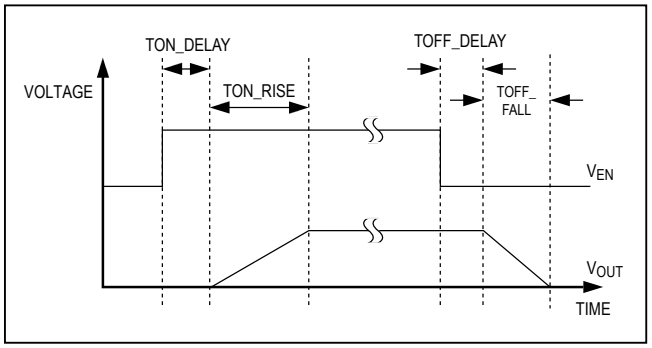


Figure 3. Turn-On/-Off Delays and Soft-Start/-Stop Times

Device Initialization

The MAX15301AA02 includes power-on reset circuits that monitor the internal bias supplies and the external supply voltage. When all supplies are above their UVLO thresholds, the following self-test sequence occurs:

1) Run self test and CRC check on the memory.
2) Read resistor settings and set command values and program working memory accordingly.
3) Confirm absence of any faults that would prevent turn-on.
4) Begin wait for a valid output enable condition (hardware or PMBus command).

The power-up and initialization process takes approximately 25ms, depending upon the specific combination of pin-strap resistor values to be read. The IC will not enable output regulation until initialization is complete.

Output-Voltage Sequencing

In a system with multiple MAX15301AA02 devices or other PMBus-controlled ICs, output-voltage sequencing can be achieved by configuring each power supply with different turn-on/turn-off delays and output rise/fall times. All power supplies are then commanded to turn on (or off) simultaneously using a combined EN signal.

The IC supports soft-start and soft-stop functionality as shown in Figure 3. The PMBus TON_RISE and TOFF_FALL commands determine the soft-start and soft-stop ramp times. The TON_DELAY command sets the time from a valid enable condition to the beginning of the output-voltage ramp. Similarly, the TOFF_DELAY command sets the time between loss of valid enable condition and the beginning of the output ramp down to 0V. The default setting for TON_DELAY is the minimum value of 1ms and the default setting for the TON_RISE is 5ms.

The output-voltage slew-rates for turn-on and turn-off are given by VOUT_COMMAND ÷ TON_RISE and

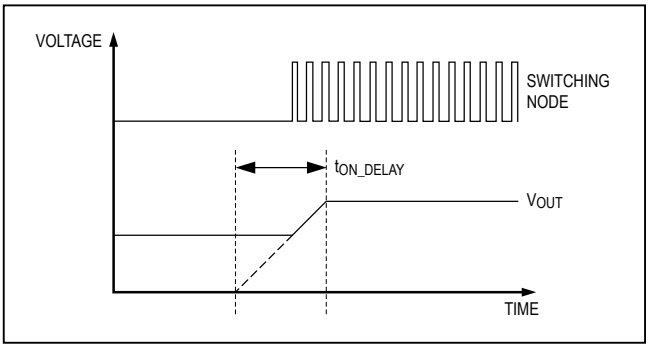


Figure 4. Startup into a Prebiased Output

VOUT_COMMAND ÷ TOFF_FALL, respectively. It is recommended to set TON_RISE and TOFF_FALL to at least 1ms to prevent excessive inrush currents due to high dV/dt. The output voltage ramp-up rises monotonically above 300mV regardless of input voltage, output voltage, or prebias voltage on the output. Note that the IC initiates the InTune calibration process after the soft-start ramp-up is complete.

Startup with Prebias

The MAX15301AA02 supports soft-start into a prebias output voltage condition. A prebias condition occurs when there is already a voltage at the output of the power supply before it has been enabled. This can be caused by precharged output capacitors, or a parasitic ESD diode in the load IC that pulls the output up to another system supply rail. When EN is asserted, the IC checks the output for the presence of prebias voltage. If the prebias voltage is less than 200mV, startup is performed normally assuming no prebias. If the prebias is greater than 200mV but below the target set point for the output, the IC ramps up the output voltage from the prebias voltage to the regulation set point as shown in Figure 4. If the prebias is above the VOUT_OV_FAULT_LIMIT value, the IC does not attempt soft-start.

If prebias was detected at the time of enable, the IC saves the prebias voltage level in a register and terminates the output voltage ramp-down at the prebias voltage when disabled. This register is not user accessable.

Voltage Tracking

The MAX15301AA02 supports voltage tracking of the output from a reference input. To select the tracking mode, connect the SET pin to SGND. The IC's output tracks the V_{TRACK} voltage with a preset ratio governed by an internal feedback divider (RDIV) and an external resistive voltage-divider (R1, R2) which is placed from the supply being tracked to SGND (Figure 5). The center tap of the external divider should be connected to the CIO input.

In tracking mode, V_{OUT} is regulated to the lower of:

$$V_{OUT} = \frac{V_{TRACK}}{RDIV} \times \frac{R1}{R1 + R2}$$

or the output set-point voltage $V_{OUT(SET)}$ as determined by the VOUT_COMMAND. As seen in the above equa-

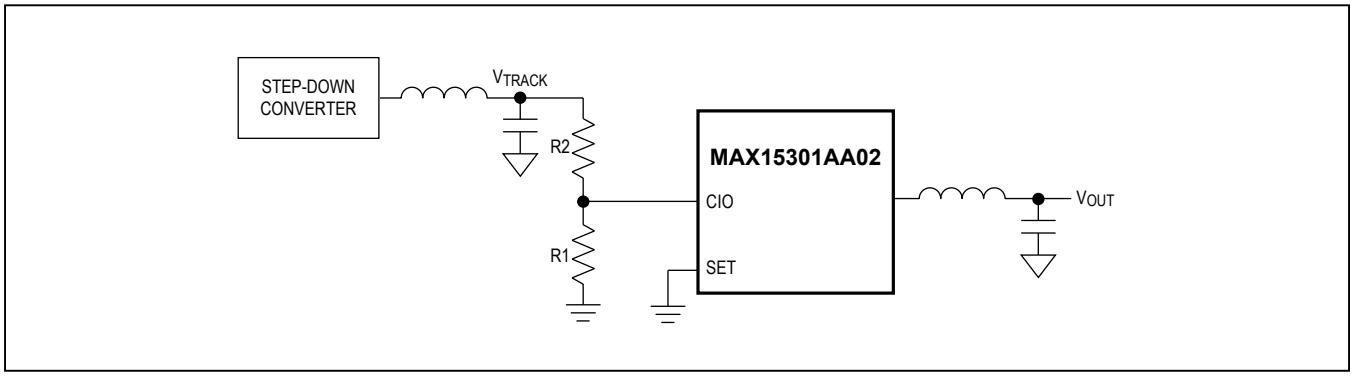


Figure 5. Tracking Mode Configuration

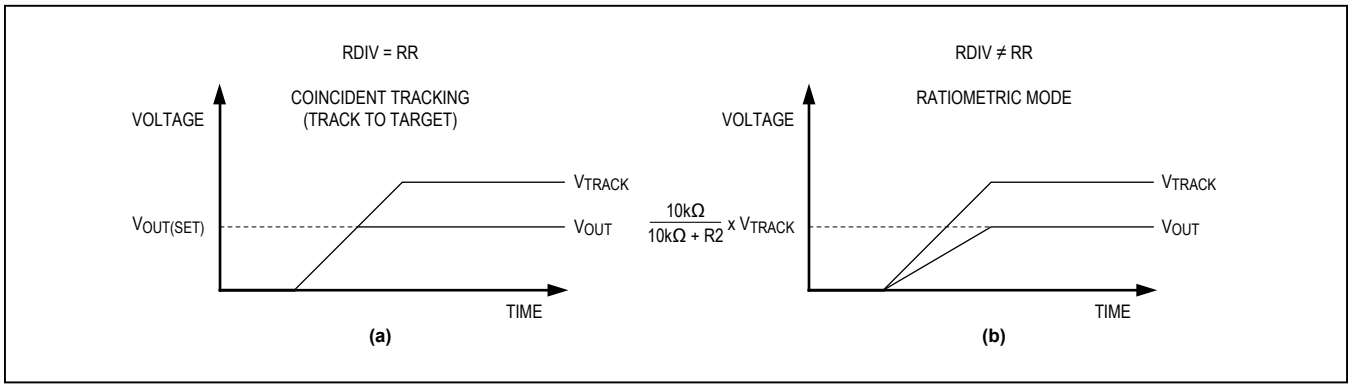


Figure 6. Tracking

tion, if the resistor-divider ratio RR = R1/(R1 + R2) is chosen such that it is equal to the operational RDIV, the output voltage follows the tracking voltage coincidentally (Figure 6a). For all other cases, the V_{OUT} follows a ratiometric tracking (Figure 6b) depending on the ratio of RR and RDIV. The IC automatically selects RDIV based on the output set-point voltage as shown in Table 5. For example, if $V_{OUT(SET)}$ is set to 1.6V by the VOUT_COMMAND, RDIV is set to 0.54247. For a reliable voltage tracking, it is recommended that once the IC is powered up, the VOUT_COMMAND should not be changed so as to cause a change to the operational RDIV (Table 5). If such a change in VOUT_COMMAND is required, the user should save the new VOUT(SET) in the device memory (using STORE_USER_ALL_COMMAND) and recycle the input power to set a new RDIV operational value. For simplicity, fix R1 at 10kΩ and use the following equation to determine R2:

$$R2 = 10k \times \left(\frac{V_{TRACK}}{R_{DIV} \times V_{OUT}} - 1 \right)$$

Table 5. Required Divider Ratio (RDIV) as a Function of V_{OUT}

VOUT_COMMAND (V)	RDIV
< 0.65	0.99547
0.65 to < 1.12	0.88222
1.12 to < 1.28	0.76897
1.28 to < 1.50	0.65572
1.50 to < 1.82	0.54247
1.82 to < 2.29	0.42922
2.29 to < 3.12	0.31597
3.12 to < 5.25	0.20272

For the best voltage regulation, RR should be set such that the final V_{OUT} tracking target voltage is slightly higher than the output set-point voltage determined by VOUT_COMMAND. The output ramp tracks the V_{TRACK} input as shown in Figure 6 until reaching the VOUT_COMMAND value. If the application requires continuous ratiometric tracking, VOUT_COMMAND should be set higher than the desired V_{OUT} tracking target or left at the 5.0V default value. In this case, there is a small regulation inaccuracy due to the tolerance of the external resistors.

Output-Voltage Margining

The IC supports voltage margining, which can be used to test the end equipment's design margin associated with power-supply variation. The margin set-point commands VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW are set to ±5% of VOUT_COMMAND by default, but can be changed via the PMBus interface. Output voltage margining is controlled by the OPERATION command.

Output Voltage Ranges and Fault Limits

The MAX15301AA02 features output undervoltage and overvoltage protection. The PMBus VOUT_OV_FAULT_LIMIT is set to 115% of VOUT_COMMAND by default, and VOUT_UV_FAULT_LIMIT is set to 85%. These thresholds can be changed through PMBus and set anywhere between 0V and the lower of either the ADC full-scale value or VOUT_MAX (VOUT_MAX is 110% of VOUT_COMMAND by default.

The IC continuously monitors the output voltage. If the voltage exceeds the protection limits, the IC follows the actions prescribed by the VOUT_OV_FAULT_RESPONSE or VOUT_UV_FAULT_RESPONSE commands as appropriate. By default, an overvoltage fault results in an immediate shutdown with no retry attempts, whereas undervoltage faults are ignored. The fault response commands can be changed at any time, but changes to the fault-response commands only take effect when the output is disabled.

Output-Overcurrent Protection

The MAX15301AA02 monitors the voltage across the output inductor resistance (or other resistive sense element) to provide output current monitoring and overload protection. The voltage signal at the current-sense element is divided by the IOUT_CAL_GAIN value to yield output current in Amps. The value of IOUT_CAL_GAIN is initially set by the ADDR1 resistance according to Table 4b and should be set as close as possible to the inductor DCR (or the resistive sense element's resistance.) More accurate output current measurement can be achieved by calibrating the IOUT_CAL_GAIN value; contact Maxim for an application note describing the READ_IOUT calibration process.

The overcurrent fault threshold is set by the IOUT_OC_FAULT_LIMIT command; the default value is 25A. If an overcurrent condition is detected, the IC shuts down, delays for 700ms, and then attempts to restart the regulator. This process repeats indefinitely until the fault condition no longer persists. This fault response behavior can be changed using the PMBus IOUT_OC_FAULT_RESPONSE command.

Fault Handling

The MAX15301AA02 monitors input voltage, output voltage, output current, and both internal and external temperatures. The fault thresholds and responses are factory-set, but may be changed using PMBus commands. Fault detection can be individually enabled or disabled for the parameters through PMBus. The default limits are as indicated in Table 6. The response to a fault condition can be changed through PMBus. Refer to Maxim's **User Guide 5793: *MAX15301 PMBus Command Set User's Guide*** for more information on setting fault thresholds and fault responses.

Nonvolatile PMBus Memory

The MAX15301AA02 includes three nonvolatile stores for PMBus configuration values. The first is the MAXIM store, which contains a read-only copy of all default command settings. The next is the read/write-accessible DEFAULT store, which is intended to contain an equipment manufacturer's preferred or suggested settings. Third is the read/write accessible USER store, which is intended to store the end-user's preferred settings.

When the device is enabled, a combination of the pin-configurable command values and the contents of the USER store are loaded into working memory. Any command values that have been edited and stored to the USER memory takes precedence over their corresponding pin-configured values.

Equipment manufacturers should ensure that the DEFAULT and USER stores are saved with duplicate copies of the manufacturer's preferred or suggested command values. In this manner, an end user can restore the DEFAULT memory and save to the USER store any time they wish to return the device to the manufacturer's original configuration.

Special security commands and features are included so that a manufacturer user can store and lock the regulator's configuration on a command-by-command basis. Contact Maxim for application notes describing these security features.

Table 6. Fault Conditions

FAULT CONDITION	DEFAULT THRESHOLD	RANGE
V_{IN} Overvoltage	14V	0 to 14.7V
V_{IN} Undervoltage	4.2V	0 to 14.7V
V_{OUT} Overvoltage	VOUT_COMMAND x 115%	0 to 5.5V
V_{OUT} Undervoltage	VOUT_COMMAND x 85%	0 to 5.5V
I_{OUT} Overcurrent	25A	0 to 30A
Overtemperature	115°C	-40°C to +150°C

Power Good (PG)

PG, power good, is an open-drain output used to indicate when the MAX15301AA02 is ready to provide regulated output voltage to the load. During startup and during a fault condition, PG is held low. PG is asserted high after the output has ramped to a voltage above the POWER_GOOD_ON (5Eh) threshold and a successful InTune calibration has completed. If the output regulation voltage falls below the POWER_GOOD_OFF (5Fh) threshold, PG will be deasserted.

PMBus Digital Interface

The MAX15301AA02 is a PMBus-compatible device that includes many of the standard PMBus commands. A PMBus 1.2-compliant device uses the System Management Bus (SMBus) version 2.0 for transport protocol and responds to the SMBus slave address. In this data sheet, the term SMBus is used to refer to the electri-

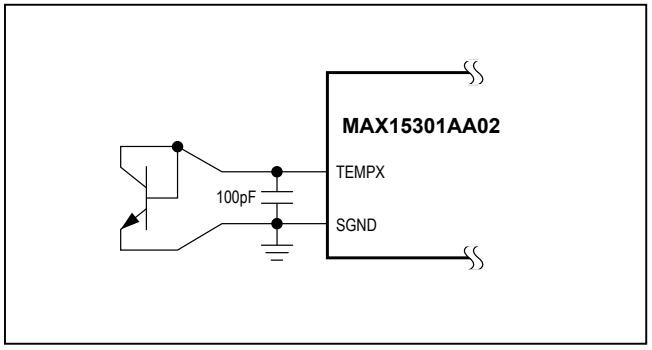


Figure 7. Temperature Sensing with a 2N3904 npn Transistor

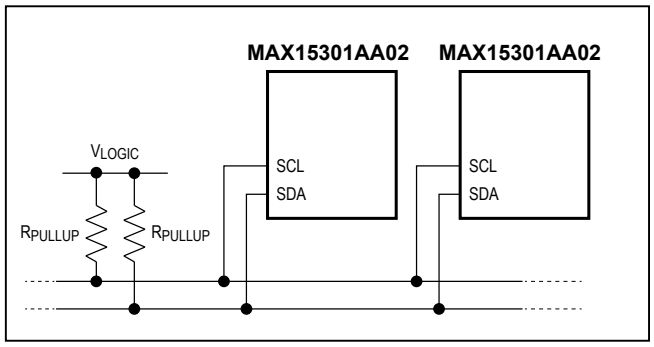


Figure 8. SMBus Multidevice Configuration

Table 7. PMBus Command Summary

COMMAND CODE	COMMAND NAME	SMBus TRANSFER TYPE	# OF DATA BYTES	MIN	MAX	DEFAULT VALUE	UNITS
0x01	OPERATION	R/W Byte	1	—	—	0x40	—
0x02	ON_OFF_CONFIG	R/W Byte	1	—	—	0x16	—
0x03	CLEAR_FAULTS	Send Byte	0	—	—	—	—
0x10	WRITE_PROTECT	R/W Byte	1	—	—	0	—
0x11	STORE_DEFAULT_ALL	Send Byte	0	—	—	—	—
0x12	RESTORE_DEFAULT_ALL	Send Byte	0	—	—	—	—
0x15	STORE_USER_ALL	Send Byte	0	—	—	—	—
0x16	RESTORE_USER_ALL	Send Byte	0	—	—	—	—
0x19	CAPABILITY	Read Byte	1	—	—	0xA0	—
0x20	VOUT_MODE	Read Byte	1	—	—	0x14	—
0x21	VOUT_COMMAND	R/W Word	2	0.5	5.25	SET pin resistor setting	V
0x22	VOUT_TRIM	R/W Word	2	—	—	0	V
0x23	VOUT_CAL_OFFSET	R/W Word	2	—	—	0	V
0x24	VOUT_MAX	R/W Word	2	—	—	VOUT_COMMAND + 10%	V
0x25	VOUT_MARGIN_HIGH	R/W Word	2	—	—	VOUT_COMMAND + 5%	V
0x26	VOUT_MARGIN_LOW	R/W Word	2	—	—	VOUT_COMMAND - 5%	V
0x27	VOUT_TRANSITION_RATE	R/W Word	2	—	—	0.1	mV/µs
0x28	VOUT_DROOP	R/W Word	2	—	—	0	mΩ
0x33	FREQUENCY_SWITCH	R/W Word	2	300	1000	SYNC pin resistor setting	kHz
0x35	VIN_ON	R/W Word	2	4	12	6	V
0x36	VIN_OFF	R/W Word	2	4	12	5.5	V
0x37	INTERLEAVE	R/W Word	2	—	—	See Table 2	—
0x38	IOUT_CAL_GAIN	R/W Word	2	—	—	ADDR1 pin resistor setting	mΩ
0x39	IOUT_CAL_OFFSET	R/W Word	2	—	—	0	A
0x40	VOUT_OV_FAULT_LIMIT	R/W Word	2	—	—	VOUT_COMMAND + 15%	V
0x41	VOUT_OV_FAULT_RESPONSE	R/W Byte	1	—	—	0x80	—
0x44	VOUT_UV_FAULT_LIMIT	R/W Word	2	—	—	VOUT_COMMAND - 15%	V
0x45	VOUT_UV_FAULT_RESPONSE	R/W Byte	1	—	—	0x00	—
0x46	IOUT_OC_FAULT_LIMIT	R/W Word	2	—	—	25	A
0x47	IOUT_OC_FAULT_RESPONSE	R/W Byte	1	—	—	0xBF	—
0x4F	OT_FAULT_LIMIT	R/W Word	2	—	—	115	°C
0x50	OT_FAULT_RESPONSE	R/W Byte	1	—	—	0xC0	—
0x51	OT_WARN_LIMIT	R/W Word	2	—	—	95	°C

Table 7. PMBus Command Summary (continued)

COMMAND CODE	COMMAND NAME	SMBus TRANSFER TYPE	# OF DATA BYTES	MIN	MAX	DEFAULT VALUE	UNITS
0x55	VIN_OV_FAULT_LIMIT	R/W Word	2	—	—	14	V
0x56	VIN_OV_FAULT_RESPONSE	R/W Byte	1	—	—	0xC0	—
0x59	VIN_UV_FAULT_LIMIT	R/W Word	2	—	—	4.2	V
0x5A	VIN_UV_FAULT_RESPONSE	R/W Byte	1	—	—	0xC0	—
0x5E	POWER_GOOD_ON	R/W Word	2	—	—	VOUT_COMMAND - 10%	V
0x5F	POWER_GOOD_OFF	R/W Word	2	—	—	VOUT_COMMAND - 15%	V
0x60	TON_DELAY	R/W Word	2	—	—	5	ms
0x61	TON_RISE	R/W Word	2	—	—	5	ms
0x64	TOFF_DELAY	R/W Word	2	—	—	1	ms
0x65	TOFF_FALL	R/W Word	2	—	—	5	ms
0x78	STATUS_BYTE	Read Byte	1	—	—	—	—
0x79	STATUS_WORD	Read Word	2	—	—	—	—
0x7A	STATUS_VOUT	Read Byte	1	—	—	—	—
0x7B	STATUS_IOUT	Read Byte	1	—	—	—	—
0x7C	STATUS_INPUT	Read Byte	1	—	—	—	—
0x7D	STATUS_TEMPERATURE	Read Byte	1	—	—	—	—
0x7E	STATUS_CML	Read Byte	1	—	—	—	—
0x88	READ_VIN	Read Word	2	—	—	—	V
0x8B	READ_VOUT	Read Word	2	—	—	—	V
0x8C	READ_IOUT	Read Word	2	—	—	—	A
0x8D	READ_TEMPERATURE_1	Read Word	2	—	—	—	°C
0x8E	READ_TEMPERATURE_2	Read Word	2	—	—	—	°C
0x94	READ_DUTY_CYCLE	Read Word	2	—	—	—	%
0x95	READ_FREQUENCY	Read Word	2	—	—	—	kHz
0x98	PMBUS_REVISION	Read Byte	1	—	—	0x22	—
0x99	MFR_ID	R/W Block	8	—	—	Null	—
0x9A	MFR_MODEL	R/W Block	13	—	—	Null	—
0x9B	MFR_REVISION	R/W Block	7	—	—	Null	—
0x9C	MFR_LOCATION	R/W Block	8	—	—	Null	—
0x9D	MFR_DATE	R/W Block	6	—	—	Null	—
0x9E	MFR_SERIAL	R/W Block	13	—	—	Null	—
0xAD	IC_DEVICE_ID	Read Block	8	—	—	“MAX15301AA02”	—
0xAE	IC_DEVICE_REV	Read Word	8	—	—	<firmware revision>	—

Table 7. PMBus Command Summary (continued)

COMMAND CODE	COMMAND NAME	SMBus TRANSFER TYPE	# OF DATA BYTES	MIN	MAX	DEFAULT VALUE	UNITS
0xD0	ADAPTIVE_MODE	Write Byte	2	—	—	0x024B	—
0xD3	FEEDBACK_EFFORT	R/W Word	2	—	—	0.5	—
0xD5	LOOP_CONFIG	R/W Word	2	—	—	0x0100	—
0xDB	COMP_MODEL	R/W Block	6	—	—	0.03167, 0.5, 0.5	—
0xE0	MANUF_CONF	R/W Block	32	—	—	0	—
0xE1	MANUF_LOCK	Write Word	2	—	—	0	—
0xE2	MANUF_PASSWD	Write Word	2	—	—	0	—
0xE3	USER_CONF	R/W Block	32	—	—	0	—
0xE4	USER_LOCK	Write Word	2	—	—	0	—
0xE5	USER_PASSWD	R/W Word	2	—	—	0	—
0xE6	SECURITY_LEVEL	Read Byte	1	—	—	0x00	—
0xE7	DEADTIME_GCTRL	R/W Block	19	—	—	See PMBus Application Note	—
0xE8	ZETAP	R/W Word	2	—	—	1.5	—
0xEA	RESTORE_MAXIM_ALL	Send Byte	0	—	—	—	—
0xF8	EXT_TEMP_CAL	R/W Block	4	—	—	1.0391, -8	—

cal characteristics of the PMBus communication using the SMBus physical layer. The term PMBus is used to refer to the PMBus command protocol.

The IC employs six standard SMBus protocols (Write Byte, Read Byte, Write Word, Read Word, Write Block, and Read Block) to program output voltage and warning/faults thresholds, read monitored data, and provide access to all manufacturer-specific commands.

When the data word is transmitted, the lower order byte is sent first and the higher order byte is sent last. Within any byte, the most significant bit (MSB) is sent first and the least significant bit (LSB) is sent last.

Contact the factory for detailed PMBus command support.

Supported PMBus Commands

The IC supports the standard PMBus commands given in Table 7. Contact Maxim for an application note that describes all MAX15301AA02 PMBus command functionality in detail.

A single pair of pullup resistors (one each for SCL and SDA) is required for each shared bus as shown in Figure 8. Consult the SMBus 2.0 specifications as well as the guaranteed drive capability of SDA in the *Electrical Characteristics* table to determine the value of the pullup resistors. Refer to Maxim's **User Guide 5793: *MAX15301 PMBus Command Set User's Guide*** for more information on setting fault thresholds and fault responses.

Design Procedure

Switching Frequency Selection

The first step in selecting a buck controller's output filter is to select the desired switching frequency (f_{SW}) for the PWM. The MAX15301AA02 will switch at frequencies in the range of 300kHz ≤ f_{SW} ≤ 1MHz. Select a low frequency for higher efficiency. Use a higher frequency to reduce the size of the external filter components and to improve transient response. Also consider system frequency requirements when choosing f_{SW}, such that the harmonics of the switching frequencies do not interfere with the system operation. The switching frequency for the IC is set by the SYNC pin connection per Table 3. The switching frequency can be changed via the FREQUENCY_SWITCH PMBus command at anytime the controller is disabled. The selection of 600kHz provides a good balance of efficiency, small size, and good transient response.

Inductor Selection

Three key inductor parameters must be specified to select an inductor for operation with the MAX15301AA02: inductance value (L), inductor saturation current (I_{SAT}), and maximum DC resistance (DCR).

1) Inductor value selection: For automatic compensation using InTune technology, the inductor is selected such that the peak-to-peak inductor ripple current (LIR) is 20% to 40% of the maximum operating current (I_{OUTMAX}). Using a low LIR ratio (higher inductor value) will result in higher DC resistance in the inductor and will reduce efficiency. Using a high value of LIR will increase the RMS current which will also decrease efficiency. Maxim recommends 30% for a peak-to-peak ripple to maximum operating current ratio (LIR = 0.3).

   The nominal inductor value can now be calculated using LIR, f_{SW}, V_{IN}, V_{OUT}, and I_{OUTMAX} (the maximum DC load current) using the following equation:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{OUT} LIR}$$
$$0.2 \le LIR \le 0.4$$

   The exact inductor value in this range is not critical and can be adjusted to make trade-offs among size, cost, and efficiency. A higher inductance can increase efficiency by reducing the RMS current. Lower inductor values minimize size and cost. Lower inductor values may also improve transient response but reduce efficiency due to higher peak currents.

2) The selected inductor's saturation current rating (I_{SAT}) must exceed the user-defined current limit. I_{SAT} should generally be selected such that it is greater than I_{LIM} + LIR/2 +10% to provide adequate margin in the event of a large load transient. It is important to select an inductor that has a high enough I_{SAT} to satisfy this requirement though this parameter typically forces a certain dimension of inductor to be used.

3) Finally, the user should select an inductor with minimal DCR (DC series resistance) to reduce overall losses in efficiency. See the Current Sense section for more information on selecting the inductor DCR.

Output Capacitor Selection

The MAX15301AA02 has been optimized to operate with low-ESR output capacitors. These capacitors typically have X5R and X7R dielectrics. High-ESR capacitors can be added, but would provide little benefit to system performance. The output capacitor requirement is dependent upon two considerations:

1) Output-ripple voltage

2) Load current transient envelope

Both requirements are easily achieved with all-ceramic output capacitors. The total output-voltage ripple is a function of the output capacitor's ESR and capacitance and typically chosen to be ~1% of the output voltage. For typical applications, the ripple voltage is dominated by the capacitance. The following equations calculate the minimum output capacitance and maximum allowable ESR:

$$ESR_{MAX} = \frac{V_{RIPPLE}}{\Delta I}$$
$$C_{OUTMIN} = \frac{\Delta I}{8 \times V_{RIPPLE} \times f_{SW}}$$

where ΔI is:

$$\Delta I = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

The worst-case output-voltage ripple is:

$$V_{RIPPLE} = \Delta I \times \left(\frac{1}{8 \times C_{OUT} \times f_{SW}} + ESR \right)$$

An ESR below 10mΩ is typically required. The use of two or more 100µF ceramic capacitors in parallel is typically sufficient to achieve a good ripple voltage.

When all-ceramic output capacitors are used, load-current transient envelope is the primary concern for capacitor selection. Designs with small-load transients can use fewer capacitors and designs with larger load transients require more load capacitance to reduce output "sag" and "soar." The allowable deviation of the output voltage during fast-load transient determines the output capacitance. The following two equations calculate the

minimum capacitance required to meet the voltage sag and soar requirements from a load transient:
To meet load current transient envelope requirements, the IC compensates for output filters with natural (resonant) frequencies f_{LC} such that the following is met:

$$C_{OUT} = \frac{L \times \Delta I^2}{2 \times \Delta V_{SAG} \times (V_{IN} - V_O)} + \frac{\Delta I_O}{2 \times \pi \times BW \times \Delta V_{SAG}}$$

$$C_{OUT} = \frac{L \times \Delta I^2}{2 \times \Delta V_{SOAR} \times V_O} + \frac{\Delta I_O}{2 \times \pi \times BW \times \Delta V_{SOAR}}$$

where BW is the power-supply crossover frequency in Hz, which is approximately $f_{SW}/10$ for the device and C_{OUT} for the out capacitance.

The total output-voltage ripple also includes a voltage ripple due to quantization noise. This quantization noise is inherent to the digital control loop and is not affected by adding or removing output capacitors. The noise appears as random noise on the output voltage at a frequency between 10kHz and 60kHz. The amplitude is approximately 4mV at V_{OUT} = 1.2V and 12mV at V_{OUT} = 3.3V. See the Typical Operating Characteristics for the typical waveforms.

Compensating the Power Supply

Unlike most power-supply designs, the device does not require designing and testing a compensation circuit. The device automatically measures the output filter's resonant frequency and uses this information to set the appropriate compensation parameters. The device is stable if the output-filter corner frequency meets the following requirements:

$$25 \le f_{SW}/f_{LC} \le 70$$

where:

$$f_{LC} \doteq 1 \Big/ \left(2\pi\sqrt{LC}\right)$$

Therefore:

$$\frac{1}{L}\left(\frac{25}{2\pi f_{SW}}\right)^2 \le C \le \frac{1}{L}\left(\frac{70}{2\pi f_{SW}}\right)^2$$

Most 600kHz PoL designs (10A to 25A) are satisfied using between 200µF and 1000µF of ceramic output capacitance and no additional electrolytic capacitors. The InTune adaptive compensation permits a large range of output inductors and capacitors.

Input Capacitor Selection

The input filter capacitor reduces peak current drawn from the power source and reduces noise and voltage ripple on the input caused by the switching circuitry. The value of the input capacitor is selected to limit the ripple voltage (δV) as follows:

$$C_{IN} \ge \frac{I_{OUT} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{f_{SW} \times \Delta V}$$

where DV is the input ripple voltage. This calculation assumes there is measurable inductance back to the original V_{IN} source thus this calculation provides low source impedance at the input of the DC-DC converter. The capacitance requirement is greatest when the duty cycle is 50% and decreases as duty cycle increases (i.e. input voltage increases).

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents as defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

I_{RMS} attains a maximum value when the input voltage equals twice the output voltage (V_{IN} = $2V_{OUT}$), so $I_{RMS(MAX)}$ = $I_{LOAD(MAX)}/2$. For most applications, nontantalum capacitors (ceramic, aluminum, polymer, or OS-CON) are preferred at the inputs due to the robustness of non-tantalum capacitors to accommodate high inrush currents of systems being powered from very low impedance sources. Additionally, two (or more) smaller-value low-ESR capacitors should be connected in parallel to reduce high-frequency noise.

MOSFET Selection

The following guidelines address the challenge of selecting the appropriate MOSFETs for high-current application. The high-side MOSFET (Q_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both these sums. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of Q_H (reducing $R_{DS(ON)}$ but increasing C_{GATE}). Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of Q_H (increasing $R_{DS(ON)}$ but reducing C_{GATE}). If input voltage does not vary over a wide range, the minimum power dissipation occurs where the

resistive losses equal the switching losses. Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package, and is reasonably priced. Ensure that the DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems can occur.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty cycle extremes. For the high-side MOSFET (Q_H), the worst-case conduction losses occur at the minimum input voltage:

$$P_{Q_H-COND} = \frac{V_{OUT}}{V_{IN(MIN)}} \times I_{OUT}^2 \times R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package-power dissipation often limits how small the MOSFETs can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses.

Calculating the power dissipation in high-side MOSFETs (NH) due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics.

The following switching-loss calculation provides only a very rough estimate and is no substitute for prototype evaluation, preferably including verification using a thermocouple mounted on Q_H:

$$P_{Q_H-SW} = \left(\frac{1}{2} \times \frac{V_{IN(MAX)} I_{LOAD} f_{SW} Q_G}{I_{SWH-SOURCE}}\right) + \left(\frac{1}{2} \times \frac{V_{IN(MAX)} I_{LOAD} f_{SW} Q_{G(SW)}}{I_{SWH-SINK}}\right) + \left(\frac{C_{OSS} V_{IN(MAX)}^2 f_{SW}}{2}\right)$$

where C_{OSS} is the Q_H MOSFET's output capacitance, $Q_{G(SW)}$ is the charge needed to turn on the high-side MOSFET, $I_{DH-SOURCE}$ is the peak gate-drive source current (2A typ), and $I_{DH-SINK}$ is the peak gate-drive sink current (4A typ).

Switching losses in the high-side MOSFET can become an insidious heat problem when the maximum input voltage is applied due to the squared term in the switching-loss equation above. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low input voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (Q_L), the worst-case power dissipation always occurs at the maximum input voltage and is due primarily to conduction losses. Switching losses in the low-side FET are minimal because it is turned on and off when the body diode is conducting and hence under zero-voltage conditions.

$$P_{Q_L-COND} = \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \times I_{OUT}^2 \times R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy load conditions that are greater than $I_{OUT(MAX)}$, but are not quite high enough to exceed the current limit and cause the fault latch to trip. The MOSFETs must have a good-sized heatsink to handle the overload power dissipation. The heatsink can be a large copper field on the PCB or an externally mounted device.

Avoiding dV/dt Turn-On of the Low-Side MOSFET

At high input voltages, fast turn-on of the high-side MOSFET can momentarily turn on the low-side MOSFET due to the high dV/dt appearing at the drain of the low-side MOSFET. The high dV/dt causes a current flow through the Miller capacitance (C_{RSS}) and the input capacitance (C_{ISS}) of the low-side MOSFET. Improper selection of the low-side MOSFET that results in a high ratio of C_{RSS}/C_{ISS} makes the problem more severe. To avoid this problem, minimize the ratio of C_{RSS}/C_{ISS} when selecting the low-side MOSFET. Adding a 1Ω to 4.7Ω resistor in series with the high-side MOSFET gate can slow the high-side MOSFET turn-on. Similarly, adding a small capacitor from the gate to the source of the high-side MOSFET has the same effect. However, both methods work at the expense of increased switching losses (lower efficiency).

Boost Capacitor

The MAX15301AA02 uses a bootstrap circuit to generate the necessary gate-to-source voltage to turn on the high-side MOSFET. The selected n-channel high-side MOSFET determines the appropriate boost capacitance value (C_{BST} in the *Typical Operating Circuit*) according to the following equation:

$$C_{BST} = \frac{QG}{\Delta V_{BST}}$$

where Q_G is the total gate charge of the high-side MOSFET and DV_{BST} is the voltage variation allowed

on the high-side MOSFET driver after turn-on. Choose DV_{BST} such that the available gate-drive voltage is not significantly degraded (e.g. DV_{BST} = 100mV to 300mV) when determining C_{BST}.

For most applications, a 0.22µF low-ESR ceramic capacitor will suffice.

Current Sense

The MAX15301AA02 uses lossless DCR current sensing to reduce the overall power dissipation and improve efficiency. Lossless sensing is configured by connecting a series RC circuit across the inductor as shown in Figure 9. Select the resistor and capacitor such that their time constant is equal to that of the inductor and its DCR:

$$R_L C_L = \frac{L}{DCR}$$

Use the typical inductance and DCR values provided by the inductor manufacturer. The resistor value should be set to 2kΩ. Use high-accuracy and low-tempco C0G ceramic capacitors for C_L. The maximum sense voltage produced using lossless sensing is:

$$V_{DCRP} - V_{DCRN} = DCR \times I_{OUT(MAX)}$$

Choose the DCR so the maximum current-sense voltage is between 10mV and 150mV. A higher current-sense voltage improves the measurement signal-to-noise ratio, but increases power dissipation. Carefully observe the PCB layout guidelines provided in the data sheet to ensure the noise and DC errors do not corrupt the differential current-sense signals seen by DCRP and DCRN. Place the RC network close to the inductor and Kelvin sense the voltage across the capacitor.

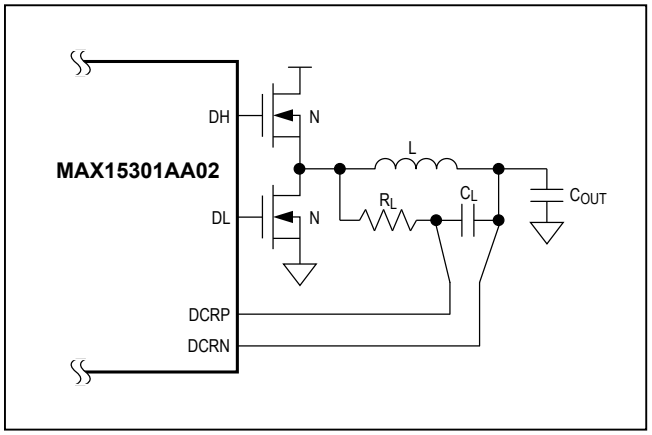


Figure 9. Lossless DCR Current Sensing

More accurate current sensing can be achieved by sensing across a current-sense resistor placed between the inductor and the output capacitors. A dedicated current-sense resistor provides a more accurate resistance and lower tempco than sensing across the inductor. If using a current-sense resistor, connect DCRP to the node between the inductor and the current-sense resistor. Connect DCRN to the node between the current-sense resistor and the output capacitors. Be sure to use Kelvin sensing across the resistor. For accurate current sensing, program the device's IOUT_CAL_GAIN to be equal to the current-sense element's resistance. Note that the default IOUT_CAL_ GAIN is set by the pin-strap resistor connected between ADDR1 and SGND. This default IOUT_CAL_GAIN can be change through the PMBus. If IOUT_CAL_GAIN is not configured to match the actual current-sense resistance, the actual load current is scaled from the measured current by the ratio of IOUT_CAL_GAIN to DCR. In this case, the actual load current is: ILOAD = READ_IOUT x IOUT_CAL_GAIN/DCR As an example, if IOUT_CAL_GAIN is pin strapped to 0.8mΩ, the actual inductor DCR is 1.6mΩ, and a PMBus READ_IOUT command returns 20A; the actual load current is 10A.

Current Limit

The MAX15301AA02 provides current protection utilizing inductor DCR current sense or a current-sense resistor. The details for selecting the current-sense element are described in the previous paragraph. When the measured current equals the IOUT_FAULT_LIMIT, the device acts on the current faults, as defined by the PMBus IOUT_OC_FAULT_RESPONSE setting. For the most accurate current sensing, configure IOUT_CAL_GAIN through the PMBus to equal the current-sense element. If only the pin-strapped values of IOUT_CAL_GAIN are used, select the R_{ADDR1} resistor such that:

$$IOUT\_CAL\_GAIN \geq DCR \times I_{OUT(MAX)} / 25A$$

Output-Voltage Remote Sensing

The MAX15301AA02 uses two dedicated inputs (OUTP and OUTN) for the output differential voltage sensing to reduce the common-mode noise sensitivity. This sensing circuitry is part of the feedback loop. The output voltage is connected to the IC directly through these two inputs without the need for an external resistive divider. The PCB traces to the OUTP and OUTN pins should be routed as a differential pair to the desired regulation sense point to minimize noise induced in the sensed signal. A 100pF to 1000pF capacitor can be placed directly across OUTP to OUTN to minimize noise.

BabyBuck Component Selection

The MAX15301AA02 features an internal DC-DC switching regulator to power internal circuitry and provide the gate-drive voltage for the external MOSFETs. Competing parts with internal driver circuits use linear regulators to provide these voltages which leads to significant efficiency loss when operating from an input voltage above ~6V. The patent-pending BabyBuck circuit improves overall efficiency in a typical application by more than 1% at full load and more than 10% in lightly loaded conditions.

The BabyBuck uses a tiny (1008-size) low current inductor connected across LBI and LBO (Figure 10). A 10µH inductor with a saturation rating of at least 200mA and a 2.2µF ceramic capacitor at GDRV pin is recommended.

In addition to the efficiency improvement from using a DC-DC regulator to power the MOSFETs, the BabyBuck can vary the gate-drive voltage to improve the efficiency over different load current conditions. The variable gate-drive function can be disabled and the gate-drive voltage levels can be modified using PMBus commands.

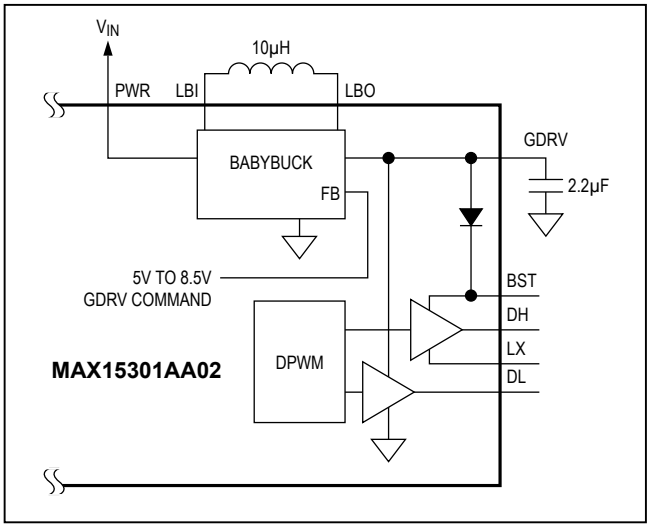


Figure 10. Gate Drivers Powered by Switching Regulator

For applications where efficiency is not critical, the inductor can be omitted and the BabyBuck automatically operates as a linear regulator (Figure 11). In this configuration, bypass GDRV to PGND with a 2.2µF ceramic capacitor and connect LBI to PWR through a 100kΩ resistor. The linear regulator can be bypassed altogether with an external power source. An external 5V to 9V supply can also be applied directly to the GDRV pin to power the gate drivers (Figure 12). Pull LBI up to PWR with a 2kΩ resistor and leave LBO unconnected to allow external gate drive supply.

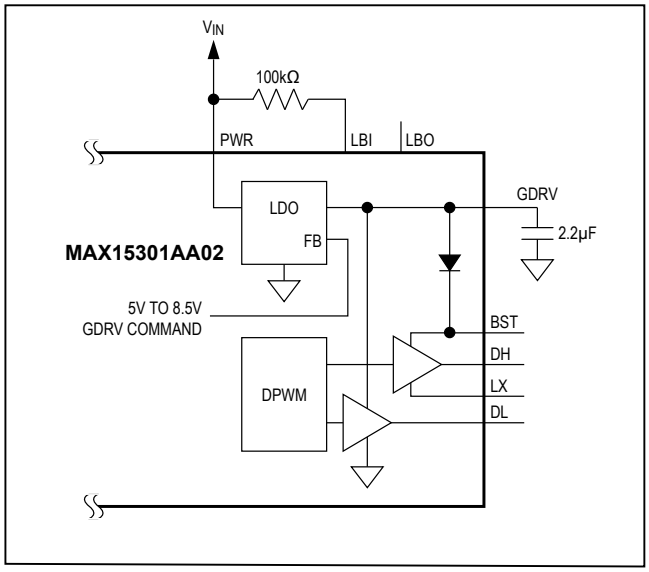


Figure 11. Gate Drivers Powered by Linear Regulator

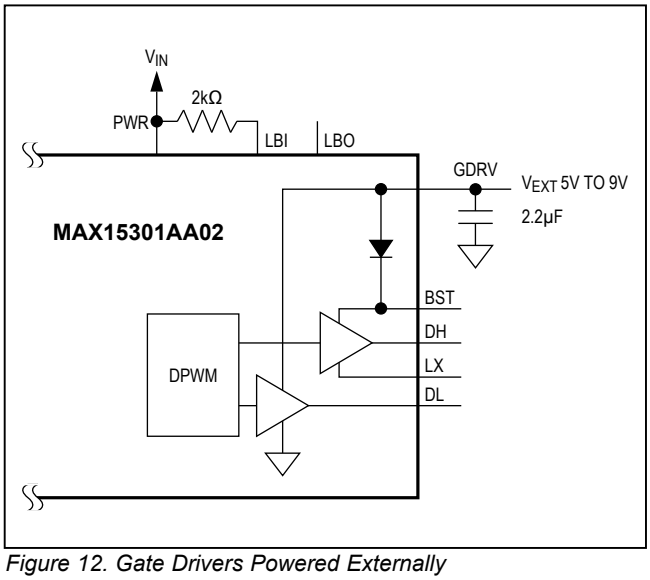


Figure 12. Gate Drivers Powered Externally

Design Examples

See Table 8 for the component values in the *Typical Operating Circuit*. For additional examples and detailed layout information, refer to the MAX15301 evaluation kit.

Applications Information

PCB Layout Guidelines

Careful PCB layout is critical to achieve clean and stable operation. The switching power stage requires particular attention. Follow these guidelines for best thermal performance and signal integrity:

1) When using a resistor to set a command value, connect its return terminal to SGND.
2) Connect the power ground plane (connected to PGND), digital return (connected to DGND), and analog ground plane (SGND) at one point near the device.
3) Bypass GDRV to PGND, 3P3 to SGND, and 1P8 to DGND with ceramic decoupling capacitors. Place the capacitors as close as possible to the pins.
4) Minimize the length of the high-current loop from the input capacitor, the high-side switching MOSFET, and the low-side MOSFET back to the input-capacitor negative terminal.
5) Provide enough copper area at and around the switching MOSFETs and inductors to aid in thermal dissipation. Maintain a good balance between the LX copper area for thermal performance and electromagnetic radiation.
6) Route high-speed switching nodes (BST, LX, DH, and DL) away from sensitive sense inputs (OUTP, OUTN, DCRP, and DCRN).
7) Route the DCRP, DCRN and OUTP, OUTN traces as differential pairs.
8) Connect PGND of the IC as close as possible to the source of the low-side MOSFET.

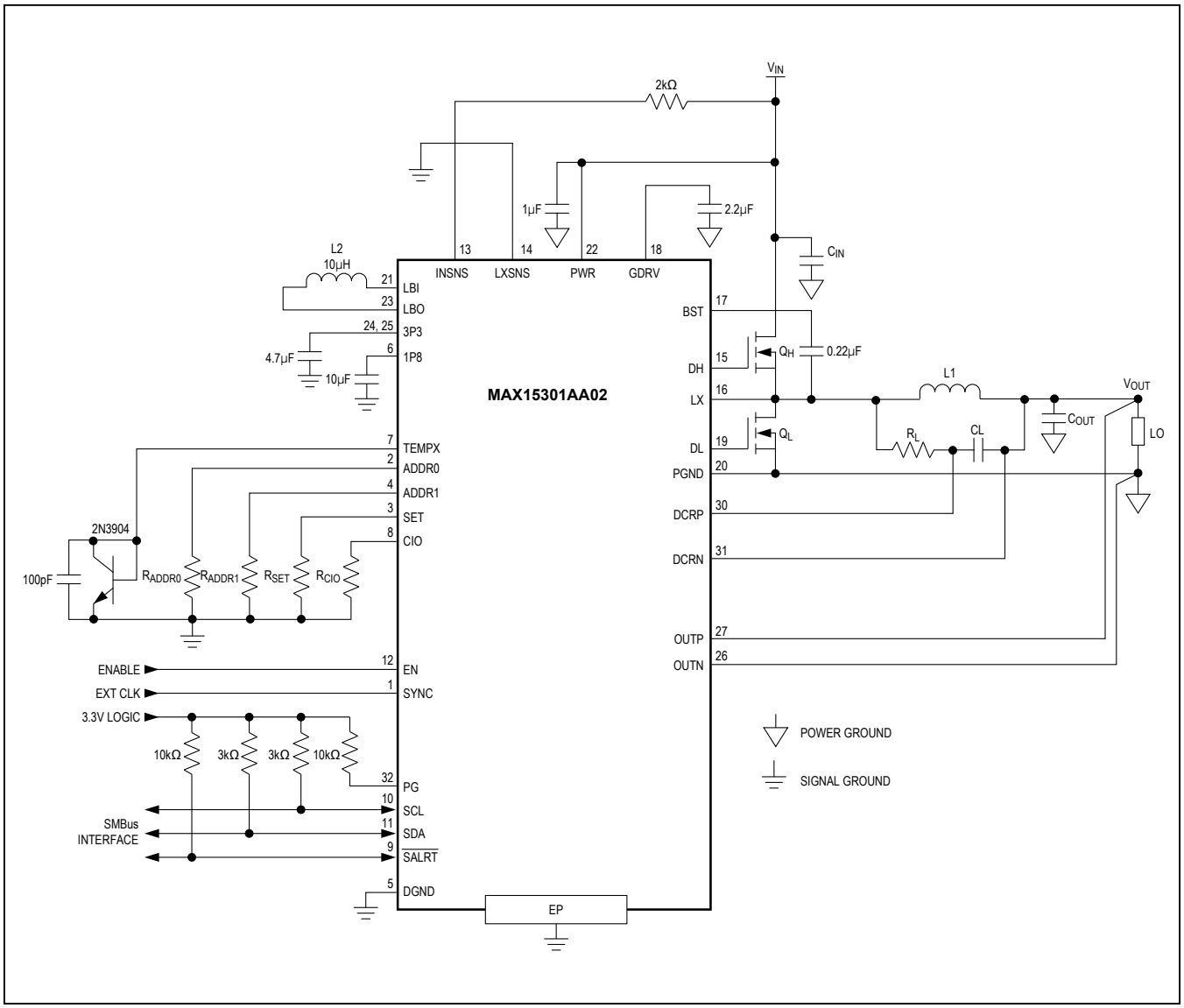
Table 8. Typical Component Values

COMPONENT	APPLICATION 1	APPLICATION 2	APPLICATION 3
Input Supply	12V	12V	12V
Output Voltage	1.0V	3.3V	1.0V
R_{SET}	14.7kΩ	51.1kΩ	14.7kΩ
Output Current	20A	12A	35A
R_{ADDR1}	2.15, 5.11, 6.19, 7.15, or 8.25kΩ	21.5, 26.1, 31.6, 38.3, or 44.2kΩ	2.15, 5.11, 6.19, 7.15, or 8.25kΩ
R_{ADDR0}	User defined (see Table 4a)	User defined (see Table 4a)	User defined (see Table 4a)
Switching Frequency	750kHz	600kHz	850kHz
R_{SYNC}	21.5kΩ	12.7kΩ	31.6kΩ
Inductor L1	Würth 744308033, 330nH, 370µΩ	Würth 744332082, 820nH, 1.17mΩ	Coilcraft SLC1049-125
Inductor L2	TDK NLCV25T-100K-PF, 10µH	TDK NLCV25T-100K-PF, 10µH	TDK NLCV25T-100K-PF, 10µH
R_{FILTER}	665Ω	634Ω	2.10kΩ
C_{FILTER}	1µF	1µF	0.22µF
High-Side MOSFET	CSD86350Q5D, (5mm x 6mm)	FDPC8011S, 7.3mΩ	Infineon BSC032NE2LS, 3.2mΩ (5mm x 6mm)
Low-Side MOSFET	as above (MOSFET pair)	as above (MOSFET pair), 2.1mΩ	Infineon BSC010NE2LS, 1.0mΩ (5mm x 6mm)
Output Capacitance	5 x 100µF, X5R, 1206, 6.3V	3 x 100µF, X5R, 1206, 6.3V	10 x 100µF, X5R, 1206, 6.3V
Input Capacitance	3 x 47µF, X5R, 1210, 16V	1 x 47µF, X5R, 1210, 16V	4 x 47µF, X5R, 1210, 16V

Thermal Layout

The MAX15301AA02 is available in a small 5mm x 5mm TQFN package with exposed pad to remove heat from the internal semiconductor junctions. The exposed pad must be soldered to the copper on the PCB directly underneath the device package reducing the θ_{JA} down to approximately 40°C/W. The IC will shut down if its temperature increases beyond +115°C. (This threshold can be changed using a PMBus command). An evaluation kit is available that demonstrates the recommended layout practices for the MAX15301AA02.

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	FIRMWARE
MAX15301AA02+CJK	-40°C to +85°C	32 TQFN-EP*	4328
MAX15301AA02+TCJK	-40°C to +85°C	32 TQFN-EP*	4328

Note: *Refer to User Guide 5793: MAX15301 PMBus Command Set User's Guide for more information on the differences between MAX15301 IC firmware options.*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255M+5	21-0140	90-0013

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/15	Initial release	—

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View MAX15301AA02+CJK on WIN SOURCE
- Maxim Integrated Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management