WINSOURCE ELECTRONICS

# THE DATASHEET OF

# S29PL127J70BAI020

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**S29PL-J**

# 128-/64-/32-Mbit (8/4/2M × 16-Bit), 3 V, Flash with Enhanced VersatileIO™

## Distinctive Characteristics

### Architectural Advantages

- 128-/64-/32-Mbit Page Mode devices
  - Page size of 8 words: Fast page read access from random locations within the page
- Single power supply operation
  - Full Voltage range: 2.7 to 3.6 V read, erase, and program operations for battery-powered applications
- Simultaneous Read/Write Operation
  - Data can be continuously read from one bank while executing erase/program functions in another bank
  - Zero latency switching from write to read operations
- FlexBank Architecture (PL127J/PL064J/PL032J)
  - 4 separate banks, with up to two simultaneous operations per device
  - Bank A:
    PL127J -16 Mbit (4 Kw × 8 and 32 Kw × 31)
    PL064J - 8 Mbit (4 Kw × 8 and 32 Kw × 15)
    PL032J - 4 Mbit (4 Kw × 8 and 32 Kw × 7)
  - Bank B:
    PL127J - 48 Mbit (32 Kw × 96)
    PL064J - 24 Mbit (32 Kw × 48)
    PL032J - 12 Mbit (32 Kw × 24)
  - Bank C:
    PL127J - 48 Mbit (32 Kw × 96)
    PL064J - 24 Mbit (32 Kw × 48)
    PL032J - 12 Mbit (32 Kw × 24)
  - Bank D:
    PL127J -16 Mbit (4 Kw × 8 and 32 Kw × 31)
    PL064J - 8 Mbit (4 Kw × 8 and 32 Kw × 15)
    PL032J - 4 Mbit (4 Kw × 8 and 32 Kw × 7)
- Enhanced VersatileI/O™ ($V_{IO}$) Control
  - Output voltage generated and input voltages tolerated on all control inputs and I/Os is determined by the voltage on the $V_{IO}$ pin
  - $V_{IO}$ options at 1.8 V and 3 V I/O for PL127J devices
  - 3V $V_{IO}$ for PL064J and PL032J devices
- Secured Silicon Sector region
  - Up to 128 words accessible through a command sequence
  - Up to 64 factory-locked words
  - Up to 64 customer-lockable words
- Both top and bottom boot blocks in one device
- Manufactured on 110-nm process technology
- Data Retention: 20 years typical
- Cycling Endurance: 1 million cycles per sector typical

### Performance Characteristics

- High Performance
  - Page access times as fast as 20 ns
  - Random access times as fast as 55 ns
- Power consumption (typical values at 10 MHz)
  - 45 mA active read current
  - 17 mA program/erase current
  - 0.2 µA typical standby mode current

### Software Features

- Software command-set compatible with JEDEC 42.4 standard
  - Backward compatible with Am29F, Am29LV, Am29DL, and AM29PDL families and MBM29QM/RM, MBM29LV, MBM29DL, MBM29PDL families
- CFI (Common Flash Interface) compliant
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- Erase Suspend / Erase Resume
  - Suspends an erase operation to allow read or program operations in other sectors of same bank
- Program Suspend / Program Resume
  - Suspends a program operation to allow read operation from sectors other than the one being programmed
- Unlock Bypass Program command
- Reduces overall programming time when issuing multiple program command sequences

### Hardware Features

- Ready/Busy# pin (RY/BY#)
  - Provides a hardware method of detecting program or erase cycle completion
- Hardware reset pin (RESET#)
  - Hardware method to reset the device to reading array data
- WP#/ ACC (Write Protect/Acceleration) input
  - At $V_{IL}$, hardware level protection for the first and last two 4K word sectors.
  - At $V_{IH}$, allows removal of sector protection
  - At $V_{HH}$, provides accelerated programming in a factory setting
- Persistent Sector Protection
  - A command sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector
  - Sectors can be locked and unlocked in-system at $V_{CC}$ level

- Password Sector Protection
  - A sophisticated sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector using a user-defined 64-bit password

- Package Options
  - 11 × 8 mm, 80-ball Fine-pitch BGA (PL127J) (VBG080) 8.15 × 6.15 mm, 48-ball Fine pitch BGA (PL064J/PL032J) (VBK048)
  - 20 × 14 mm, 56-pin TSOP (PL127J) (TS056)

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# 1. General Description

The PL127J/PL064J/PL032J is a 128/128/64/32 Mbit, 3.0 V-only Page Mode and Simultaneous Read/Write Flash memory device organized as 8/8/4/2 Mwords.

The devices are offered in the following packages:

- 11 mm × 8 mm, 80-ball Fine-pitch BGA standalone (PL127J)
- 8 mm × 11.6 mm, 64-ball Fine-pitch BGA multi-chip compatible (PL127J)
- 8.15 mm × 6.15 mm, 48-ball Fine-pitch BGA standalone (PL064J/PL032J)
- 7 mm × 9 mm, 56-ball Fine-pitch BGA multi-chip compatible (PL064J and PL032J)
- 20 mm × 14 mm, 56-pin TSOP (PL127J)

The word-wide data (x16) appears on DQ15-DQ0. This device can be programmed in-system or in standard EPROM programmers. A 12.0 V $V_{PP}$ is not required for write or erase operations.

# 2. Simultaneous Read/Write Operation with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into 4 banks, which can be considered to be four separate memory arrays as far as certain operations are concerned. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from another bank with zero latency (with two simultaneous operations operating at any one time). This releases the system from waiting for the completion of a program or erase operation, greatly improving system performance.

The device can be organized in both top and bottom sector configurations. The banks are organized as shown in Table 1.

**Table 1. Bank Organization**

| Bank | PL127J Sectors | PL064J Sectors | PL032J Sectors |
|---|---|---|---|
| A | 16 Mbit (4 Kw × 8 and 32 Kw × 31) | 8 Mbit (4 Kw × 8 and 32 Kw × 15) | 4 Mbit (4 Kw × 8 and 32 Kw × 7) |
| B | 48 Mbit (32 Kw × 96) | 24 Mbit (32 Kw × 48) | 12 Mbit (32 Kw × 24) |
| C | 48 Mbit (32 Kw × 96) | 24 Mbit (32 Kw × 48) | 12 Mbit (32 Kw × 24) |
| D | 16 Mbit (4 Kw x 8 and 32 Kw × 31) | 8 Mbit (4 Kw × 8 and 32 Kw × 15) | 4 Mbit (4 Kw × 8 and 32 Kw × 7) |

## 2.1 Page Mode Features

The page size is 8 words. After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page.

## 2.2 Standard Flash Memory Features

The device requires a **single 3.0 volt power supply** (2.7 V to 3.6 V) for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC 42.4 single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. The Unlock Bypass mode facilitates faster programming times by requiring only two write cycles to program data instead of four. Device erasure occurs by executing the erase command sequence.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

**Hardware data protection** measures include a low $V_{CC}$ detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

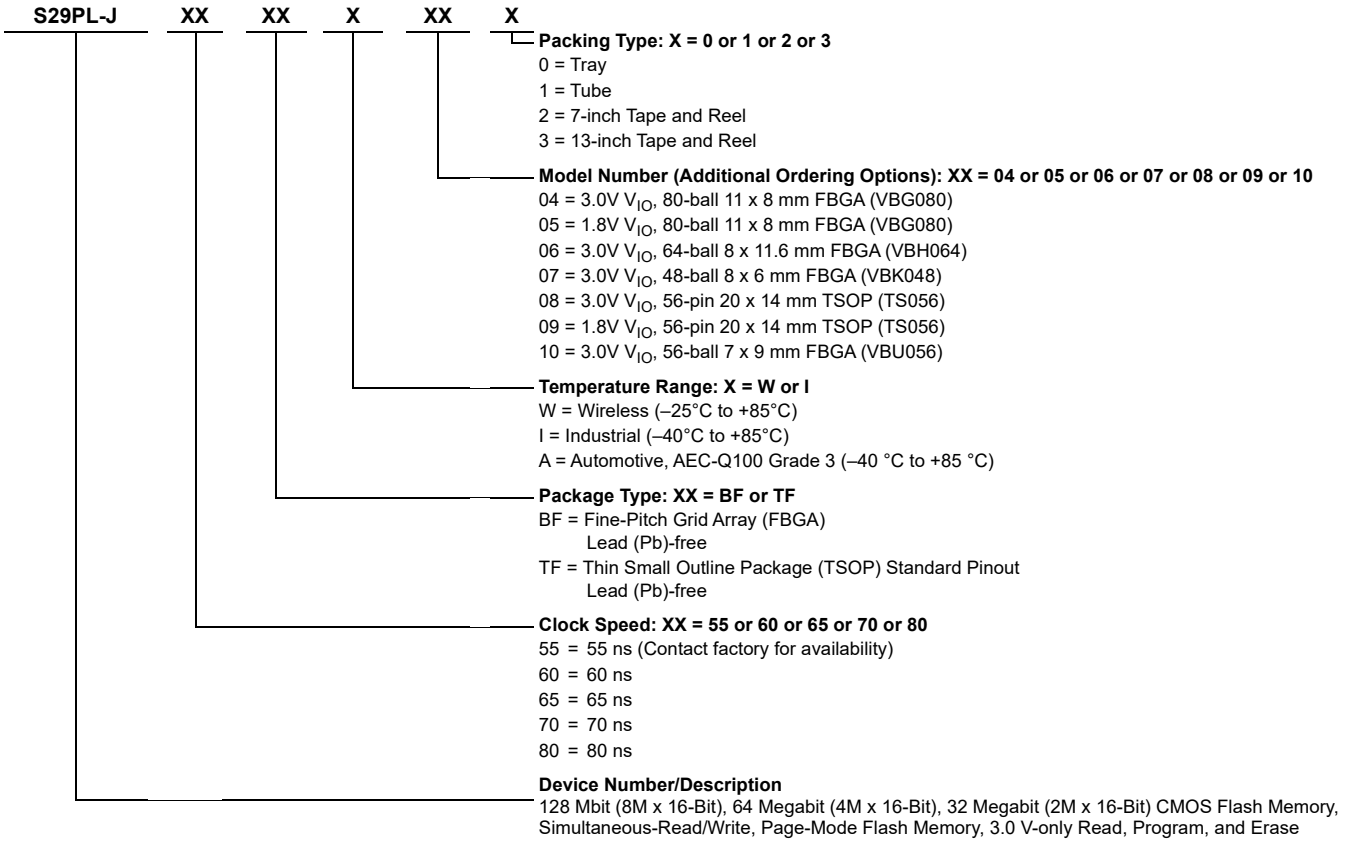
**The Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the Secured Silicon Sector area (One Time Program area) after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The **Program Suspend/Program Resume** feature enables the user to hold the program operation to read data from any sector that is not selected for programming. If a read is needed from the Secured Silicon Sector area, Persistent Protection area, Dynamic Protection area, or the CFI area, after a program suspend, then the user must use the proper command sequence to enter and exit this region.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the standby mode. Power consumption is greatly reduced in both these modes. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

# 3. Ordering Information

The order number (Valid Combination) is formed by a valid combinations of the following:



## 3.1 Valid Combinations - Standard

Valid Combinations list configurations planned to be supported in volume for this device. Contact your local sales office to confirm availability of specific valid combinations.

**Table 2. Standard 128 Mb Products Based on 110 nm Floating Gate Technology**

| Device Number/ Description | Speed (ns) | Package Type | Temperature Range | Additional Ordering Options |
|---|---|---|---|---|
| S29PL127J | 60, 65, 70 | BF, TF | W, I | 04, 06, 08 |
| S29PL127J | 80 | BF | W, I | 05 |
| S29PL127J | 80 | TF | W, I | 09 |

**Table 3. Standard 64 Mb Products Based on 110 nm Floating Gate Technology**

| Device Number /Description | Speed (ns) | Package Type | Temperature Range | Additional Ordering Options |
|---|---|---|---|---|
| S29PL064J | 55, 60, 70 | BF | W, I | 07, 10 |

**Table 4. Standard 32 Mb Products Based on 110 nm Floating Gate Technology**

| Device Number /Description | Speed (ns) | Package Type | Temperature Range | Additional Ordering Options |
|---|---|---|---|---|
| S29PL032J | 55, 60, 70 | BF | W, I | 07, 10 |

**Table 5. Standard Valid Combinations for BGA Packages[1]**

| Order Number | Speed (ns) | $V_{IO}$ Range |
|---|---|---|
| PL127J,PL064J, PL032J | 55, 60, 65, 70[2] | 2.7–3.6 |
| PL127J | 80 | 1.65–1.95 |

**Notes**
1. BGA package marking omits leading S29 and packing type designator from ordering part number.
2. 55 ns speed only supported for PL032J and PL127J.

**Table 6. Standard Valid Combinations for TSOP Packages[3]**

| Order Number | Speed (ns) | $V_{IO}$ Range |
|---|---|---|
| S29PL127J | 60, 70 | 2.7–3.6 |

**Note**
3. TSOP package markings omit packing type designator from ordering part number.

## 3.2 Valid Combinations - Automotive Grade / AEC-Q100

The table below lists configurations that are Automotive Grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Contact your local sales representative to confirm availability of specific combinations and to check on newly released combinations. Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products. Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements. AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

**Table 7. Automotive 128 Mb Products Based on 110 nm Floating Gate Technology**

| Device Number/ Description | Speed (ns) | Package Type | Temperature Range | Additional Ordering Options |
|---|---|---|---|---|
| S29PL127J | 60, 65, 70 | BF, TF | A | 04, 06, 08 |
| S29PL127J | 80 | BF | A | 05 |
| S29PL127J | 80 | TF | A | 09 |

**Table 8. Automotive 64 Mb Products Based on 110 nm Floating Gate Technology**

| Device Number /Description | Speed (ns) | Package Type | Temperature Range | Additional Ordering Options |
|---|---|---|---|---|
| S29PL064J | 55, 60, 70 | BF | A | 07, 10 |

**Table 9. Automotive 32 Mb Products Based on 110 nm Floating Gate Technology**

| Device Number /Description | Speed (ns) | Package Type | Temperature Range | Additional Ordering Options |
|---|---|---|---|---|
| S29PL032J | 55, 60, 70 | BF | A | 07, 10 |

**Table 10. Automotive Valid Combinations for BGA Packages**[4]

| Order Number | Speed (ns) | $V_{IO}$ Range |
|---|---|---|
| PL127J,PL064J, PL032J | 55, 60, 65, 70[5] | 2.7–3.6 |
| PL127J | 80 | 1.65–1.95 |

**Notes**
4. BGA package marking omits leading S29 and packing type designator from ordering part number.
5. 55 ns speed only supported for PL032J and PL127J.

**Table 11. Automotive Valid Combinations for TSOP Packages**[6]

| Order Number | Speed (ns) | $V_{IO}$ Range |
|---|---|---|
| S29PL127J | 60, 70 | 2.7–3.6 |

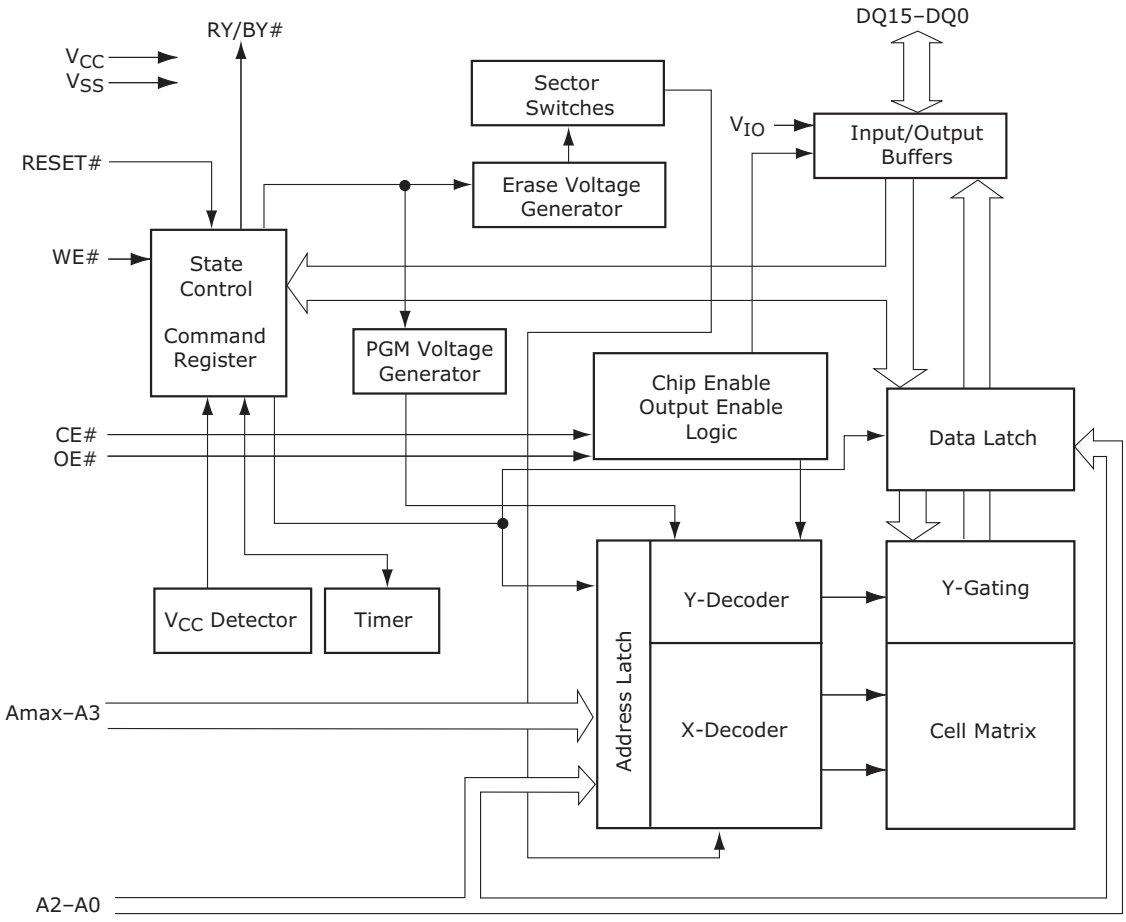
**Note**
6. TSOP package markings omit packing type designator from ordering part number.

# 4. Product Selector Guide

| Part Number → | | S29PL032J/S29PL064J/S29PL0127J | | | | |
|---|---|---|---|---|---|---|
| Speed Option | $V_{CC}$,$V_{IO}$ = 2.7 V – 3.6 V | 55[7] | 60 | 65 | — | 70 |
| | $V_{CC}$ = 2.7 V – 3.6 V, $V_{IO}$ = 1.65 V – 1.95 V (PL127J) | — | — | — | 80 | — |
| Max Access Time, ns ($t_{ACC}$) | | 55[7] | 60 | 65 | 80 | 70 |
| Max CE# Access, ns ($t_{CE}$) | | | | | | |
| Max Page Access, ns ($t_{PACC}$) | | 20[7] | 25 | | 30 | 30 |
| Max OE# Access, ns ($t_{OE}$) | | | | | | |

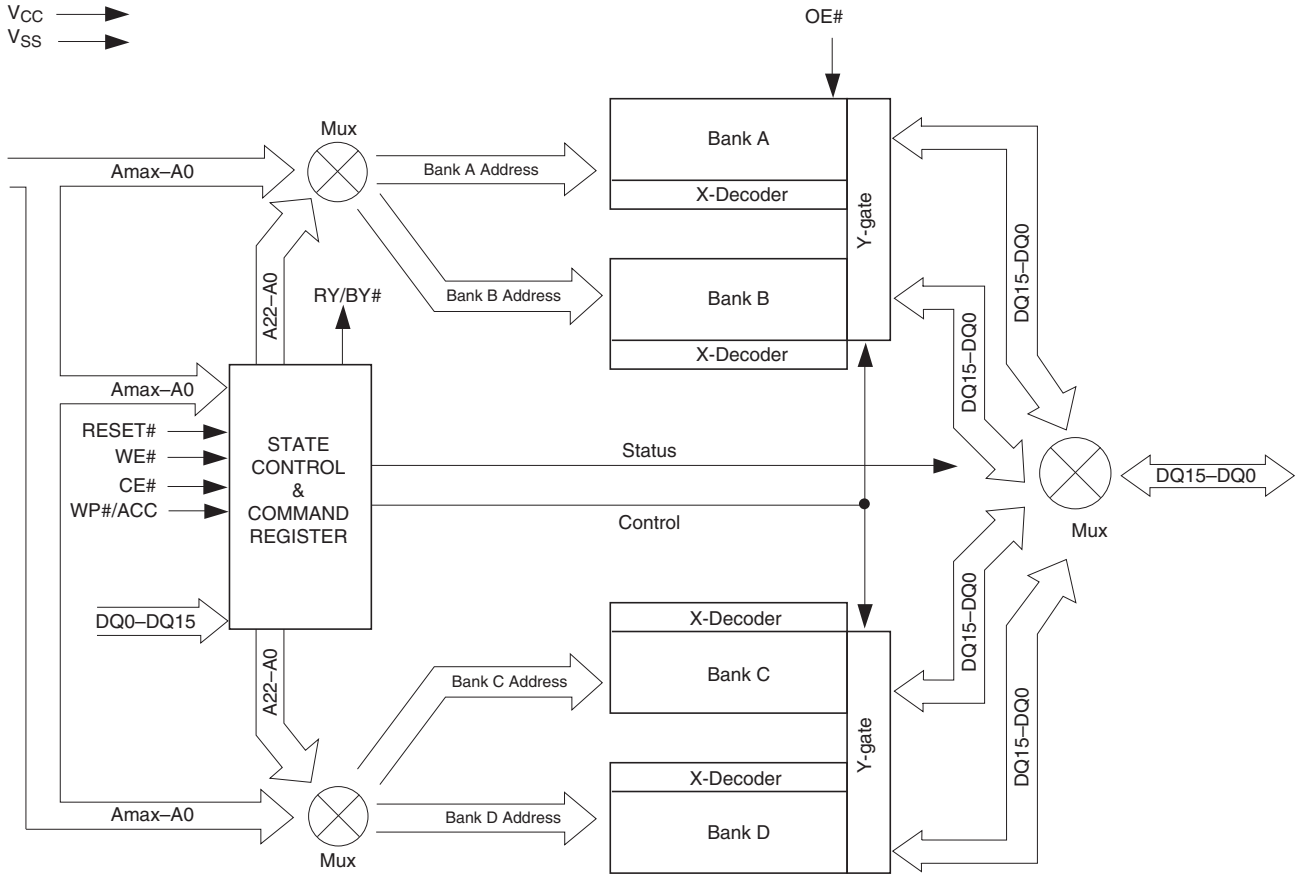
**Note**
7. 55 ns speed bin only supported for PL032J and PL064J.

# 5. Block Diagram




**Notes**
8. RY/BY# is an open drain output.
9. Amax = A22 (PL127J), A21 (PL064J), A20 (PL032J).

# 6. Simultaneous Read/Write Block Diagram




**Note**
10. Amax = A22 (PL127J), A21 (PL064J), A20 (PL032J).

# 7. Connection Diagrams

## 7.1 Special Package Handling Instructions

### 7.1.1 TSOP, BGA, PDIP, SSOP, and PLCC Packages

Special handling is required for Flash Memory products in molded packages.

The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

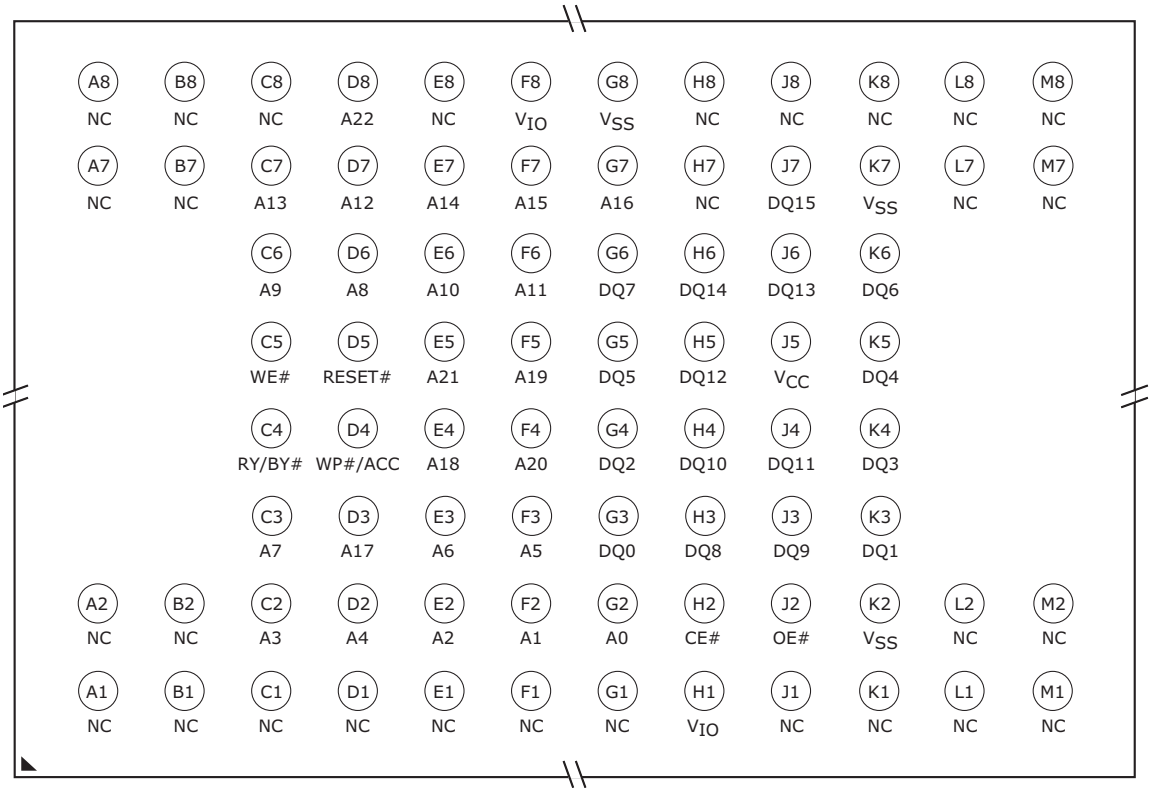
### 7.1.2 FBGA Packages

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

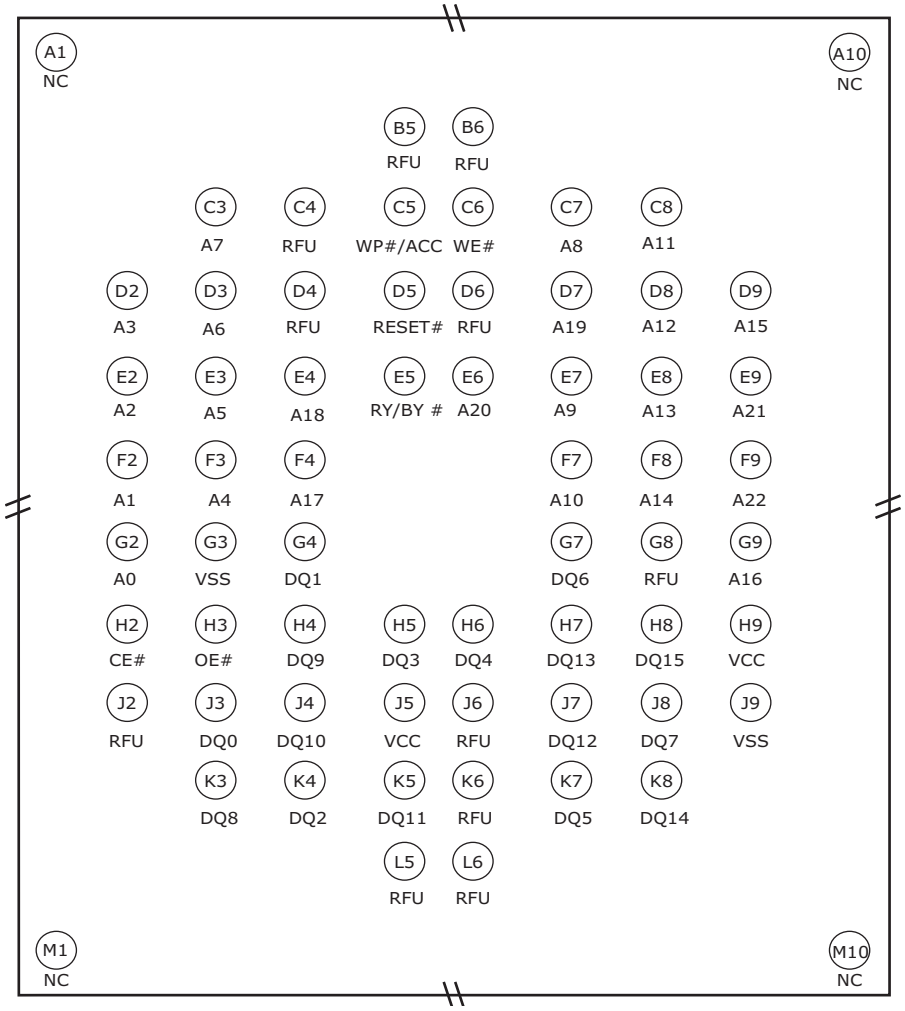
## 7.2 80-Ball Fine-Pitch BGA—PL127J

**Figure 1. 80-Ball Fine-Pitch BGA, Top View, Balls Facing Down—PL127J**



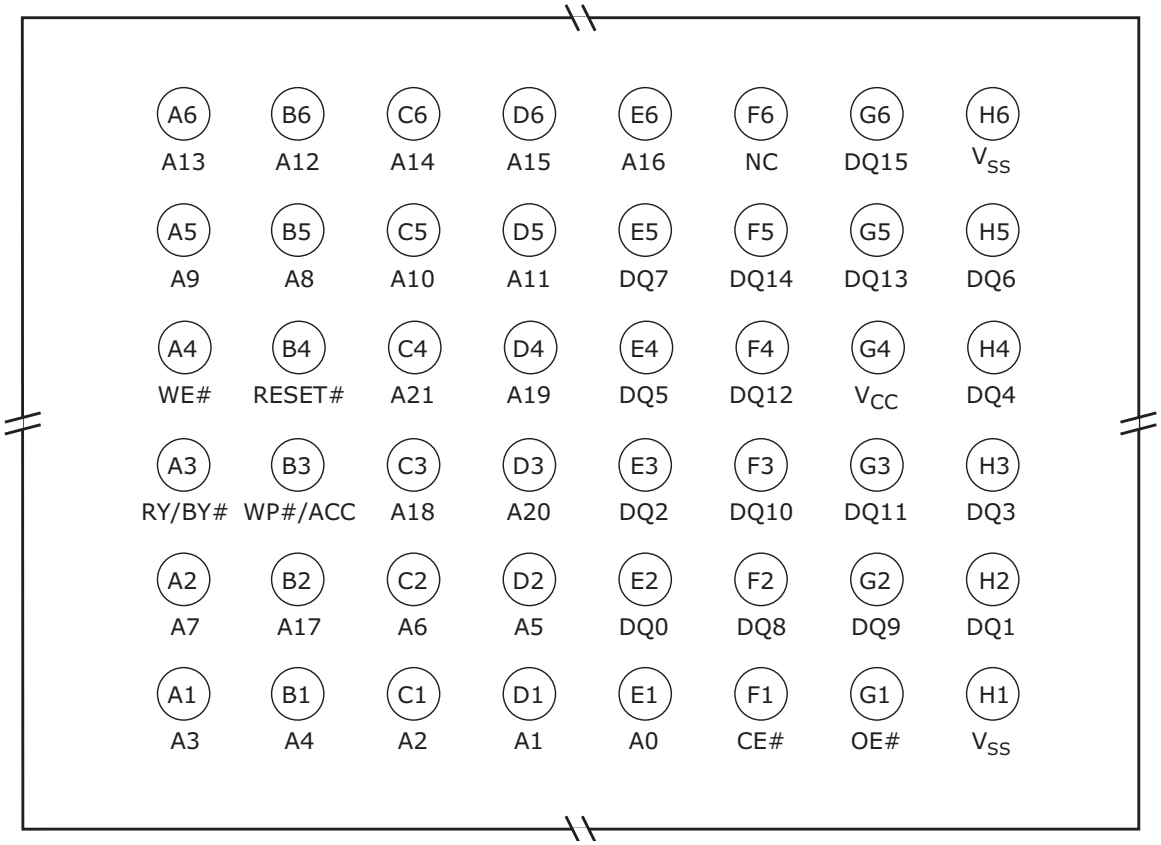
## 7.3 64-Ball Fine-Pitch BGA—PL127J

**Figure 2. 64-Ball Fine-Pitch BGA, Top View, Balls Facing Down—PL127J**



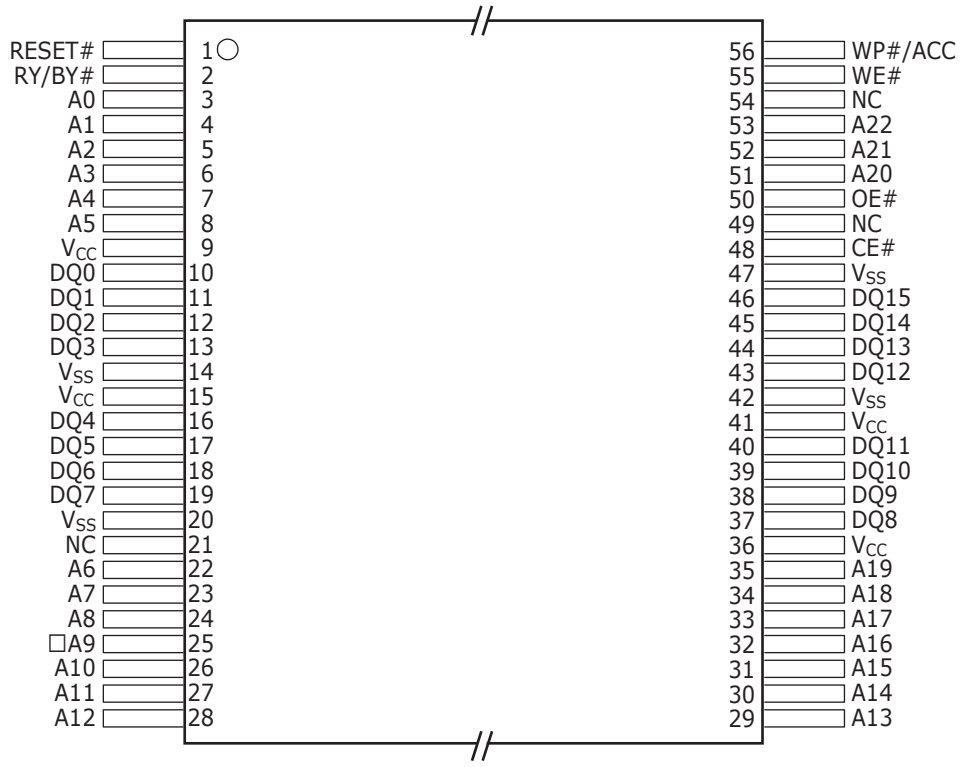
## 7.4 48-Ball Fine-Pitch BGA, PL064J and PL032J

**Figure 3. 48-Ball Fine-Pitch BGA, Top View, Balls Facing Down—PL064J—PL032J: C4(A21)=NC**



## 7.5 56-Pin TSOP 20 x 14 mm

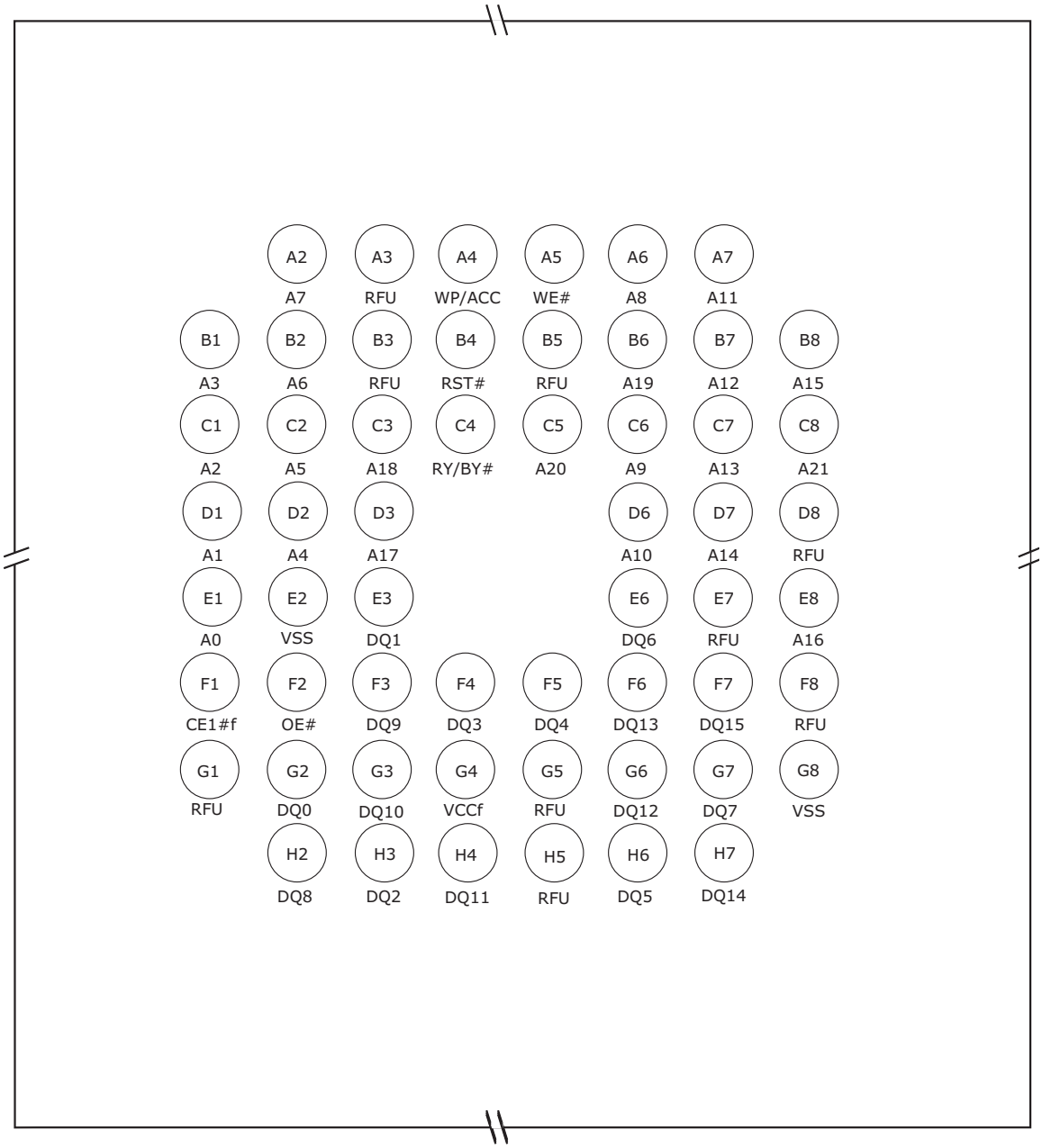
**Figure 4. 56-Pin TSOP 20 x 14 mm Configuration—PL127J**




For this family of products, a single multi-chip compatible package (TSOP) is offered for each density to allow both standalone and multi-chip qualification using a single, adaptable package. This new methodology allows package standardization resulting in faster development. The multi-chip compatible package includes all the pins required for standalone device operation and verification. In addition, extra pins are included for insertion of common data storage or logic devices to be used for multi-chip products. If a standalone device is required, the extra multi-chip specific pins are not connected and the standalone device operates normally. The multi-chip compatible package sizes were chosen to serve the largest number of combinations possible. There are only a few cases where a larger package size would be required to accommodate the multi-chip combination. This multi-chip compatible package set does not allow for direct package migration from the Am29BDS128H, Am29BDS128G, Am29BDS640G products, which use legacy standalone packages.

## 7.6 56-Ball Fine-Pitch Ball Grid Array, PL064J and PL032J

**Figure 5. 56-ball Fine-Pitch BGA, Top View, Balls Facing Down—PL064J and PL032J**



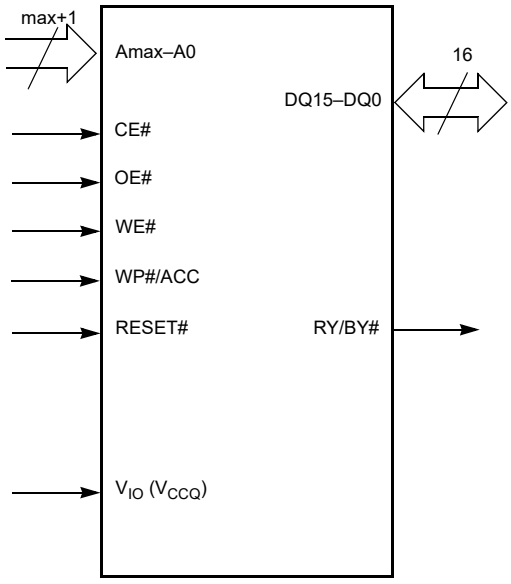
# 8. Pin Description

**Table 12. Pin Description**

| Pin Name | Description |
|---|---|
| Amax–A0 | Address bus |
| DQ15–DQ0 | 16-bit data inputs/outputs/float |
| CE# | Chip Enable Inputs |
| OE# | Output Enable Input |
| WE# | Write Enable |
| $V_{SS}$ | Device Ground |
| NC | Not Connected. No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). |
| RFU | Reserved for Future Use. Not currently connected internally but the pin/ball location should be left unconnected and unused by PCB routing channel for future compatibility. The pin/ball may be used by a signal in the future. |
| RY/BY# | Ready/Busy output and open drain.<br>When RY/BY#= $V_{IH}$, the device is ready to accept read operations and commands. When RY/BY#= $V_{OL}$, the device is either executing an embedded algorithm or the device is executing a hardware reset operation. |
| WP#/ACC | Write Protect/Acceleration Input.<br>When WP#/ACC= $V_{IL}$, the highest and lowest two 4K-word sectors are write protected regardless of other sector protection configurations. When WP#/ACC= $V_{IH}$, these sector are unprotected unless the DYB or PPB is programmed. When WP#/ACC= $V_{HH}$, program and erase operations are accelerated. |
| $V_{IO}$ | Input/Output Buffer Power Supply<br>(1.65 V to 1.95 V (for PL127J) or 2.7 V to 3.6 V (for all PLxxxJ devices)) |
| $V_{CC}$ | Chip Power Supply (2.7 V to 3.6 V or 2.7 to 3.3 V) |
| RESET# | Hardware Reset Pin |

**Note**
11. Amax = A22 (PL127J), A21 (PL064J), A20 (PL032J).

# 9. Logic Symbol



# 10. Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 13 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

**Table 13. PL127J Device Bus Operations**

| Operation | CE# | OE# | WE# | RESET# | WP#/ACC | Addresses (Amax–A0) | DQ15–DQ0 |
|---|---|---|---|---|---|---|---|
| Read | L | L | H | H | X | $A_{IN}$ | $D_{OUT}$ |
| Write | L | H | L | H | X[13] | $A_{IN}$ | $D_{IN}$ |
| Standby | $V_{IO}$±0.3 V | X | X | $V_{IO}$ ±0.3 V | X[13] | X | High-Z |
| Output Disable | L | H | H | H | X | X | High-Z |
| Reset | X | X | X | L | X | X | High-Z |
| Temporary Sector Unprotect (High Voltage) | X | X | X | $V_{ID}$ | X | $A_{IN}$ | $D_{IN}$ |

**Legend**
L = Logic Low = $V_{IL}$, H = Logic High = $V_{IH}$, $V_{ID}$ = 11.5–12.5 V, $V_{HH}$ = 8.5–9.5 V, X = Don't Care, SA = Sector Address, $A_{IN}$ = Address In, $D_{IN}$ = Data In, $D_{OUT}$ = Data Out

## 10.1 Requirements for Reading Array Data

To read array data from the outputs, the system must drive the OE# and appropriate CE# pins to $V_{IL}$. CE# is the power control. OE# is the output control and gates array data to the output pins. WE# should remain at $V_{IH}$.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

Refer to Table 34 on page 61 for timing specifications and to Figure 16 on page 62 for the timing diagram. $I_{CC1}$ in the DC Characteristics table represents the active current specification for reading array data.

### 10.1.1 Random Read (Non-Page Read)

Address access time ($t_{ACC}$) is equal to the delay from stable addresses to valid output data. The chip enable access time ($t_{CE}$) is the delay from the stable addresses and stable CE# to valid data at the output inputs. The output enable access time is the delay from the falling edge of the OE# to valid data at the output inputs (assuming the addresses have been stable for at least $t_{ACC}$–$t_{OE}$ time).

### 10.1.2 Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. Address bits Amax–A3 select an 8 word page, and address bits A2–A0 select a specific word within that page. This is an asynchronous operation with the microprocessor supplying the specific word location.

The random or initial page access is $t_{ACC}$ or $t_{CE}$ and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to $t_{PACC}$. When CE# is deasserted (=$V_{IH}$), the reassertion of CE# for subsequent access has access time of $t_{ACC}$ or $t_{CE}$. Here again, CE# selects the device and OE# is the output control and should be used to gate data to the output inputs if the device is selected. Fast page mode accesses are obtained by keeping Amax–A3 constant and changing A2–A0 to select the specific word within that page.

**Notes**
12. The sector protect and sector unprotect functions may also be implemented via programming equipment. See *High Voltage Sector Protection* on page 35.
13. WP#/ACC must be high when writing to upper two and lower two sectors.

**Table 14. Page Select**

| Word | A2 | A1 | A0 |
|---|---|---|---|
| Word 0 | 0 | 0 | 0 |
| Word 1 | 0 | 0 | 1 |
| Word 2 | 0 | 1 | 0 |
| Word 3 | 0 | 1 | 1 |
| Word 4 | 1 | 0 | 0 |
| Word 5 | 1 | 0 | 1 |
| Word 6 | 1 | 1 | 0 |
| Word 7 | 1 | 1 | 1 |

## 10.2 Simultaneous Read/Write Operation

In addition to the conventional features (read, program, erase-suspend read, erase-suspend program, and program-suspend read), the device is capable of reading data from one bank of memory while a program or erase operation is in progress in another bank of memory (simultaneous operation). The bank can be selected by bank addresses (PL127J: A22–A20, PL064J: A21–A19, PL032J: A20–A18) with zero latency.

The simultaneous operation can execute multi-function mode in the same bank.

**Table 15. Bank Select**

| Bank | PL127J: A22–A20, PL064J: A21–A19, PL032J: A20–A18 |
|---|---|
| Bank A | 000 |
| Bank B | 001, 010, 011 |
| Bank C | 100, 101, 110 |
| Bank D | 111 |

## 10.3 Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to $V_{IL}$, and OE# to $V_{IH}$.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four. Section 15.5 Word Program Command Sequence on page 44 has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 15 indicates the set of address space that each sector occupies. A “bank address” is the set of address bits required to uniquely select a bank. Similarly, a “sector address” refers to the address bits required to uniquely select a sector. Section 15. Command Definitions on page 43 has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

$I_{CC2}$ in the Section 19. DC Characteristics on page 59 represents the active current specification for the write mode. See the timing specification tables and timing diagrams in section Section 20.4 Reset on page 63 for write operations.

### 10.3.1 Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts $V_{HH}$ on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing $V_{HH}$ from the WP#/ACC pin returns the device to normal operation. *Note that $V_{HH}$ must not be asserted on WP#/ACC for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin should be raised to $V_{CC}$ when not in use. That is, the WP#/ACC pin should not be left floating or unconnected; inconsistent behavior of the device may result.*

### 10.3.2 Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ15–DQ0. Standard read cycle timings apply in this mode. Refer to the Table 19 on page 27 and Section 15.3 Autoselect Command Sequence on page 43 for more information.

## 10.4 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{IO}$ ± 0.3 V. (Note that this is a more restricted voltage range than $V_{IH}$.) If CE# and RESET# are held at $V_{IH}$, but not within $V_{IO}$ ± 0.3 V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time ($t_{CE}$) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

ICC3 in Section 19. DC Characteristics on page 59 represents the CMOS standby current specification.

## 10.5 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for $t_{ACC}$ + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Note that during automatic sleep mode, OE# must be at $V_{IH}$ before the device reduces current to the stated sleep mode specification. $I_{CC5}$ in Section 19. DC Characteristics on page 59 represents the automatic sleep mode current specification.

## 10.6 RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of $t_{RP}$, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS}$±0.3 V, the device draws CMOS standby current (ICC4). If RESET# is held at $V_{IL}$ but not within $V_{SS}$±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of $t_{READY}$ (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of $t_{READY}$ (not during Embedded Algorithms). The system can read data $t_{RH}$ after the RESET# pin returns to $V_{IH}$.

Refer to the tables in Section 20. AC Characteristics on page 60 for RESET# parameters and to Figure 18 on page 63 for the timing diagram.

## 10.7 Output Disable Mode

When the OE# input is at $V_{IH}$, output from the device is disabled. The output pins (except for RY/BY#) are placed in the highest Impedance state.

**Table 16. PL127J Sector Architecture**

| Bank | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|---|---|---|---|---|
| Bank A | SA0 | 00000000000 | 4 | 000000h–000FFFh |
| | SA1 | 00000000001 | 4 | 001000h–001FFFh |
| | SA2 | 00000000010 | 4 | 002000h–002FFFh |
| | SA3 | 00000000011 | 4 | 003000h–003FFFh |
| | SA4 | 00000000100 | 4 | 004000h–004FFFh |
| | SA5 | 00000000101 | 4 | 005000h–005FFFh |
| | SA6 | 00000000110 | 4 | 006000h–006FFFh |
| | SA7 | 00000000111 | 4 | 007000h–007FFFh |
| | SA8 | 00000001XXX | 32 | 008000h–00FFFFh |
| | SA9 | 00000010XXX | 32 | 010000h–017FFFh |
| | SA10 | 00000011XXX | 32 | 018000h–01FFFFh |
| | SA11 | 00000100XXX | 32 | 020000h–027FFFh |
| | SA12 | 00000101XXX | 32 | 028000h–02FFFFh |
| | SA13 | 00000110XXX | 32 | 030000h–037FFFh |
| | SA14 | 00000111XXX | 32 | 038000h–03FFFFh |
| | SA15 | 00001000XXX | 32 | 040000h–047FFFh |
| | SA16 | 00001001XXX | 32 | 048000h–04FFFFh |
| | SA17 | 00001010XXX | 32 | 050000h–057FFFh |
| | SA18 | 00001011XXX | 32 | 058000h–05FFFFh |
| | SA19 | 00001100XXX | 32 | 060000h–067FFFh |
| | SA20 | 00001101XXX | 32 | 068000h–06FFFFh |
| | SA21 | 00001110XXX | 32 | 070000h–077FFFh |
| | SA22 | 00001111XXX | 32 | 078000h–07FFFFh |
| | SA23 | 00010000XXX | 32 | 080000h–087FFFh |
| | SA24 | 00010001XXX | 32 | 088000h–08FFFFh |
| | SA25 | 00010010XXX | 32 | 090000h–097FFFh |
| | SA26 | 00010011XXX | 32 | 098000h–09FFFFh |
| | SA27 | 00010100XXX | 32 | 0A0000h–0A7FFFh |
| | SA28 | 00010101XXX | 32 | 0A8000h–0AFFFFh |
| | SA29 | 00010110XXX | 32 | 0B0000h–0B7FFFh |
| | SA30 | 00010111XXX | 32 | 0B8000h–0BFFFFh |
| | SA31 | 00011000XXX | 32 | 0C0000h–0C7FFFh |
| | SA32 | 00011001XXX | 32 | 0C8000h–0CFFFFh |
| | SA33 | 00011010XXX | 32 | 0D0000h–0D7FFFh |
| | SA34 | 00011011XXX | 32 | 0D8000h–0DFFFFh |
| | SA35 | 00011100XXX | 32 | 0E0000h–0E7FFFh |
| | SA36 | 00011101XXX | 32 | 0E8000h–0EFFFFh |
| | SA37 | 00011110XXX | 32 | 0F0000h–0F7FFFh |
| | SA38 | 00011111XXX | 32 | 0F8000h–0FFFFFh |
| Bank B | SA39 | 00100000XXX | 32 | 100000h–107FFFh |
| | SA40 | 00100001XXX | 32 | 108000h–10FFFFh |
| | SA41 | 00100010XXX | 32 | 110000h–117FFFh |
| | SA42 | 00100011XXX | 32 | 118000h–11FFFFh |
| | SA43 | 00100100XXX | 32 | 120000h–127FFFh |
| | SA44 | 00100101XXX | 32 | 128000h–12FFFFh |

**Table 16. PL127J Sector Architecture** (Continued)

| Bank | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|---|---|---|---|---|
| Bank B | SA45 | 00100110XXX | 32 | 130000h–137FFFh |
| | SA46 | 00100111XXX | 32 | 138000h–13FFFFh |
| | SA47 | 00101000XXX | 32 | 140000h–147FFFh |
| | SA48 | 00101001XXX | 32 | 148000h–14FFFFh |
| | SA49 | 00101010XXX | 32 | 150000h–157FFFh |
| | SA50 | 00101011XXX | 32 | 158000h–15FFFFh |
| | SA51 | 00101100XXX | 32 | 160000h–167FFFh |
| | SA52 | 00101101XXX | 32 | 168000h–16FFFFh |
| | SA53 | 00101110XXX | 32 | 170000h–177FFFh |
| | SA54 | 00101111XXX | 32 | 178000h–17FFFFh |
| | SA55 | 00110000XXX | 32 | 180000h–187FFFh |
| | SA56 | 00110001XXX | 32 | 188000h–18FFFFh |
| | SA57 | 00110010XXX | 32 | 190000h–197FFFh |
| | SA58 | 00110011XXX | 32 | 198000h–19FFFFh |
| | SA59 | 00110100XXX | 32 | 1A0000h–1A7FFFh |
| | SA60 | 00110101XXX | 32 | 1A8000h–1AFFFFh |
| | SA61 | 00110110XXX | 32 | 1B0000h–1B7FFFh |
| | SA62 | 00110111XXX | 32 | 1B8000h–1BFFFFh |
| | SA63 | 00111000XXX | 32 | 1C0000h–1C7FFFh |
| | SA64 | 00111001XXX | 32 | 1C8000h–1CFFFFh |
| | SA65 | 00111010XXX | 32 | 1D0000h–1D7FFFh |
| | SA66 | 00111011XXX | 32 | 1D8000h–1DFFFFh |
| | SA67 | 00111100XXX | 32 | 1E0000h–1E7FFFh |
| | SA68 | 00111101XXX | 32 | 1E8000h–1EFFFFh |
| | SA69 | 00111110XXX | 32 | 1F0000h–1F7FFFh |
| | SA70 | 00111111XXX | 32 | 1F8000h–1FFFFFh |
| | SA71 | 01000000XXX | 32 | 200000h–207FFFh |
| | SA72 | 01000001XXX | 32 | 208000h–20FFFFh |
| | SA73 | 01000010XXX | 32 | 210000h–217FFFh |
| | SA74 | 01000011XXX | 32 | 218000h–21FFFFh |
| | SA75 | 01000100XXX | 32 | 220000h–227FFFh |
| | SA76 | 01000101XXX | 32 | 228000h–22FFFFh |
| | SA77 | 01000110XXX | 32 | 230000h–237FFFh |
| | SA78 | 01000111XXX | 32 | 238000h–23FFFFh |
| | SA79 | 01001000XXX | 32 | 240000h–247FFFh |
| | SA80 | 01001001XXX | 32 | 248000h–24FFFFh |
| | SA81 | 01001010XXX | 32 | 250000h–257FFFh |
| | SA82 | 01001011XXX | 32 | 258000h–25FFFFh |
| | SA83 | 01001100XXX | 32 | 260000h–267FFFh |
| | SA84 | 01001101XXX | 32 | 268000h–26FFFFh |
| | SA85 | 01001110XXX | 32 | 270000h–277FFFh |
| | SA86 | 01001111XXX | 32 | 278000h–27FFFFh |
| | SA87 | 01010000XXX | 32 | 280000h–287FFFh |
| | SA88 | 01010001XXX | 32 | 288000h–28FFFFh |
| | SA89 | 01010010XXX | 32 | 290000h–297FFFh |

**Table 16. PL127J Sector Architecture** (Continued)

| Bank | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|---|---|---|---|---|
| Bank B | SA90 | 01010011XXX | 32 | 298000h–29FFFFh |
| | SA91 | 01010100XXX | 32 | 2A0000h–2A7FFFh |
| | SA92 | 01010101XXX | 32 | 2A8000h–2AFFFFh |
| | SA93 | 01010110XXX | 32 | 2B0000h–2B7FFFh |
| | SA94 | 01010111XXX | 32 | 2B8000h–2BFFFFh |
| | SA95 | 01011000XXX | 32 | 2C0000h–2C7FFFh |
| | SA96 | 01011001XXX | 32 | 2C8000h–2CFFFFh |
| | SA97 | 01011010XXX | 32 | 2D0000h–2D7FFFh |
| | SA98 | 01011011XXX | 32 | 2D8000h–2DFFFFh |
| | SA99 | 01011100XXX | 32 | 2E0000h–2E7FFFh |
| | SA100 | 01011101XXX | 32 | 2E8000h–2EFFFFh |
| | SA101 | 01011110XXX | 32 | 2F0000h–2F7FFFh |
| | SA102 | 01011111XXX | 32 | 2F8000h–2FFFFFh |
| | SA103 | 01100000XXX | 32 | 300000h–307FFFh |
| | SA104 | 01100001XXX | 32 | 308000h–30FFFFh |
| | SA105 | 01100010XXX | 32 | 310000h–317FFFh |
| | SA106 | 01100011XXX | 32 | 318000h–31FFFFh |
| | SA107 | 01100100XXX | 32 | 320000h–327FFFh |
| | SA108 | 01100101XXX | 32 | 328000h–32FFFFh |
| | SA109 | 01100110XXX | 32 | 330000h–337FFFh |
| | SA110 | 01100111XXX | 32 | 338000h–33FFFFh |
| | SA111 | 01101000XXX | 32 | 340000h–347FFFh |
| | SA112 | 01101001XXX | 32 | 348000h–34FFFFh |
| | SA113 | 01101010XXX | 32 | 350000h–357FFFh |
| | SA114 | 01101011XXX | 32 | 358000h–35FFFFh |
| | SA115 | 01101100XXX | 32 | 360000h–367FFFh |
| | SA116 | 01101101XXX | 32 | 368000h–36FFFFh |
| | SA117 | 01101110XXX | 32 | 370000h–377FFFh |
| | SA118 | 01101111XXX | 32 | 378000h–37FFFFh |
| | SA119 | 01110000XXX | 32 | 380000h–387FFFh |
| | SA120 | 01110001XXX | 32 | 388000h–38FFFFh |
| | SA121 | 01110010XXX | 32 | 390000h–397FFFh |
| | SA122 | 01110011XXX | 32 | 398000h–39FFFFh |
| | SA123 | 01110100XXX | 32 | 3A0000h–3A7FFFh |
| | SA124 | 01110101XXX | 32 | 3A8000h–3AFFFFh |
| | SA125 | 01110110XXX | 32 | 3B0000h–3B7FFFh |
| | SA126 | 01110111XXX | 32 | 3B8000h–3BFFFFh |
| | SA127 | 01111000XXX | 32 | 3C0000h–3C7FFFh |
| | SA128 | 01111001XXX | 32 | 3C8000h–3CFFFFh |
| | SA129 | 01111010XXX | 32 | 3D0000h–3D7FFFh |
| | SA130 | 01111011XXX | 32 | 3D8000h–3DFFFFh |
| | SA131 | 01111100XXX | 32 | 3E0000h–3E7FFFh |
| | SA132 | 01111101XXX | 32 | 3E8000h–3EFFFFh |
| | SA133 | 01111110XXX | 32 | 3F0000h–3F7FFFh |
| | SA134 | 01111111XXX | 32 | 3F8000h–3FFFFFh |

**Table 16. PL127J Sector Architecture** (Continued)

| Bank | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|---|---|---|---|---|
| Bank C | SA135 | 10000000XXX | 32 | 400000h–407FFFh |
| | SA136 | 10000001XXX | 32 | 408000h–40FFFFh |
| | SA137 | 10000010XXX | 32 | 410000h–417FFFh |
| | SA138 | 10000011XXX | 32 | 418000h–41FFFFh |
| | SA139 | 10000100XXX | 32 | 420000h–427FFFh |
| | SA140 | 10000101XXX | 32 | 428000h–42FFFFh |
| | SA141 | 10000110XXX | 32 | 430000h–437FFFh |
| | SA142 | 10000111XXX | 32 | 438000h–43FFFFh |
| | SA143 | 10001000XXX | 32 | 440000h–447FFFh |
| | SA144 | 10001001XXX | 32 | 448000h–44FFFFh |
| | SA145 | 10001010XXX | 32 | 450000h–457FFFh |
| | SA146 | 10001011XXX | 32 | 458000h–45FFFFh |
| | SA147 | 10001100XXX | 32 | 460000h–467FFFh |
| | SA148 | 10001101XXX | 32 | 468000h–46FFFFh |
| | SA149 | 10001110XXX | 32 | 470000h–477FFFh |
| | SA150 | 10001111XXX | 32 | 478000h–47FFFFh |
| | SA151 | 10010000XXX | 32 | 480000h–487FFFh |
| | SA152 | 10010001XXX | 32 | 488000h–48FFFFh |
| | SA153 | 10010010XXX | 32 | 490000h–497FFFh |
| | SA154 | 10010011XXX | 32 | 498000h–49FFFFh |
| | SA155 | 10010100XXX | 32 | 4A0000h–4A7FFFh |
| | SA156 | 10010101XXX | 32 | 4A8000h–4AFFFFh |
| | SA157 | 10010110XXX | 32 | 4B0000h–4B7FFFh |
| | SA158 | 10010111XXX | 32 | 4B8000h–4BFFFFh |
| | SA159 | 10011000XXX | 32 | 4C0000h–4C7FFFh |
| | SA160 | 10011001XXX | 32 | 4C8000h–4CFFFFh |
| | SA161 | 10011010XXX | 32 | 4D0000h–4D7FFFh |
| | SA162 | 10011011XXX | 32 | 4D8000h–4DFFFFh |
| | SA163 | 10011100XXX | 32 | 4E0000h–4E7FFFh |
| | SA164 | 10011101XXX | 32 | 4E8000h–4EFFFFh |
| | SA165 | 10011110XXX | 32 | 4F0000h–4F7FFFh |
| | SA166 | 10011111XXX | 32 | 4F8000h–4FFFFFh |
| | SA167 | 10100000XXX | 32 | 500000h–507FFFh |
| | SA168 | 10100001XXX | 32 | 508000h–50FFFFh |
| | SA169 | 10100010XXX | 32 | 510000h–517FFFh |
| | SA170 | 10100011XXX | 32 | 518000h–51FFFFh |
| | SA171 | 10100100XXX | 32 | 520000h–527FFFh |
| | SA172 | 10100101XXX | 32 | 528000h–52FFFFh |
| | SA173 | 10100110XXX | 32 | 530000h–537FFFh |
| | SA174 | 10100111XXX | 32 | 538000h–53FFFFh |
| | SA175 | 10101000XXX | 32 | 540000h–547FFFh |
| | SA176 | 10101001XXX | 32 | 548000h–54FFFFh |
| | SA177 | 10101010XXX | 32 | 550000h–557FFFh |
| | SA178 | 10101011XXX | 32 | 558000h–15FFFFh |
| | SA179 | 10101100XXX | 32 | 560000h–567FFFh |

**Table 16. PL127J Sector Architecture** (Continued)

| Bank | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|---|---|---|---|---|
| Bank C | SA180 | 10101101XXX | 32 | 568000h–56FFFFh |
| | SA181 | 10101110XXX | 32 | 570000h–577FFFh |
| | SA182 | 10101111XXX | 32 | 578000h–57FFFFh |
| | SA183 | 10110000XXX | 32 | 580000h–587FFFh |
| | SA184 | 10110001XXX | 32 | 588000h–58FFFFh |
| | SA185 | 10110010XXX | 32 | 590000h–597FFFh |
| | SA186 | 10110011XXX | 32 | 598000h–59FFFFh |
| | SA187 | 10110100XXX | 32 | 5A0000h–5A7FFFh |
| | SA188 | 10110101XXX | 32 | 5A8000h–5AFFFFh |
| | SA189 | 10110110XXX | 32 | 5B0000h–5B7FFFh |
| | SA190 | 10110111XXX | 32 | 5B8000h–5BFFFFh |
| | SA191 | 10111000XXX | 32 | 5C0000h–5C7FFFh |
| | SA192 | 10111001XXX | 32 | 5C8000h–5CFFFFh |
| | SA193 | 10111010XXX | 32 | 5D0000h–5D7FFFh |
| | SA194 | 10111011XXX | 32 | 5D8000h–5DFFFFh |
| | SA195 | 10111100XXX | 32 | 5E0000h–5E7FFFh |
| | SA196 | 10111101XXX | 32 | 5E8000h–5EFFFFh |
| | SA197 | 10111110XXX | 32 | 5F0000h–5F7FFFh |
| | SA198 | 10111111XXX | 32 | 5F8000h–5FFFFFh |
| | SA199 | 11000000XXX | 32 | 600000h–607FFFh |
| | SA200 | 11000001XXX | 32 | 608000h–60FFFFh |
| | SA201 | 11000010XXX | 32 | 610000h–617FFFh |
| | SA202 | 11000011XXX | 32 | 618000h–61FFFFh |
| | SA203 | 11000100XXX | 32 | 620000h–627FFFh |
| | SA204 | 11000101XXX | 32 | 628000h–62FFFFh |
| | SA205 | 11000110XXX | 32 | 630000h–637FFFh |
| | SA206 | 11000111XXX | 32 | 638000h–63FFFFh |
| | SA207 | 11001000XXX | 32 | 640000h–647FFFh |
| | SA208 | 11001001XXX | 32 | 648000h–64FFFFh |
| | SA209 | 11001010XXX | 32 | 650000h–657FFFh |
| | SA210 | 11001011XXX | 32 | 658000h–65FFFFh |
| | SA211 | 11001100XXX | 32 | 660000h–667FFFh |
| | SA212 | 11001101XXX | 32 | 668000h–66FFFFh |
| | SA213 | 11001110XXX | 32 | 670000h–677FFFh |
| | SA214 | 11001111XXX | 32 | 678000h–67FFFFh |
| | SA215 | 11010000XXX | 32 | 680000h–687FFFh |
| | SA216 | 11010001XXX | 32 | 688000h–68FFFFh |
| | SA217 | 11010010XXX | 32 | 690000h–697FFFh |
| | SA218 | 11010011XXX | 32 | 698000h–69FFFFh |
| | SA219 | 11010100XXX | 32 | 6A0000h–6A7FFFh |
| | SA220 | 11010101XXX | 32 | 6A8000h–6AFFFFh |
| | SA221 | 11010110XXX | 32 | 6B0000h–6B7FFFh |
| | SA222 | 11010111XXX | 32 | 6B8000h–6BFFFFh |
| | SA223 | 11011000XXX | 32 | 6C0000h–6C7FFFh |
| | SA224 | 11011001XXX | 32 | 6C8000h–6CFFFFh |

**Table 16. PL127J Sector Architecture** (Continued)

| Bank | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|---|---|---|---|---|
| Bank C | SA225 | 11011010XXX | 32 | 6D0000h–6D7FFFh |
| | SA226 | 11011011XXX | 32 | 6D8000h–6DFFFFh |
| | SA227 | 11011100XXX | 32 | 6E0000h–6E7FFFh |
| | SA228 | 11011101XXX | 32 | 6E8000h–6EFFFFh |
| | SA229 | 11011110XXX | 32 | 6F0000h–6F7FFFh |
| | SA230 | 11011111XXX | 32 | 6F8000h–6FFFFFh |
| Bank D | SA231 | 11100000XXX | 32 | 700000h–707FFFh |
| | SA232 | 11100001XXX | 32 | 708000h–70FFFFh |
| | SA233 | 11100010XXX | 32 | 710000h–717FFFh |
| | SA234 | 11100011XXX | 32 | 718000h–71FFFFh |
| | SA235 | 11100100XXX | 32 | 720000h–727FFFh |
| | SA236 | 11100101XXX | 32 | 728000h–72FFFFh |
| | SA237 | 11100110XXX | 32 | 730000h–737FFFh |
| | SA238 | 11100111XXX | 32 | 738000h–73FFFFh |
| | SA239 | 11101000XXX | 32 | 740000h–747FFFh |
| | SA240 | 11101001XXX | 32 | 748000h–74FFFFh |
| | SA241 | 11101010XXX | 32 | 750000h–757FFFh |
| | SA242 | 11101011XXX | 32 | 758000h–75FFFFh |
| | SA243 | 11101100XXX | 32 | 760000h–767FFFh |
| | SA244 | 11101101XXX | 32 | 768000h–76FFFFh |
| | SA245 | 11101110XXX | 32 | 770000h–777FFFh |
| | SA246 | 11101111XXX | 32 | 778000h–77FFFFh |
| | SA247 | 11110000XXX | 32 | 780000h–787FFFh |
| | SA248 | 11110001XXX | 32 | 788000h–78FFFFh |
| | SA249 | 11110010XXX | 32 | 790000h–797FFFh |
| | SA250 | 11110011XXX | 32 | 798000h–79FFFFh |
| | SA251 | 11110100XXX | 32 | 7A0000h–7A7FFFh |
| | SA252 | 11110101XXX | 32 | 7A8000h–7AFFFFh |
| | SA253 | 11110110XXX | 32 | 7B0000h–7B7FFFh |
| | SA254 | 11110111XXX | 32 | 7B8000h–7BFFFFh |
| | SA255 | 11111000XXX | 32 | 7C0000h–7C7FFFh |
| | SA256 | 11111001XXX | 32 | 7C8000h–7CFFFFh |
| | SA257 | 11111010XXX | 32 | 7D0000h–7D7FFFh |
| | SA258 | 11111011XXX | 32 | 7D8000h–7DFFFFh |
| | SA259 | 11111100XXX | 32 | 7E0000h–7E7FFFh |
| | SA260 | 11111101XXX | 32 | 7E8000h–7EFFFFh |
| | SA261 | 11111110XXX | 32 | 7F0000h–7F7FFFh |
| | SA262 | 11111111000 | 4 | 7F8000h–7F8FFFh |
| | SA263 | 11111111001 | 4 | 7F9000h–7F9FFFh |
| | SA264 | 11111111010 | 4 | 7FA000h–7FAFFFh |
| | SA265 | 11111111011 | 4 | 7FB000h–7FBFFFh |
| | SA266 | 11111111100 | 4 | 7FC000h–7FCFFFh |
| | SA267 | 11111111101 | 4 | 7FD000h–7FDFFFh |
| | SA268 | 11111111110 | 4 | 7FE000h–7FEFFFh |
| | SA269 | 11111111111 | 4 | 7FF000h–7FFFFFh |

**Table 17. PL064J Sector Architecture**

| Bank | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|---|---|---|---|---|
| Bank A | SA0 | 0000000000 | 4 | 000000h–000FFFh |
| | SA1 | 0000000001 | 4 | 001000h–001FFFh |
| | SA2 | 0000000010 | 4 | 002000h–002FFFh |
| | SA3 | 0000000011 | 4 | 003000h–003FFFh |
| | SA4 | 0000000100 | 4 | 004000h–004FFFh |
| | SA5 | 0000000101 | 4 | 005000h–005FFFh |
| | SA6 | 0000000110 | 4 | 006000h–006FFFh |
| | SA7 | 0000000111 | 4 | 007000h–007FFFh |
| | SA8 | 0000001XXX | 32 | 008000h–00FFFFh |
| | SA9 | 0000010XXX | 32 | 010000h–017FFFh |
| | SA10 | 0000011XXX | 32 | 018000h–01FFFFh |
| | SA11 | 0000100XXX | 32 | 020000h–027FFFh |
| | SA12 | 0000101XXX | 32 | 028000h–02FFFFh |
| | SA13 | 0000110XXX | 32 | 030000h–037FFFh |
| | SA14 | 0000111XXX | 32 | 038000h–03FFFFh |
| | SA15 | 0001000XXX | 32 | 040000h–047FFFh |
| | SA16 | 0001001XXX | 32 | 048000h–04FFFFh |
| | SA17 | 0001010XXX | 32 | 050000h–057FFFh |
| | SA18 | 0001011XXX | 32 | 058000h–05FFFFh |
| | SA19 | 0001100XXX | 32 | 060000h–067FFFh |
| | SA20 | 0001101XXX | 32 | 068000h–06FFFFh |
| | SA21 | 0001110XXX | 32 | 070000h–077FFFh |
| | SA22 | 0001111XXX | 32 | 078000h–07FFFFh |
| Bank B | SA23 | 0010000XXX | 32 | 080000h–087FFFh |
| | SA24 | 0010001XXX | 32 | 088000h–08FFFFh |
| | SA25 | 0010010XXX | 32 | 090000h–097FFFh |
| | SA26 | 0010011XXX | 32 | 098000h–09FFFFh |
| | SA27 | 0010100XXX | 32 | 0A0000h–0A7FFFh |
| | SA28 | 0010101XXX | 32 | 0A8000h–0AFFFFh |
| | SA29 | 0010110XXX | 32 | 0B0000h–0B7FFFh |
| | SA30 | 0010111XXX | 32 | 0B8000h–0BFFFFh |
| | SA31 | 0011000XXX | 32 | 0C0000h–0C7FFFh |
| | SA32 | 0011001XXX | 32 | 0C8000h–0CFFFFh |
| | SA33 | 0011010XXX | 32 | 0D0000h–0D7FFFh |
| | SA34 | 0011011XXX | 32 | 0D8000h–0DFFFFh |
| | SA35 | 0011100XXX | 32 | 0E0000h–0E7FFFh |
| | SA36 | 0011101XXX | 32 | 0E8000h–0EFFFFh |
| | SA37 | 0011110XXX | 32 | 0F0000h–0F7FFFh |
| | SA38 | 0011111XXX | 32 | 0F8000h–0FFFFFh |
| | SA39 | 0100000XXX | 32 | 100000h–107FFFh |
| | SA40 | 0100001XXX | 32 | 108000h–10FFFFh |
| | SA41 | 0100010XXX | 32 | 110000h–117FFFh |
| | SA42 | 0100011XXX | 32 | 118000h–11FFFFh |

**Table 17. PL064J Sector Architecture** (Continued)

| Bank | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|---|---|---|---|---|
| Bank B | SA43 | 0100100XXX | 32 | 120000h–127FFFh |
| | SA44 | 0100101XXX | 32 | 128000h–12FFFFh |
| | SA45 | 0100110XXX | 32 | 130000h–137FFFh |
| | SA46 | 0100111XXX | 32 | 138000h–13FFFFh |
| | SA47 | 0101000XXX | 32 | 140000h–147FFFh |
| | SA48 | 0101001XXX | 32 | 148000h–14FFFFh |
| | SA49 | 0101010XXX | 32 | 150000h–157FFFh |
| | SA50 | 0101011XXX | 32 | 158000h–15FFFFh |
| | SA51 | 0101100XXX | 32 | 160000h–167FFFh |
| | SA52 | 0101101XXX | 32 | 168000h–16FFFFh |
| | SA53 | 0101110XXX | 32 | 170000h–177FFFh |
| | SA54 | 0101111XXX | 32 | 178000h–17FFFFh |
| | SA55 | 0110000XXX | 32 | 180000h–187FFFh |
| | SA56 | 0110001XXX | 32 | 188000h–18FFFFh |
| | SA57 | 0110010XXX | 32 | 190000h–197FFFh |
| | SA58 | 0110011XXX | 32 | 198000h–19FFFFh |
| | SA59 | 0110100XXX | 32 | 1A0000h–1A7FFFh |
| | SA60 | 0110101XXX | 32 | 1A8000h–1AFFFFh |
| | SA61 | 0110110XXX | 32 | 1B0000h–1B7FFFh |
| | SA62 | 0110111XXX | 32 | 1B8000h–1BFFFFh |
| | SA63 | 0111000XXX | 32 | 1C0000h–1C7FFFh |
| | SA64 | 0111001XXX | 32 | 1C8000h–1CFFFFh |
| | SA65 | 0111010XXX | 32 | 1D0000h–1D7FFFh |
| | SA66 | 0111011XXX | 32 | 1D8000h–1DFFFFh |
| | SA67 | 0111100XXX | 32 | 1E0000h–1E7FFFh |
| | SA68 | 0111101XXX | 32 | 1E8000h–1EFFFFh |
| | SA69 | 0111110XXX | 32 | 1F0000h–1F7FFFh |
| | SA70 | 0111111XXX | 32 | 1F8000h–1FFFFFh |
| Bank C | SA71 | 1000000XXX | 32 | 200000h–207FFFh |
| | SA72 | 1000001XXX | 32 | 208000h–20FFFFh |
| | SA73 | 1000010XXX | 32 | 210000h–217FFFh |
| | SA74 | 1000011XXX | 32 | 218000h–21FFFFh |
| | SA75 | 1000100XXX | 32 | 220000h–227FFFh |
| | SA76 | 1000101XXX | 32 | 228000h–22FFFFh |
| | SA77 | 1000110XXX | 32 | 230000h–237FFFh |
| | SA78 | 1000111XXX | 32 | 238000h–23FFFFh |
| | SA79 | 1001000XXX | 32 | 240000h–247FFFh |
| | SA80 | 1001001XXX | 32 | 248000h–24FFFFh |
| | SA81 | 1001010XXX | 32 | 250000h–257FFFh |
| | SA82 | 1001011XXX | 32 | 258000h–25FFFFh |
| | SA83 | 1001100XXX | 32 | 260000h–267FFFh |
| | SA84 | 1001101XXX | 32 | 268000h–26FFFFh |
| | SA85 | 1001110XXX | 32 | 270000h–277FFFh |

**Table 17. PL064J Sector Architecture** (Continued)

| Bank | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|---|---|---|---|---|
| Bank C | SA86 | 1001111XXX | 32 | 278000h–27FFFFh |
| | SA87 | 1010000XXX | 32 | 280000h–287FFFh |
| | SA88 | 1010001XXX | 32 | 288000h–28FFFFh |
| | SA89 | 1010010XXX | 32 | 290000h–297FFFh |
| | SA90 | 1010011XXX | 32 | 298000h–29FFFFh |
| | SA91 | 1010100XXX | 32 | 2A0000h–2A7FFFh |
| | SA92 | 1010101XXX | 32 | 2A8000h–2AFFFFh |
| | SA93 | 1010110XXX | 32 | 2B0000h–2B7FFFh |
| | SA94 | 1010111XXX | 32 | 2B8000h–2BFFFFh |
| | SA95 | 1011000XXX | 32 | 2C0000h–2C7FFFh |
| | SA96 | 1011001XXX | 32 | 2C8000h–2CFFFFh |
| | SA97 | 1011010XXX | 32 | 2D0000h–2D7FFFh |
| | SA98 | 1011011XXX | 32 | 2D8000h–2DFFFFh |
| | SA99 | 1011100XXX | 32 | 2E0000h–2E7FFFh |
| | SA100 | 1011101XXX | 32 | 2E8000h–2EFFFFh |
| | SA101 | 1011110XXX | 32 | 2F0000h–2F7FFFh |
| | SA102 | 1011111XXX | 32 | 2F8000h–2FFFFFh |
| | SA103 | 1100000XXX | 32 | 300000h–307FFFh |
| | SA104 | 1100001XXX | 32 | 308000h–30FFFFh |
| | SA105 | 1100010XXX | 32 | 310000h–317FFFh |
| | SA106 | 1100011XXX | 32 | 318000h–31FFFFh |
| | SA107 | 1100100XXX | 32 | 320000h–327FFFh |
| | SA108 | 1100101XXX | 32 | 328000h–32FFFFh |
| | SA109 | 1100110XXX | 32 | 330000h–337FFFh |
| | SA110 | 1100111XXX | 32 | 338000h–33FFFFh |
| | SA111 | 1101000XXX | 32 | 340000h–347FFFh |
| | SA112 | 1101001XXX | 32 | 348000h–34FFFFh |
| | SA113 | 1101010XXX | 32 | 350000h–357FFFh |
| | SA114 | 1101011XXX | 32 | 358000h–35FFFFh |
| | SA115 | 1101100XXX | 32 | 360000h–367FFFh |
| | SA116 | 1101101XXX | 32 | 368000h–36FFFFh |
| | SA117 | 1101110XXX | 32 | 370000h–377FFFh |
| | SA118 | 1101111XXX | 32 | 378000h–37FFFFh |

**Table 17. PL064J Sector Architecture** (Continued)

| Bank | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|---|---|---|---|---|
| Bank D | SA119 | 1110000XXX | 32 | 380000h–387FFFh |
| | SA120 | 1110001XXX | 32 | 388000h–38FFFFh |
| | SA121 | 1110010XXX | 32 | 390000h–397FFFh |
| | SA122 | 1110011XXX | 32 | 398000h–39FFFFh |
| | SA123 | 1110100XXX | 32 | 3A0000h–3A7FFFh |
| | SA124 | 1110101XXX | 32 | 3A8000h–3AFFFFh |
| | SA125 | 1110110XXX | 32 | 3B0000h–3B7FFFh |
| | SA126 | 1110111XXX | 32 | 3B8000h–3BFFFFh |
| | SA127 | 1111000XXX | 32 | 3C0000h–3C7FFFh |
| | SA128 | 1111001XXX | 32 | 3C8000h–3CFFFFh |
| | SA129 | 1111010XXX | 32 | 3D0000h–3D7FFFh |
| | SA130 | 1111011XXX | 32 | 3D8000h–3DFFFFh |
| | SA131 | 1111100XXX | 32 | 3E0000h–3E7FFFh |
| | SA132 | 1111101XXX | 32 | 3E8000h–3EFFFFh |
| | SA133 | 1111110XXX | 32 | 3F0000h–3F7FFFh |
| | SA134 | 1111111000 | 4 | 3F8000h–3F8FFFh |
| | SA135 | 1111111001 | 4 | 3F9000h–3F9FFFh |
| | SA136 | 1111111010 | 4 | 3FA000h–3FAFFFh |
| | SA137 | 1111111011 | 4 | 3FB000h–3FBFFFh |
| | SA138 | 1111111100 | 4 | 3FC000h–3FCFFFh |
| | SA139 | 1111111101 | 4 | 3FD000h–3FDFFFh |
| | SA140 | 1111111110 | 4 | 3FE000h–3FEFFFh |
| | SA141 | 1111111111 | 4 | 3FF000h–3FFFFFh |

**Table 18. PL032J Sector Architecture**

| Bank | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|---|---|---|---|---|
| Bank A | SA0 | 000000000 | 4 | 000000h–000FFFh |
| | SA1 | 000000001 | 4 | 001000h–001FFFh |
| | SA2 | 000000010 | 4 | 002000h–002FFFh |
| | SA3 | 000000011 | 4 | 003000h–003FFFh |
| | SA4 | 000000100 | 4 | 004000h–004FFFh |
| | SA5 | 000000101 | 4 | 005000h–005FFFh |
| | SA6 | 000000110 | 4 | 006000h–006FFFh |
| | SA7 | 000000111 | 4 | 007000h–007FFFh |
| | SA8 | 000001XXX | 32 | 008000h–00FFFFh |
| | SA9 | 000010XXX | 32 | 010000h–017FFFh |
| | SA10 | 000011XXX | 32 | 018000h–01FFFFh |
| | SA11 | 000100XXX | 32 | 020000h–027FFFh |
| | SA12 | 000101XXX | 32 | 028000h–02FFFFh |
| | SA13 | 000110XXX | 32 | 030000h–037FFFh |
| | SA14 | 000111XXX | 32 | 038000h–03FFFFh |
| Bank B | SA15 | 001000XXX | 32 | 040000h–047FFFh |
| | SA16 | 001001XXX | 32 | 048000h–04FFFFh |
| | SA17 | 001010XXX | 32 | 050000h–057FFFh |
| | SA18 | 001011XXX | 32 | 058000h–05FFFFh |
| | SA19 | 001100XXX | 32 | 060000h–067FFFh |
| | SA20 | 001101XXX | 32 | 068000h–06FFFFh |
| | SA21 | 001110XXX | 32 | 070000h–077FFFh |
| | SA22 | 001111XXX | 32 | 078000h–07FFFFh |
| | SA23 | 010000XXX | 32 | 080000h–087FFFh |
| | SA24 | 010001XXX | 32 | 088000h–08FFFFh |
| | SA25 | 010010XXX | 32 | 090000h–097FFFh |
| | SA26 | 010011XXX | 32 | 098000h–09FFFFh |
| | SA27 | 010100XXX | 32 | 0A0000h–0A7FFFh |
| | SA28 | 010101XXX | 32 | 0A8000h–0AFFFFh |
| | SA29 | 010110XXX | 32 | 0B0000h–0B7FFFh |
| | SA30 | 010111XXX | 32 | 0B8000h–0BFFFFh |
| | SA31 | 011000XXX | 32 | 0C0000h–0C7FFFh |
| | SA32 | 011001XXX | 32 | 0C8000h–0CFFFFh |
| | SA33 | 011010XXX | 32 | 0D0000h–0D7FFFh |
| | SA34 | 011011XXX | 32 | 0D8000h–0DFFFFh |
| | SA35 | 011100XXX | 32 | 0E0000h–0E7FFFh |
| | SA36 | 011101XXX | 32 | 0E8000h–0EFFFFh |
| | SA37 | 011110XXX | 32 | 0F0000h–0F7FFFh |
| | SA38 | 011111XXX | 32 | 0F8000h–0FFFFFh |
| Bank C | SA39 | 100000XXX | 32 | 100000h–107FFFh |
| | SA40 | 100001XXX | 32 | 108000h–10FFFFh |
| | SA41 | 100010XXX | 32 | 110000h–117FFFh |
| | SA42 | 100011XXX | 32 | 118000h–11FFFFh |
| | SA43 | 100100XXX | 32 | 120000h–127FFFh |

**Table 18. PL032J Sector Architecture** (Continued)

| Bank | Sector | Sector Address (A22-A12) | Sector Size (Kwords) | Address Range (x16) |
|---|---|---|---|---|
| Bank C | SA44 | 100101XXX | 32 | 128000h–12FFFFh |
| | SA45 | 100110XXX | 32 | 130000h–137FFFh |
| | SA46 | 100111XXX | 32 | 138000h–13FFFFh |
| | SA47 | 101000XXX | 32 | 140000h–147FFFh |
| | SA48 | 101001XXX | 32 | 148000h–14FFFFh |
| | SA49 | 101010XXX | 32 | 150000h–157FFFh |
| | SA50 | 101011XXX | 32 | 158000h–15FFFFh |
| | SA51 | 101100XXX | 32 | 160000h–167FFFh |
| | SA52 | 101101XXX | 32 | 168000h–16FFFFh |
| | SA53 | 101110XXX | 32 | 170000h–177FFFh |
| | SA54 | 101111XXX | 32 | 178000h–17FFFFh |
| | SA55 | 110000XXX | 32 | 180000h–187FFFh |
| | SA56 | 110001XXX | 32 | 188000h–18FFFFh |
| | SA57 | 110010XXX | 32 | 190000h–197FFFh |
| | SA58 | 110011XXX | 32 | 198000h–19FFFFh |
| | SA59 | 110100XXX | 32 | 1A0000h–1A7FFFh |
| | SA60 | 110101XXX | 32 | 1A8000h–1AFFFFh |
| | SA61 | 110110XXX | 32 | 1B0000h–1B7FFFh |
| | SA62 | 110111XXX | 32 | 1B8000h–1BFFFFh |
| Bank D | SA63 | 111000XXX | 32 | 1C0000h–1C7FFFh |
| | SA64 | 111001XXX | 32 | 1C8000h–1CFFFFh |
| | SA65 | 111010XXX | 32 | 1D0000h–1D7FFFh |
| | SA66 | 111011XXX | 32 | 1D8000h–1DFFFFh |
| | SA67 | 111100XXX | 32 | 1E0000h–1E7FFFh |
| | SA68 | 111101XXX | 32 | 1E8000h–1EFFFFh |
| | SA69 | 111110XXX | 32 | 1F0000h–1F7FFFh |
| | SA70 | 111111000 | 4 | 1F8000h–1F8FFFh |
| | SA71 | 111111001 | 4 | 1F9000h–1F9FFFh |
| | SA72 | 111111010 | 4 | 1FA000h–1FAFFFh |
| | SA73 | 111111011 | 4 | 1FB000h–1FBFFFh |
| | SA74 | 111111100 | 4 | 1FC000h–1FCFFFh |
| | SA75 | 111111101 | 4 | 1FD000h–1FDFFFh |
| | SA76 | 111111110 | 4 | 1FE000h–1FEFFFh |
| | SA77 | 111111111 | 4 | 1FF000h–1FFFFFh |

**Table 19. Secured Silicon Sector Addresses**

| | Sector Size | Address Range |
|---|---|---|
| Factory-Locked Area | 64 words | 000000h-00003Fh |
| Customer-Lockable Area | 64 words | 000040h-00007Fh |

## 10.8 Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires $V_{ID}$ on address pin A9. Address pins must be as shown in Table 20 on page 27. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 15 on page 19). Table 20 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0. However, the autoselect codes can also be accessed in-system through the command register, for instances when the device is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 28 on page 49. *Note that if a Bank Address (BA) (on address bits PL127J: A22–A20, PL064J: A21–A19, PL032J: A20–*A18*) is asserted during the third write cycle of the autoselect command, the host system can read autoselect data that bank and then immediately read array data from the other bank, without exiting the autoselect mode.*

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 28. This method does not require $V_{ID}$. Refer to the Section 15.3 Autoselect Command Sequence on page 43 for more information.

**Table 20. Autoselect Codes (High Voltage Method)**

| Description | | CE# | OE# | WE# | Amax to A12 | A10 | A9 | A8 | A7 | A6 | A5 to A4 | A3 | A2 | A1 | A0 | DQ15 to DQ0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer ID: Cypress products | | L | L | H | BA | X | $V_{ID}$ | X | L | L | X | L | L | L | L | 0001h |
| Device ID | Read Cycle 1 | L | L | H | BA | X | $V_{ID}$ | X | L | L | L | L | L | L | H | 227Eh |
| | Read Cycle 2 | L | | | | | | | | | | H | H | H | L | 2220h (PL127J)<br>2202h (PL064J)<br>220Ah (PL032J) |
| | Read Cycle 3 | L | | | | | | | | | | H | H | H | H | 2200h (PL127J)<br>2201h (PL064J)<br>2201h (PL032J) |
| Sector Protection Verification | | L | L | H | SA | X | $V_{ID}$ | X | L | L | L | L | L | H | L | 0001h (protected),<br>0000h (unprotected) |
| Secured Silicon Indicator Bit (DQ7, DQ6) | | L | L | H | BA[14] | X | $V_{ID}$ | X | X | L | X | L | L | H | H | DQ7=1 (factory locked),<br>DQ6=1 (factory and customer locked) |

**Note**

14. When Polling the Secured Silicon indicator bit the Bank Address (BA) should be set within the address range 004000h-03FFFFh.

**Legend**

L = Logic Low = $V_{IL}$, H = Logic High = $V_{IH}$, BA = Bank Address, SA = Sector Address, X = Don't care.

**Table 21. PL127J Boot Sector/Sector Block Addresses for Protection/Unprotection**

| Sector | A22-A12 | Sector/Sector Block Size |
|---|---|---|
| SA0 | 00000000000 | 4 Kwords |
| SA1 | 00000000001 | 4 Kwords |
| SA2 | 00000000010 | 4 Kwords |
| SA3 | 00000000011 | 4 Kwords |
| SA4 | 00000000100 | 4 Kwords |
| SA5 | 00000000101 | 4 Kwords |
| SA6 | 00000000110 | 4 Kwords |
| SA7 | 00000000111 | 4 Kwords |
| SA8 | 00000001XXX | 32 Kwords |
| SA9 | 00000010XXX | 32 Kwords |
| SA10 | 00000011XXX | 32 Kwords |
| SA11-SA14 | 000001XXXXX | 128 (4x32) Kwords |
| SA15-SA18 | 000010XXXXX | 128 (4x32) Kwords |
| SA19-SA22 | 000011XXXXX | 128 (4x32) Kwords |
| SA23-SA26 | 000100XXXXX | 128 (4x32) Kwords |
| SA27-SA30 | 000101XXXXX | 128 (4x32) Kwords |
| SA31-SA34 | 000110XXXXX | 128 (4x32) Kwords |
| SA35-SA38 | 000111XXXXX | 128 (4x32) Kwords |
| SA39-SA42 | 001000XXXXX | 128 (4x32) Kwords |
| SA43-SA46 | 001001XXXXX | 128 (4x32) Kwords |
| SA47-SA50 | 001010XXXXX | 128 (4x32) Kwords |
| SA51-SA54 | 001011XXXXX | 128 (4x32) Kwords |
| SA55-SA58 | 001100XXXXX | 128 (4x32) Kwords |
| SA59-SA62 | 001101XXXXX | 128 (4x32) Kwords |
| SA63-SA66 | 001110XXXXX | 128 (4x32) Kwords |
| SA67-SA70 | 001111XXXXX | 128 (4x32) Kwords |
| SA71-SA74 | 010000XXXXX | 128 (4x32) Kwords |
| SA75-SA78 | 010001XXXXX | 128 (4x32) Kwords |
| SA79-SA82 | 010010XXXXX | 128 (4x32) Kwords |
| SA83-SA86 | 010011XXXXX | 128 (4x32) Kwords |
| SA87-SA90 | 010100XXXXX | 128 (4x32) Kwords |
| SA91-SA94 | 010101XXXXX | 128 (4x32) Kwords |
| SA95-SA98 | 010110XXXXX | 128 (4x32) Kwords |
| SA99-SA102 | 010111XXXXX | 128 (4x32) Kwords |
| SA103-SA106 | 011000XXXXX | 128 (4x32) Kwords |
| SA107-SA110 | 011001XXXXX | 128 (4x32) Kwords |
| SA111-SA114 | 011010XXXXX | 128 (4x32) Kwords |
| SA115-SA118 | 011011XXXXX | 128 (4x32) Kwords |
| SA119-SA122 | 011100XXXXX | 128 (4x32) Kwords |
| SA123-SA126 | 011101XXXXX | 128 (4x32) Kwords |
| SA127-SA130 | 011110XXXXX | 128 (4x32) Kwords |
| SA131-SA134 | 011111XXXXX | 128 (4x32) Kwords |
| SA135-SA138 | 100000XXXXX | 128 (4x32) Kwords |
| SA139-SA142 | 100001XXXXX | 128 (4x32) Kwords |
| SA143-SA146 | 100010XXXXX | 128 (4x32) Kwords |
| SA147-SA150 | 100011XXXXX | 128 (4x32) Kwords |
| SA151-SA154 | 100100XXXXX | 128 (4x32) Kwords |
| SA155-SA158 | 100101XXXXX | 128 (4x32) Kwords |
| SA159-SA162 | 100110XXXXX | 128 (4x32) Kwords |
| SA163-SA166 | 100111XXXXX | 128 (4x32) Kwords |
| SA167-SA170 | 101000XXXXX | 128 (4x32) Kwords |
| SA171-SA174 | 101001XXXXX | 128 (4x32) Kwords |
| SA175-SA178 | 101010XXXXX | 128 (4x32) Kwords |
| SA179-SA182 | 101011XXXXX | 128 (4x32) Kwords |
| SA183-SA186 | 101100XXXXX | 128 (4x32) Kwords |
| SA187-SA190 | 101101XXXXX | 128 (4x32) Kwords |
| SA191-SA194 | 101110XXXXX | 128 (4x32) Kwords |
| SA195-SA198 | 101111XXXXX | 128 (4x32) Kwords |
| SA199-SA202 | 110000XXXXX | 128 (4x32) Kwords |
| SA203-SA206 | 110001XXXXX | 128 (4x32) Kwords |
| SA207-SA210 | 110010XXXXX | 128 (4x32) Kwords |
| SA211-SA214 | 110011XXXXX | 128 (4x32) Kwords |
| SA215-SA218 | 110100XXXXX | 128 (4x32) Kwords |
| SA219-SA222 | 110101XXXXX | 128 (4x32) Kwords |
| SA223-SA226 | 110110XXXXX | 128 (4x32) Kwords |
| SA227-SA230 | 110111XXXXX | 128 (4x32) Kwords |
| SA231-SA234 | 111000XXXXX | 128 (4x32) Kwords |
| SA235-SA238 | 111001XXXXX | 128 (4x32) Kwords |
| SA239-SA242 | 111010XXXXX | 128 (4x32) Kwords |
| SA243-SA246 | 111011XXXXX | 128 (4x32) Kwords |
| SA247-SA250 | 111100XXXXX | 128 (4x32) Kwords |
| SA251-SA254 | 111101XXXXX | 128 (4x32) Kwords |
| SA255-SA258 | 111110XXXXX | 128 (4x32) Kwords |
| SA259 | 11111100XXX | 32 Kwords |
| SA260 | 11111101XXX | 32 Kwords |
| SA261 | 11111110XXX | 32 Kwords |
| SA262 | 11111111000 | 4 Kwords |
| SA263 | 11111111001 | 4 Kwords |
| SA264 | 11111111010 | 4 Kwords |
| SA265 | 11111111011 | 4 Kwords |

The device is shipped with all sectors unprotected. Optional Cypress programming services enable programming and protecting sectors at the factory prior to shipping the device. Contact your local sales office for details.

It is possible to determine whether a sector is protected or unprotected. See Table 19 on page 27 for details.

## 10.9 Selecting a Sector Protection Mode

**Table 22. PL064J Boot Sector/Sector Block Addresses for Protection/Unprotection**

| Sector | A21-A12 | Sector/Sector Block Size |
|---|---|---|
| SA0 | 0000000000 | 4 Kwords |
| SA1 | 0000000001 | 4 Kwords |
| SA2 | 0000000010 | 4 Kwords |
| SA3 | 0000000011 | 4 Kwords |
| SA4 | 0000000100 | 4 Kwords |
| SA5 | 0000000101 | 4 Kwords |
| SA6 | 0000000110 | 4 Kwords |
| SA7 | 0000000111 | 4 Kwords |
| SA8 | 0000001XXX | 32 Kwords |
| SA9 | 0000010XXX | 32 Kwords |
| SA10 | 0000011XXX | 32 Kwords |
| SA11-SA14 | 00001XXXXX | 128 (4x32) Kwords |
| SA15-SA18 | 00010XXXXX | 128 (4x32) Kwords |
| SA19-SA22 | 00011XXXXX | 128 (4x32) Kwords |
| SA23-SA26 | 00100XXXXX | 128 (4x32) Kwords |
| SA27-SA30 | 00101XXXXX | 128 (4x32) Kwords |
| SA31-SA34 | 00110XXXXX | 128 (4x32) Kwords |
| SA35-SA38 | 00111XXXXX | 128 (4x32) Kwords |
| SA39-SA42 | 01000XXXXX | 128 (4x32) Kwords |
| SA43-SA46 | 01001XXXXX | 128 (4x32) Kwords |
| SA47-SA50 | 01010XXXXX | 128 (4x32) Kwords |
| SA51-SA54 | 01011XXXXX | 128 (4x32) Kwords |
| SA55-SA58 | 01100XXXXX | 128 (4x32) Kwords |
| SA59-SA62 | 01101XXXXX | 128 (4x32) Kwords |
| SA63-SA66 | 01110XXXXX | 128 (4x32) Kwords |
| SA67-SA70 | 01111XXXXX | 128 (4x32) Kwords |
| SA71-SA74 | 10000XXXXX | 128 (4x32) Kwords |
| SA75-SA78 | 10001XXXXX | 128 (4x32) Kwords |
| SA79-SA82 | 10010XXXXX | 128 (4x32) Kwords |
| SA83-SA86 | 10011XXXXX | 128 (4x32) Kwords |
| SA87-SA90 | 10100XXXXX | 128 (4x32) Kwords |
| SA91-SA94 | 10101XXXXX | 128 (4x32) Kwords |
| SA95-SA98 | 10110XXXXX | 128 (4x32) Kwords |
| SA99-SA102 | 10111XXXXX | 128 (4x32) Kwords |
| SA103-SA106 | 11000XXXXX | 128 (4x32) Kwords |
| SA107-SA110 | 11001XXXXX | 128 (4x32) Kwords |
| SA111-SA114 | 11010XXXXX | 128 (4x32) Kwords |
| SA115-SA118 | 11011XXXXX | 128 (4x32) Kwords |
| SA119-SA122 | 11100XXXXX | 128 (4x32) Kwords |
| SA123-SA126 | 11101XXXXX | 128 (4x32) Kwords |
| SA127-SA130 | 11110XXXXX | 128 (4x32) Kwords |
| SA131 | 1111100XXX | 32 Kwords |
| SA132 | 1111101XXX | 32 Kwords |
| SA133 | 1111110XXX | 32 Kwords |
| SA134 | 1111111000 | 4 Kwords |
| SA135 | 1111111001 | 4 Kwords |
| SA136 | 1111111010 | 4 Kwords |
| SA137 | 1111111011 | 4 Kwords |
| SA138 | 1111111100 | 4 Kwords |

**Table 23. Sector Protection Schemes**

| DYB | PPB | PPB Lock | Sector State |
|---|---|---|---|
| 0 | 0 | 0 | Unprotected—PPB and DYB are changeable |
| 0 | 0 | 1 | Unprotected—PPB not changeable, DYB is changeable |
| 0 | 1 | 0 | Protected—PPB and DYB are changeable |
| 1 | 0 | 0 | |
| 1 | 1 | 0 | |
| 0 | 1 | 1 | Protected—PPB not changeable, DYB is changeable |
| 1 | 0 | 1 | |
| 1 | 1 | 1 | |

# 11. Sector Protection

The PL127J, PL064J, and PL032J features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups:

## 11.1 Persistent Sector Protection

A command sector protection method that replaces the old 12 V controlled protection method.

## 11.2 Password Sector Protection

A highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted

## 11.3 WP# Hardware Protection

A write protect pin that can prevent program or erase operations in sectors SA1-133, SA1-134, SA2-0 and SA2-1.

The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

## 11.4 Selecting a Sector Protection Mode

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method will be used. If the Persistent Sector Protection method is desired, programming the Persistent Sector Protection Mode Locking Bit permanently sets the device to the Persistent Sector Protection mode. If the Password Sector Protection method is desired, programming the Password Mode Locking Bit permanently sets the device to the Password Sector Protection mode. It is not possible to switch between the two protection modes once a locking bit has been set. One of the two modes must be selected when the device is first programmed. This prevents a program or virus from later setting the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.
The device is shipped with all sectors unprotected. Optional Cypress programming services enable programming and protecting sectors at the factory prior to shipping the device. Contact your local sales office for details.

It is possible to determine whether a sector is protected or unprotected. See *Autoselect Mode* on page 27 for details.

# 12. Persistent Sector Protection

The Persistent Sector Protection method replaces the 12 V controlled protection method in previous flash devices. This new method provides three different sector protection states:

- Persistently Locked—The sector is protected and cannot be changed.
- Dynamically Locked—The sector is protected and can be changed by a simple command.
- Unlocked—The sector is unprotected and can be changed by a simple command.

To achieve these states, three types of “bits” are used:

- Persistent Protection Bit
- Persistent Protection Bit Lock
- Persistent Sector Protection Mode Locking Bit

## 12.1 Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to a maximum four sectors (see the sector address tables for specific sector protection groupings). All 4 Kword boot-block sectors have individual sector Persistent Protection Bits (PPBs) for greater flexibility. Each PPB is individually modifiable through the PPB Write Command.

The device erases all PPBs in parallel. If any PPB requires erasure, the device must be instructed to preprogram all of the sector PPBs prior to PPB erasure. Otherwise, a previously erased sector PPBs can potentially be over-erased. The flash device does not have a built-in means of preventing sector PPBs over-erasure.

## 12.2 Persistent Protection Bit Lock (PPB Lock)

The Persistent Protection Bit Lock (PPB Lock) is a global volatile bit. When set to “1”, the PPBs cannot be changed. When cleared (“0”), the PPBs are changeable. There is only one PPB Lock bit per device. The PPB Lock is cleared after power-up or hardware reset. There is no command sequence to unlock the PPB Lock.

## 12.3 Dynamic Protection Bit (DYB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DYBs is “0”. Each DYB is individually modifiable through the DYB Write Command.

When the parts are first shipped, the PPBs are cleared, the DYBs are cleared, and PPB Lock is defaulted to power up in the cleared state – meaning the PPBs are changeable.

When the device is first powered on the DYBs power up cleared (sectors not protected). The Protection State for each sector is determined by the logical OR of the PPB and the DYB related to that sector. For the sectors that have the PPBs cleared, the DYBs control whether or not the sector is protected or unprotected. By issuing the DYB Write command sequences, the DYBs will be set or cleared, thus placing each sector in the protected or unprotected state. These are the so-called Dynamic Locked or Unlocked states. They are called dynamic states because it is very easy to switch back and forth between the protected and unprotected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DYBs maybe set or cleared as often as needed.

The PPBs allow for a more static, and difficult to change, level of protection. The PPBs retain their state across power cycles because they are non-volatile. Individual PPBs are set with a command but must all be cleared as a group through a complex sequence of program and erasing commands. The PPBs are also limited to 100 erase cycles.

The PPB Lock bit adds an additional level of protection. Once all PPBs are programmed to the desired settings, the PPB Lock may be set to “1”. Setting the PPB Lock disables all program and erase commands to the non-volatile PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle. System boot code can determine if any changes to the PPB are needed; for example, to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock to disable any further changes to the PPBs during system operation.

The WP#/ACC write protect pin adds a final level of hardware protection to sectors SA1-133, SA1-134, SA2-0 and SA2-1. When this pin is low it is not possible to change the contents of these sectors. These sectors generally hold system boot code. The WP#/ACC pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

For customers who are concerned about malicious viruses there is another level of security - the persistently locked state. To persistently protect a given sector or sector group, the PPBs associated with that sector need to be set to “1”. Once all PPBs are programmed to the desired settings, the PPB Lock should be set to “1”. Setting the PPB Lock automatically disables all program and erase commands to the Non-Volatile PPBs. In effect, the PPB Lock “freezes” the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Write command sequence is all that is necessary. The DYB write command for the dynamic sectors switch the DYBs to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock bit must be disabled by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB lock bit once again will lock the PPBs, and the device operates normally again.

The best protection is achieved by executing the PPB lock bit set command early in the boot code, and protect the boot code by holding WP#/ACC = VIL.

Table 23 on page 30 contains all possible combinations of the DYB, PPB, and PPB lock relating to the status of the sector.

In summary, if the PPB is set, and the PPB lock is set, the sector is protected and the protection can not be removed until the next power cycle clears the PPB lock. If the PPB is cleared, the sector can be dynamically locked or unlocked. The DYB then controls whether or not the sector is protected or unprotected.

If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1 µs before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50 µs after which the device returns to read mode without having erased the protected sector.

The programming of the DYB, PPB, and PPB lock for a given sector can be verified by writing a DYB/PPB/PPB lock verify command to the device. There is an alternative means of reading the protection status. Take RESET# to $V_{IL}$ and hold WE# at $V_{IH}$. (The high voltage A9 Autoselect Mode also works for reading the status of the PPBs). Scanning the addresses (A18–A11) while (A6, A1, A0) = (0, 1, 0) will produce a logical ‘1” code at device output DQ0 for a protected sector or a “0” for an unprotected sector. In this mode, the other addresses are don’t cares. Address location with A1 = $V_{IL}$ are reserved for autoselect manufacturer and device codes.

## 12.4 Persistent Sector Protection Mode Locking Bit

Like the password mode locking bit, a Persistent Sector Protection mode locking bit exists to guarantee that the device remain in software sector protection. Once set, the Persistent Sector Protection locking bit prevents programming of the password protection mode locking bit. This guarantees that a hacker could not place the device in password protection mode.

# 13. Password Protection Mode

The Password Sector Protection Mode method allows an even higher level of security than the Persistent Sector Protection Mode. There are two main differences between the Persistent Sector Protection and the Password Sector Protection Mode:

When the device is first powered on, or comes out of a reset cycle, the PPB Lock bit set to the locked state, rather than cleared to the unlocked state.

The only means to clear the PPB Lock bit is by writing a unique 64-bit Password to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

Once the Password Mode Locking Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear the PPB Lock bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock bit is cleared, and the PPBs can be altered. If they do not match, the flash device does nothing. There is a built-in 2 µs delay for each “password check.” This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

## 13.1 Password and Password Mode Locking Bit

In order to select the Password sector protection scheme, the customer must first program the password. The password may be correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:

Permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.

Disables all further commands to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is afterwards. If the password is lost after setting the Password Mode Locking Bit, there will be no way to clear the PPB Lock bit.

The Password Mode Locking Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Mode Locking Bit is not erasable. Once Password Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

## 13.2 64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Verify commands (see “Password Verify Command”). The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

## 13.3 Write Protect (WP#)

The Write Protect feature provides a hardware method of protecting the upper two and lower two sectors without using $V_{ID}$. This function is provided by the WP# pin and overrides the previously discussed Section 13.4 High Voltage Sector Protection on page 35 method.

If the system asserts $V_{IL}$ on the WP#/ACC pin, the device disables program and erase functions in the two outermost 4 Kword sectors on both ends of the flash array independent of whether it was previously protected or unprotected.

If the system asserts $V_{IH}$ on the WP#/ACC pin, the device reverts the upper two and lower two sectors to whether they were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected using the method described in the Section 13.4 High Voltage Sector Protection on page 35.

Note that the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

### 13.3.1 Persistent Protection Bit Lock

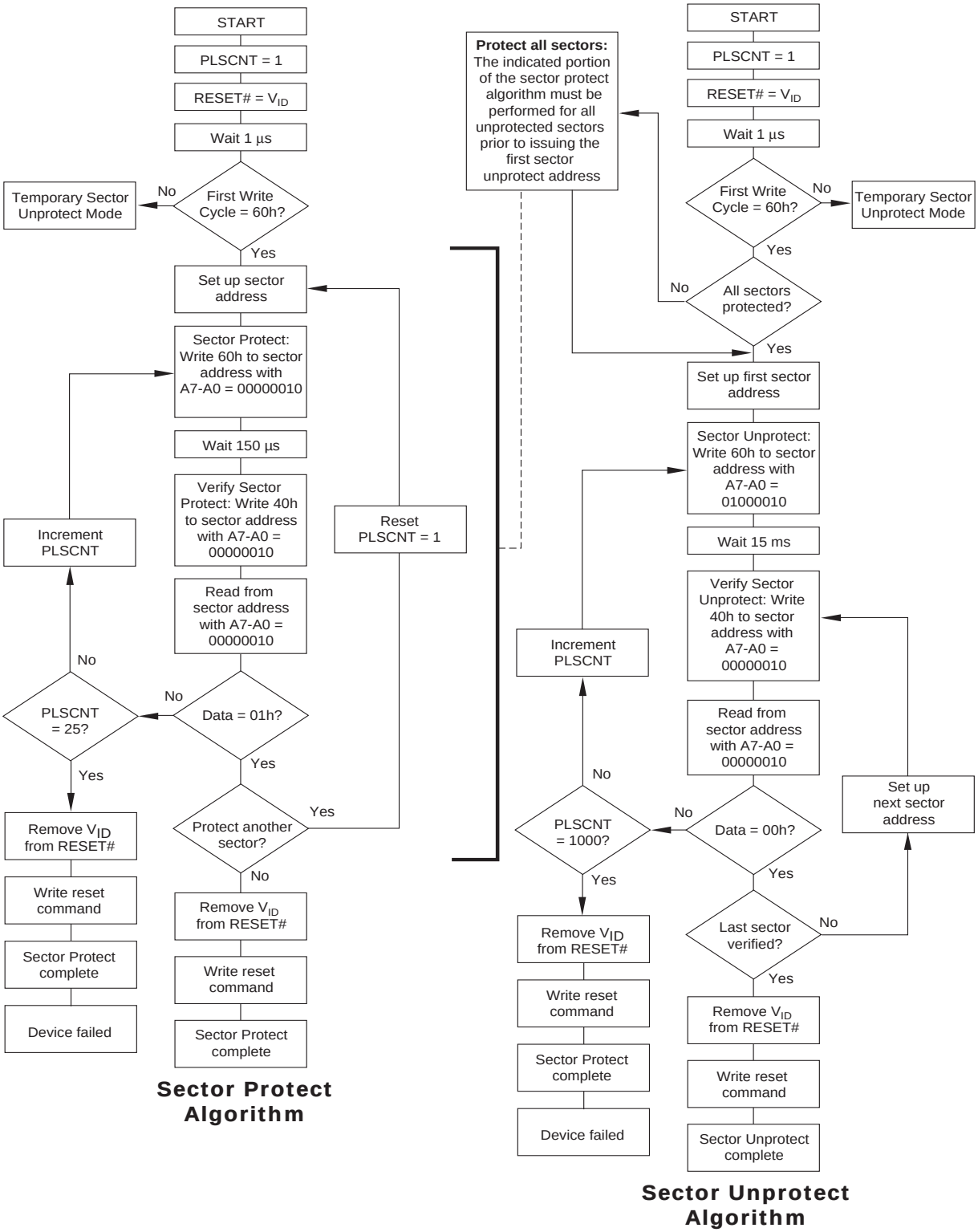
The Persistent Protection Bit (PPB) Lock is a volatile bit that reflects the state of the Password Mode Locking Bit after power-up reset. If the Password Mode Lock Bit is also set after a hardware reset (RESET# asserted) or a power-up reset, the ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command clears the PPB Lock Bit, allowing for sector PPBs modifications. Asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a “1” when the Password Mode Lock Bit is not set.

If the Password Mode Locking Bit is not set, including Persistent Protection Mode, the PPB Lock Bit is cleared after power-up or hardware reset. The PPB Lock Bit is set by issuing the PPB Lock Bit Set command. Once set the only means for clearing the PPB Lock Bit is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Protection Mode.

## 13.4 High Voltage Sector Protection

Sector protection and unprotection may also be implemented using programming equipment. The procedure requires high voltage ($V_{ID}$) to be placed on the RESET# pin. Refer to Figure 6 on page 36 for details on this procedure. Note that for sector unprotect, all unprotected sectors must first be protected prior to the first sector write cycle.

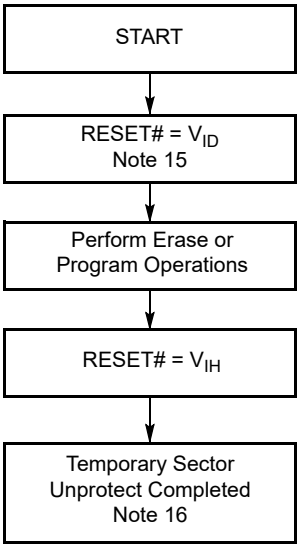
**Figure 6. In-System Sector Protection/Sector Unprotection Algorithms**



## 13.5 Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to $V_{ID}$. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once $V_{ID}$ is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 7 on page 37 shows the algorithm, and Figure 26 on page 68 shows the timing diagrams, for this feature. While PPB lock is set, the device cannot enter the Temporary Sector Unprotection Mode.

**Figure 7. Temporary Sector Unprotect Operation**[15, 16]




## 13.6 Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN) The 128-word Secured Silicon sector is divided into 64 factory-lockable words that can be programmed and locked by the customer. The Secured Silicon sector is located at addresses 000000h-00007Fh in both Persistent Protection mode and Password Protection mode. Indicator bits DQ6 and DQ7 are used to indicate the factory-locked and customer locked status of the part.

The system accesses the Secured Silicon Sector through a command sequence (see Section 15.4 Enter/Exit Secured Silicon Sector Command Sequence on page 44). After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. Once the Enter SecSi Sector Command sequence has been entered, the standard array cannot be accessed until the Exit SecSi Sector command has been entered or the device has been reset. On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Sector is enabled.*

### 13.6.1 Factory-Locked Area (64 words)

The factory-locked area of the Secured Silicon Sector (000000h-00003Fh) is locked when the part is shipped, whether or not the area was programmed at the factory. The Secured Silicon Sector Factory-locked Indicator Bit (DQ7) is permanently set to a “1”. Optional Cypress programming services can program the factory-locked area with a random ESN, a customer-defined code, or any combination of the two. Because only Cypress can program and protect the factory-locked area, this method ensures the security of the ESN once the product is shipped to the field. Contact your local sales office for details on using Cypress’s programming services. Note that the ACC function and unlock bypass modes are not available when the Secured Silicon sector is enabled.

**Notes**
15. All protected sectors unprotected (If WP#/ACC = $V_{IL}$, upper two and lower two sectors will remain protected).
16. All previously protected sectors are protected once again.

### 13.6.2 Customer-Lockable Area (64 words)

The customer-lockable area of the Secured Silicon Sector (000040h-00007Fh) is shipped unprotected, which allows the customer to program and optionally lock the area as appropriate for the application. The Secured Silicon Sector Customer-locked Indicator Bit (DQ6) is shipped as “0” and can be permanently locked to “1” by issuing the Secured Silicon Protection Bit Program Command. The Secured Silicon Sector can be read any number of times, but can be programmed and locked only once. Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the Secured Silicon Sector.

The Customer-lockable Secured Silicon Sector area can be protected using one of the following procedures:

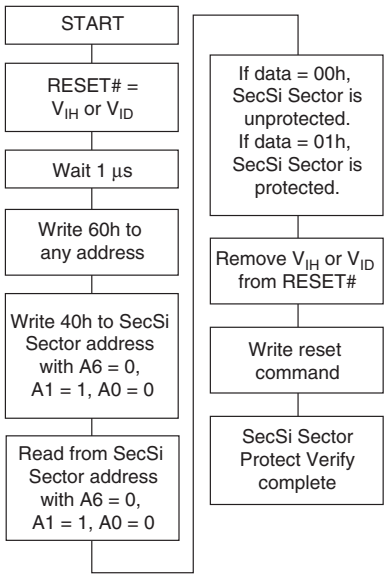
- Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 6 on page 36, except that *RESET# may be at either $V_{IH}$ or $V_{ID}$*. This allows in-system protection of the Secured Silicon Sector Region without raising any device pin to a high voltage. Note that this method is only applicable to the Secured Silicon Sector.
- To verify the protect/unprotect status of the Secured Silicon Sector, follow the algorithm shown in Figure 8 on page 38.
- Once the Secured Silicon Sector is locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing the remainder of the array.

The Secured Silicon Sector lock must be used with caution since, once locked, there is no procedure available for unlocking the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

### 13.6.3 Secured Silicon Sector Protection Bits

The Secured Silicon Sector Protection Bits prevent programming of the Secured Silicon Sector memory area. Once set, the Secured Silicon Sector memory area contents are non-modifiable.

**Figure 8. Secured Silicon Sector Protect Verify**



## 13.7 Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes. In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during $V_{CC}$ power-up and power-down transitions, or from system noise.

### 13.7.1 Low $V_{CC}$ Write Inhibit

When $V_{CC}$ is less than $V_{LKO}$, the device does not accept any write cycles. This protects data during $V_{CC}$ power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until $V_{CC}$ is greater than $V_{LKO}$. The system must provide the proper signals to the control pins to prevent unintentional writes when $V_{CC}$ is greater than $V_{LKO}$.

### 13.7.2 Write Pulse “Glitch” Protection

Noise pulses of less than 3 ns (typical) on OE#, CE#, or WE# do not initiate a write cycle.

### 13.7.3 Logical Inhibit

Write cycles are inhibited by holding any one of OE# = $V_{IL}$, CE# = $V_{IH}$ or WE# = $V_{IH}$. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

### 13.7.4 Power-Up Write Inhibit

If WE# = CE# = $V_{IL}$ and OE# = $V_{IH}$ during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

# 14. Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 24 on page 40 to Table 27 on page 42. To terminate reading CFI data, the system must write the reset command. The CFI Query mode is not accessible when the device is executing an Embedded Program or embedded Erase algorithm.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table 24 through Table 27. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100. Contact your local sales office for copies of these documents.

**Table 24. CFI Query Identification String**

| Addresses | Data | Description |
|---|---|---|
| 10h<br>11h<br>12h | 0051h<br>0052h<br>0059h | Query Unique ASCII string “QRY” |
| 13h<br>14h | 0002h<br>0000h | Primary OEM Command Set |
| 15h<br>16h | 0040h<br>0000h | Address for Primary Extended Table |
| 17h<br>18h | 0000h<br>0000h | Alternate OEM Command Set (00h = none exists) |
| 19h<br>1Ah | 0000h<br>0000h | Address for Alternate OEM Extended Table (00h = none exists) |

**Table 25. System Interface String**

| Addresses | Data | Description |
|---|---|---|
| 1Bh | 0027h | $V_{CC}$ Min. (write/erase)<br>D7–D4: volt, D3–D0: 100 millivolt |
| 1Ch | 0036h | $V_{CC}$ Max. (write/erase)<br>D7–D4: volt, D3–D0: 100 millivolt |
| 1Dh | 0000h | $V_{PP}$ Min. voltage (00h = no $V_{PP}$ pin present) |
| 1Eh | 0000h | $V_{PP}$ Max. voltage (00h = no $V_{PP}$ pin present) |
| 1Fh | 0003h | Typical timeout per single byte/word write $2^N$ µs |
| 20h | 0000h | Typical timeout for Min. size buffer write $2^N$ µs (00h = not supported) |
| 21h | 0009h | Typical timeout per individual block erase $2^N$ ms |
| 22h | 0000h | Typical timeout for full chip erase $2^N$ ms (00h = not supported) |
| 23h | 0004h | Max. timeout for byte/word write $2^N$ times typical |
| 24h | 0000h | Max. timeout for buffer write $2^N$ times typical |
| 25h | 0004h | Max. timeout per individual block erase $2^N$ times typical |
| 26h | 0000h | Max. timeout for full chip erase $2^N$ times typical (00h = not supported) |

**Table 26. Device Geometry Definition**

| Addresses | Data | Description |
|---|---|---|
| 27h | 0018h (PL127J)<br>0017h (PL064J)<br>0016h (PL032J) | Device Size = $2^N$ byte |
| 28h<br>29h | 0001h<br>0000h | Flash Device Interface description (refer to CFI publication 100) |
| 2Ah<br>2Bh | 0000h<br>0000h | Max. number of byte in multi-byte write = $2^N$<br>(00h = not supported) |
| 2Ch | 0003h | Number of Erase Block Regions within device |
| 2Dh<br>2Eh<br>2Fh<br>30h | 0007h<br>0000h<br>0020h<br>0000h | Erase Block Region 1 Information<br>(refer to the CFI specification or CFI publication 100) |
| 31h | 00FDh (PL127J)<br>007Dh (PL064J)<br>003Dh (PL032J) | Erase Block Region 2 Information<br>(refer to the CFI specification or CFI publication 100) |
| 32h<br>33h<br>34h | 0000h<br>0000h<br>0001h | |
| 35h<br>36h<br>37h<br>38h | 0007h<br>0000h<br>0020h<br>0000h | Erase Block Region 3 Information<br>(refer to the CFI specification or CFI publication 100) |
| 39h<br>3Ah<br>3Bh<br>3Ch | 0000h<br>0000h<br>0000h<br>0000h | Erase Block Region 4 Information<br>(refer to the CFI specification or CFI publication 100) |

**Table 27. Primary Vendor-Specific Extended Query**

| Addresses | Data | Description |
|---|---|---|
| 40h<br>41h<br>42h | 0050h<br>0052h<br>0049h | Query-unique ASCII string “PRI” |
| 43h | 0031h | Major version number, ASCII (reflects modifications to the silicon) |
| 44h | 0033h | Minor version number, ASCII (reflects modifications to the CFI table) |
| 45h | TBD | Address Sensitive Unlock (Bits 1-0)<br>0 = Required, 1 = Not Required<br>Silicon Revision Number (Bits 7-2) |
| 46h | 0002h | Erase Suspend<br>0 = Not Supported, 1 = To Read Only, 2 = To Read & Write |
| 47h | 0001h | Sector Protect<br>0 = Not Supported, X = Number of sectors in per group |
| 48h | 0001h | Sector Temporary Unprotect<br>00 = Not Supported, 01 = Supported |
| 49h | 0007h (PLxxxJ) | Sector Protect/Unprotect scheme<br>07 = Advanced Sector Protection |
| 4Ah | 00E7h (PL127J)<br>0077h (PL064J)<br>003Fh (PL032J) | Simultaneous Operation<br>00 = Not Supported, X = Number of Sectors excluding Bank 1 |
| 4Bh | 0000h | Burst Mode Type<br>00 = Not Supported, 01 = Supported |
| 4Ch | 0002h (PLxxxJ) | Page Mode Type<br>00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page |
| 4Dh | 0085h | ACC (Acceleration) Supply Minimum<br>00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV |
| 4Eh | 0095h | ACC (Acceleration) Supply Maximum<br>00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV |
| 4Fh | 0001h | Top/Bottom Boot Sector Flag<br>00h = Uniform device, 01h = Both top and bottom boot with write protect,<br>02h = Bottom Boot Device, 03h = Top Boot Device,<br>04h = Both Top and Bottom |
| 50h | 0001h | Program Suspend<br>0 = Not supported, 1 = Supported |
| 57h | 0004h | Bank Organization<br>00 = Data at 4Ah is zero, X = Number of Banks |
| 58h | 0027h (PL127J)<br>0017h (PL064J)<br>000Fh (PL032J) | Bank 1 Region Information<br>X = Number of Sectors in Bank 1 |
| 59h | 0060h (PL127J)<br>0030h (PL064J)<br>0018h (PL032J) | Bank 2 Region Information<br>X = Number of Sectors in Bank 2 |
| 5Ah | 0060h (PL127J)<br>0030h (PL064J)<br>0018h (PL032J) | Bank 3 Region Information<br>X = Number of Sectors in Bank 3 |
| 5Bh | 0027h (PL127J)<br>0017h (PL064J)<br>000Fh (PL032J) | Bank 4 Region Information<br>X = Number of Sectors in Bank 4 |

# 15. Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 28 on page 49 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** may place the device in an unknown state. A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to Section 20. AC Characteristics on page 60 for timing diagrams.

## 15.1 Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. The system can read array data using the standard read timing, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See Section 15.8 Erase Suspend/Erase Resume Commands on page 47 for more information.

After the device accepts a Program Suspend command, the corresponding bank enters the program-suspend-read mode, after which the system can read data from any non-program-suspended sector within the same bank. See Section 15.9 Program Suspend/Program Resume Commands on page 48 for more information.

The system *must* issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See Section 15.2 Reset Command on page 43 for more information.

See also Section 10.1 Requirements for Reading Array Data on page 18 for more information. Section 20. AC Characteristics on page 60 provides the read parameters, and Figure 12 on page 54 shows the timing diagram.

## 15.2 Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend and program-suspend-read mode if that bank was in Program Suspend).

## 15.3 Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read any number of autoselect codes without reinitiating the command sequence.

Table 28 on page 49 shows the address and data requirements. To determine sector protection information, the system must write to the appropriate bank address (BA) and sector address (SA). Table 15 on page 19 shows the address range and bank number associated with each sector.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

## 15.4 Enter/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing a random, eight word electronic serial number (ESN). The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. The Secured Silicon Sector is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. Table 28 on page 49 shows the address and data requirements for both command sequences. See also Section 13.6 Secured Silicon Sector Flash Memory Region on page 37 for further information. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Sector is enabled.*

## 15.5 Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 28 on page 49 shows the address and data requirements for the program command sequence. *Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.*

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to Section 16. Write Operation Status on page 52 for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity. Note that the Secured Silicon Sector, autoselect and CFI functions are unavailable when the Secured Silicon Sector is enabled.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from “0” back to a “1.”** Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still “0.” Only erase operations can convert a “0” to a “1.”

### 15.5.1 Unlock Bypass Command Sequence

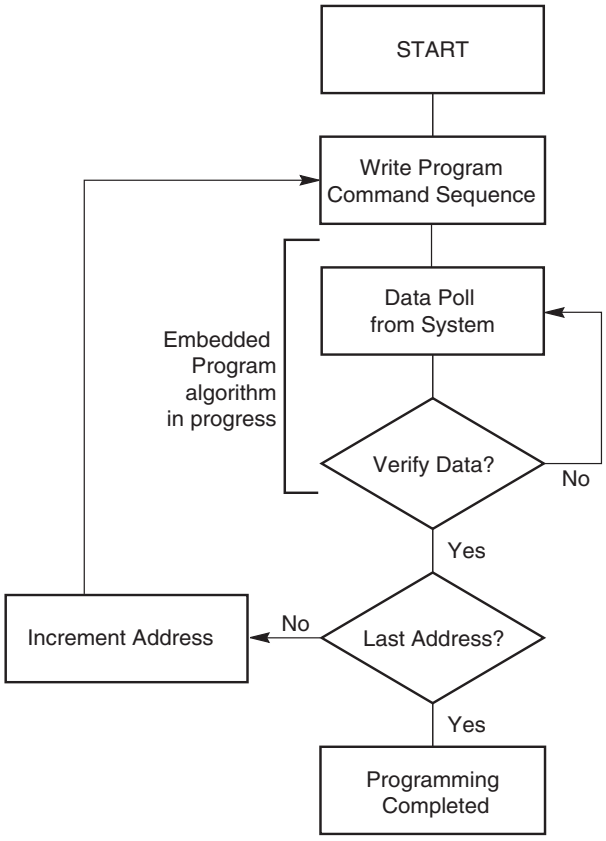
The unlock bypass feature allows the system to program data to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 28 on page 49 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. (See Table 29 on page 50)

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts $V_{HH}$ on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. *Note that the WP#/ACC pin must not be at $V_{HH}$ any operation other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.*

Figure 9 on page 45 illustrates the algorithm for the program operation. Refer to the table Section 20.5 Erase/Program Operations on page 64 for parameters, and Figure 19 on page 65 for timing diagrams.

**Figure 9. Program Operation**[17]




**Note**
17. See Table 28 on page 49 for program command sequence.

## 15.6 Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 28 on page 49 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or
RY/BY#. Refer to Section 16. Write Operation Status on page 52 for information on these status bits.

Any commands written during the chip erase operation are ignored. *Note that Secured Silicon Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.* However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 10 on page 47 illustrates the algorithm for the erase operation. Refer to the tables in Section 20.5 Erase/Program Operations on page 64 for parameters, and Figure 21 on page 66 for timing diagrams.

## 15.7 Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 28 on page 49 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **If any command other than 30h, B0h, F0h is input during the time-out period, the normal operation will not be guaranteed.** The system must rewrite the command sequence and any additional addresses and commands. *Note that Secured Silicon Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.*

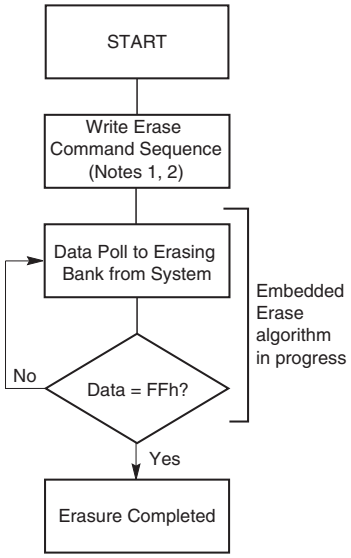
The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing bank. The system can determine the status of the erase operation by reading DQ7, DQ6, DQ2, or RY/BY# in the erasing bank. Refer to Section 16. Write Operation Status on page 52 for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 2 on page 12 illustrates the algorithm for the erase operation. Refer to the tables in Section 20.5 Erase/Program Operations on page 64 for parameters, and Figure 21 on page 66 for timing diagrams.

**Figure 10. Erase Operation**




## 15.8 Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 35 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. Addresses are “don’t-cares” when writing the Erase suspend command.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to Section 16. Write Operation Status on page 52 for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard Word Program operation. Refer to Section 16. Write Operation Status on page 52 for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. Refer to Table 19 on page 27 and Section 15.3 Autoselect Command Sequence on page 43 for details.

To resume the sector erase operation, the system must write the Erase Resume command (address bits are don’t care). The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

**Notes**
18. See Table 28 on page 49 for erase command sequence.
19. See the section on DQ3 for information on the sector erase timer.

*If the Persistent Sector Protection Mode Locking Bit is verified as programmed without margin, the Persistent Sector Protection Mode Locking Bit Program Command should be reissued to improve program margin. If the Secured Silicon Sector Protection Bit is verified as programmed without margin, the Secured Silicon Sector Protection Bit Program Command should be reissued to improve program margin.* μμ*After programming a PPB, two additional cycles are needed to determine whether the PPB has been programmed with margin. If the PPB has been programmed without margin, the program command should be reissued to improve the program margin. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed.*

After erasing the PPBs, two additional cycles are needed to determine whether the PPB has been erased with margin. If the PPBs has been erased without margin, the erase command should be reissued to improve the program margin. The programming of either the PPB or DYB for a given sector or sector group can be verified by writing a Sector Protection Status command to the device.

Note that there is no single command to independently verify the programming of a DYB for a given sector group.

## 15.9 Program Suspend/Program Resume Commands

The Program Suspend command allows the system to interrupt an embedded programming operation so that data can read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the programming operation within $t_{PSL}$ (program suspend latency) and updates the status bits. Addresses are “don’t-cares” when writing the Program Suspend command. After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area, then user must use the proper command sequences to enter and exit this region. The system may also write the autoselect command sequence when the device is in Program Suspend mode. The device allows reading autoselect codes in the suspended sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to Program Suspend mode, and is ready for another valid operation. See Section 15.3 Autoselect Command Sequence on page 43 for more information. After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Section 16. Write Operation Status on page 52 for more information. The system must write the Program Resume command (address bits are “don’t care”) to exit the Program Suspend mode and continue the programming operation. Further writes of the Program Resume command are ignored. Another Program Suspend command can be written after the device has resumed programming.

## 15.10 Command Definitions Tables

Table 28 contains the Memory Array Command Definitions.

**Table 28. Memory Array Command Definitions**

| Command (Notes) | | Cycles | Bus Cycles (Notes 20–23) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Read[24] | | 1 | RA | RD | | | | | | | | | | |
| Reset[25] | | 1 | XXX | F0 | | | | | | | | | | |
| Autoselect[26] | Manufacturer ID | 4 | 555 | AA | 2AA | 55 | (BA) 555 | 90 | (BA) X00 | 01 | | | | |
| | Device ID[29] | 6 | 555 | AA | 2AA | 55 | (BA) 555 | 90 | (BA) X01 | 227E | (BA) X0E | Note [29] | (BA) X0F | Note [29] |
| | Secured Silicon Sector Factory Protect[27] | 4 | 555 | AA | 2AA | 55 | (BA) 555 | 90 | X03 | Note [27] | | | | |
| | Sector Group Protect Verify[28] | 4 | 555 | AAA | 2AA | 55 | (BA) 555 | 90 | (SA) X02 | XX00/ XX01 | | | | |
| Program | | 4 | 555 | AA | 2AA | 55 | 555 | A0 | PA | PD | | | | |
| Chip Erase | | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | 555 | 10 |
| Sector Erase | | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | SA | 30 |
| Program/Erase Suspend[30] | | 1 | BA | B0 | | | | | | | | | | |
| Program/Erase Resume[31] | | 1 | BA | 30 | | | | | | | | | | |
| CFI Query[32] | | 1 | 55 | 98 | | | | | | | | | | |
| Accelerated Program[33] | | 2 | XX | A0 | PA | PD | | | | | | | | |
| Unlock Bypass Entry[33] | | 3 | 555 | AA | 2AA | 55 | 555 | 20 | | | | | | |
| Unlock Bypass Program[33] | | 2 | XX | A0 | PA | PD | | | | | | | | |
| Unlock Bypass Erase[33] | | 2 | XX | 80 | XX | 10 | | | | | | | | |
| Unlock Bypass CFI[32, 33] | | 1 | XX | 98 | | | | | | | | | | |
| Unlock Bypass Reset[33] | | 2 | XXX | 90 | XXX | 00 | | | | | | | | |

**Legend**

BA = Address of bank switching to autoselect mode, bypass mode, or erase operation. Determined by PL127J: Amax:A20, PL064J: Amax:A19, PL032J: Amax:A18.

PA = Program Address (Amax:A0). Addresses latch on falling edge of WE# or CE# pulse, whichever happens later.

PD = Program Data (DQ15:DQ0) written to location PA. Data latches on rising edge of WE# or CE# pulse, whichever happens first.

RA = Read Address (Amax:A0).

RD = Read Data (DQ15:DQ0) from location RA.

SA = Sector Address (Amax:A12) for verifying (in autoselect mode) or erasing.

WD = Write Data. See “Configuration Register” definition for specific write data. Data latched on rising edge of WE#.

X = Don’t care

**Notes**

20. See Table 13 for description of bus operations.
21. All values are in hexadecimal.
22. Shaded cells in table denote read cycles. All other cycles are write operations.
23. During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don’t cares.
24. No unlock or command cycles required when bank is reading array data.
25. The Reset command is required to return to reading array (or to erase-suspend-read mode if previously in Erase Suspend) when bank is in autoselect mode, or if DQ5 goes high (while bank is providing status information).
26. Fourth cycle of autoselect command sequence is a read cycle. System must provide bank address to obtain manufacturer ID or device ID information. See Section 15.3 Autoselect Command Sequence on page 43 for more information.
27. The data is DQ6=1 for factory and customer locked and DQ7=1 for factory locked.
28. The data is 00h for an unprotected sector group and 01h for a protected sector group.
29. Device ID must be read across cycles 4, 5, and 6. PL127J (X0Eh = 2220h, X0Fh = 2200h), PL064J (X0Eh = 2202h, X0Fh = 2201h), PL032J (X0Eh = 220Ah, X0Fh = 2201h).
30. System may read and program in non-erasing sectors, or enter autoselect mode, when in Program/Erase Suspend mode. Program/Erase Suspend command is valid only during a sector erase operation, and requires bank address.
31. Program/Erase Resume command is valid only during Erase Suspend mode, and requires bank address.
32. Command is valid when device is ready to read array data or when device is in autoselect mode.
33. WP#/ACC must be at $V_{ID}$ during the entire operation of command.

### Table 29. Sector Protection Command Definitions

| Command (Notes) | Cycles | Bus Cycles (Notes 34-37) | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Reset | 1 | XXX | F0 | | | | | | | | | | | | |
| Secured Silicon Sector Entry[49] | 3 | 555 | AA | 2AA | 55 | 555 | 88 | | | | | | | | |
| Secured Silicon Sector Exit[49] | 4 | 555 | AA | 2AA | 55 | 555 | 90 | XX | 00 | | | | | | |
| Secured Silicon Protection Bit Program[38, 39] | 6 | 555 | AA | 2AA | 55 | 555 | 60 | OW | 68 | OW | 48 | OW | RD (0) | | |
| Secured Silicon Protection Bit Status | 5 | 555 | AA | 2AA | 55 | 555 | 60 | OW | 48 | OW | RD (0) | | | | |
| Password Program[38, 40, 41] | 4 | 555 | AA | 2AA | 55 | 555 | 38 | XX [0-3] | PD [0-3] | | | | | | |
| Password Verify[39, 41, 42] | 4 | 555 | AA | 2AA | 55 | 555 | C8 | PWA [0-3] | PWD [0-3] | | | | | | |
| Password Unlock[40, 43, 44] | 7 | 555 | AA | 2AA | 55 | 555 | 28 | PWA [0] | PWD [0] | PWA [1] | PWD [1] | PWA [2] | PWD [2] | PWA [3] | PWD [3] |
| PPB Program[38, 39, 44] | 6 | 555 | AA | 2AA | 55 | 555 | 60 | (SA) WP | 68 | (SA) WP | 48 | (SA) WP | RD(0) | | |
| PPB Status | 4 | 555 | AA | 2AA | 55 | BA+555 | 90 | (SA) WP | RD (0) | | | | | | |
| All PPB Erase[38, 39, 46, 47] | 6 | 555 | AA | 2AA | 55 | 555 | 60 | WP | 60 | (SA) | 40 | (SA) WP | RD(0) | | |
| PPB Lock Bit Set | 3 | 555 | AA | 2AA | 55 | 555 | 78 | | | | | | | | |
| PPB Lock Bit Status[48] | 4 | 555 | AA | 2AA | 55 | BA+555 | 58 | SA | RD (1) | | | | | | |
| DYB Write[40] | 4 | 555 | AA | 2AA | 55 | 555 | 48 | SA | X1 | | | | | | |
| DYB Erase[40] | 4 | 555 | AA | 2AA | 55 | 555 | 48 | SA | X0 | | | | | | |
| DYB Status[39] | 4 | 555 | AA | 2AA | 55 | BA+555 | 58 | SA | RD (0) | | | | | | |
| PPMLB Program[38, 39, 45] | 6 | 555 | AA | 2AA | 55 | 555 | 60 | PL | 68 | PL | 48 | PL | RD(0) | | |
| PPMLB Status[38] | 5 | 555 | AA | 2AA | 55 | 555 | 60 | PL | 48 | PL | RD (0) | | | | |
| SPMLB Program[38, 39, 45] | 6 | 555 | AA | 2AA | 55 | 555 | 60 | SL | 68 | SL | 48 | SL | RD(0) | | |
| SPMLB Status[38] | 5 | 555 | AA | 2AA | 55 | 555 | 60 | SL | 48 | SL | RD (0) | | | | |

**Legend**

DYB = Dynamic Protection Bit
OW = Address (A7:A0) is (00011010)
PD[3:0] = Password Data (1 of 4 portions)
PPB = Persistent Protection Bit
PWA = Password Address. A1:A0 selects portion of password.
PWD = Password Data being verified.
PL = Password Protection Mode Lock Address (A7:A0) is (00001010)
RD(0) = Read Data DQ0 for protection indicator bit.
RD(1) = Read Data DQ1 for PPB Lock status.
SA = Sector Address where security command applies. Address bits Amax:A12 uniquely select any sector.
SL = Persistent Protection Mode Lock Address (A7:A0) is (00010010)
WP = PPB Address (A7:A0) is (00000010)
X = Don't care
PPMLB = Password Protection Mode Locking Bit
SPMLB = Persistent Protection Mode Locking Bit

**Notes**

34. See Table 13 on page 18 for description of bus operations.
35. All values are in hexadecimal.
36. Shaded cells in table denote read cycles. All other cycles are write operations.
37. During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.
38. The reset command returns device to reading array.
39. Cycle 4 programs the addressed locking bit. Cycles 5 and 6 validate bit has been fully programmed when DQ0 = 1. If DQ0 = 0 in cycle 6, program command must be issued and verified again.
40. Data is latched on the rising edge of WE#.
41. Entire command sequence must be entered for each portion of password.
42. Command sequence returns FFh if PPMLB is set.
43. The password is written over four consecutive cycles, at addresses 0-3.
44. A 2 µs timeout is required between any two portions of password.
45. A 100 µs timeout is required between cycles 4 and 5.
46. A 1.2 ms timeout is required between cycles 4 and 5.
47. Cycle 4 erases all PPBs. Cycles 5 and 6 validate bits have been fully erased when DQ0 = 0. If DQ0 = 1 in cycle 6, erase command must be issued and verified again. Before issuing erase command, all PPBs should be programmed to prevent PPB overerasure.
48. DQ1 = 1 if PPB locked, 0 if unlocked.
49. Once the Secured Silicon Sector Entry Command sequence has been entered, the standard array cannot be accessed until the Exit SecSi Sector command has been entered or the device has been reset.

# 16. Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 30 on page 56 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

## 16.1 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

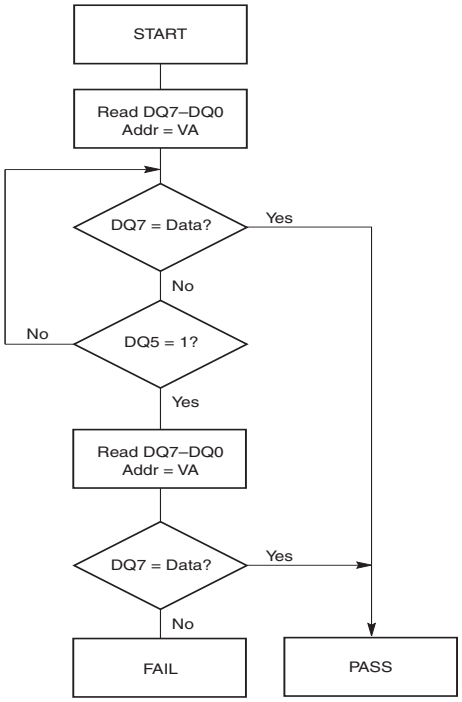
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 400 µs, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ15–DQ0 on the *following* read cycles. Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ15–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ15–DQ0 may be still invalid. Valid data on DQ15–DQ0 will appear on successive read cycles. Table 30 on page 56 shows the outputs for Data# Polling on DQ7. Figure 11 on page 52 shows the Data# Polling algorithm. Figure 23 on page 67 shows the Data# Polling timing diagram.

**Figure 11. Data# Polling Algorithm**[50, 51]




**Notes**

50. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.
51. DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.

## 16.2 RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to $V_{CC}$.

If the output is low (Busy), the device is actively erasing or programming. This includes programming in the Erase Suspend mode. If the output is high (Ready), the device is in the read mode, the standby mode, or one of the banks is in the erase-suspend-read mode.

Table 30 on page 56 shows the outputs for RY/BY#.

## 16.3 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 400 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

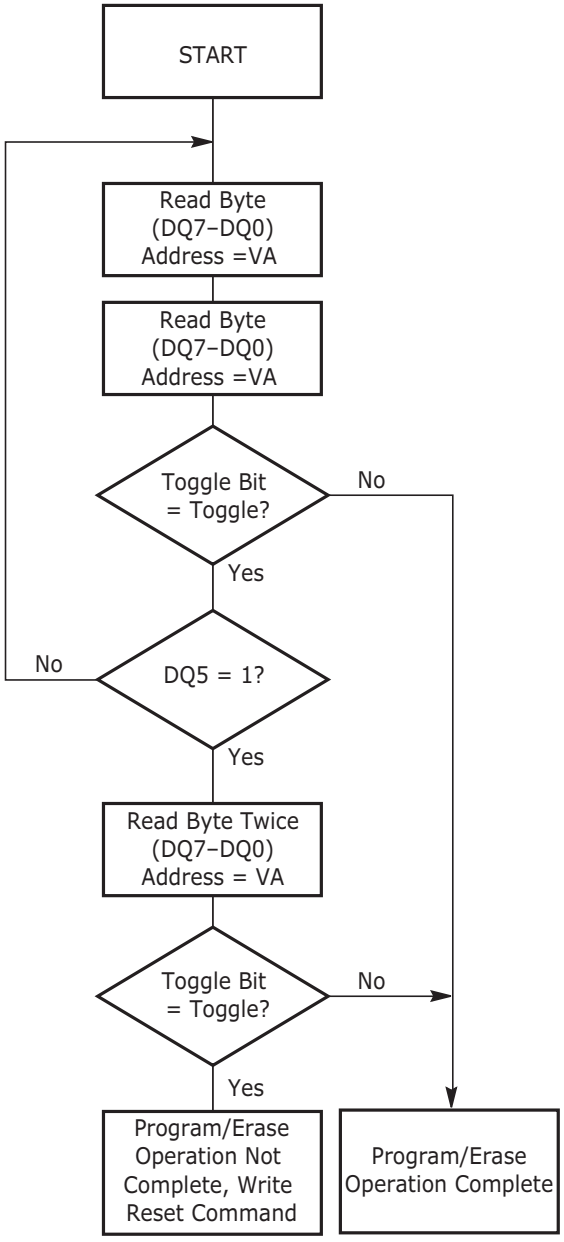
The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the Section 16.1 DQ7: Data# Polling on page 52).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 30 on page 56 shows the outputs for Toggle Bit I on DQ6. Figure 12 on page 54 shows the toggle bit algorithm. Figure 24 on page 67 in shows the toggle bit timing diagrams. Figure 25 on page 68 shows the differences between DQ2 and DQ6 in graphical form. See also Section 16.4 DQ2: Toggle Bit II on page 55.

**Figure 12. Toggle Bit Algorithm**[52]




**Note**

52. The system should recheck the toggle bit even if DQ5 = “1” because the toggle bit may stop toggling as DQ5 changes to “1.” See the Section 16.3 DQ6: Toggle Bit I on page 53 and Section 16.4 DQ2: Toggle Bit II on page 55 for more information.

## 16.4 DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 30 on page 56 to compare outputs for DQ2 and DQ6.

Figure 12 on page 54 shows the toggle bit algorithm in flowchart form, and the Section 16.4 DQ2: Toggle Bit II on page 55 explains the algorithm. See also the Section 16.3 DQ6: Toggle Bit I on page 53. Figure 24 on page 67 shows the toggle bit timing diagram. Figure 25 on page 68 shows the differences between DQ2 and DQ6 in graphical form.

## 16.5 Reading Toggle Bits DQ6/DQ2

Refer to Figure 12 on page 54 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the devic did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 12).

## 16.6 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1,” indicating that the program or erase cycle was not successfully completed.

The device may output a “1” on DQ5 if the system tries to program a “1” to a location that was previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a “1.”

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

## 16.7 DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a “0” to a “1.” See also Section 15.7 Sector Erase Command Sequence on page 46.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is “1,” the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0,” the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 30 shows the status of DQ3 relative to the other status bits.

**Table 30. Write Operation Status**

| Status | | | DQ7[54] | DQ6 | DQ5[53] | DQ3 | DQ2[54] | RY/BY# |
|---|---|---|---|---|---|---|---|---|
| Standard Mode | Embedded Program Algorithm | | DQ7# | Toggle | 0 | N/A | No toggle | 0 |
| | Embedded Erase Algorithm | | 0 | Toggle | 0 | 1 | Toggle | 0 |
| Erase Suspend Mode | Erase Suspend-Read | Erase Suspended Sector | 1 | No toggle | 0 | N/A | Toggle | 1 |
| | | Non-Erase Suspended Sector | Data | Data | Data | Data | Data | 1 |
| | Erase-Suspend -Program | | DQ7# | Toggle | 0 | N/A | N/A | 0 |
| Program Suspend Mode[55] | Reading within Program Suspended Sector | | Invalid (Not Allowed) | Invalid (Not Allowed) | Invalid (Not Allowed) | Invalid (Not Allowed) | Invalid (Not Allowed) | 1 |
| | Reading within Non-program Suspended Sector | | Data | Data | Data | Data | Data | 1 |

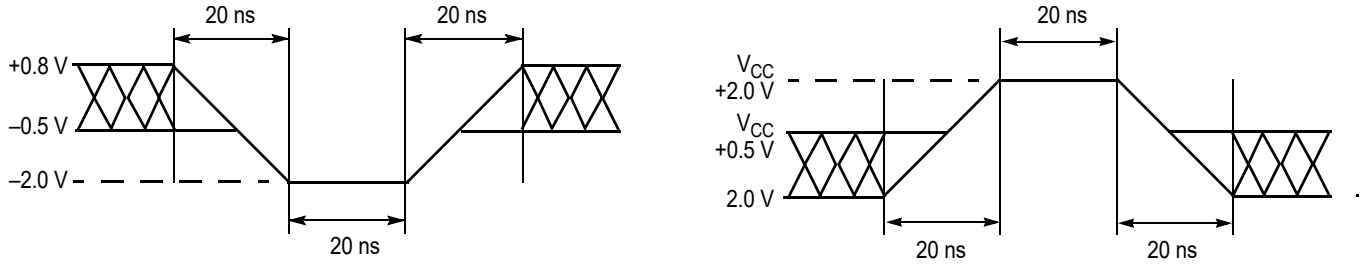
**Notes**

53. DQ5 switches to ‘1’ when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to Section 16.6 DQ5: Exceeded Timing Limits on page 55 for more information.
54. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
55. When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.

# 17. Absolute Maximum Ratings

| | |
|---|---|
| Storage Temperature Plastic Packages | –65°C to +150°C |
| Ambient Temperature with Power Applied | –65°C to +125°C |
| Voltage with Respect to Ground | |
| $V_{CC}$[56] | –0.5 V to +4.0 V |
| A9, OE#, and RESET#[57] | –0.5 V to +12.5 V |
| WP#/ACC[57] | –0.5 V to +10.5 V |
| All other pins[56] | –0.5 V to $V_{CC}$ +0.5 V |
| Output Short Circuit Current[58] | 200 mA |

**Figure 13. Maximum Overshoot Waveforms**




Maximum Negative Overshoot Waveform

Maximum Positive Overshoot Waveform

**Notes**

56. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot $V_{SS}$ to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is $V_{CC}$ +0.5 V. During voltage transitions, input or I/O pins may overshoot to $V_{CC}$ +2.0 V for periods up to 20 ns. See Figure 13 on page 57.
57. Minimum DC input voltage on pins A9, OE#, RESET#, and WP#/ACC is –0.5 V. During voltage transitions, A9, OE#, WP#/ACC, and RESET# may overshoot $V_{SS}$ to –2.0 V for periods of up to 20 ns. See Figure 13 on page 57. Maximum DC input voltage on pin A9, OE#, and RESET# is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns. Maximum DC input voltage on WP#/ACC is +9.5 V which may overshoot to +12.0 V for periods up to 20 ns.
58. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
59. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

# 18. Operating Ranges

Operating ranges define those limits between which the functionality of the device is guaranteed.

### Industrial (I) Devices

Ambient Temperature ($T_A$)..... –40°C to +85°C

### Wireless (W) Devices

Ambient Temperature ($T_A$)..... –25°C to +85°C

### Supply Voltages

$V_{CC}$ .....2.7–3.6 V

$V_{IO}$ (see Note)1.65–1.95 V (for PL127J) or 2.7–3.6 V (for all PLxxxJ devices)

**Note**

60. For all AC and DC specifications, $V_{IO} = V_{CC}$; contact your local sales office for other $V_{IO}$ options.

# 19. DC Characteristics

**Table 31. CMOS Compatible**

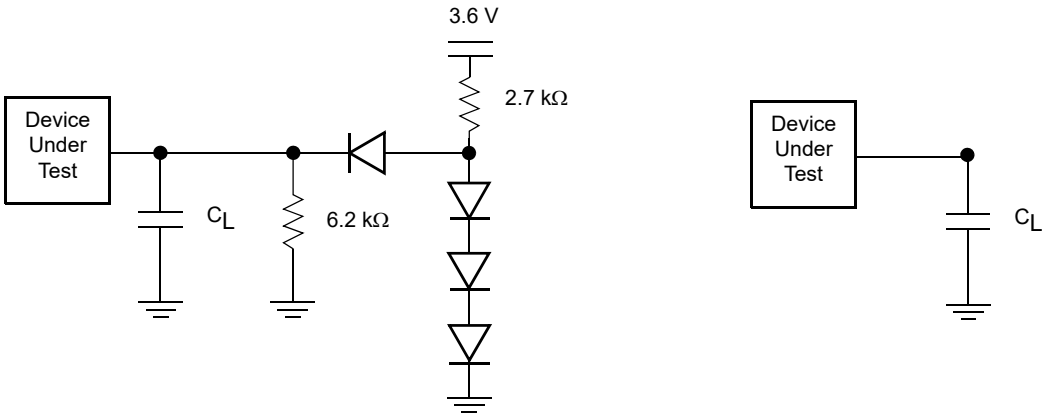
| Parameter | Parameter Description (notes) | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN} = V_{SS}$ to $V_{CC}$, $V_{CC} = V_{CC\ max}$ | | | | ±1.0 | µA |
| $I_{LIT}$ | A9, OE#, RESET# Input Load Current | $V_{CC} = V_{CC\ max}$; $V_{ID}$= 12.5 V | | | | 35 | µA |
| $I_{LR}$ | Reset Leakage Current | $V_{CC} = V_{CC\ max}$; $V_{ID}$= 12.5 V | | | | 35 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT} = V_{SS}$ to $V_{CC}$, OE# = $V_{IH}$ $V_{CC} = V_{CC\ max}$ | | | | ±1.0 | µA |
| $I_{CC1}$ | $V_{CC}$ Active Read Current[61, 62] | OE# = $V_{IH}$, $V_{CC} = V_{CC\ max}$ | 5 MHz | | 20 | 30 | mA |
| | | | 10 MHz | | 45 | 55 | |
| $I_{CC2}$ | $V_{CC}$ Active Write Current[62, 63] | OE# = $V_{IH}$, WE# = $V_{IL}$ | | | 15 | 25 | mA |
| $I_{CC3}$ | $V_{CC}$ Standby Current[62] | CE#, RESET#, WP#/ACC = $V_{IO}$ ± 0.3 V | | | 0.2 | 5 | µA |
| $I_{CC4}$ | $V_{CC}$ Reset Current[62] | RESET# = $V_{SS}$ ± 0.3 V | | | 0.2 | 5 | µA |
| $I_{CC5}$ | Automatic Sleep Mode[62, 64] | $V_{IH} = V_{IO}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V | | | 0.2 | 5 | µA |
| $I_{CC6}$ | $V_{CC}$ Active Read-While-Program Current[61, 62] | OE# = $V_{IH}$, | 5 MHz | | 21 | 45 | mA |
| | | | 10 MHz | | 46 | 70 | |
| $I_{CC7}$ | $V_{CC}$ Active Read-While-Erase Current[61, 62] | OE# = $V_{IH}$, | 5 MHz | | 21 | 45 | mA |
| | | | 10 MHz | | 46 | 70 | |
| $I_{CC8}$ | $V_{CC}$ Active Program-While-Erase-Suspended Current[62, 65] | OE# = $V_{IH}$ | | | 17 | 25 | mA |
| $I_{CC9}$ | $V_{CC}$ Active Page Read Current[62] | OE# = $V_{IH}$, 8 word Page Read | | | 10 | 15 | mA |
| $V_{IL}$ | Input Low Voltage | $V_{IO}$ = 1.65–1.95 V (PL127J) | | –0.4 | | 0.4 | V |
| | | $V_{IO}$ = 2.7–3.6 V | | –0.5 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | $V_{IO}$ = 1.65–1.95 V (PL127J) | | $V_{IO}$–0.4 | | $V_{IO}$+0.4 | V |
| | | $V_{IO}$ = 2.7–3.6 V | | 2.0 | | $V_{CC}$+0.3 | V |
| $V_{HH}$ | Voltage for ACC Program Acceleration | $V_{CC}$ = 3.0 V ± 10% | | 8.5 | | 9.5 | V |
| $V_{ID}$ | Voltage for Autoselect and Temporary Sector Unprotect | $V_{CC}$ = 3.0 V ± 10% | | 11.5 | | 12.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 100 µA, $V_{CC} = V_{CC\ min}$, $V_{IO}$ = 1.65–1.95 V (PL127J) | | | | 0.1 | V |
| | | $I_{OL}$ = 2.0 mA, $V_{CC} = V_{CC\ min}$, $V_{IO}$ = 2.7–3.6 V | | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –100 µA, $V_{CC} = V_{CC\ min}$, $V_{IO}$ = 1.65–1.95 V (PL127J) | | $V_{IO}$–0.1 | | | V |
| | | $I_{OH}$ = —100 µA, $V_{IO} = V_{CC\ min}$ | | $V_{CC}$–0.2V | | | V |
| $V_{LKO}$ | Low $V_{CC}$ Lock-Out Voltage[65] | | | 2.3 | | 2.5 | V |

**Notes**
61. The $I_{CC}$ current listed is typically less than 5 mA/MHz, with OE# at $V_{IH}$.
62. Maximum $I_{CC}$ specifications are tested with $V_{CC} = V_{CCmax}$.
63. $I_{CC}$ active while Embedded Erase or Embedded Program is in progress.
64. Automatic sleep mode enables the low power mode when addresses remain stable for $t_{ACC}$ + 30 ns. Typical sleep mode current is 2 µA.
65. Not 100% tested.

# 20. AC Characteristics

## 20.1 Test Conditions

**Figure 14. Test Setups**[66]




**$V_{IO}$ = 3.0 V** **$V_{IO}$ = 1.8 V (PL127J)**

**Table 32. Test Specifications**

| Test Conditions | | All Speeds | Unit |
|---|---|---|---|
| Output Load | | 1 TTL gate | |
| Output Load Capacitance, $C_L$ (including jig capacitance) | | 30 | pF |
| Input Rise and Fall Times | $V_{IO}$ = 1.8 V (PL127J) | 5 | ns |
| | $V_{IO}$ = 3.0 V | | |
| Input Pulse Levels | $V_{IO}$ = 1.8 V (PL127J) | 0.0 - 1.8 | V |
| | $V_{IO}$ = 3.0 V | 0.0–3.0 | |
| Input timing measurement reference levels | | $V_{IO}/2$ | V |
| Output timing measurement reference levels | | $V_{IO}/2$ | V |

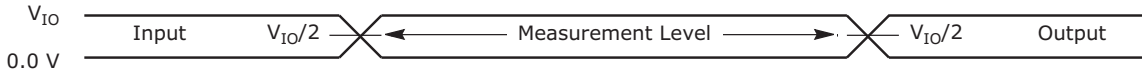
**Note**
66. Diodes are IN3064 or equivalent.

## 20.2 Switching Waveforms

**Table 33. Key To Switching Waveforms**

| Waveform | Inputs | Outputs |
|---|---|---|
| | Steady | |
| | Changing from H to L | |
| | Changing from L to H | |
| | Don't Care, Any Change Permitted | Changing, State Unknown |
| | Does Not Apply | Center Line is High Impedance State (High Z) |

**Figure 15. Input Waveforms and Measurement Levels**




## 20.3 Read Operations

**Table 34. Read-Only Operations**

| Parameter | | Description (Notes) | | Test Setup | | Speed Options | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Std. | | | | | 55 | 60 | 65 | 70 | 80 | |
| $t_{AVAV}$ | $t_{RC}$ | Read Cycle Time[67] | | | Min | 55 | 60 | 65 | 70 | 80 | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address to Output Delay | | CE#, OE# = $V_{IL}$ | Max | 55 | 60 | 65 | 70 | 80 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable to Output Delay | | OE# = $V_{IL}$ | Max | 55 | 60 | 65 | 70 | 80 | ns |
| | $t_{PACC}$ | Page Access Time | | | Max | 20 | 25 | 25 | 30 | 30 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable to Output Delay | | | Max | 20 | 25 | 30 | | 35 | ns |
| $t_{EHQZ}$ | $t_{DF}$ | Chip Enable to Output High Z[69] | | | Max | 16 | | | | | ns |
| $t_{GHQZ}$ | $t_{DF}$ | Output Enable to Output High Z[67, 69] | | | Max | 16 | | | | | ns |
| $t_{AXQX}$ | $t_{OH}$ | Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First[69] | | | Min | 5 | | | | | ns |
| | $t_{OEH}$ | Output Enable Hold Time[67] | Read | | Min | 0 | | | | | ns |
| | | | Toggle and Data# Polling | | Min | 10 | | | | | ns |

**Notes**
67. Not 100% tested.
68. See Figure 14 on page 60 and Table 32 on page 60 for test specifications
69. Measurements performed by placing a 50 ohm termination on the data pin with a bias of $V_{CC}$ /2. The time from OE# high to the data bus driven to $V_{CC}$ /2 is taken as $t_{DF}$.
70. For 70 pF Output Load Capacitance, 2 ns will be added to the above $t_{ACC}$,$t_{CE}$,$t_{PACC}$,$t_{OE}$ values for all speed grades

**Figure 16. Read Operation Timings**

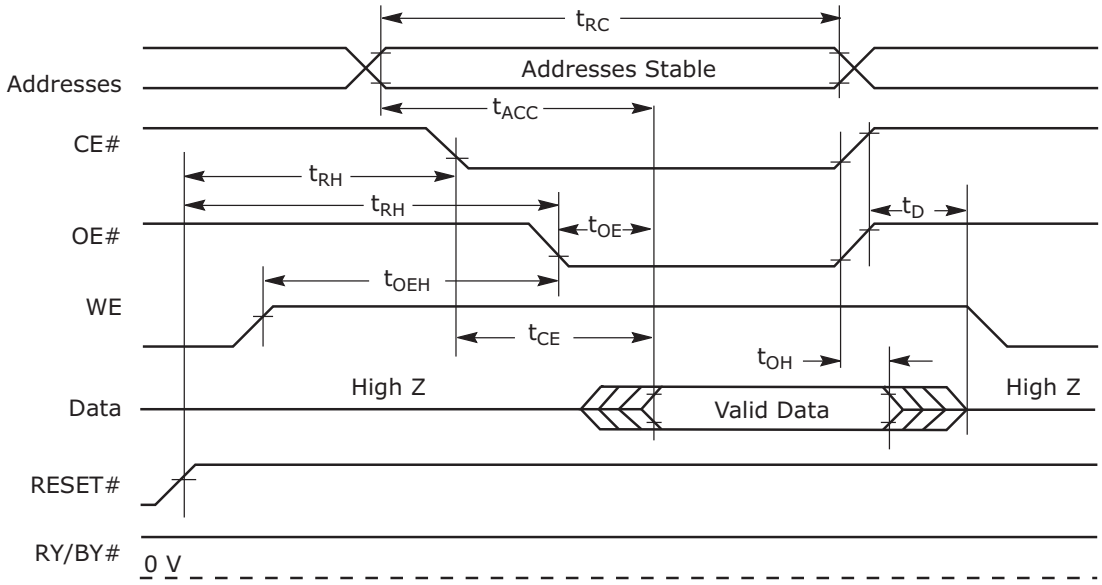
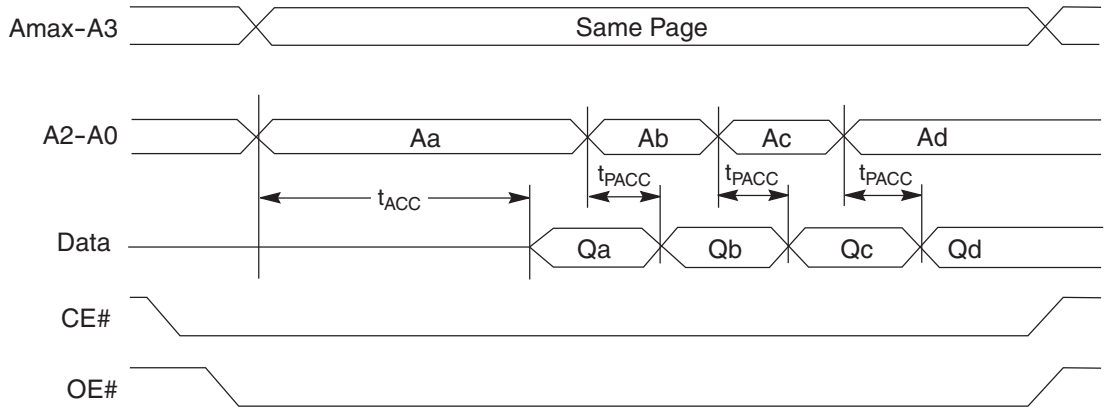



**Figure 17. Page Read Operation Timings**



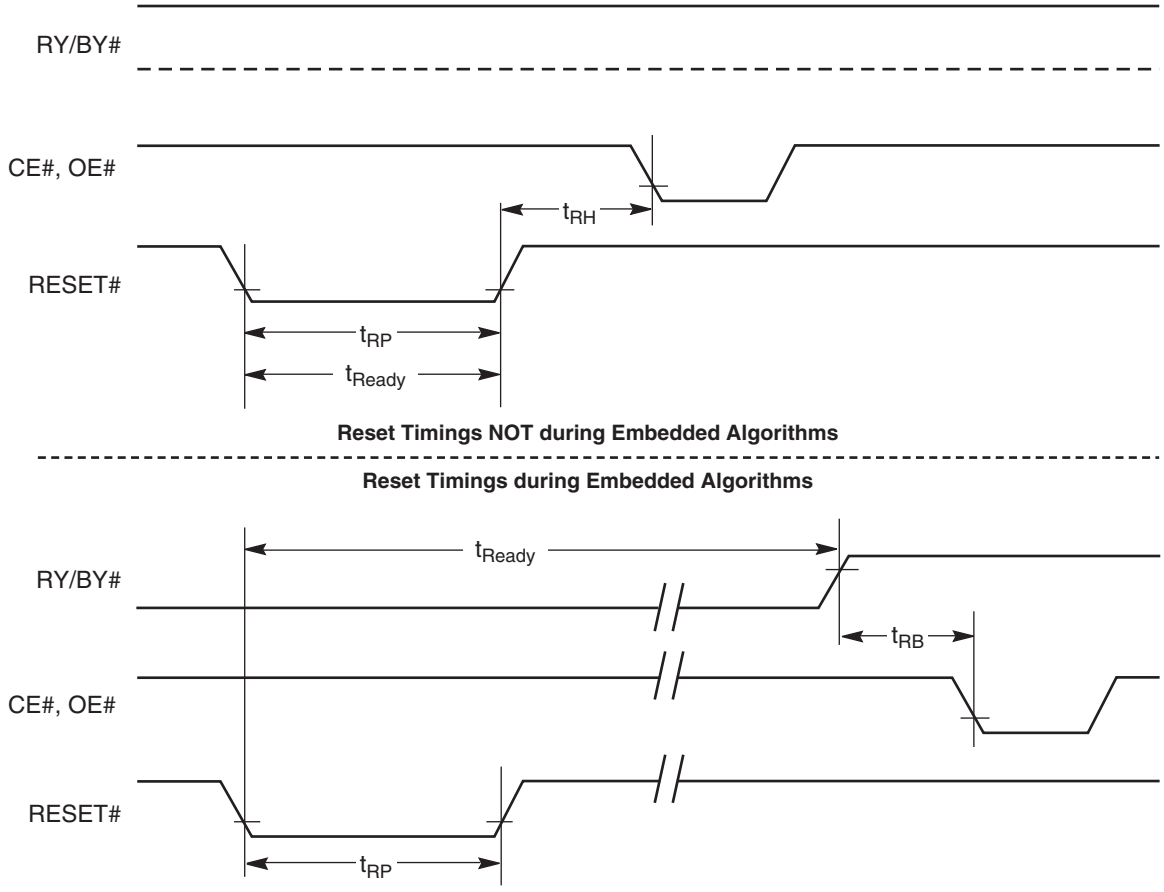
## 20.4 Reset

**Table 35. Hardware Reset (RESET#)**

| Parameter | | Description | | All Speed Options | Unit |
|---|---|---|---|---|---|
| JEDEC | Std | | | | |
| | $t_{Ready}$ | RESET# Pin Low (During Embedded Algorithms) to Read Mode[71] | Max | 20 | µs |
| | $t_{Ready}$ | RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode[71] | Max | 500 | ns |
| | $t_{RP}$ | RESET# Pulse Width | Min | 500 | ns |
| | $t_{RH}$ | Reset High Time Before Read[71] | Min | 50 | ns |
| | $t_{RPD}$ | RESET# Low to Standby Mode | Min | 20 | µs |
| | $t_{RB}$ | RY/BY# Recovery Time | Min | 0 | ns |

**Note**
71. Not 100% tested.

**Figure 18. Reset Timings**



## 20.5 Erase/Program Operations

**Table 36. Erase and Program Operations**

| Parameter | | Description | | Speed Options (ns) | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Std | | | 55 | 60 | 65 | 70 | 80 | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time[72] | Min | 55 | 60 | 65 | 70 | 80 | |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | Min | 0 | | | | | ns |
| | $t_{ASO}$ | Address Setup Time to OE# low during toggle bit polling | Min | 15 | | | | | ns |
| $t_{WLAX}$ | $t_{AH}$ | Address Hold Time | Min | 30 | 35 | | | | ns |
| | $t_{AHT}$ | Address Hold Time From CE# or OE# high during toggle bit polling | Min | 0 | | | | | ns |
| $t_{DVWH}$ | $t_{DS}$ | Data Setup Time | Min | 25 | 30 | | | | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data Hold Time | Min | 0 | | | | | ns |
| | $t_{OEPH}$ | Output Enable High during toggle bit polling | Min | 10 | | | | | ns |
| $t_{GHWL}$ | $t_{GHWL}$ | Read Recovery Time Before Write (OE# High to WE# Low) | Min | 0 | | | | | ns |
| $t_{ELWL}$ | $t_{CS}$ | CE# Setup Time | Min | 0 | | | | | ns |
| $t_{WHEH}$ | $t_{CH}$ | CE# Hold Time | Min | 0 | | | | | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Pulse Width | Min | 35 | | | | | ns |
| $t_{WHDL}$ | $t_{WPH}$ | Write Pulse Width High | Min | 20 | 25 | | | | ns |
| | $t_{SR/W}$ | Latency Between Read and Write Operations | Min | 0 | | | | | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Programming Operation[73] | Typ | 6 | | | | | µs |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Accelerated Programming Operation[73] | Typ | 4 | | | | | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation[73] | Typ | 0.5 | | | | | sec |
| | $t_{VCS}$ | $V_{CC}$ Setup Time[72] | Min | 50 | | | | | µs |
| | $t_{RB}$ | Write Recovery Time from RY/BY# | Min | 0 | | | | | ns |
| | $t_{BUSY}$ | Program/Erase Valid to RY/BY# Delay | Max | 90 | | | | | ns |
| | | | Min | 35 | | | | | ns |
| | $t_{PSL}$ | Program Suspend Latency | Max | 35 | | | | | µs |
| | $t_{ESL}$ | Erase Suspend Latency | Max | 35 | | | | | µs |

**Notes**
72. Not 100% tested.
73. See Table 39 on page 71 for more information.

## 20.6 Timing Diagrams

**Figure 19. Program Operation Timings**[74]

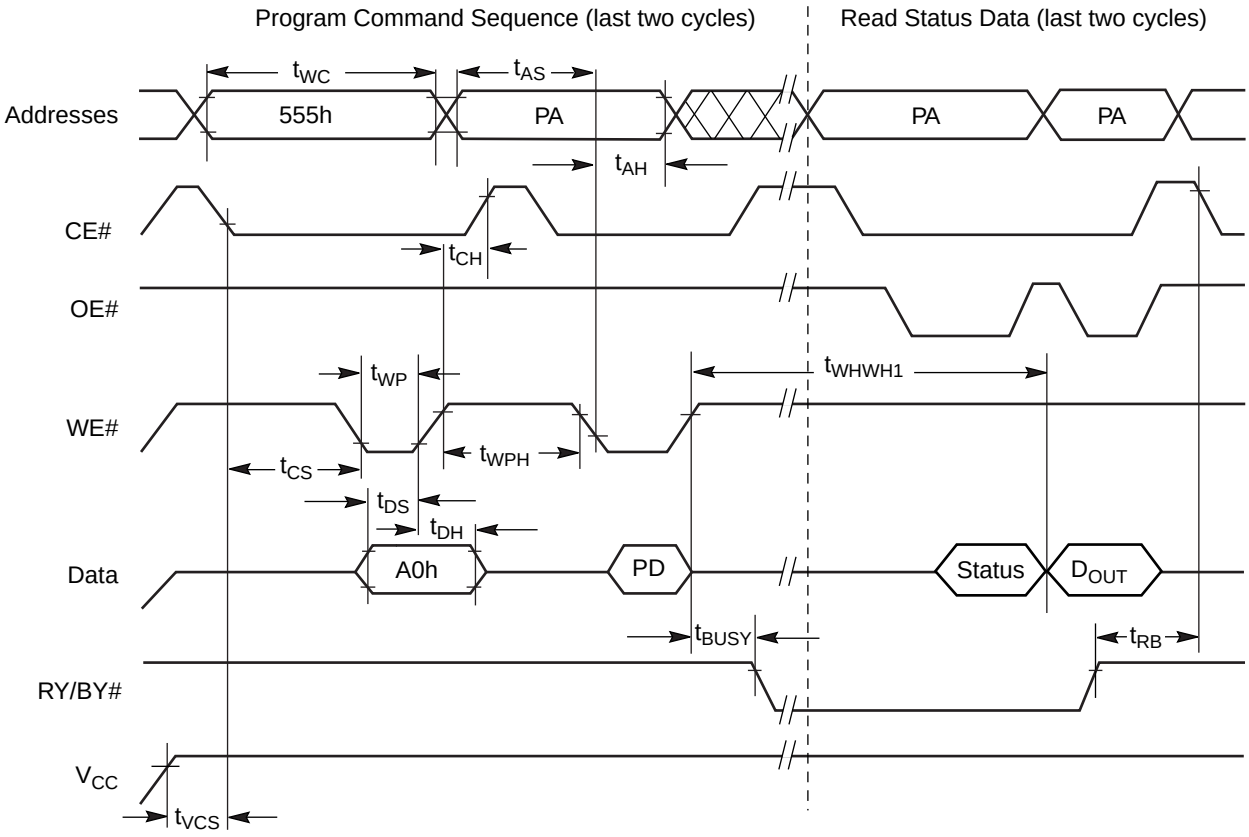
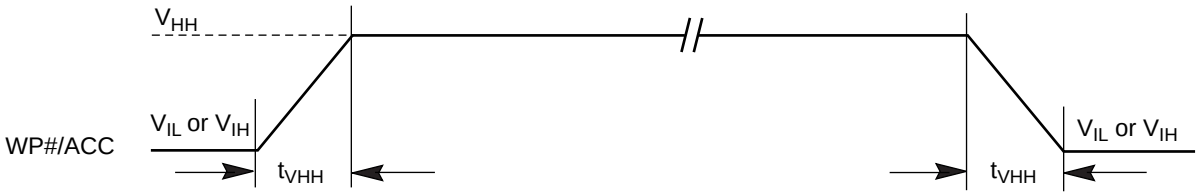



**Figure 20. Accelerated Program Timing Diagram**




**Note**
74. PA = program address, PD = program data, $D_{OUT}$ is the true data at the program address.

**Figure 21. Chip/Sector Erase Operation Timings**[75]

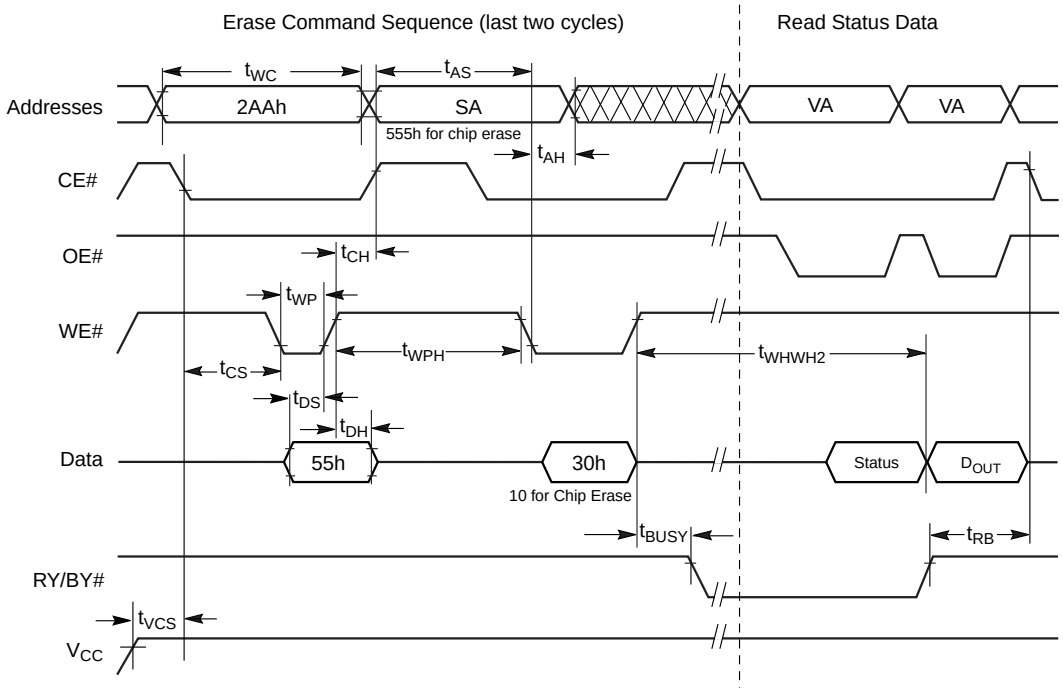
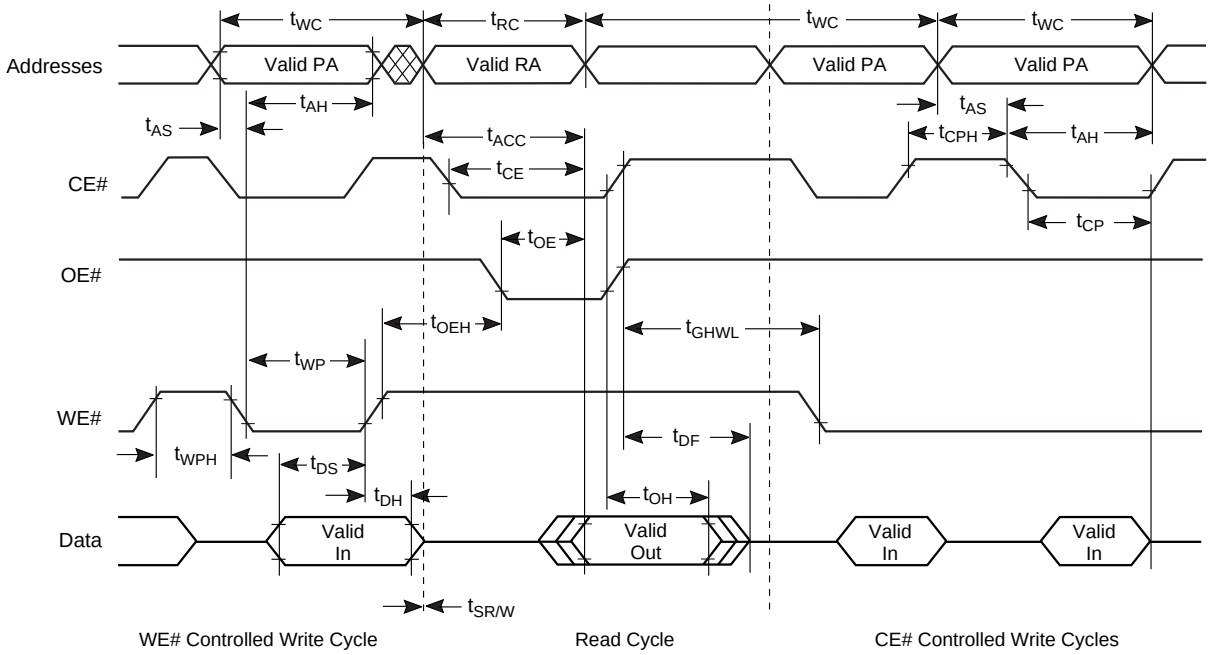



**Figure 22. Back-to-back Read/Write Cycle Timings**




**Note**
75. SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see Section 16. Write Operation Status on page 52).

**Figure 23. Data# Polling Timings (During Embedded Algorithms)[76]**

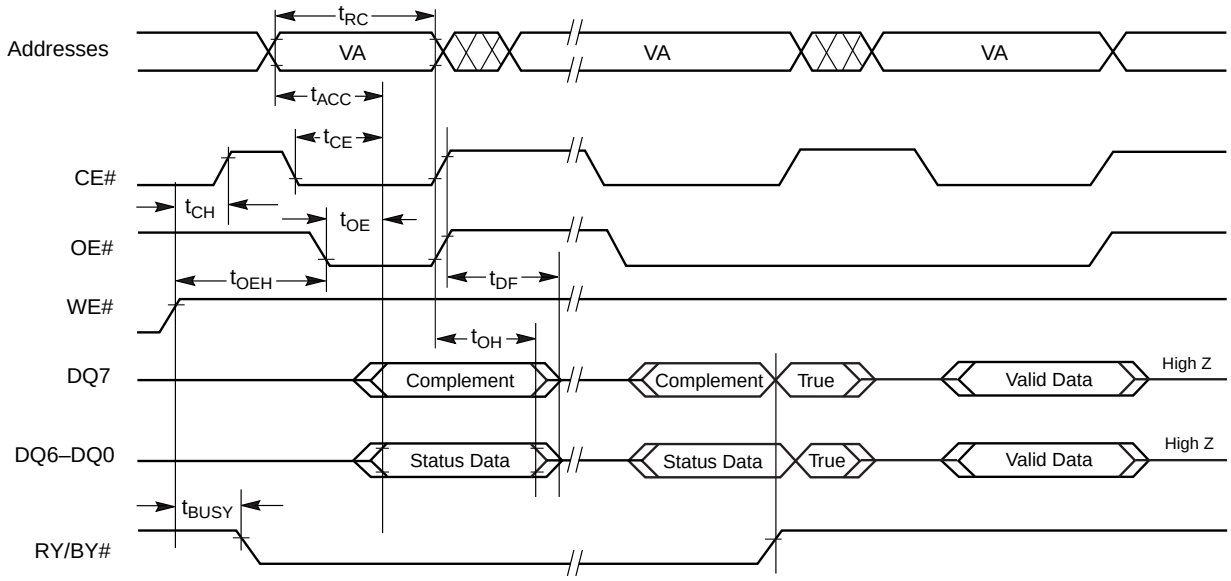
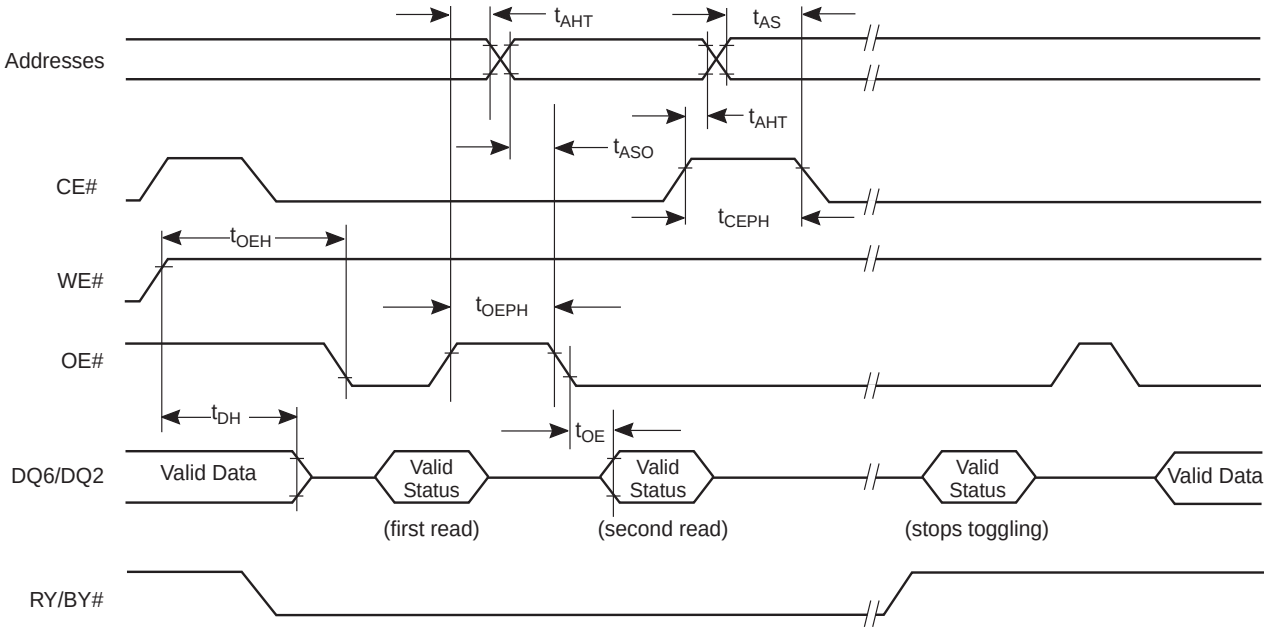
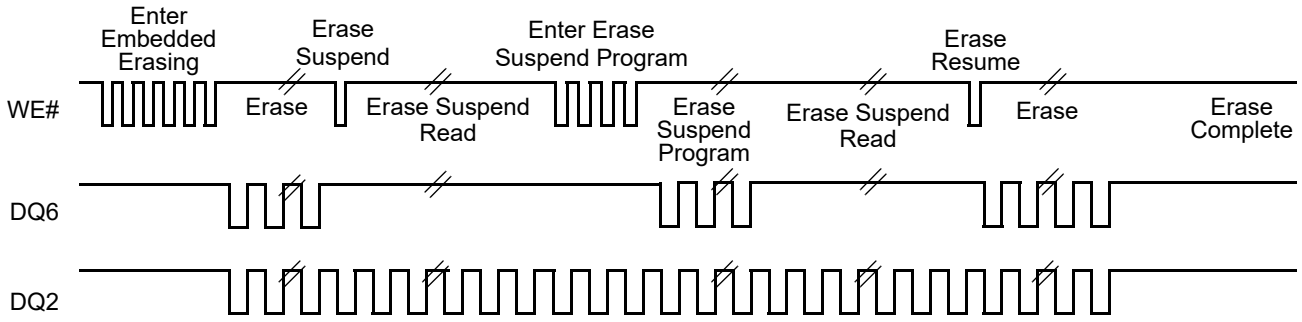



**Figure 24. Toggle Bit Timings (During Embedded Algorithms)[77]**




**Notes**
76. VA = Valid address. The illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.
77. VA = Valid address; not required for DQ6. The illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

**Figure 25. DQ2 vs. DQ6**[78]



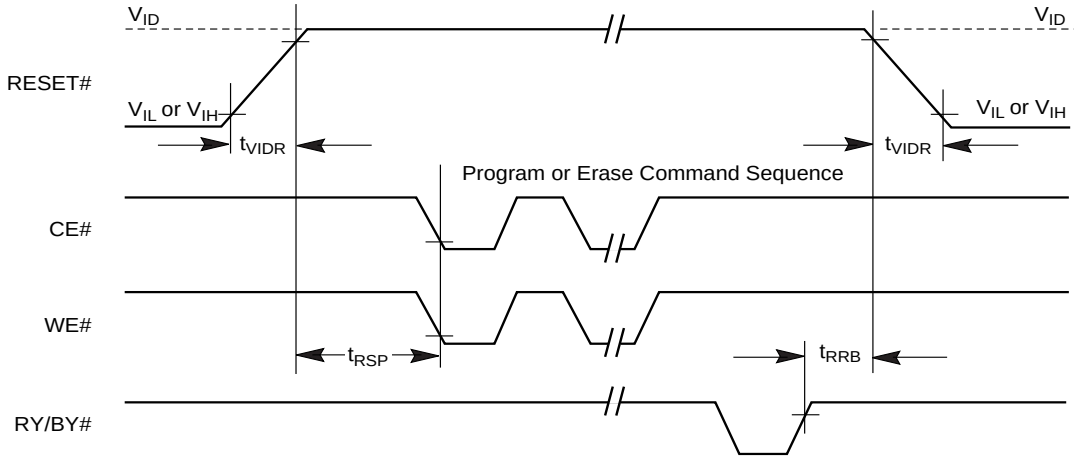

# 21. Protect/Unprotect

**Table 37. Temporary Sector Unprotect**[79]

| Parameter | | Description | | All Speed Options | Unit |
|---|---|---|---|---|---|
| JEDEC | Std | | | | |
| | $t_{VIDR}$ | $V_{ID}$ Rise and Fall Time (See Note) | Min | 500 | ns |
| | $t_{VHH}$ | $V_{HH}$ Rise and Fall Time (See Note) | Min | 250 | ns |
| | $t_{RSP}$ | RESET# Setup Time for Temporary Sector Unprotect | Min | 4 | µs |
| | $t_{RRB}$ | RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect | Min | 4 | µs |

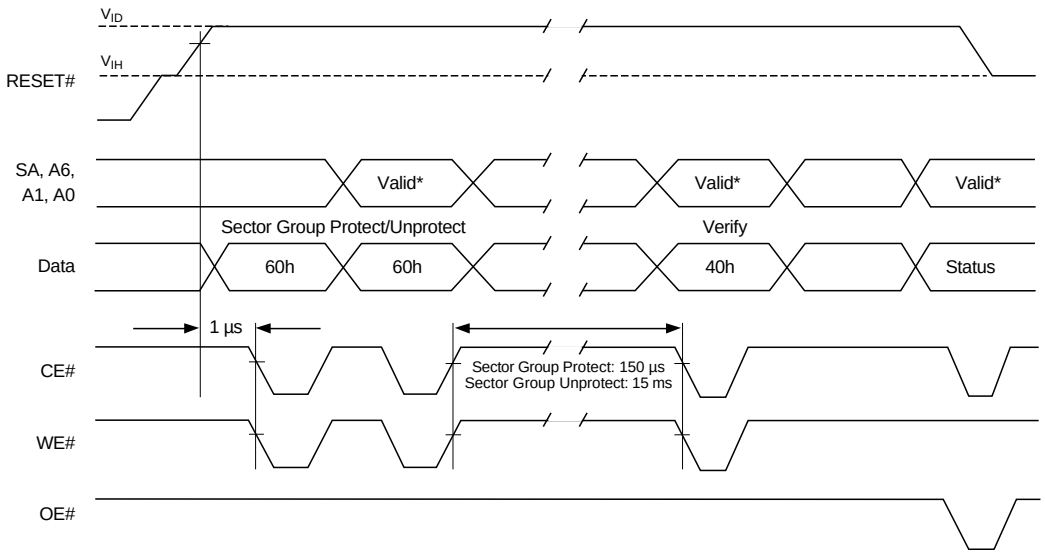
**Note**
79. Not 100% tested.

**Figure 26. Temporary Sector Unprotect Timing Diagram**




**Note**
78. DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.

**Figure 27. Sector/Sector Block Protect and Unprotect Timing Diagram[80]**




## 21.1 Controlled Erase Operations

**Table 38. Alternate CE# Controlled Erase and Program Operations**

| Parameter | | Description (Notes) | | Speed Options | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| JEDEC | Std | | | 55 | 60 | 65 | 70 | 80 | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time[81, 82] | Min | 55 | 60 | 65 | 70 | 80 | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | Min | 0 | | | | | ns |
| $t_{ELAX}$ | $t_{AH}$ | Address Hold Time | Min | 30 | 35 | | | | ns |
| $t_{DVEH}$ | $t_{DS}$ | Data Setup Time | Min | 25 | 30 | | | | ns |
| $t_{EHDX}$ | $t_{DH}$ | Data Hold Time | Min | 0 | | | | | ns |
| $t_{GHEL}$ | $t_{GHEL}$ | Read Recovery Time Before Write (OE# High to WE# Low) | Min | 0 | | | | | ns |
| $t_{WLEL}$ | $t_{WS}$ | WE# Setup Time | Min | 0 | | | | | ns |
| $t_{EHWH}$ | $t_{WH}$ | WE# Hold Time | Min | 0 | | | | | ns |
| $t_{ELEH}$ | $t_{CP}$ | CE# Pulse Width | Min | 35 | 40 | | | | ns |
| $t_{EHEL}$ | $t_{CPH}$ | CE# Pulse Width High | Min | 20 | 25 | | | | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Programming Operation[82] | Typ | 6 | | | | | µs |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Accelerated Programming Operation[82] | Typ | 4 | | | | | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation[82] | Typ | 0.5 | | | | | sec |

**Notes**
81. Not 100% tested.
82. See Section 39 Erase And Programming Performance on page 71 for more information.

**Note**
80. For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.

**Figure 28. Alternate CE# Controlled Write (Erase/Program) Operation Timings**[83, 84, 85]

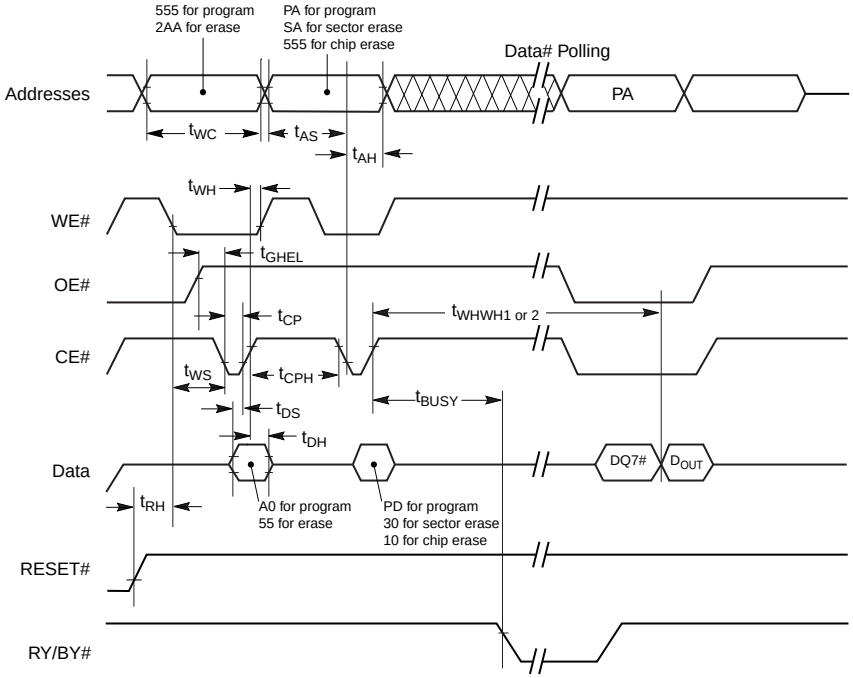
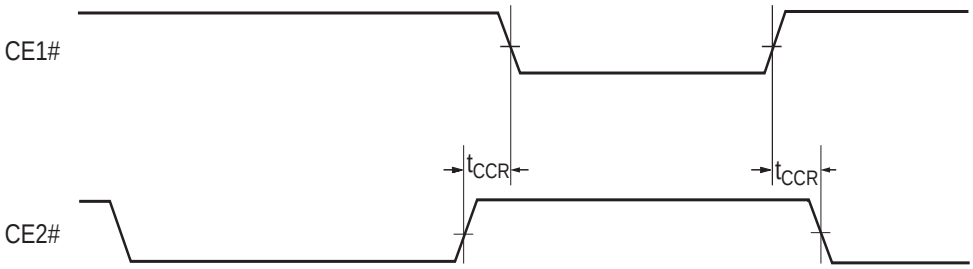



**Figure 29. Timing Diagram for Alternating Between CE1# and CE2# Control**




**Notes**
83. Figure indicates last two bus cycles of a program or erase operation.
84. PA = program address, SA = sector address, PD = program data.
85. DQ7# is the complement of the data written to the device. $D_{OUT}$ is the data written to the device.

**Table 39. Erase And Programming Performance**

| Parameter | | Typ[86] | Max[87] | Unit | Comments |
|---|---|---|---|---|---|
| Sector Erase Time | | 0.5 | 5 | sec | Excludes 00h programming prior to erasure[89] |
| Chip Erase Time | PL127J | 135 | 216 | sec | |
| | PL064J | 71 | 113.6 | sec | |
| | PL032J | 39 | 62.4 | sec | |
| Word Program Time | | 6 | 100 | µs | Excludes system level overhead[90] |
| Accelerated Word Program | | 4 | 60 | µs | |
| Chip Program Time[88] | PL127J | 50.4 | 200 | sec | |
| | PL064J | 25.2 | 50.4 | sec | |
| | PL032J | 12.6 | 25.2 | sec | |

**Notes**

86. Typical program and erase times assume the following conditions: 25°C, 3.0 V $V_{CC}$, 100,000 cycles. Additionally, programming typicals assume checkerboard pattern. All values are subject to change.
87. Under worst case conditions of 90°C, $V_{CC}$ = 2.7 V, 1,000,000 cycles. All values are subject to change.
88. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.
89. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
90. System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 28 on page 49 for further information on command definitions.
91. The device has a minimum erase and program cycle endurance of 100,000 cycles.

# 22. Pin Capacitance

## 22.1 BGA Pin Capacitance

| Parameter Symbol | Parameter Description | Test Setup | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 | 6.3 | 7 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 | 7.0 | 8 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN}$ = 0 | 5.5 | 8 | pF |
| $C_{IN3}$ | WP#/ACC Pin Capacitance | $V_{IN}$ = 0 | 11 | 12 | pF |

**Notes**
92. Sampled, not 100% tested.
93. Test conditions $T_A$ = 25°C, f = 1.0 MHz.

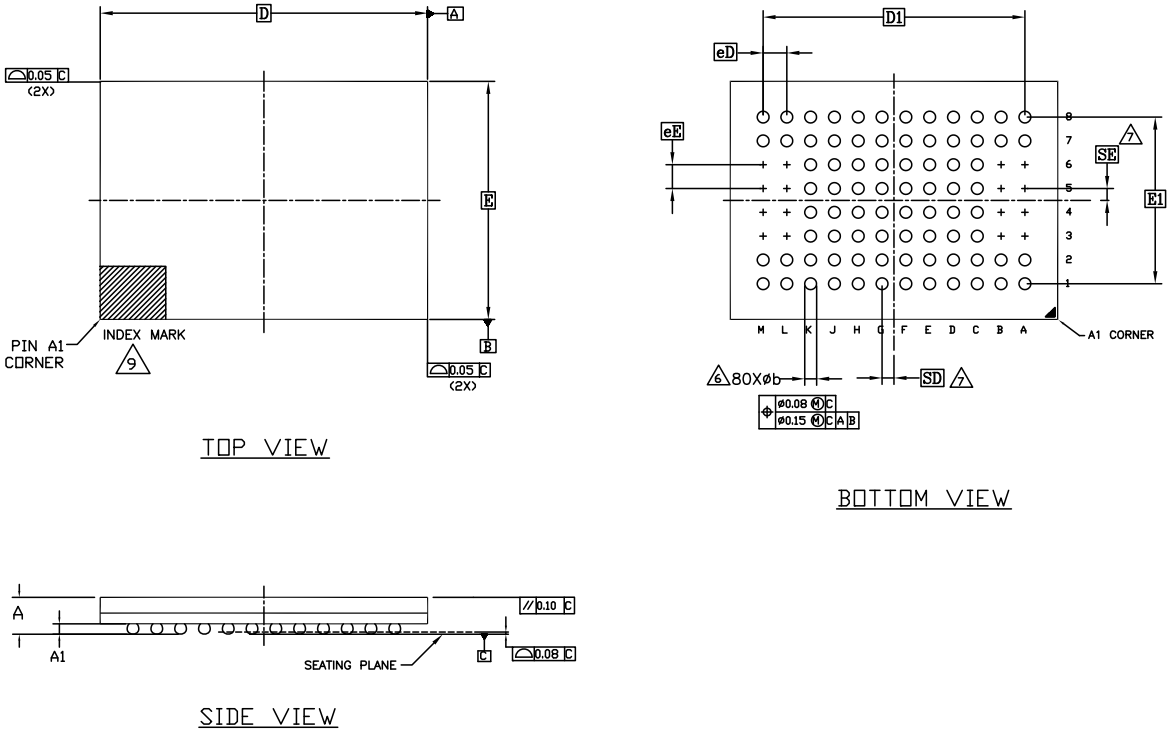
## 22.2 TSOP Pin Capacitance

| Parameter Symbol | Parameter Description | Test Setup | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 | 10 | 10.5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 | 5.5 | 6.5 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN}$ = 0 | 8 | 10 | pF |
| $C_{IN3}$ | WP#/ACC Pin Capacitance | $V_{IN}$ = 0 | 9.5 | 10 | pF |

**Notes**
94. Sampled, not 100% tested.
95. Test conditions $T_A$ = 25°C, f = 1.0 MHz.

# 23. Physical Dimensions

**Figure 30. VBG080—80-Ball Fine-pitch Ball Grid Array 8 × 11 mm Package (PL127J)**




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | – | – | 1.00 |
| A1 | 0.18 | – | – |
| D | 11.00 BSC. | | |
| E | 8.00 BSC. | | |
| D1 | 8.80 BSC. | | |
| E1 | 5.60 BSC. | | |
| MD | 12 | | |
| ME | 8 | | |
| N | 80 | | |
| øb | 0.33 | – | 0.43 |
| eD/eE | 0.80 BSC. | | |
| SD/SE | 0.40 BSC. | | |

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP–020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE"=0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD"=eD/2 AND "SE"=eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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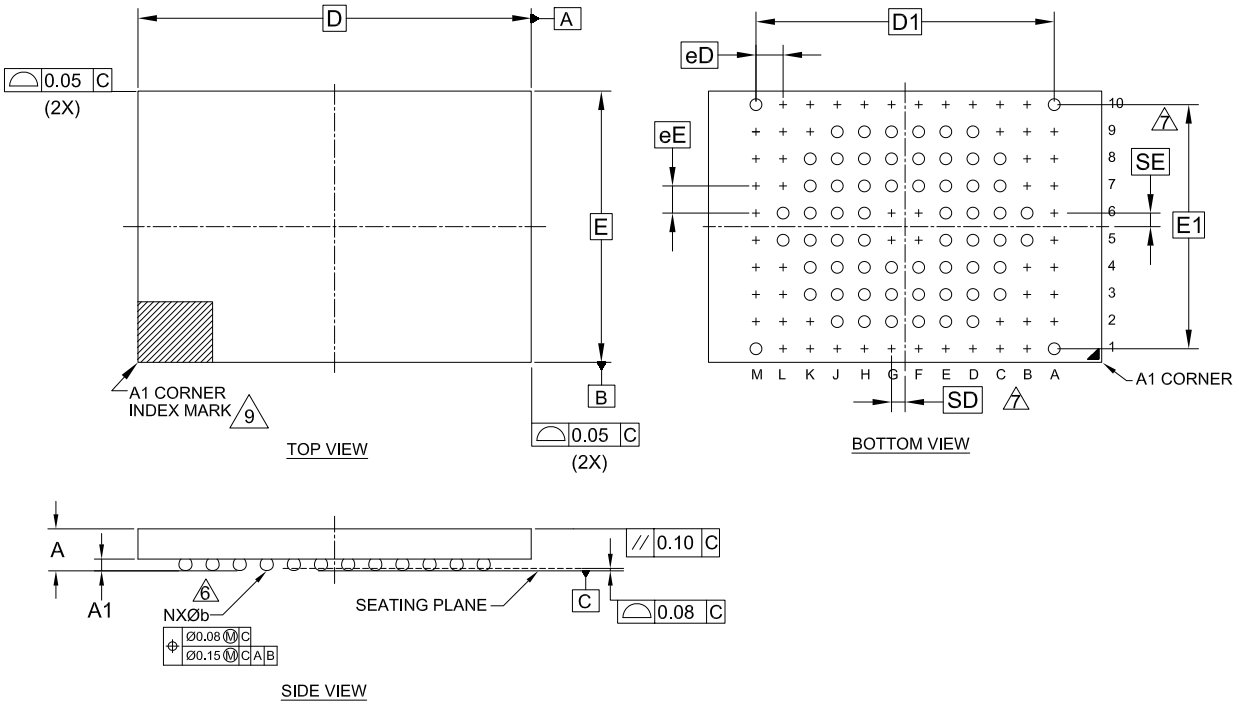
**Figure 31. VBH064—64-Ball Fine-pitch Ball Grid Array 8 × 11.6 mm package (PL127J)**




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | - | - | 1.00 |
| A1 | 0.18 | - | - |
| D | 11.60 BSC. | | |
| E | 8.00 BSC. | | |
| D1 | 8.80 BSC. | | |
| E1 | 7.20 BSC. | | |
| MD | 12 | | |
| ME | 10 | | |
| N | 64 | | |
| Øb | 0.33 | - | 0.43 |
| eD/eE | 0.80 BSC. | | |
| SD/SE | 0.40 BSC. | | |

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE"=0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD"=eD/2 AND "SE"=eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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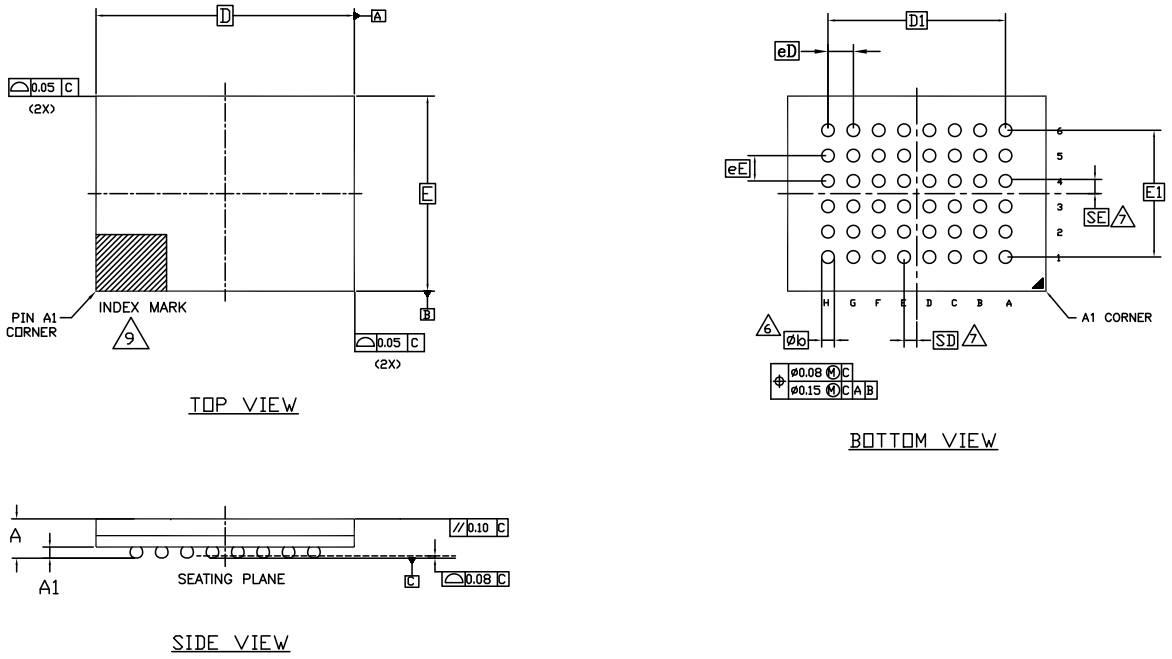
**Figure 32. VBK048—48-Ball Fine-pitch Ball Grid Array 8.15 × 6.15 mm package (PL032J and PL064J)**




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | – | – | 1.00 |
| A1 | 0.18 | – | – |
| D | 8.15 BSC. | | |
| E | 6.15 BSC. | | |
| D1 | 5.60 BSC. | | |
| E1 | 4.00 BSC. | | |
| MD | 8 | | |
| ME | 6 | | |
| n | 48 | | |
| øb | 0.33 | – | 0.43 |
| eD/eE | 0.80 BSC. | | |
| SD/SE | 0.40 BSC. | | |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP–010/020.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE TOTAL NUMBER OF POPULATED SOLDER BALLS FOR MATRIX SIZE MD AND ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 and "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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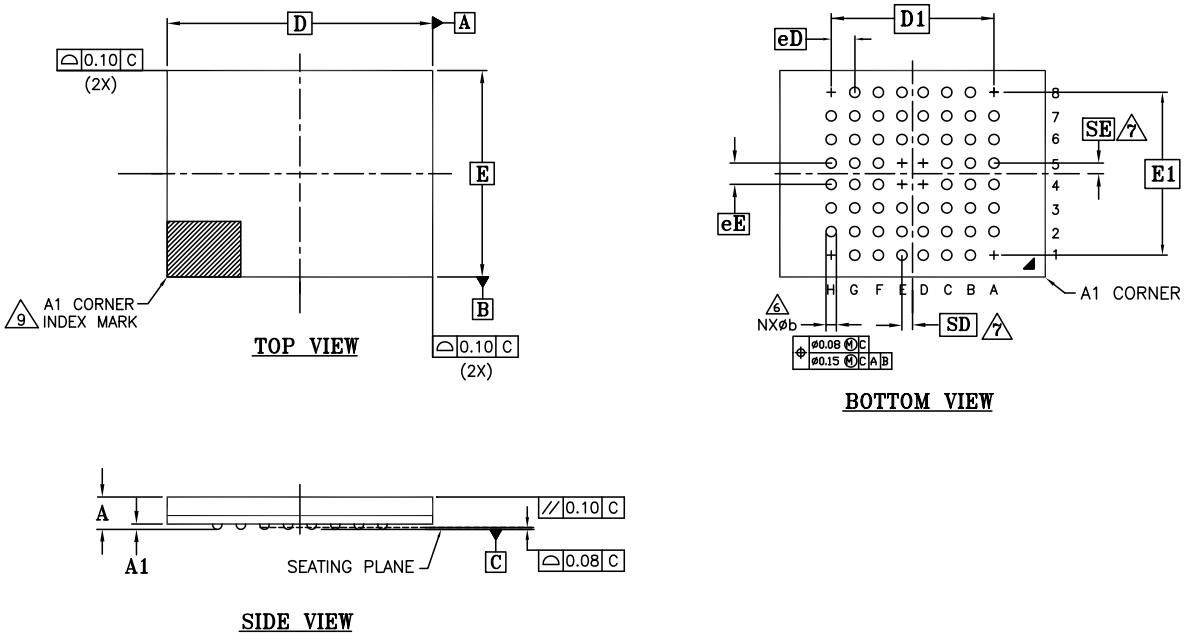
**Figure 33. VBU056—56-Ball Fine-pitch BGA 7 × 9mm package (PL064J and PL032J)**




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | - | - | 1.00 |
| A1 | 0.17 | - | - |
| D | 9.00 BSC. | | |
| E | 7.00 BSC. | | |
| D1 | 5.60 BSC. | | |
| E1 | 5.60 BSC. | | |
| MD | 8 | | |
| ME | 8 | | |
| n | 56 | | |
| Øb | 0.33 | - | 0.45 |
| eD/eE | 0.80 BSC. | | |
| SD/SE | 0.40 BSC. | | |

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010/020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE TOTAL NUMBER OF POPULATED SOLDER BALLS FOR MATRIX SIZE MD AND ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 and "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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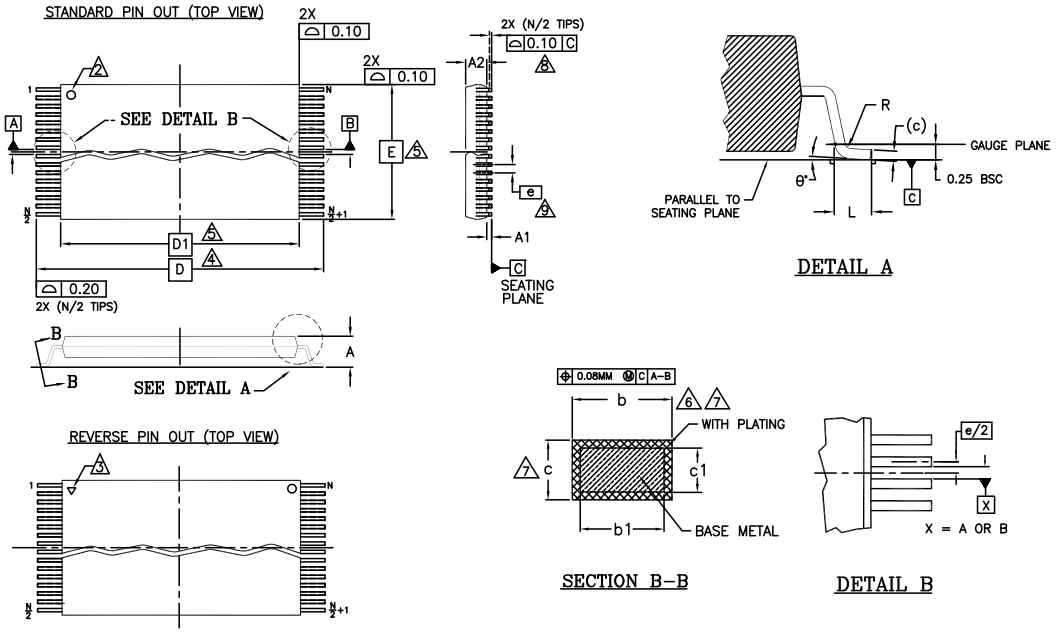
**Figure 34. TS056—20 × 14 mm, 56-pin TSOP (PL127J)**




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b1 | 0.17 | 0.20 | 0.23 |
| b | 0.17 | 0.22 | 0.27 |
| c1 | 0.10 | — | 0.16 |
| c | 0.10 | — | 0.21 |
| D | 20.00 BASIC | | |
| D1 | 18.40 BASIC | | |
| E | 14.00 BASIC | | |
| e | 0.50 BASIC | | |
| L | 0.50 | 0.60 | 0.70 |
| θ | 0° | — | 8 |
| R | 0.08 | — | 0.20 |
| N | 56 | | |

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm .
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)EC.

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# 22. Document History Page

| Document Title: S29PL-J, 128-/64-/32-Mbit (8/4/2M × 16-Bit), 3 V, Flash with Enhanced VersatileIO™<br>Document Number: 002-00615 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | – | RYSU | 01/29/2004 to 04/18/2013 | Initial release<br>Included backward compatibility with MBM29xx families.<br>48-ball BGA package is not supported and was removed.<br>Model numbers for the 48-ball BGA configurations were removed.<br>An illustration was added to show the pin-out configuration.<br>Added the description of 01h for address 4Fh and removed the 0004 data.<br>Provided the time units of measure for the erase and programming performances.<br>Corrected typo in device ID.<br>Added 3V VIO for PL064J and PL032J devices.<br>Corrected the voltage rating, ball configuration, and physical dimensions for model numbers 12 and 13.<br>Removed the 64-ball, 8x9 mm diagram.<br>Clarified the supply voltages that apply to the PL127J/PL129J and all other PLxxxJ products.<br>Added information applicable to the CIN3 symbol.<br>Removed the 9x8 mm package drawing.<br>Added the 56-ball 7x9 mm pinout diagram.<br>Updated to include the 8 x 6 mm, 48-ball Fine pitch BGA and 7 x 9 mm, 56-ball Fine-pitch BGA options.<br>Added the VBK048 package drawing.<br>Changed names.<br>Updated specs in this table.<br>Updated the Model Number offerings.<br>Corrected the Package Markings for the 64-ball FBGA packages.<br>Added combinations for the TLC056 package on the PL064J and PL032J devices.<br>Valid Combinations for BGA Packages (128Mb)<br>Package Options<br>Added the 7 x 9mm 56-ball package.<br>56-ball connection diagram<br>Notes 1 and 2 corrected to reflect accurate temperature ranges and cycling.<br>Updated the Model Number offerings<br>Updated the Package Types information.<br>Figure 6, In-System Sector Protection/Sector Unprotection Algorithms<br>Program Suspend/Program Resume Commands<br>New section added. Made global changes to include program suspend/resume commands.<br>Added Erase Suspend Latency.<br>Updated table and added a notes section.<br>Added the VBU056 package<br>Added note: When Polling the SecSi indicator bit the A21 to A12 should be set within the address range 004000h-03FFFFh.<br>Added sentence: Once the Enter Secured Silicon Sector Command sequence has been entered, the standard array cannot be accessed until the Exit Secured Silicon Sector command has been entered or the device has been reset.<br>Added note 16: Once the Secured Silicon Sector Entry Command sequence has been entered, the standard array cannot be accessed until the Exit Secured Silicon Sector command has been entered or the device has been reset.<br>Content the same, tables consolidated to match Ordering Information Descriptions<br>Consolidated Special Package Handling Instructions and put the information before the package/pinout descriptions.<br>Added Figure numbers to the connection diagram graphics.<br>Updated operating temperatures.<br>Updated VOH parameter.<br>Added tESL parameter<br>Updated the product that uses this package from PL127J to PL064J and PL032J<br>64-Ball Fine-Pitch BGA—MCP Compatible—PL127JChanged ball F9 to A22<br>Pin DescriptionCorrected WP#/ACC description.<br>GlobalChanged data sheet status from Advanced Information to Full Production<br>Ordering InformationModified/Added note to the Valid Combinations to be Supported for this Device tables<br>VCC Ramp RateRemoved Section<br>Connection DiagramCorrected 64-Ball Fine-Pitch BGA ball description (H9 and L5)<br>Ordering InformationUnder Package Type, changed wording of “Lead (Pb)-free compliant” material type to “Standard”.<br>GlobalRemoved 55 ns as a valid speed supported by PL127J.<br>Product Selector GuideCorrected the 55 ns Speed Option's Max Page Access and Max OE# Access time from 2 to 20 ns.<br>Corrected the 65 ns Speed Option's Max Access and Max CE# Access time from 25 to 65 ns.<br>Dynamic Protection Bit (DYB)Corrected reference to Table 17 to Table 10.15.<br>Erase Suspend/Erase Resume CommandsCorrected “This command is valid only during the sector erase operation, including the 80 µs time-out period...” to “This command is valid only during the sector erase operation, including the 50 µs time-out period...”.<br>Command Definitions TablesIn Table 15.2, corrected the value of the third bus cycle of the “PPB Status”, “PPB Lock Bit Status” and “DYB Status” commands from 555 to BA+555. |

| Document Title: S29PL-J, 128-/64-/32-Mbit (8/4/2M × 16-Bit), 3 V, Flash with Enhanced VersatileIO™<br>Document Number: 002-00615 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** (cont'd) | - | RYSU | 01/29/2004 to 04/18/2013 | Absolute Maximum RatingsCorrected the A9, OE# and RESET# “Voltage with Respect to Ground” maximum range value from +13.0V to +12.5V.<br>DQ6: Toggle Bit ICorrected Figure 16.2: Toggle Bit Algorithm.<br>Pin CapacitanceAdded TSOP package pin capacitance values.<br>Ordering InformationFor model number 13, corrected “56-ball” TSOP package description to “56-pin”.<br>GlobalChanged 65 ns and 70 ns initial access time for VIO=1.8V to 80 ns. |
| *A | 4959015 | RYSU | 10/13/2015 | Updated to Cypress template. |
| *B | 5398456 | NFB | 08/10/2016 | Updated Section 3. Ordering Information on page 6:<br>Added 1.8V $V_{IO}$ TSOP package.<br>Updated *Valid Combinations - Standard*:<br>Added 14 in “Additional Ordering Options” column in “128 Mb Products Based on 110 nm Floating Gate Technology”.<br>Updated to new template. |
| *C | 5644215 | SZZX | 02/27/2017 | Updated Section 3. Ordering Information on page 6:<br>Removed “BA” and “TA” details under “Package Type”.<br>Updated *Valid Combinations - Standard*:<br>Removed “BA” and “TA” related information.<br>Updated to new template.<br>Completing Sunset Review. |
| *D | 5755150 | NIBK | 05/31/2017 | Updated Cypress Logo and Copyright. |
| *E | 6381371 | PRIT | 12/05/2018 | Updated Section 3. Ordering Information on page 6.<br>Updated Max Sector Erase Time.<br>Updated Section 23. Physical Dimensions on page 73. |
| *F | 6654238 | BWHA | 08/20/2019 | Removed S29PL129J MCP Device.<br>Added Automotive Device: A = Automotive, AEC-Q100 Grade 3 (-40°C to +85°C).<br>Updated Cypress template. |

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