THE DATASHEET OF

S25FL256LAGBHI033

www.win-source.net 0086-755-83957316

128 Mb (16 MB) / 256 Mb (32 MB) FL-L flash

SPI multi-I/O, 3.0 V

General description

The FL-L family devices are flash non-volatile memory products using:

- Floating gate technology
- 65-nm process lithography

The FL-L family connects to a host system via a serial peripheral interface (SPI). Traditional SPI single bit serial input and output (single I/O or SIO) is supported as well as optional two bit (dual I/O or DIO) and four bit wide Quad I/O (QIO) and quad peripheral interface (QPI) commands. In addition, there are double data rate (DDR) read commands for QIO and QPI that transfer address and read data on both edges of the clock.

The architecture features a page programming buffer that allows up to 256-bytes to be programmed in one operation and provides individual 4KB sector, 32KB half block, 64KB block, or entire chip erase.

By using FL-L family devices at the higher clock rates supported, with Quad commands, the instruction read transfer rate can match or exceed traditional parallel interface, asynchronous, NOR flash memories, while reducing signal count dramatically.

The FL-L family products offer high densities coupled with the flexibility and fast performance required by a variety of mobile or embedded applications. Provides an ideal storage solution for systems with limited space, signal connections, and power. These memories offer flexibility and performance well beyond ordinary serial flash devices. They are ideal for code shadowing to RAM, executing code directly (XIP), and storing re-programmable data.

Features

- SPI with multi-I/O
  - Clock polarity and phase modes 0 and 3
  - Double data rate (DDR) option
  - Quad peripheral interface (QPI) option
  - Extended addressing: 24- or 32-bit address options
  - Serial command subset and footprint compatible with S25FL-A, S25FL1-K, S25FL-P, S25FL-S and S25FS-S SPI families
  - Multi I/O command subset and footprint compatible with S25FL-P, S25FL-S and S25FS-S SPI families
- Read
  - Commands: normal, fast, dual I/O, Quad I/O, dualO, QuadO, DDR Quad I/O.
  - Modes: Burst wrap, continuous (XIP), QPI
  - Serial flash discoverable parameters (SFDP) for configuration information.
- Program architecture
  - 256 bytes page programming buffer
  - 256 Mb (32 MB)/128 Mb (16 MB), 3.0 V FL-L flash memory
  - Program suspend and resume
- Erase architecture
  - Uniform 4 KB sector erase
  - Uniform 32 KB half block erase
  - Uniform 64 KB block erase
  - Chip erase
  - Erase suspend and resume
- 100,000 program/erase cycles, minimum
- 20 year data retention, minimum

Features

- Security features
  - Status and Configuration Register protection
  - Four security regions of 256 bytes each outside the main flash array
  - Legacy block protection: Block range
  - Individual and region protection
    - Individual block lock: Volatile individual sector/block
    - Pointer region: Non-volatile sector/block range
    - Power supply lock-down, password, or permanent protection of security regions 2 and 3 and pointer region
- Technology
  - 65-nm floating gate technology
- Single supply voltage with CMOS I/O
  - 2.7 V to 3.6 V
- Temperature range / grade
  - Industrial (–40°C to +85°C)
  - Industrial Plus (–40°C to +105°C)
  - Automotive, AEC-Q100 grade 3 (–40°C to +85°C)
  - Automotive, AEC-Q100 grade 2 (–40°C to +105°C)
  - Automotive, AEC-Q100 grade 1 (–40°C to +125°C)
- Packages (all Pb-free)
  - 8-pin SOIC 208 mil (SOC008) – S25FL128L only
  - WSON 5 × 6 mm (WND008) – S25FL128L only
  - WSON 6 × 8 mm (WNG008) – S25FL256L and S25FL128L
  - 16-pin SOIC 300 mil (SO3016)
  - BGA-24 6 × 8 mm
    - 5 × 5 ball (FAB024) footprint
    - 4 × 6 ball (FAC024) footprint

Performance summary

Maximum read rates SDR

Command	Clock rate (MHz)	MBps
Read	50	6.25
Fast Read	133	16.5
Dual Read		33
Quad Read		66

Maximum read rates DDR

Command	Clock rate (MHz)	MBps
DDR Quad Read	66	66

Typical program and erase rates

Operation	KBps
Page programming	854
4 KB sector erase	80
32 KB half block erase	168
64 KB block erase	237

Typical current consumption, –40°C to +85°C

Operation	Typical current	Unit
Fast Read 5 MHz	10	mA
Fast Read 10 MHz	10	
Fast Read 20 MHz	10	
Fast Read 50 MHz	15	
Fast Read 108 MHz	25	
Fast Read 133 MHz	30	
Quad I/O / QPI Read 108 MHz	25	
Quad I/O / QPI Read 133 MHz	30	
Quad I/O / QPI DDR Read 33 MHz	15	
Quad I/O / QPI DDR Read 66 MHz	30	
Program	40	
Erase	40	
Standby SPI	20	µA
Standby QPI	60	
Deep power down	2	

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1 Product overview

1.1 Migration notes

1.1.1 Features comparison

The FL-L family is command subset and footprint compatible with prior generation FL-S, FL1-K and FL-P families.

Table 1 Infineon SPI families comparison

Parameter	FL-L	FL-S	FL1-K	FL-P
Technology node	65-nm	65-nm	90-nm	90-nm
Architecture	Floating gate	MIRRORBIT™ Eclipse	Floating Gate	MIRRORBIT™
Release date	In production	In production	In production	In production
Density	256 Mb	128 Mb–1 Gb	4 Mb–64 Mb	32 Mb–256 Mb
Bus width	×1, ×2, ×4	×1, ×2, ×4	×1, ×2, ×4	×1, ×2, ×4
Supply voltage	2.7 V–3.6 V	2.7 V–3.6 V / 1.65 V–3.6 V V_{IO}	2.7 V–3.6 V	2.7 V–3.6 V
Normal Read speed	6 MBps (50 MHz)	6 MBps (50 MHz)	6 MBps (50 MHz)	5 MBps (40 MHz)
Fast Read speed	16.5 MBps (133 MHz)	17 MBps (133 MHz)	13 MBps (108 MHz)	13 MBps (104 MHz)
Dual Read speed	33 MBps (133 MHz)	26 MBps (104 MHz)	26 MBps (108 MHz)	20 MBps (80 MHz)
Quad Read speed	66 MBps (133 MHz)	52 MBps (104 MHz)	52 MBps (108 MHz)	40 MBps (80 MHz)
Quad Read speed (DDR)	66 MBps (66 MHz)	80 MBps (80 MHz)	–	–
Program buffer size	256B	256B / 512B	256B	256B
Erase sector/block size	4 KB / 32 KB / 64 KB	64 KB / 256 KB	4 KB / 64 KB	64 KB / 256 KB
Parameter sector size	–	4 KB (option)	–	4 KB
Sector / block erase rate (typ.)	80 KBps (4 KB) 168 KBps (32 KB 237 KBps (64 KB)	500 KBps	136 KBps (4 KB) 437 KBps (64 KB)	130 KBps
Page programming rate (typ.)	854 KBps (256B)	1.2 MBps (256B) 1.5 MBps (512B)	365 KBps	170 KBps
Security Region / OTP	1024B	1024B	768B (3 × 256B)	506B
Individual and Region protection or advanced sector protection	Yes	Yes	No	No
Erase suspend/resume			Yes	
Program suspend/resume				
Operating temperature	–40°C to +85°C –40°C to +105°C –40°C to +125°C	–40°C to +85°C –40°C to +105°C	–40°C to +85°C	–40°C to +85°C –40°C to +105°C

Note
1. Refer to individual datasheets for further details.

2 Pinouts

2.1 SOIC 16-lead

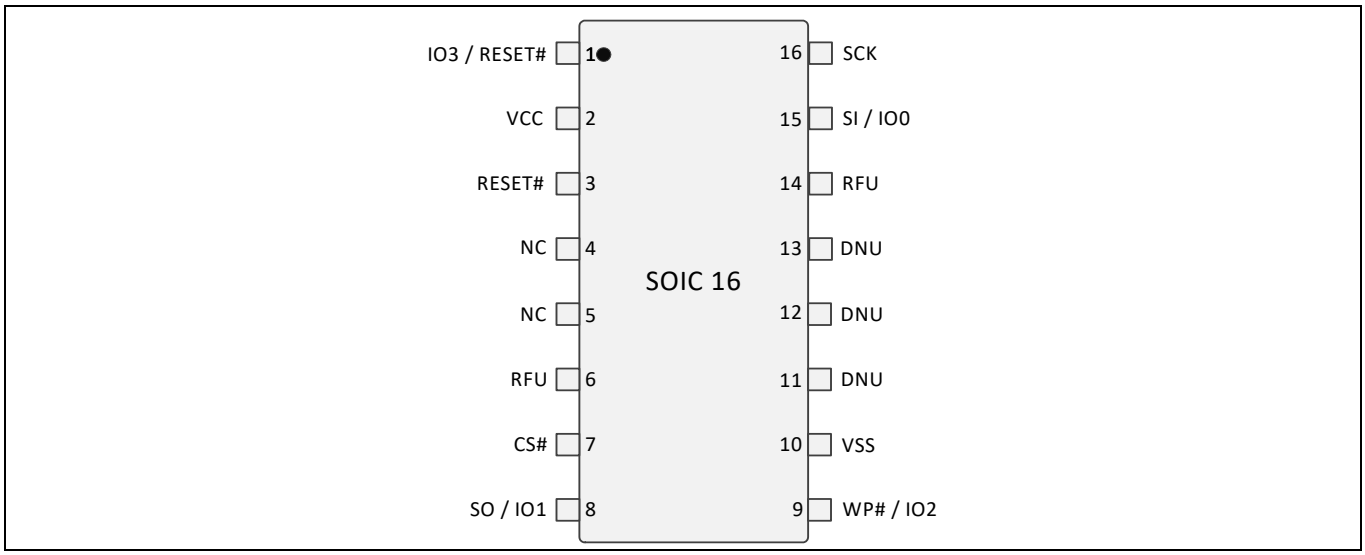


Figure 1 16-lead SOIC package (SO3016), top view

Note
2. The RESET# and IO3 / RESET# inputs have an internal pull-up and may be left unconnected in the system if quad mode, mode and hardware reset are not in use.

2.2 8 connector packages

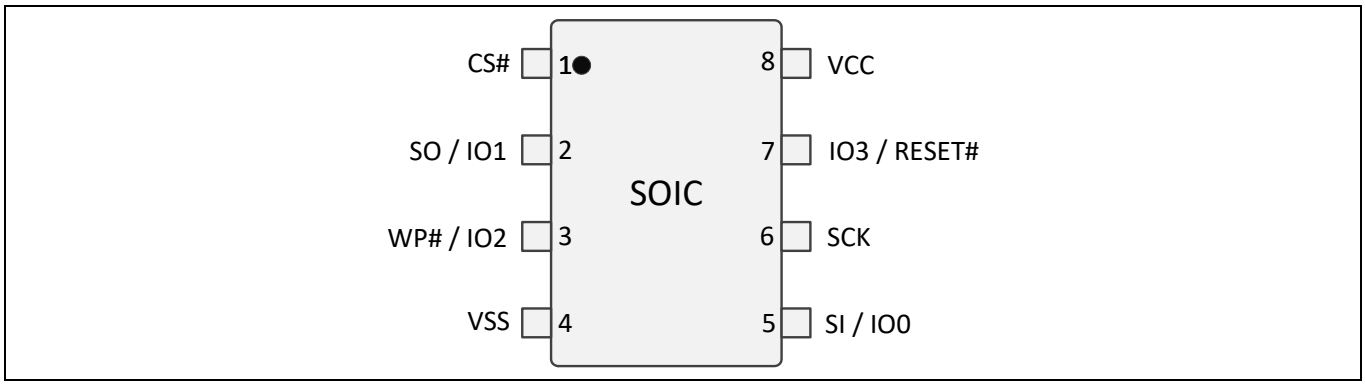


Figure 2 8-Pin plastic small outline package (SOIC8)

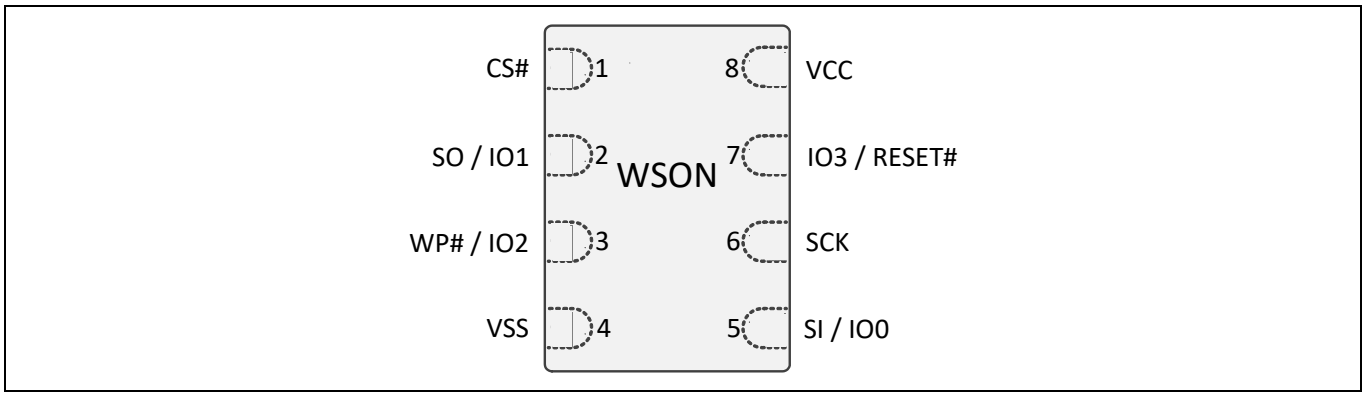


Figure 3 8-Connector package (WSON 6 x 8) (WSON 5 x 6), top view

Note
3. The RESET# input has an internal pull-up and may be left unconnected in the system if quad mode and hardware reset are not in use.

2.3 BGA ball footprint

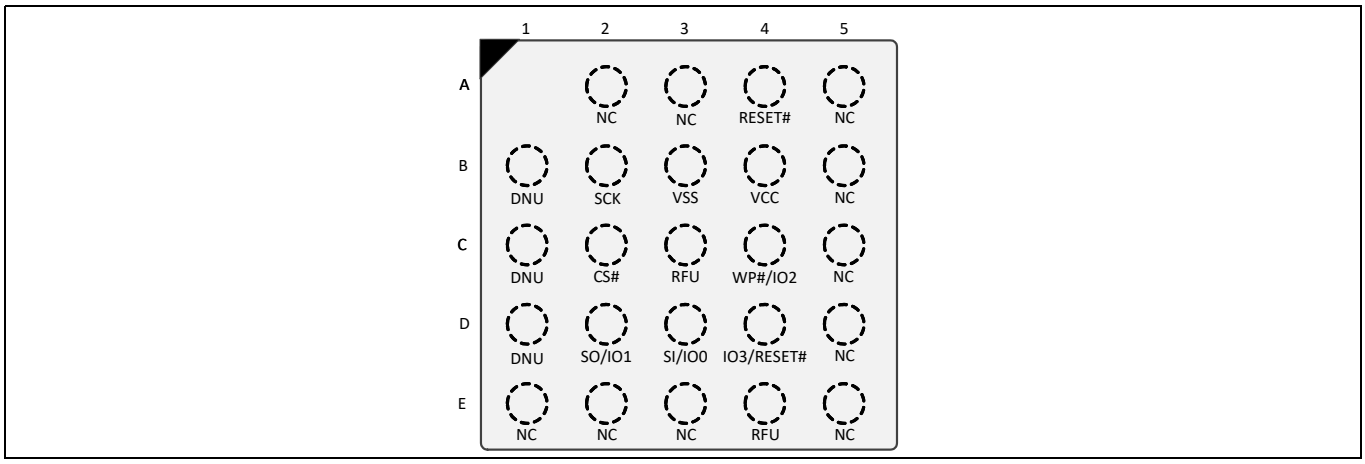


Figure 4 24-ball BGA, 5 x 5 ball footprint (FAB024), top view

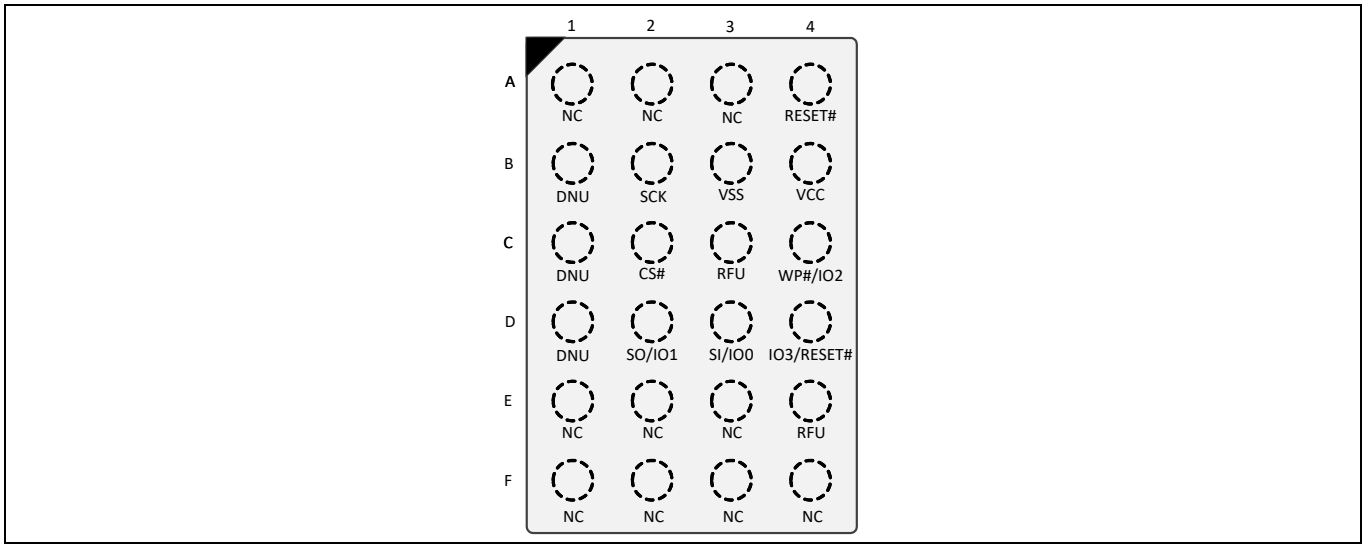


Figure 5 24-ball BGA, 4 x 6 ball footprint (FAC024), top view

2.4 Special handling instructions for FBGA packages

Flash memory devices in BGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

Notes

4. Signal connections are in the same relative positions as FAC024 BGA, allowing a single PCB footprint to use either package.
5. The RESET# input has an internal pull-up and may be left unconnected in the system if quad mode and hardware reset are not in use.
6. The RESET# input has an internal pull-up and may be left unconnected in the system if quad mode and hardware reset are not in use.

3 Signal descriptions

3.1 Serial peripheral interface with multiple input / output (SPI-MIO)

Many memory devices connect to their host system with separate parallel control, address, and data signals that require a large number of signal connections and larger package size. The large number of connections increase power consumption due to so many signals switching and the larger package increases cost.

The FL-L family reduces the number of signals for connection to the host system by serially transferring all control, address, and data information over 6 signals. This reduces the cost of the memory package, reduces signal switching power, and either reduces the host connection count or frees host connectors for use in providing other features.

The FL-L family uses the industry standard single bit SPI and also supports optional extension commands for two bit (Dual) and four bit (Quad) wide serial transfers. This multiple width interface is called SPI multi-I/O or SPI-MIO.

3.2 Input/output summary

Table 2 Signal list

Signal name	Type	Description
RESET#	Input	**Hardware Reset.** Low = device resets and returns to standby state, ready to receive a command. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used.
SCK		**Serial Clock**
CS#		**Chip Select**
SI / IO0	I/O	**Serial Input** for single bit data commands or IO0 for Dual or Quad commands.
SO / IO1		**Serial Output** for single bit data commands. IO1 for Dual or Quad commands.
WP# / IO2		**Write Protect** when not in Quad mode (CR1V[1] = 0 and SR1NV[7] = 1). **IO2** when in Quad mode (CR1V[1] = 1). The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands or write protection. If write protection is enabled by SR1NV[7] = 1 and CR1V[1] = 0, the host system is required to drive WP# high or low during a WRR or WRAR command.
IO3 / RESET#		**IO3** in Quad-I/O mode, when Configuration Register 1 QUAD bit, CR1V[1] =1, or in QPI mode, when Configuration Register 2 QPI bit, CR2V[3] =1 and CS# is low. **RESET#** when enabled by CR2V[7] = 1 and not in Quad-I/O mode, CR1V[1] = 0, or when enabled in Quad mode, CR1V[1] = 1 and CS# is high. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands or RESET#.
V_{CC}	Supply	**Power Supply.**
V_{SS}		**Ground.**
NC	Unused	**Not Connected.** No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). However, any signal connected to an NC must not have voltage levels higher than V_{CC}.
RFU	Reserved	**Reserved for Future Use.** No device internal signal is currently connected to the package connector but there is potential future use of the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.
DNU		**Do Not Use.** A device internal signal may be connected to the package connector. The connection may be used by Infineon for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to this connection.

Note

7. Inputs with internal pull-ups or pull-downs drive less than 2 µA. Only during power-up is the current larger at 150 µA for 4 µs. Resistance of pull-ups or pull-down resistors with the typical process at V_{CC} = 3.3 V at –40°C is ~4.5 MΩ and at 90°C is ~6.6 MΩ.

3.3 Multiple Input / Output (MIO)

Traditional SPI single bit wide commands (Single or SIO) send information from the host to the memory only on the Serial Input (SI) signal. Data may be sent back to the host serially on the Serial Output (SO) signal.

Dual or Quad Input / Output (I/O) commands send instructions to the memory only on the SI/IO0 signal. Address or data is sent from the host to the memory as bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3.

QPI mode transfers all instructions, addresses, and data from the host to the memory as four bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as four bit (nibble) groups on IO0, IO1, IO2, and IO3.

3.4 Serial Clock (SCK)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCK signal. Data output changes after the falling edge of SCK, in SDR commands.

3.5 Chip Select (CS#)

The Chip Select signal indicates when a command is transferring information to or from the device and the other signals are relevant for the memory device.

When the CS# signal is at the logic HIGH state, the device is not selected and all input signals are ignored and all output signals are high impedance. The device will be in the Standby Power mode, unless an internal embedded operation is in progress. An embedded operation is indicated by the Status Register 1 Write-In-Progress bit (SR1V[0]) set to '1', until the operation is completed. Some example embedded operations are: Program, Erase, or Write Registers (WRR) operations.

Driving the CS# input to the logic LOW state enables the device, placing it in the Active Power mode. After Power-up, a falling edge on CS# is required prior to the start of any command.

3.6 Serial Input (SI) / IO0

This input signals used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCK clock signal. SI becomes IO0 - an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

3.7 Serial Output (SO) / IO1

This output signals used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCK clock signal. SO becomes IO1 - an input and output during Dual and Quad commands for receiving addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK in SDR commands, and on every edge of SCK, in DDR commands).

3.8 Write Protect (WP#) / IO2

When WP# is driven Low (V_{IL}), when the Status Register Protect 0 (SRP0_NV) or (SRP0) bit of Status Register 1 (SR1NV[7]) or (SR1V[7]) is set to '1', it is not possible to write to Status Registers, Configuration Registers or DLR registers. In this situation, the command selecting SR1NV, SR1V, CR1NV,CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV is ignored, and no error is set.

This prevents any alteration of the Legacy Block Protection settings. As a consequence, all the data bytes in the memory area that are protected by the Legacy Block Protection feature are also hardware protected against data modification if WP# is Low during commands changing Status Registers, Configuration Registers or DLR registers, with SRP0_NV set to 1. Similarly, the Security Region Lock Bits (LB3-LB0) are protected against programming.

The WP# function is not available when the Quad mode is enabled (CR1V[1] = 1) or QPI mode is enabled (CR2V[3] = 1). The WP# function is replaced by IO2 for input and output during Quad mode or QPI mode is enabled (CR2V[3] = 1) for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

WP# has an internal pull-up resistance; when unconnected, WP# is at V_{IH} and may be left unconnected in the host system if not used for Quad mode or QPI mode or protection.

3.9 IO3 / RESET#

IO3 is used for input and output during Quad mode (CR1V[1] = 1) or QPI mode is enabled (CR2V[3] = 1) for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

The IO3 / RESET# input may also be used to initiate the hardware reset function when the IO3 / RESET# feature is enabled by writing Configuration Register 2 non-volatile bit 7 (CR2NV[7] = 1). The input is only treated as RESET# when the device is not in Quad modes (114,144,444), CR1V[1] = 0, or when CS# is high. When Quad modes are in use, CR1V[1] = 1 or QPI mode is enabled (CR2V[3] = 1), and the device is selected with CS# LOW, the IO3 / RESET# is used only as IO3 for information transfer. When CS# is HIGH, the IO3 / RESET# is not in use for information transfer and is used as the reset input. By conditioning the reset operation on CS# HIGH during Quad modes (114,144,444), the reset function remains available during Quad modes (114,144,444).

When the system enters a reset condition, the CS# signal must be driven HIGH as part of the reset process and the IO3 / RESET# signal is driven LOW. When CS# goes HIGH, the IO3 / RESET# input transitions from being IO3 to being the reset input. The reset condition is then detected when CS# remains HIGH and the IO3 / RESET# signal remains LOW for t_{RP}. If a reset is not intended, the system is required to actively drive IO3 / RESET# to HIGH along with CS# being driven HIGH at the end of a transfer of data to the memory. Following transfers of data to the host system, the memory will drive IO3 HIGH during t_{CS}. This will ensure that IO3 / RESET# is not left floating or being pulled slowly to HIGH by the internal or an external passive pull-up. Thus, an unintended reset is not triggered by the IO3 / RESET# not being recognized as high before the end of t_{RP}.

The IO3 / RESET# input reset feature is disabled when (CR2V[7] = 0).

The IO3 / RESET# input has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad mode or the reset function. The internal pull-up will hold IO3 / RESET# HIGH after the host system has actively driven the signal high and then stops driving the signal.

Note that IO3 / RESET# input cannot be shared by more than one SPI-MIO memory if any of them are operating in Quad I/O mode as IO3 being driven to or from one selected memory may look like a reset signal to a second non-selected memory sharing the same IO3 / RESET# signal.

3.10 RESET#

The RESET# input provides a hardware method of resetting the device to standby state, ready for receiving a command. When RESET# is driven to logic low (V_{IL}) for at least a period of t_{RP}, the device starts the hardware reset process.

RESET# causes the same initialization process as is performed when power comes up and requires t_{PU} time.

RESET# may be asserted low at any time. To ensure data integrity any operation that was interrupted by a hardware, reset should be reinitiated once the device is ready to accept a command sequence.

RESET# has an internal pull-up resistor and may be left unconnected in the host system if not used. The internal pull-up will hold Reset high after the host system has actively driven the signal high and then stops driving the signal.

The RESET# input is not available on all packages options. When not available the RESET# input of the device is tied to the inactive state.

3.11 Voltage Supply (V_{CC})

V_{CC} is the voltage source for all device internal logic. It is the single voltage used for all device internal functions including read, program, and erase.

3.12 Supply and Signal Ground (V_{SS})

V_{SS} is the common voltage drain and ground reference for the device core, input signal receivers, and output drivers.

3.13 Not Connected (NC)

No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a printed circuit board (PCB).

3.14 Reserved for Future Use (RFU)

No device internal signal is currently connected to the package connector but there is potential future use of the connector. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.

3.15 Do Not Use (DNU)

A device internal signal may be connected to the package connector. The connection may be used by Infineon for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections.

4 Block diagram

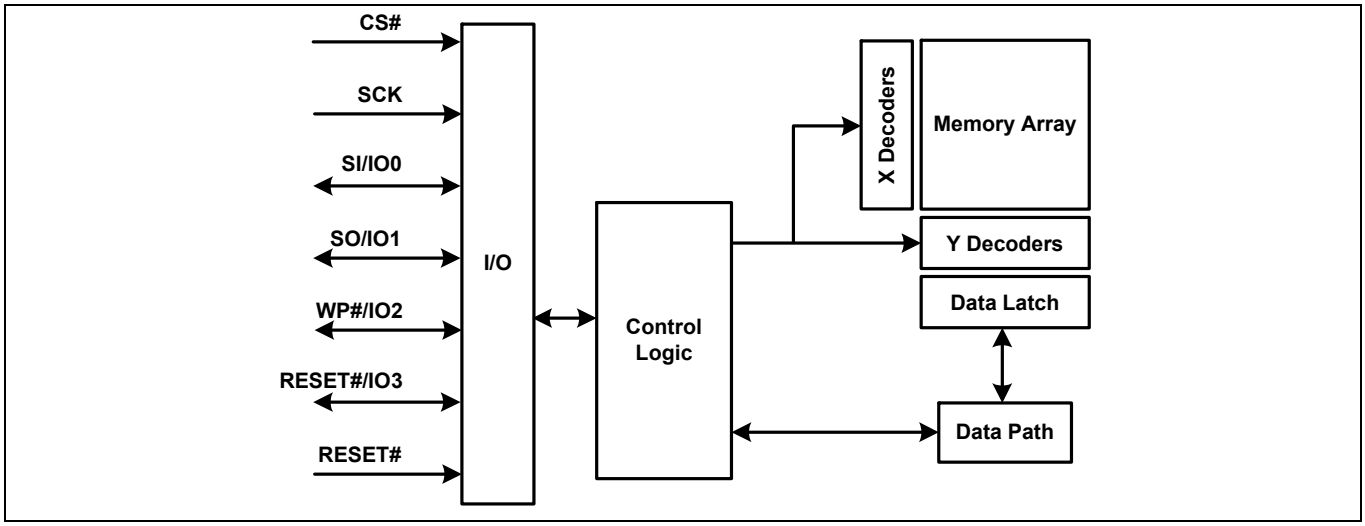


Figure 6 Logic block diagram

4.1 System block diagrams

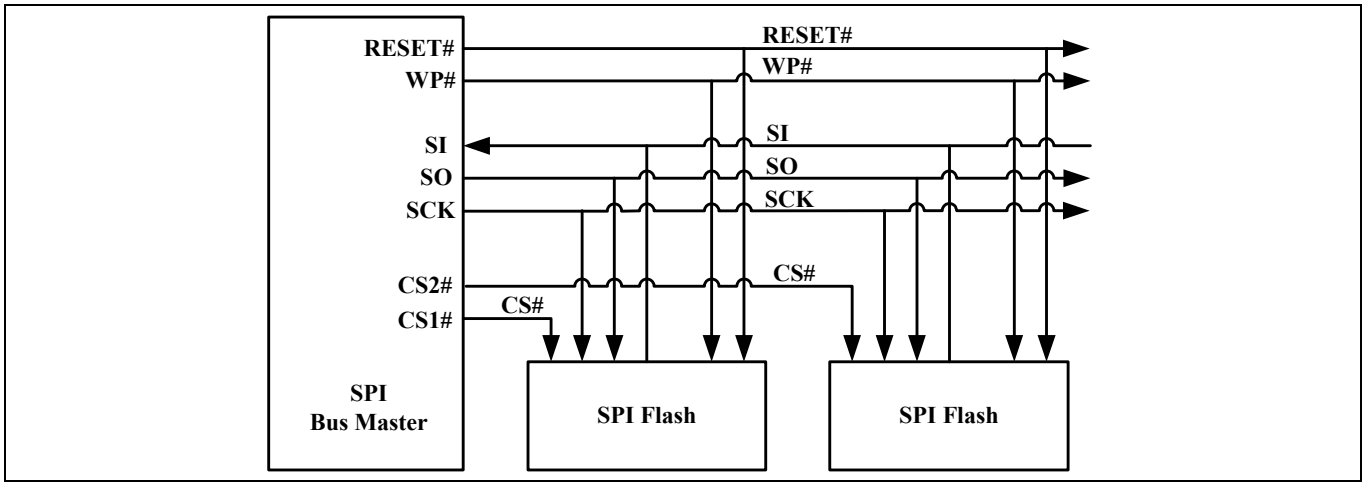


Figure 7 Bus master and memory devices on the SPI bus - single bit data path

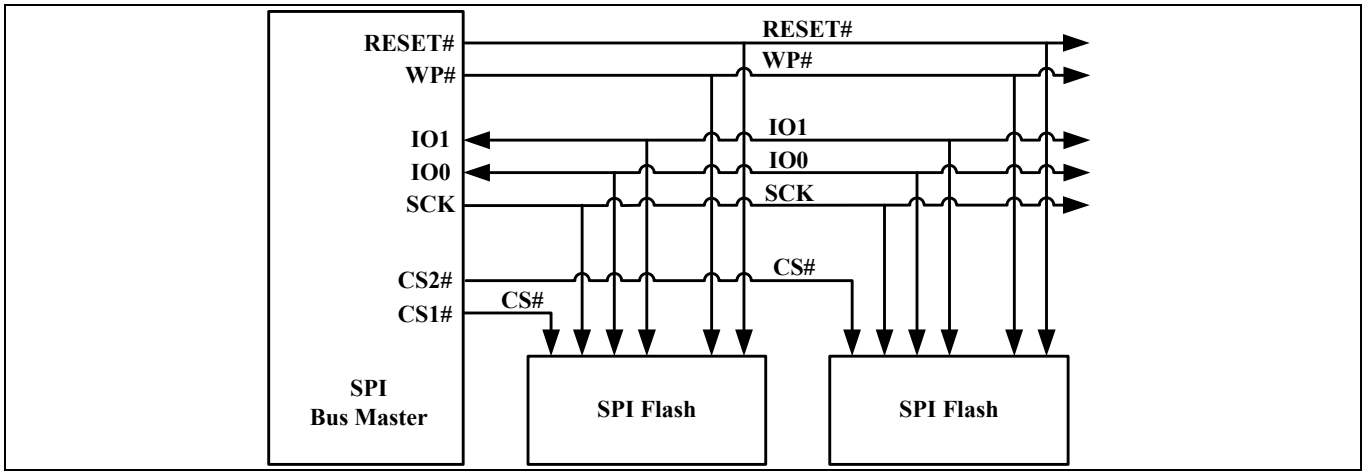


Figure 8 Bus master and memory devices on the SPI bus - dual bit data path

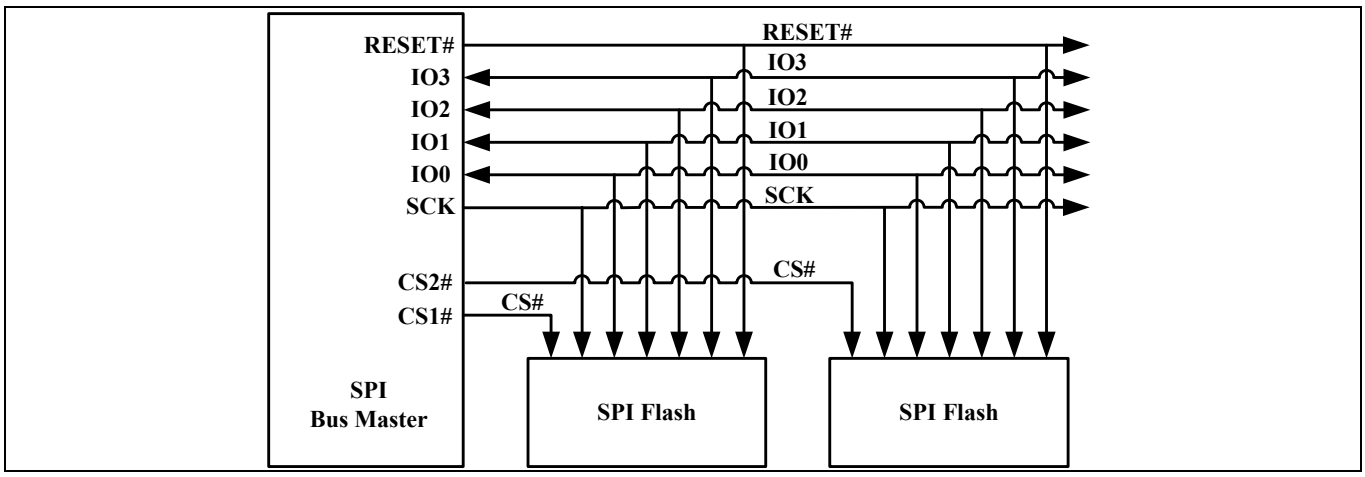


Figure 9 Bus master and memory devices on the SPI bus - quad bit data path - Separate RESET#

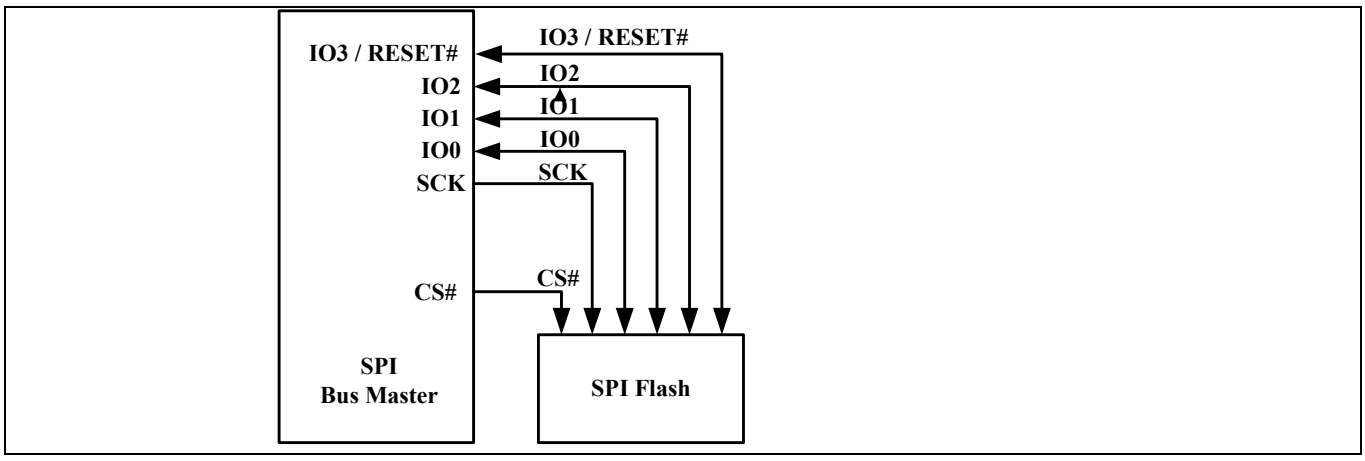


Figure 10 Bus master and memory devices on the SPI bus - quad bit data path - I/O3 / RESET#

5 Signal protocols

5.1 SPI clock modes

5.1.1 Single data rate (SDR)

The FL-L family can be driven by an embedded micro-controller (bus master) in either of the two following clocking modes.

- **Mode 0** with clock polarity (CPOL) = 0 and, clock phase (CPHA) = 0
- **Mode 3** with CPOL = 1 and, CPHA = 1

For these two modes, input data into the device is always latched in on the rising edge of the SCK signal and the output data is always available from the falling edge of the SCK clock signal.

The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring any data.

- SCK will stay at logic LOW state with CPOL = 0, CPHA = 0
- SCK will stay at logic HIGH state with CPOL = 1, CPHA = 1

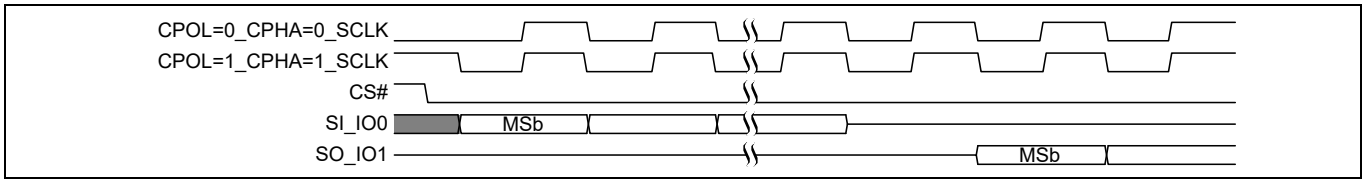


Figure 11 SPI SDR modes supported

Timing diagrams throughout the remainder of the document are generally shown as both Mode 0 and 3 by showing SCK as both HIGH and LOW at the fall of CS#. In some cases a timing diagram may show only Mode 0 with SCK LOW at the fall of CS#. In such a case, Mode 3 timing simply means clock is HIGH at the fall of CS# so no SCK rising edge set up or hold time to the falling edge of CS# is needed for Mode 3.

SCK cycles are measured (counted) from one falling edge of SCK to the next falling edge of SCK. In Mode 0, the beginning of the first SCK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCK because SCK is already low at the beginning of a command.

5.1.2 Double data rate (DDR)

Mode 0 and Mode 3 are also supported for DDR commands. In DDR commands, the instruction bits are always latched on the rising edge of clock, the same as in SDR commands. However, the address and input data that follow the instruction are latched on both the rising and falling edges of SCK. The first address bit is latched on the first rising edge of SCK following the falling edge at the end of the last instruction bit. The first bit of output data is driven on the falling edge at the end of the last access latency (dummy) cycle.

SCK cycles are measured (counted) in the same way as in SDR commands, from one falling edge of SCK to the next falling edge of SCK. In Mode 0, the beginning of the first SCK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCK because SCK is already LOW at the beginning of a command.

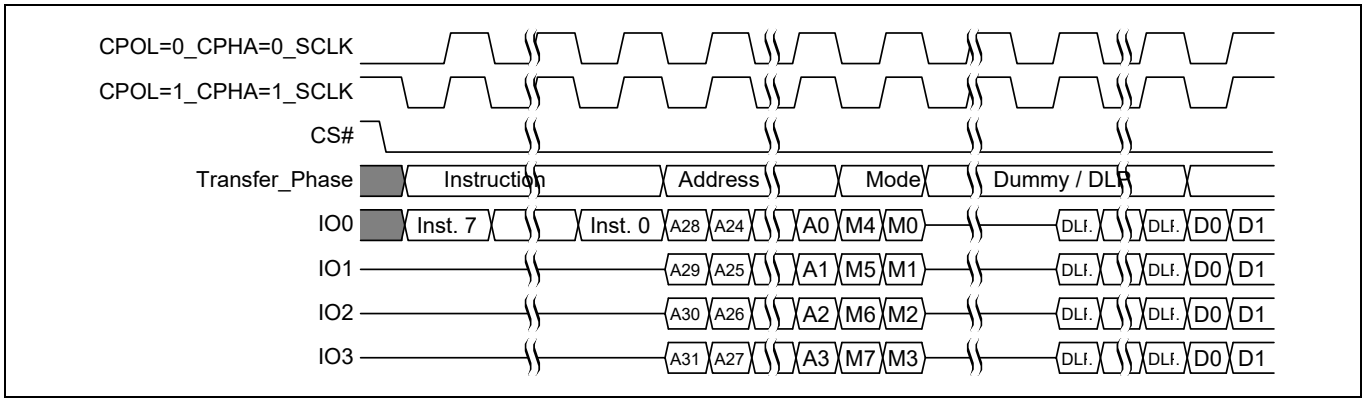


Figure 12 SPI DDR modes supported

5.2 Command protocol

All communication between the host system and FL-L family memory devices is in the form of units called commands. See **"Commands"** on page 70 for definition and details for all commands.

All commands begin with an 8-bit instruction that selects the type of information transfer or device operation to be performed. Commands may also have an address, instruction modifier, latency period, data transfer to the memory, or data transfer from the memory. All instruction, address, and data information is transferred sequentially between the host system and memory device.

Command protocols are also classified by a numerical nomenclature using three numbers to reference the transfer width of three command phases:

- instruction;
- address and instruction modifier (continuous read mode bits);
- data.

Single bit wide commands start with an instruction and may provide an address or data, all sent only on the SI signal. Data may be sent back to the host serially on the SO signal. This is referenced as a 1-1-1 command protocol for single bit width instruction, single bit width address and modifier, single bit data.

Dual-O or Quad-O commands provide an address sent from the host as serial on SI (IO0) then followed by dummy cycles. Data is returned to the host as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3. This is referenced as 1-1-2 for Dual-O and 1-1-4 for Quad-O command protocols.

Dual or Quad Input / Output (I/O) commands provide an address sent from the host as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3 then followed by dummy cycles. Data is returned to the host similarly as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3. This is referenced as 1-2-2 for Dual I/O and 1-4-4 for Quad I/O command protocols.

The FL-L family also supports a QPI mode in which all information is transferred in 4-bit width, including the instruction, address, modifier, and data. This is referenced as a 4-4-4 command protocol.

Commands are structured as follows:

- Each command begins with CS# going LOW and ends with CS# returning HIGH. The memory device is selected by the host driving the Chip Select (CS#) signal LOW throughout a command.
- The serial clock (SCK) marks the transfer of each bit or group of bits between the host and memory.
- Each command begins with an eight bit (byte) instruction. The instruction selects the type of information transfer or device operation to be performed. The instruction transfers occur on SCK rising edges. However, some read commands are modified by a prior read command, such that the instruction is implied from the earlier command. This is called Continuous Read Mode. When the device is in Continuous Read mode, the instruction bits are not transmitted at the beginning of the command because the instruction is the same as the read command that initiated the Continuous Read Mode. In Continuous Read mode, the command will begin with the read address. Thus, Continuous Read Mode removes eight instruction bits from each read command in a series of same type read commands.
- The instruction may be stand alone or may be followed by address bits to select a location within one of several address spaces in the device. The instruction determines the address space used. The address may be either a 24-bit or a 32-bit, byte boundary, address. The address transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- In legacy SPI mode, the width of all transfers following the instruction are determined by the instruction sent. Following transfers may continue to be single bit serial on only the SI or Serial Output (SO) signals, they may be done in two bit groups per (dual) transfer on the IO0 and IO1 signals, or they may be done in 4-bit groups per (quad) transfer on the IO0-IO3 signals. Within the dual or quad groups the least significant bit is on IO0. More significant bits are placed in significance order on each higher numbered IO signal. Single bits or parallel bit groups are transferred in most to LSb order.
- In QPI mode, the width of all transfers is a 4-bit wide (quad) transfer on the IO0–IO3 signals.

- Dual and Quad I/O read instructions send an instruction modifier called Continuous Read mode bits, following the address, to indicate whether the next command will be of the same type with an implied, rather than an explicit, instruction. These mode bits initiate or end the continuous read mode. In continuous read mode, the next command thus does not provide an instruction byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands. The mode bit transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- The address or mode bits may be followed by write data to be stored in the memory device or by a read latency period before read data is returned to the host.
- Write data bit transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- SCK continues to toggle during any read access latency period. The latency may be zero to several SCK cycles (also referred to as dummy cycles). At the end of the read latency cycles, the first read data bits are driven from the outputs on SCK falling edge at the end of the last read latency cycle. The first read data bits are considered transferred to the host on the following SCK rising edge. Each following transfer occurs on the next SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- If the command returns read data to the host, the device continues sending data transfers until the host takes the CS# signal high. The CS# signal can be driven high after any transfer in the read data sequence. This will terminate the command.
- At the end of a command that does not return data, the host drives the CS# input HIGH. The CS# signal must go HIGH after the eighth bit, of a stand alone instruction or, of the last write data byte that is transferred. That is, the CS# signal must be driven HIGH when the number of bits after the CS# signal was driven LOW is an exact multiple of eight bits. If the CS# signal does not go HIGH exactly at the eight bit boundary of the instruction or write data, the command is rejected and not executed.
- All instruction, address, and mode bits are shifted into the device with the MSb first. The data bits are shifted in and out of the device MSb first. All data is transferred in byte units with the lowest address byte sent first. Following bytes of data are sent in lowest to highest byte address order i.e. the byte address increments.
- All attempts to read the flash memory array during a program, erase, or a write cycle (embedded operations) are ignored. The embedded operation will continue to execute without any affect. A very limited set of commands are accepted during an embedded operation. These are discussed in the individual command descriptions.
- Depending on the command, the time for execution varies. A command to read status information from an executing command is available to determine when the command completes execution and whether the command was successful.

5.2.1 Command sequence examples

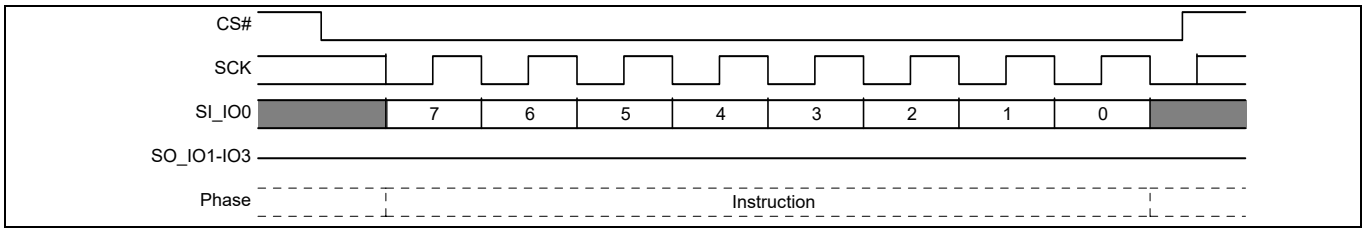


Figure 13 Standalone Instruction command

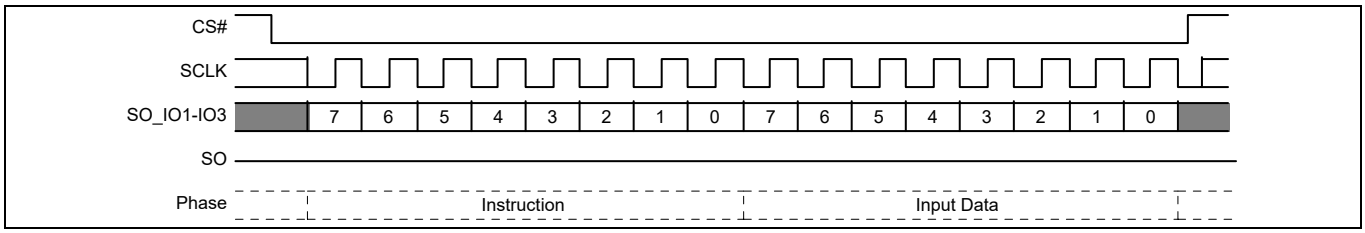


Figure 14 Single Bit Wide Input command

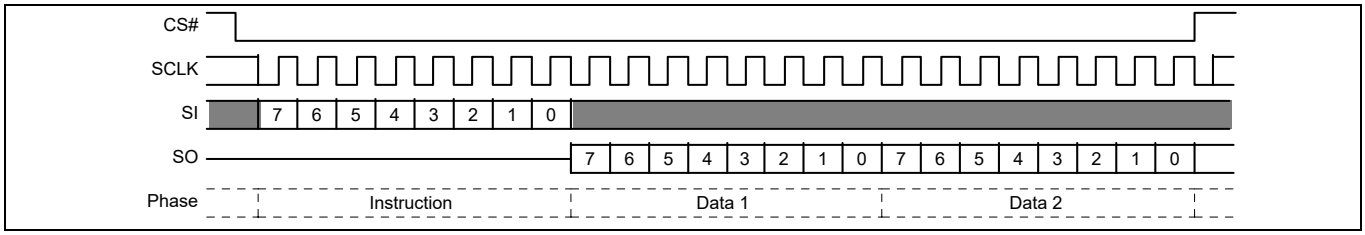


Figure 15 Single Bit Wide Output command without latency

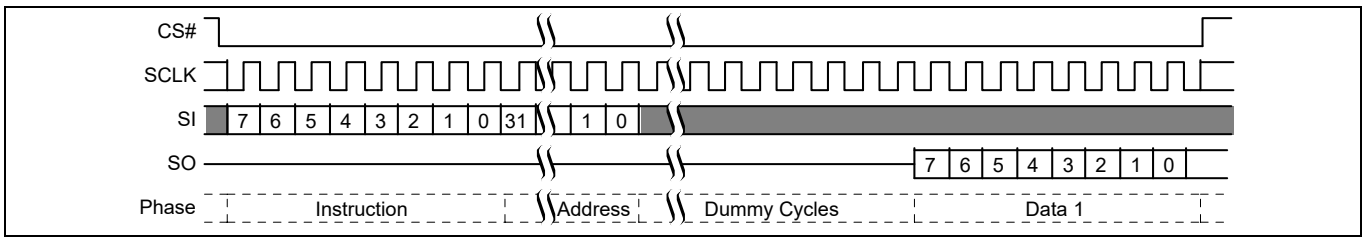


Figure 16 Single Bit Wide I/O command with latency

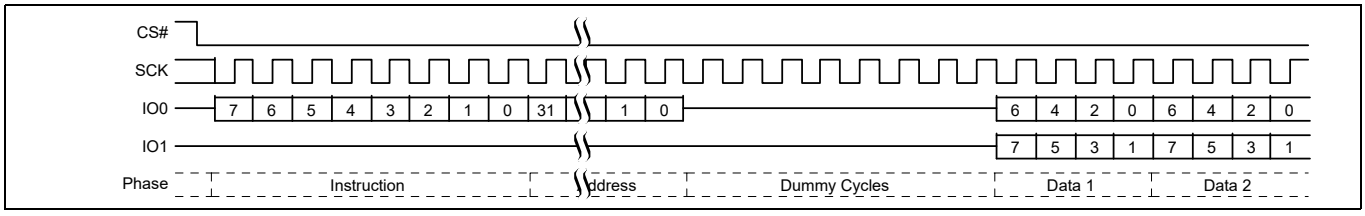


Figure 17 Dual Output Read command

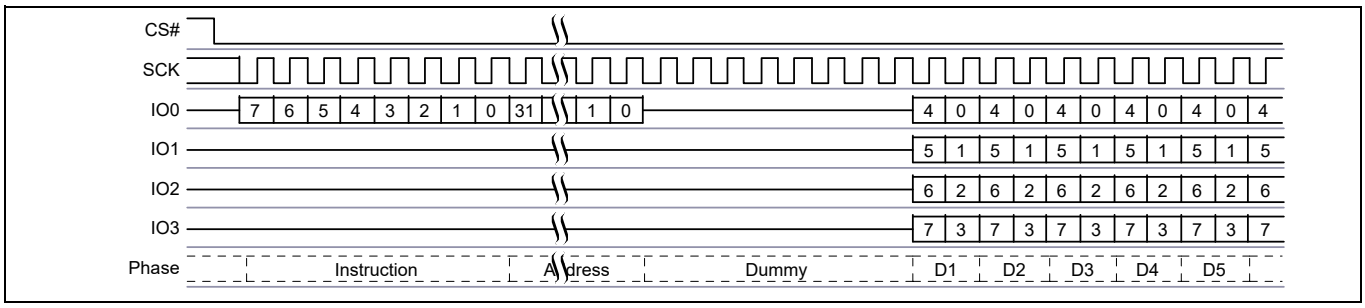


Figure 18 Quad Output Read command

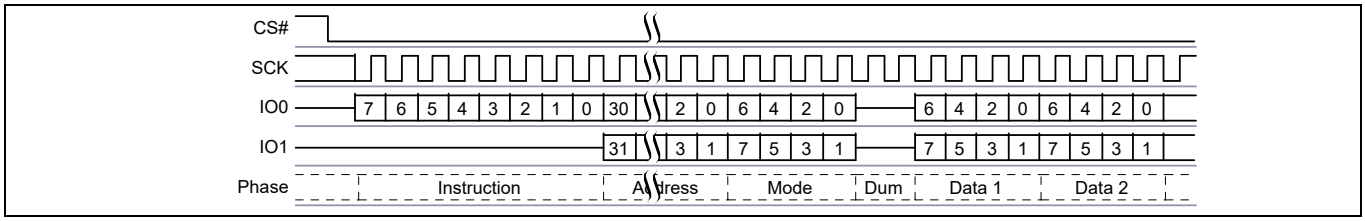


Figure 19 Dual I/O command

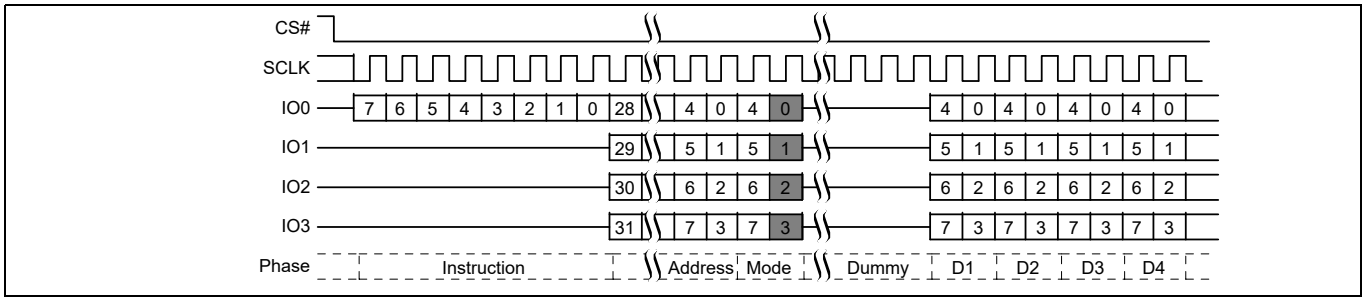


Figure 20 Quad I/O command[8]

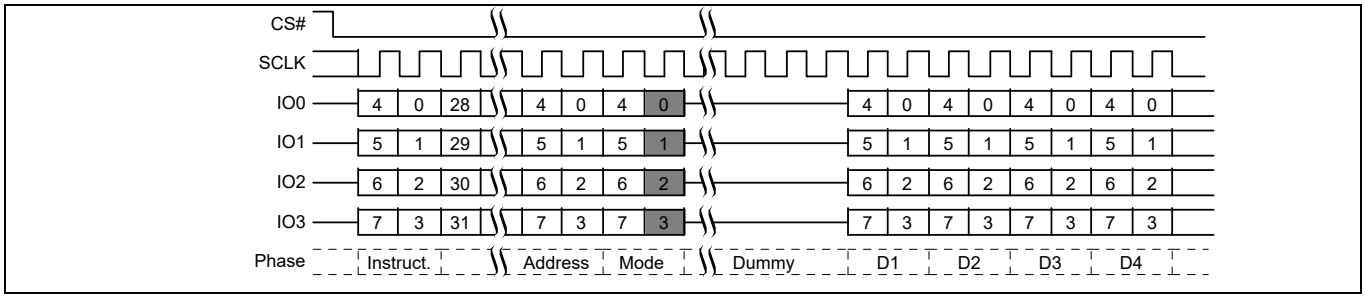


Figure 21 Quad I/O Read command in QPI mode[8]

Note
8. The gray bits are optional, the host does not have to drive bits during that cycle.

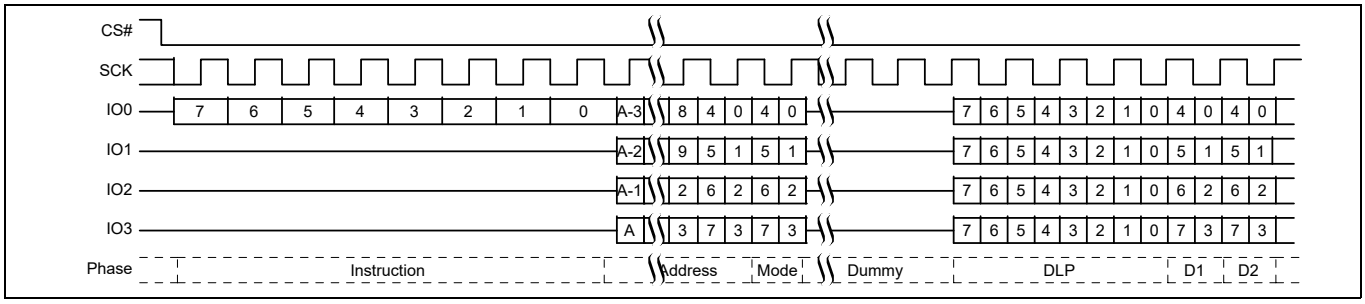


Figure 22 DDR Quad I/O Read command

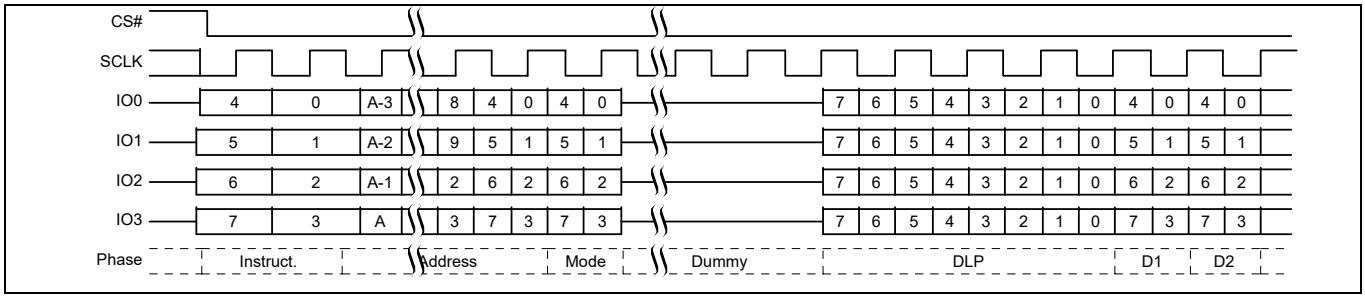


Figure 23 DDR Quad I/O Read command QPI mode

Additional sequence diagrams, specific to each command, are provided in **"Commands"** on page 70.

5.3 Interface states

This section describes the input and output signal levels as related to the SPI interface behavior.

Table 3 Interface states summary

Interface state	V_{CC}	SCK	CS#	RESET#	IO3 / RESET#	WP# / IO2	SO / IO1	SI / IO0
Power-off	<V_{CC} (low)	X	X	X	X	X	Z	X
Low power hardware data protection	<V_{CC} (cut-off)							
Power-On (Cold) Reset	≥V_{CC} (min)		HH					
Hardware (warm) reset non-quad mode			X	HL	HL			
Hardware (warm) reset quad mode			HH					
Interface standby				HH	HH	X		
Instruction cycle (legacy SPI)		HT	HL			HV		HV
Single input cycle Host to Memory transfer						X		
Single latency (dummy) cycle								X
Single output cycle Memory to Host transfer							MV	
Dual input cycle Host to Memory transfer							HV	HV
Dual latency (dummy) cycle							X	X
Dual output cycle Memory to Host transfer							MV	MV
Quad input cycle Host to Memory transfer					HV	HV	HV	HV
Quad latency (dummy) cycle					X	X	X	X
Quad output cycle Memory to Host transfer					MV	MV	MV	MV
DDR quad input cycle Host to Memory transfer					HV	HV	HV	HV
DDR latency (dummy) cycle					X	X	X	X
DDR quad output cycle Memory to Host transfer					MV	MV	MV	MV

Legend

Z = No driver - floating signal
HL = Host driving V_{IL}
HH = Host driving V_{IH}
HV = Either HL or HH
X = HL or HH or Z
HT = Toggling between HL and HH
ML = Memory driving V_{IL}
MH = Memory driving V_{IH}
MV = Either ML or MH

5.3.1 Power-off

When the core supply voltage is at or below the $V_{CC\ (Low)}$ voltage, the device is considered to be powered off. The device does not react to external signals, and is prevented from performing any program or erase operation.

5.3.2 Low power hardware data protection

When V_{CC} is less than $V_{CC\ (Cut\text{-}off)}$ the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range. When the core voltage supply remains at or below the $V_{CC\ (Low)}$ voltage for ≥ t_{PD} time, then rises to ≥ $V_{CC\ (Minimum)}$ the device will begin its Power On Reset (POR) process. POR continues until the end of t_{PU}. During t_{PU} the device does not react to external input signals nor drive any outputs. Following the end of t_{PU}, the device transitions to the Interface Standby state and can accept commands. For additional information on POR see **"Power-on (cold) reset"** on page 157.

5.3.3 Hardware (Warm) reset

A configuration option is provided to allow IO3 / RESET# to be used as a hardware reset input when the device is not in any Quad or QPI mode or when it is in any Quad mode or QPI mode and CS# is HIGH. In Quad or QPI mode on some packages a separate reset input is provided (RESET #). When IO3 / RESET# or RESET# is driven LOW for t_{RP} time the device starts the hardware reset process. The process continues for t_{RPH} time. Following the end of both t_{RPH} and the reset hold time following the rise of RESET# (t_{RH}) the device transitions to the Interface Standby state and can accept commands. For additional information on hardware reset, see **"Reset"** on page 157.

5.3.4 Interface standby

When CS# is HIGH, the SPI interface is in Standby state. Inputs other than RESET# are ignored. The interface waits for the beginning of a new command. The next interface state is instruction cycle when CS# goes LOW to begin a new command.

While in Interface Standby state, the memory device draws standby current (I_{SB}) if no embedded algorithm is in progress. If an embedded algorithm is in progress, the related current is drawn until the end of the algorithm when the entire device returns to standby current draw.

5.3.5 Instruction cycle (Legacy SPI mode)

When the host drives the MSb of an instruction and CS# goes LOW, on the next rising edge of SCK the device captures the MSb of the instruction that begins the new command. On each following rising edge of SCK, the device captures the next lower significance bit of the 8-bit instruction. The host keeps CS# LOW, and drives the Write Protect (WP#) and IO3 / RESET# signals as needed for the instruction. However, WP# is only relevant during instruction cycles of a WRR or WRAR command or any other commands which affect Status registers, Configuration registers and DLR registers, and is otherwise ignored. IO3 / RESET# is driven HIGH when the device is not in Quad Mode (CR1V[1] = 0) or QPI Mode (CR2V[3] = 0) and hardware reset is not required.

Each instruction selects the address space that is operated on and the transfer format used during the remainder of the command. The transfer format may be Single, Dual O, Quad O, Dual I/O, or Quad I/O, or DDR Quad I/O. The expected next interface state depends on the instruction received.

Some commands are standalone, needing no address or data transfer to or from the memory. The host returns CS# HIGH after the rising edge of SCK for the eighth bit of the instruction in such commands. The next interface state in this case is Interface Standby.

5.3.6 Instruction cycle (QPI mode)

In QPI mode, when CR2V[3] = 1, instructions are transferred 4 bits per cycle. In this mode instruction cycles are the same as a Quad Input cycle (see **"QPP or QOR address input cycle"** on page 27).

5.3.7 Single input cycle — Host to Memory transfer

Several commands transfer information after the instruction on the single serial input (SI) signal from host to the memory device. The host keeps RESET# HIGH, CS# LOW, and drives SI as needed for the command. The memory does not drive the Serial Output (SO) signal.

The expected next interface state depends on the instruction. Some instructions continue sending address or data to the memory using additional Single Input Cycles. Others may transition to Single Latency, or directly to Single, Dual, or Quad Output cycle states.

5.3.8 Single latency (Dummy) cycle

Read commands may have zero to several latency cycles during which read data is read from the main Flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR3V[3:0]). During the latency cycles, the host keeps RESET# and IO3 / RESET# HIGH, CS# LOW and SCK toggles. The Write Protect (WP#) signal is ignored. The host may drive the SI signal during these cycles or the host may leave SI floating. The memory does not use any data driven on SO or other I/O signals during the latency cycles. The memory does not drive the serial output (SO) or I/O signals during the latency cycles.

The next interface state depends on the command structure i.e. the number of latency cycles, and whether the read is single, dual, or quad width.

5.3.9 Single output cycle — Memory to Host transfer

Several commands transfer information back to the host on the single serial output (SO) signal. The host keeps RESET# and IO3 / RESET# HIGH, CS# LOW. The Write Protect (WP#) signal is ignored. The memory ignores the Serial Input (SI) signal. The memory drives SO with data.

The next interface state continues to be serial output cycle until the host returns CS# to HIGH ending the command.

5.3.10 Dual input cycle — Host to Memory transfer

The Read Dual I/O command transfers two address or mode bits to the memory in each cycle. The host keeps RESET# and IO3 / RESET# HIGH, CS# LOW. The Write Protect (WP#) signal is ignored. The host drives address on SI / IO0 and SO / IO1.

The next interface state following the delivery of address and mode bits is a dual latency cycle if there are latency cycles needed or dual output cycle if no latency is required.

5.3.11 Dual latency (dummy) cycle

Read commands may have zero to several latency cycles during which read data is read from the main Flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the Configuration Register (CR3V[3:0]). During the latency cycles, the host keeps RESET# and IO3 / RESET# HIGH, CS# LOW, and SCK continues to toggle. The Write Protect (WP#) signal is ignored. The host may drive the SI / IO0 and SO / IO1 signals during these cycles or the host may leave SI / IO0 and SO / IO1 floating. The memory does not use any data driven on SI / IO0 and SO / IO1 during the latency cycles. The host must stop driving SI / IO0 and SO / IO1 on the falling edge of SCK at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the SI / IO0 and SO / IO1 signals during the latency cycles.

The next interface state following the last latency cycle is a dual output cycle.

5.3.12 Dual output cycle — Memory to Host transfer

The read dual output and read dual I/O return data to the host two bits in each cycle. The host keeps RESET# and IO3 / RESET# HIGH, CS# LOW. The Write Protect (WP#) signal is ignored. The memory drives data on the SI / IO0 and SO / IO1 signals during the dual output cycles on the falling edge of SCK.

The next interface state continues to be dual output cycle until the host returns CS# to HIGH ending the command.

5.3.13 QPP or QOR address input cycle

The Quad Page Program and Quad Output Read commands send address to the memory only on IO0. The other IO signals are ignored. The host keeps RESET# and IO3 / RESET# HIGH, CS# LOW, and drives IO0.

For QPP, the next interface state following the delivery of address is the quad input cycle. For QOR, the next interface state following address is a quad latency cycle if there are latency cycles needed or quad output cycle if no latency is required.

5.3.14 Quad input cycle — Host to Memory transfer

The Quad I/O Read command transfers four address or mode bits to the memory in each cycle. In QPI mode, the Quad I/O Read and Page Program commands transfer four data bits to the memory in each cycle, including the instruction cycles. The host keeps CS# LOW, and drives the IO signals.

For Quad I/O Read, the next interface state following the delivery of address and mode bits is a quad latency cycle if there are latency cycles needed or quad output cycle if no latency is required. For QPI mode page program, the host returns CS# HIGH following the delivery of data to be programmed and the interface returns to standby state.

5.3.15 Quad latency (dummy) cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the latency code in the Configuration Register (CR3V[3:0]). During the latency cycles, the host keeps CS# LOW and continues to toggle SCK. The host may drive the IO signals during these cycles or the host may leave the IO floating. The memory does not use any data driven on IO during the latency cycles. The host must stop driving the IO signals on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the IO signals during the latency cycles.

The next interface state following the last latency cycle is a Quad Output Cycle.

5.3.16 Quad output cycle — Memory to Host transfer

The Quad-O and Quad I/O Read returns data to the host four bits in each cycle. The host keeps CS# LOW. The memory drives data on IO0–IO3 signals during the Quad output cycles.

The next interface state continues to be Quad Output Cycle until the host returns CS# to HIGH ending the command.

5.3.17 DDR Quad input cycle — Host to Memory transfer

The DDR Quad I/O Read command sends address, and mode bits to the memory on all the IO signals. Four bits are transferred on the rising edge of SCK and four bits on the falling edge in each cycle. The host keeps CS# LOW.

The next interface state following the delivery of address and mode bits is a DDR latency cycle.

5.3.18 DDR latency cycle

DDR Read commands may have one to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the latency code in the configuration register (CR3V[3:0]). During the latency cycles, the host keeps CS# LOW. The host may not drive the IO signals during these cycles. So that there is sufficient time for the host drivers to turn off before the memory begins to drive. This prevents driver conflict between host and memory when the signal direction changes. The memory has an option to drive all the IO signals with a data learning pattern (DLP) during the last 4 latency cycles. The DLP option should not be enabled when there are fewer than five latency cycles so that there is at least one cycle of high impedance for turn around of the IO signals before the memory begins driving the DLP. When there are more than 4 cycles of latency the memory does not drive the IO signals until the last four cycles of latency.

The next interface state following the last latency cycle is a DDR quad output cycle, depending on the instruction.

5.3.19 DDR quad output cycle — Memory to Host transfer

The DDR Quad I/O Read command returns bits to the host on all the IO signals. Four bits are transferred on the rising edge of SCK and four bits on the falling edge in each cycle. The host keeps CS# LOW.

The next interface state continues to be DDR quad output cycle until the host returns CS# to HIGH ending the command.

5.4 Data protection

Some basic protection against unintended changes to stored data are provided and controlled purely by the hardware design. These are described in **"Data protection"** on page 54. Other software managed protection methods are discussed in the **"Data protection"** on page 54 of this document.

5.4.1 Power-up

The device must not be selected at power-up (that is, CS# must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value as follows:

- V_{CC} (min) at power-up, and then for a further delay of t_{PU}

User is not allowed to enter any command until a valid delay of t_{PU} has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold (see **Figure 131**). However, correct operation of the device is not guaranteed if V_{CC} returns below V_{CC} (min) during t_{PU}. No command should be sent to the device until the end of t_{PU}.

5.4.2 Low power

When V_{CC} is less than $V_{CC\ (Cut\text{-}off)}$ the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

5.4.3 Clock pulse count

The device verifies that all non-volatile memory and register data modifying commands consist of a clock pulse count that is a multiple of eight bit transfers (byte boundary) before executing them. A command not ending on an 8-bit (byte) boundary is ignored and no error status is set for the command.

5.4.4 Deep power down (DPD)

In DPD mode, the device responds only to the Resume from DPD command (RES ABh). All other commands are ignored during DPD mode, thereby protecting the memory from program and erase operations. If the IO3 / RESET# function has been enabled (CR2V[7] = 1) or if RESET# is active, IO3 / RESET# or RESET# going LOW will start a hardware reset and release the device from DPD mode.

6 Address space maps

6.1 Overview

6.1.1 Extended address

The FL-L family supports 32-bit (4 byte) addresses to enable higher density devices than allowed by previous generation (legacy) SPI devices that supported only 24-bit (3 Byte) addresses. A 24-bit, byte resolution, address can access only 16 MB (128 Mb) maximum density. A 32-bit, byte resolution, address allows direct addressing of up to a 4 GB (32 Gb) address space.

Legacy commands continue to support 24-bit addresses for backward software compatibility. Extended 32-bit addresses are enabled in two ways:

- Extended address mode: a volatile configuration register bit that changes all legacy commands to expect 32 bits of address supplied from the host system.
- 4 byte address commands: that perform both legacy and new functions, which always expect 32-bit address.

The default condition for extended address mode, after power-up or reset, is controlled by a non-volatile configuration bit. The default extended address mode may be set for 24- or 32-bit addresses. This enables legacy software compatible access to the first 128 Mb of a device or for the device to start directly in 32-bit address mode.

6.1.2 Multiple address spaces

Many commands operate on the main flash memory array. Some commands operate on address spaces separate from the main Flash array. Each separate address space uses the full 24- or 32-bit address but may only define a small portion of the available address space.

6.2 Flash memory array

The main flash array is divided into uniform erase units called physical blocks (64 KB), half blocks (32 KB) and sectors (4 KB).

Table 4 S25FL256L sector address map

Block size (KB)	Block count	Block range	Half block size (KB)	Half block count	Half block range	Sector size (KB)	Sector count	Sector range	Address range (byte address)	Notes
64	1	BA00	32	1	HBA00	4	1	SA00	0000000h–0000FFFh	Sector Starting Address
						:	:	:	:	
			32	2	HBA01	4	16	SA15	000F000h–000FFFFh	
:	:	:	:	:	:	:	:	:	:	—
64	512	BA511	32	1023	HBA1022	4	8176	SA8175	1FF0000h–1FF0FFFh	
						:	:	:	:	
			32	1024	HBA1023	4	8192	SA8191	1FFF000h–1FFFFFFh	Sector Ending Address

Table 5 S25FL128L sector address map

Block size (KB)	Block count	Block range	Half block size (KB)	Half block count	Half block range	Sector size (KB)	Sector count	Sector range	Address range (byte address)	Notes
64	1	BA00	32	1	HBA00	4	1	SA00	000000h–000FFFh	Sector Starting Address
						:	:	:	:	
			32	2	HBA01	4	16	SA15	00F000h–00FFFFh	
:	:	:	:	:	:	:	:	:	:	—
64	256	BA255	32	511	HBA510	4	4080	SA4079	FF0000h–FF0FFFh	
						:	:	:	:	
			32	512	HBA511	4	4096	SA4095	FFF000h–FFFFFFh	Sector Ending Address

6.3 ID address space

The RDID command (9Fh) reads information from a separate Flash memory address space for device identification (ID). See **"Device ID address map"** on page 147 for the tables defining the contents of the ID address space. The ID address space is programmed by Infineon and read-only for the host system.

6.3.1 Device Unique ID

A 64-bit unique number is located in 8 bytes of the Unique Device ID address space, see **Table 52**. This Unique ID may be used as a software readable serial number that is unique for each device.

6.4 JEDEC JESD216 serial flash discoverable parameters (SFDP) space

The RSFDP command (5Ah) reads information from a separate Flash memory address space for device identification, feature, and configuration information, in accord with the JEDEC JESD216 standard for Serial Flash Discoverable Parameters. The ID address space is incorporated as one of the SFDP parameters. See **"JEDEC JESD216B serial flash discoverable parameters"** on page 137 for the tables defining the contents of the SFDP address space. The SFDP address space is programmed by Infineon and read-only for the host system.

6.5 Security Regions address space

Each FL-L family memory device has a 1024-byte Security Regions address space that is separate from the main Flash array. The Security Regions area is divided into 4, individually lockable 256-byte regions. The Security Regions memory space is intended to hold information that can be temporarily protected or permanently locked from further program or erase.

The regions data bytes are erased to FFh when shipped from Infineon. The regions may be programmed and erased like any other Flash memory address space when not protected or locked. Each region can be individually erased. The Security Region Lock Bits (CR1NV[5:2]) are located in the Configuration Register 1. The Security Region Lock Bits are One Time Programmable (OTP) and after being programmed (set to 1) a Lock Bit permanently protects the related region from further erase or programming.

Regions 2 and 3 also have temporary protection from program or erase by the Protection Register (PR) NVLock bit. The NVLock bit is volatile and set or cleared by the IRP logic and commands. See **"Protection Register (PR)"** on page 51.

The Security Region Password Protection Bit in the IRP Register (IRP[2]) allows Regions 2 and 3 to be protected from Program and Erase operations until a password is provided. The Security Region Read Protection Bit in the IRP Register (IRP[6]) allows Region 3 to also be protected from Read operations until a password is provided. Attempting to read in a region, that is protected from read, returns invalid and undefined data. See **"Individual and Region Protection Register (IRP)"** on page 49.

Attempting to erase or program in a region that is locked or protected will fail with the P_ERR or E_ERR bit in SR2V[6:5] set to '1' (see **"Status Register 2 Volatile (SR2V)"** on page 38 for detail descriptions).

Table 6 Security Region address map

Region	Byte address range (Hex)	Initial delivery state (Hex)
Region 0	000 to 0FF	All bytes = FF
Region 1	100 to 1FF	
Region 2	200 to 2FF	
Region 3	300 to 3FF	

6.6 Registers

Registers are small groups of memory cells used to configure how the FL-L family memory device operates or to report the status of device operations. The registers are accessed by specific commands. The commands (and hexadecimal instruction codes) used for each register are noted in each register description.

In legacy SPI memory devices, the individual register bits could be a mixture of volatile, non-volatile, or One Time Programmable (OTP) bits within the same register. In some configuration options, the type of a register bit could change e.g. from non-volatile to volatile.

The FL-L family uses separate non-volatile or volatile memory cell groups (areas) to implement the different register bit types. However, the legacy registers and commands continue to appear and behave as they always have for legacy software compatibility. There is a non-volatile and a volatile version of each legacy register when that legacy register has volatile bits or when the command to read the legacy register has zero read latency. When such a register is read the volatile version of the register is delivered. During power-on reset (POR), hardware reset, or software reset, the non-volatile version of a register is copied to the volatile version to provide the default state of the volatile register. When non-volatile register bits are written the non-volatile version of the register is erased and programmed with the new bit values and the volatile version of the register is updated with the new contents of the non-volatile version. When OTP bits are programmed, the non-volatile version of the register is programmed and the appropriate bits are updated in the volatile version of the register. When volatile register bits are written, only the volatile version of the register has the appropriate bits updated.

The type for each bit is noted in each register description. The default state shown for each bit refers to the state after power-on reset, hardware reset, or software reset if the bit is volatile. If the bit is non-volatile or OTP, the default state is the value of the bit when the device is shipped from Infineon. Special attention must be given when writing the nonvolatile registers that there is a stable power supply with no disruption, this will guarantee the correct data is written to the register.

6.6.1 Status Register 1

6.6.1.1 Status Register 1 Nonvolatile (SR1NV) S25FL256L

Related Commands: Non-volatile Write Enable (WREN 06h), Write Disable (WRDI 04h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 7 Status Register 1 Non-Volatile (SR1NV)

Bits	Field name	Function	Type	Default state	Description
7	SRP0_NV	Status Register Protect 0 Default	Non-volatile	0	Provides the default state for SRP0.
6	TBPROT_NV	TBPROT Default	Non-volatile	0	Provides the default state for TBPROT
5	BP_NV3	Legacy Block Protection Default	Non-volatile	0000b	Provides the default state for BP bits.
4	BP_NV2				
3	BP_NV1				
2	BP_NV0				
1	WEL_D	WEL Default	Non-volatile Read Only	0	Provides the default state for the WEL Status. Not user programmable.
0	WIP_D	WIP Default	Non-volatile Read Only	0	Provides the default state for the WIP Status. Not user programmable.

Status Register Protect Non-volatile (SRP0_NV) SR1NV[7]: Provides the default state for SRP0 (see **"Status Register Protect (SRP1, SRP0)"** on page 56).

Top or Bottom Protection (TBPROT_NV) SR1NV[6]: Provides the default state for TBPROT.

Legacy Block Protection (BP_NV3, BP_NV2, BP_NV1, BP_NV0) SR1NV[5:2]: Provides the default state for BP_3 to BP_0 bits.

Write Enable Latch Default (WEL_D) SR1NV[1]: Provides the default state for the WEL Status in SR1V[1]. This bit is programmed by Infineon and is not user programmable.

Write In Progress Default (WIP_D) SR1NV[0]: Provides the default state for the WIP Status in SR1V[0]. This bit is programmed by Infineon and is not user programmable.

6.6.1.2 Status Register 1 Volatile (SR1V) S25FL256L

Related Commands: Read Status Register 1 (RDSR1 05h), Write Enable for Volatile (WRENV 50h), Write Registers (WRR 01h), Clear Status Register (CLSR 30h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h). This is the register displayed by the RDSR1 command.

Table 8 S25FL256L Status Register 1 Volatile (SR1V)

Bits	Field name	Function	Type	Default state	Description
7	SRP0	Status Register Protect 0	Volatile	SR1NV	1 = Locks state of SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV when WP# is low, by not executing any command that would affect SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV 0 = No register protection, even when WP# is low.
6	TBPROT	Top or Bottom Relative Protection	Volatile		1 = BP starts at bottom (Low address) 0 = BP starts at top (High address)
5	BP3	Legacy Block Protection Volatile	Volatile		Protects the selected range of sectors (Blocks) from Program or Erase.
4	BP2				
3	BP1				
2	BP0				
1	WEL	Write Enable Latch	Volatile Read Only		0 = Not write enabled, no embedded operation can start, 1 = Write Enable, embedded operation can start This bit is not affected by WRR or WRAR, only WREN, WRENV, WRDI and CLSR commands affect this bit.
0	WIP	Write in Progress	Volatile Read Only		1 = Device Busy, an embedded operation is in progress such as program or erase 0 = Ready Device is in standby mode and can accept commands This bit is not affected by WRR or WRAR, it only provides WIP status.

Status Register Protect 0 (SRP0) SR1V[7]: Places the device in the Hardware Protected mode when this bit is set to '1' and the WP# input is driven LOW. In this mode, any commands that change Status Registers or Configuration Registers are ignored and not accepted for execution, effectively locking the state of the Status Registers and Configuration Registers SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV bits, by making the registers read-only. If WP# is HIGH, Status Registers and Configuration Registers SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV may be changed. If SRP0 is '0', WP# has no effect, the Status Registers and Configuration Registers SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV may be changed. WP# has no effect on the writing of any other registers. SRP0 tracks any changes to the non-volatile version of this bit (SRP0_NV). When QPI or QIO mode is enabled (CR2V[3] or CR1V[1] = 1), the internal WP# signal level is = 1 because the WP# external input is used as IO2 when either mode is active. This effectively turns off hardware protection. The Register SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV are unlocked and can be written (see **"Status Register Protect (SRP1, SRP0)"** on page 56).

TBPROT SR1V[6]: This bit defines the reference point of the Legacy Block Protection bits BP3, BP2, BP1, and BP0 in the Status Register. As described in the Status Register section, the BP3–0 bits allow the user to optionally protect a portion of the array, ranging from 1/64, ¼, ½, etc., up to the entire array. When TBPROT is set to a '0' the Legacy Block Protection is defined to start from the top (maximum address) of the array. When TBPROT is set to a '1', the Legacy Block Protection is defined to start from the bottom (zero address) of the array. TBPROT tracks any changes to the non-volatile version of this bit (TBPROT_NV).

Legacy Block Protection (BP3, BP2, BP1, BP0) SR1V[5:2]: These bits define the main Flash array area to be protected against program and erase commands. See **"Legacy block protection"** on page 59 for a description of how the BP bit values select the memory array area protected.

Write Enable Latch (WEL) SR1V[1]: The WEL bit must be set to '1', to enable program, write, or erase operations as a means to provide protection against inadvertent changes to memory or register values. The Write Enable (WREN) command execution sets the Write Enable Latch to a '1' to allow any program, erase, or write commands to execute afterwards. The Write Disable (WRDI) command can be used to set the Write Enable Latch to '0' to prevent all program, erase, and write commands from execution. The WEL bit is cleared to '0' at the end of any successful program, write, or erase operation. Following a failed operation the WEL bit may remain set and should be cleared with a CLSR command. After a power down / power up sequence, hardware reset, or software reset, the Write Enable Latch is set to a WEL_D. The WRR or WRAR command does not affect this bit.

Write In Progress (WIP) SR1V[0]: Indicates whether the device is performing a program, write, erase operation, or any other operation, during which a new operation command will be ignored. When the bit is set to '1' the device is busy performing an operation. While WIP is '1', only Read Status Registers (RDSR1, RDSR2), Read Any Register (RDAR), Erase / Program Suspend (EPS), Clear Status Register (CLSR), Read Configuration Registers (RDCR1, RDCR2, RDCR3) and Software Reset (RSTEN 66h followed by RST 99h) commands are accepted. EPS command will only be accepted if memory array erase or program operations are in progress. The status register E_ERR and P_ERR bits are updated while WIP = 1. When P_ERR or E_ERR bits are set to '1', the WIP bit will remain set to one indicating the device remains busy and unable to receive new operation commands. A Clear Status Register (CLSR) command must be received to return the device to Standby mode. When the WIP bit is cleared to 0, no operation is in progress. This is a read-only bit.

6.6.1.3 Status Register 1 Non-volatile (SR1NV) S25FL128L

Related Commands: Non-volatile Write Enable (WREN 06h), Write Disable (WRDI 04h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 9 S25FL128L Status Register 1 Non-volatile (SR1NV)

Bits	Field name	Function	Type	Default state	Description
7	SRP0_NV	Status Register Protect 0 Default	Non-volatile	0	Provides the default state for SRP0.
6	SEC_NV	Sector / Block Protect	Non-volatile	0	Provides the defaults state for SEC.
5	TBPROT_NV	TBPROT Default	Non-volatile	0	Provides the default state for TBPROT.
4	BP_NV2	Legacy Block Protection Default	Non-volatile	000b	Provides the default state for BP bits.
3	BP_NV1				
2	BP_NV0				
1	WEL_D	WEL Default	Non-volatile Read Only	0	Provides the default state for the WEL Status. Not user programmable.
0	WIP_D	WIP Default	Non-volatile Read Only	0	Provides the default state for the WIP Status. Not user programmable.

Status Register Protect Non-volatile (SRP0_NV) SR1NV[7]: Provides the default state for SRP0. See **"Status Register Protect (SRP1, SRP0)"** on page 56.

Sector / Block Protect (SEC_NV) SR1NV[6]: Provides the default state for SEC.

Top or Bottom Protection (TBPROT_NV) SR1NV[5]: Provides the default state for TBPROT.

Legacy Block Protection (BP_NV3, BP_NV2, BP_NV1, BP_NV0) SR1NV[4:2]: Provides the default state for BP_2 to BP_0 bits.

Write Enable Latch Default (WEL_D) SR1NV[1]: Provides the default state for the WEL Status in SR1V[1]. This bit is programmed by Infineon and is not user programmable.

Write In Progress Default (WIP_D) SR1NV[0]: Provides the default state for the WIP Status in SR1V[0]. This bit is programmed by Infineon and is not user programmable.

6.6.1.4 Status Register 1 Volatile (SR1V) S25FL128L

Related Commands: Read Status Register 1(RDSR1 05h), Write Enable for Volatile (WRENV 50h), Write Registers (WRR 01h), Clear Status Register (CLSR 30h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h). This is the register displayed by the RDSR1 command.

Table 10 S25FL128L Status Register 1 Volatile (SR1V)

Bits	Field name	Function	Type	Default state	Description
7	SRP0	Status Register Protect 0	Volatile	SR1NV	1 = Locks state of SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV when WP# is low, by not executing any commands that would affect SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV 0 = No register protection, even when WP# is low.
6	SEC	Sector / Block Protect	Volatile		0 = BP2–BP0 protect 64 KB blocks 1 = BP2–BP0 protect 4 KB sectors
5	TBPROT	Top or Bottom Relative Protection	Volatile		1 = BP starts at bottom (Low address) 0 = BP starts at top (High address)
4	BP2	Legacy Block Protection Volatile	Volatile		Protects the selected range of sectors (Blocks) from Program or Erase.
3	BP1				
2	BP0				
1	WEL	Write Enable Latch	Volatile Read Only		0 = Not write enabled, no embedded operation can start 1 = Write Enable, embedded operation can start This bit is not affected by WRR or WRAR, only WREN WRENV, WRDI and CLSR commands affect this bit.
0	WIP	Write in Progress	Volatile Read Only		1 = Device Busy, an embedded operation is in progress such as program or erase 0 = Ready Device is in standby mode and can accept commands This bit is not affected by WRR or WRAR, it only provides WIP status.

Status Register Protect 0 (SRP0) SR1V[7]: Places the device in the Hardware Protected mode when this bit is set to '1' and the WP# input is driven LOW. In this mode, any command that change status registers or configuration registers are ignored and not accepted for execution, effectively locking the state of the Status Registers and Configuration Registers SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV bits, by making the registers read-only. If WP# is HIGH, Status Registers and Configuration Registers SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV may be changed and Configuration Registers SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV may be changed. WP# has no effect on the writing of any other registers. SRP0 tracks any changes to the non-volatile version of this bit (SRP0_NV). When QPI or QIO mode is enabled (CR2V[3] or CR1V[1] = 1), the internal WP# signal level is '1' because the WP# external input is used as IO2 when either mode is active. This effectively turns off hardware protection. The Register SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV are unlocked and can be written (see **"Status Register Protect (SRP1, SRP0)"** on page 56).

Sector / Block Protect (SEC) SR1V[6]: This bit controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4 KB Sectors (SEC = 1) or 64 KB Blocks (SEC = 0). See **"Legacy block protection"** on page 59 for a description of how the SEC bit value select the memory array area protected.

TBPROT SR1V[5]: This bit defines the reference point of the Legacy Block Protection bits BP2, BP1, and BP0 in the Status Register. As described in the Status Register section, the BP2–0 bits allow the user to optionally protect a portion of the array, ranging from 1/64, ¼, ½, etc., up to the entire array. When TBPROT is set to '0', the Legacy Block Protection is defined to start from the top (maximum address) of the array. When TBPROT is set to '1', the Legacy Block Protection is defined to start from the bottom (zero address) of the array. TBPROT tracks any changes to the non-volatile version of this bit (TBPROT_NV).

Legacy Block Protection (BP2, BP1, BP0) SR1V[4:2]: These bits define the main Flash array area to be protected against program and erase commands. See **"Legacy block protection"** on page 59 for a description of how the BP bit values select the memory array area protected.

Write Enable Latch (WEL) SR1V[1]: The WEL bit must be set to '1' to enable program, write, or erase operations as a means to provide protection against inadvertent changes to memory or register values. The Write Enable (WREN) command execution sets the Write Enable Latch to '1' to allow any program, erase, or write commands to execute afterwards. The Write Disable (WRDI) command can be used to set the Write Enable Latch to '0' to prevent all program, erase, and write commands from execution. The WEL bit is cleared to '0' at the end of any successful program, write, or erase operation. Following a failed operation, the WEL bit may remain set and should be cleared with a CLSR command. After a power down / power up sequence, hardware reset, or software reset, the Write Enable Latch is set to a WEL_D. The WRR or WRAR command does not affect this bit.

Write In Progress (WIP) SR1V[0]: Indicates whether the device is performing a program, write, erase operation, or any other operation, during which a new operation command will be ignored. When the bit is set to '1', the device is busy performing an operation. While WIP is '1', only Read Status (RDSR1 or RDSR2), Read Any Register (RDAR), Erase / Program Suspend (EPS), Clear Status Register (CLSR), and Software Reset (RSTEN 66h followed by RST 99h) commands are accepted. EPS command will only be accepted if memory array erase or program operations are in progress. The Status Register E_ERR and P_ERR bits are updated while WIP = 1. When P_ERR or E_ERR bits are set to '1', the WIP bit will remain set to '1' indicating the device remains busy and unable to receive new operation commands. A Clear Status Register (CLSR) command must be received to return the device to standby mode. When the WIP bit is cleared to '0' no operation is in progress. This is a read-only bit.

6.6.2 Status Register 2 Volatile (SR2V)

Related Commands: Read Status Register 2 (RDSR2 07h), Read Any Register (RDAR 65h). Status Register 2 does not have user programmable non-volatile bits, all defined bits are volatile read only status. The default state of these bits are set by hardware.

Table 11 Status Register 2 Volatile (SR2V)

Bits	Field name	Function	Type	Default state	Description
7	RFU	Reserved		0	Reserved for Future Use
6	E_ERR	Erase Error Occurred	Volatile Read Only		1 = Error occurred 0 = No Error
5	P_ERR	Programming Error Occurred			
4	RFU	Reserved	Volatile Read Only		Reserved for Future Use
3					
2					
1	ES	Erase Suspend	Volatile Read Only		1 = In Erase Suspend mode. 0 = Not in Erase Suspend mode.
0	PS	Program Suspend			1 = In Program Suspend mode. 0 = Not in Program Suspend mode.

Erase Error (E_ERR) SR2V[6]: The Erase Error Bit is used as an Erase operation success or failure indication. When the Erase Error bit is set to '1', it indicates that there was an error in the last erase operation. This bit will also be set when the user attempts to erase an individual protected main memory sector or erase a locked Security Region. The Chip Erase command will set E_ERR if a protected sector is found during the command execution. When the Erase Error bit is set to '1', this bit can be cleared to zero with the Clear Status Register (CLSR) command. This is a read-only bit and is not affected by the WRR or WRAR commands.

Program Error (P_ERR) SR2V[5]: The Program Error Bit is used as a program operation success or failure indication. When the Program Error bit is set to '1', it indicates that there was an error in the last program operation. This bit will also be set when the user attempts to program within a protected main memory sector, or program within a locked Security Region. When the Program Error bit is set to '1', this bit can be cleared to zero with the Clear Status Register (CLSR) command. This is a read-only bit and is not affected by the WRR or WRAR commands.

Erase Suspend (ES) SR2V[1]: The Erase Suspend bit is used to determine when the device is in Erase Suspend mode. This is a status bit that cannot be written by the user. When Erase Suspend bit is set to '1', the device is in erase suspend mode. When Erase Suspend bit is cleared to '0', the device is not in erase suspend mode. Refer to **"Program or Erase Suspend (PES 75h)"** on page 112 for details about the Erase Suspend/Resume commands.

Program Suspend (PS) SR2V[0]: The Program Suspend bit is used to determine when the device is in Program Suspend mode. This is a status bit that cannot be written by the user. When Program Suspend bit is set to '1', the device is in program suspend mode. When the Program Suspend bit is cleared to '0', the device is not in program suspend mode. Refer to **"Program or Erase Suspend (PES 75h)"** on page 112 for details.

6.6.3 Configuration Register 1

Configuration Register 1 controls certain interface and data protection functions. The register bits can be changed using the WRR command with sixteen input cycles or with the WRAR command.

6.6.3.1 Configuration Register 1 Non-Volatile (CR1NV)

Related Commands: Non-volatile Write Enable (WREN 06h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 12 Configuration Register 1 Non-Volatile (CR1NV)

Bits	Field name	Function	Type	Default state	Description
7	SUS_D	Suspend Status Default	Non-volatile Read Only	0	Provides the default state for the Suspend Status. Not user programmable.
6	CMP_NV	Complement Protection Default	Non-volatile		Provides the default state for CMP.
5	LB3	Security Region Lock Bits	OTP		OTP lock Bits 3:0 for Security Regions 3:0 0 = Security Region not locked 1 = Security Region permanently locked
4	LB2				
3	LB1				
2	LB0				
1	QUAD_NV	Quad Default	Non-volatile		Provides the default state for QUAD.
0	SRP1_D	Status Register Protect 1 Default	OTP		When IRP[2:0] = 111 SRP1_D bit is programmable. Lock current state of SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV 1 = Registers permanently locked 0 = Registers not protected by SRP1 after POR

Suspend Erase/Program Status (SUS_D) CR1NV[7]: Provides the default state for the SUS bit in CR1V[7]. This bit is not user programmable.

Complement Protect (CMP_NV) CR1NV[6]: Provides the default state for the CMP bit in CR1V[6].

Security Region Lock Bits (LB3, LB2, LB1, LB0) CR1NV[5:2]: Provide the OTP write protection control of the Security Regions. When an LB bit is set to 1 the related Security Region can no longer be programmed or erased.

Quad Data Width Non-volatile (QUAD_NV) CR1NV[1]: Provides the default state for the QUAD bit in CR1V[1]. The WRR or WRAR command affects this bit. Programming CR1NV[1] = 1 will default operation to allow Quad-data-width commands at Power-on or Reset.

Status Register Protect 1 Default (SRP1_D) CR1NV[0]: Provides the default state for the SRP1 bit in CR1V[0]. When IRP[2:0] = 111, the SRP1_D OTP bit is user programmable. When SRP1_D = 1, Registers SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV are permanently locked. See **"Status Register Protect (SRP1, SRP0)"** on page 56.

6.6.3.2 Configuration Register 1 Volatile (CR1V)

Related Commands: Read Configuration Register 1 (RDCR1 35h), Write Enable for Volatile (WRENV 50h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h). This is the register displayed by the RDCR1 command.

Table 13 Configuration Register 1 Volatile (CR1V)

Bits	Field name	Function	Type	Default state	Description
7	SUS	Suspend Status	Volatile Read Only	CR1NV	1 = Erase / Program suspended 0 = Erase / Program not suspended
6	CMP	Complement Protection	Volatile		0 = Normal Protection Map 1 = Inverted Protection Map
5	LB3	Volatile copy of Security Region Lock Bits	Volatile Read Only		Not user writable See CR1NV[5:2] OTP lock Bits 3:0 for Security Regions 3:0 0 = Security Region not locked 1 = Security Region permanently locked
4	LB2				
3	LB1				
2	LB0				
1	QUAD	Quad I/O mode	Volatile		1 = Quad 0 = Dual or Serial
0	SRP1	Status register Protect 1			Lock current state of SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV 1 = Registers locked 0 = Registers un-locked

Suspend Status (SUS) CR1V[7]: The Suspend Status bit is used to determine when the device is in Erase or Program suspend mode. This is a status bit that cannot be written by the user. When Suspend Status bit is set to '1', the device is in erase or program suspend mode. When Suspend Status bit is cleared to '0', the device is not in erase or program suspend mode. Refer to **"Program or Erase Suspend (PES 75h)"** on page 112 for details about the Erase/Program Suspend/Resume commands.

Complement Protection (CMP) CR1V[6]: CMP is used in conjunction with TBPROT, BP3, BP2, BP1 and BP0 bits to provide more flexibility for the array protection map, to protect from 1/2 to all of the array.

LB[3:0] CR1V[5:2]: These bits are volatile copies of the related OTP bits of CR1NV. These bits track any changes to the related OTP version of these bits.

Quad Data Width (QUAD) CR1V[1]: When set to 1, this bit switches the data width of the device to 4-bit - Quad mode. That is, WP# becomes IO2 and IO3 / RESET# becomes an active I/O signal when CS# is low or the RESET# input when CS# is high. The WP# input is not monitored for its normal function and is internally set to high (inactive). The commands for Serial, and Dual I/O Read still function normally but, there is no need to drive the WP# input for those commands when switching between commands using different data path widths. Similarly, there is no requirement to drive the IO3 / RESET# during those commands (while CS# is low). The QUAD bit must be set to one when using the Quad Output Read, Quad I/O Read, DDR Quad I/O Read. The volatile register write for QIO mode has a short and well defined time (t_{QEN}) to switch the device interface into QIO mode and (t_{QEX}) to switch the device back to SPI mode. Following commands can then be immediately sent in QIO protocol. While QPI mode is entered or exited by the QPIEN and QPIEX commands, or by setting the CR2V[3] bit to 1, the Quad data width mode is in use whether the QUAD bit is set or not.

Status Register Protect 1(SRP1) CR1V[0]: The SRP1 Bit, when set to 1, protects the current state of the SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV registers by preventing any write of these registers.

See **"Status Register Protect (SRP1, SRP0)"** on page 56.

As long as the SRP1 bit remains cleared to logic 0 the SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV, and DLRV registers are not protected by SRP1. However, these registers may be protected by SRP0 (SR1V[7]) and the WP# input.

Once the SRP1 bit has been written to a logic 1 it can only be cleared to a logic 0 by a power-off to power-on cycle or a hardware reset. Software reset will not affect the state of the SRP1 bit.

The CR1V[0] SRP1 bit is volatile and the default state of SRP1 after power-on comes from SRP1_D in CR1NV[0]. The SRP1 bit can be set in parallel with updating other values in CR1V by a single WRR or WRAR command.

6.6.4 Configuration Register 2

Configuration Register 2 controls certain interface functions. The register bits can be read and changed using the Read Any Register and Write Any Register commands. The non-volatile version of the register provides the ability to set the POR, hardware reset, or software reset state of the controls. The volatile version of the register controls the feature behavior during normal operation.

6.6.4.1 Configuration Register 2 Non-Volatile (CR2NV)

Related Commands: Non-volatile Write Enable (WREN 06h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 14 Configuration Register 2 Non-Volatile (CR2NV)

Bits	Field name	Function	Type	Default state	Description
7	IO3R_NV	IO3_Reset	Non-volatile	0	1 = Enabled -- IO3_RESET is used as IO3 / RESET# input when CS# is high or Quad Mode is disabled CR1V[1] = 0 or QPI is disabled (CR3V[3] = 0). 0 = Disabled -- IO3 has no alternate function, hardware reset is disabled.Provides the default state for the IO3 / RESET# function enable.
6	OI_NV	Output Impedance		1	Provides the default output impedance state. See **Table 15**.
5					
4	RFU	Reserved		0	Reserved for Future Use
3	QPI_NV	QPI			1 = Enabled -- QPI (4-4-4) protocol in use 0 = Disabled -- Legacy SPI protocols in use, instruction is always serial on SI Provides the default state for QPI mode.
2	WPS_NV	Write Protect Selection			Provides the default state for WPS 0 = Legacy Protection 1 = Individual Block Lock
1	ADP_NV	Address Length at Power-up			Provides the default state for Address Length 1 = 4 byte address 0 = 3 byte address
0	RFU	Reserved			Reserved for Future Use

IO3 _Reset Non-volatile CR2NV[7]: This bit controls the POR, hardware reset, or software reset state of the IO3 signal behavior. Most legacy SPI devices do not have a hardware reset input signal due to the limited signal count and connections available in traditional SPI device packages. The FL-L family provides the option to use the IO3 signal as a hardware reset input when the IO3 signal is not in use for transferring information between the host system and the memory. This non-volatile IO3_Reset configuration bit enables the device to start immediately (boot) with IO3 enabled for use as a RESET# signal.

Output Impedance Non-volatile CR2NV[6:5]: These bits control the POR, hardware reset, or software reset state of the IO signal output impedance (drive strength). Multiple drive strength are available to help match the output impedance with the system printed circuit board environment to minimize overshoot and ringing. These non-volatile output impedance configuration bits enable the device to start immediately (boot) with the appropriate drive strength.

Table 15 Output impedance control

CR2NV[6:5] impedance selection	Typical impedance to V_{SS} (Ω)	Typical impedance to V_{CC} (Ω)	Notes
00	18	21	–
01	26	28	
10	47	45	
11	71	64	Factory default

QPI Non-volatile CR2NV[3]: This bit controls the POR, hardware reset, or software reset state of the expected instruction width for all commands. Legacy SPI commands always send the instruction one bit wide (serial I/O) on the SI (IO0) signal. The FL-L family also supports the QPI mode in which all transfers between the host system and memory are 4 bits wide on IO0 to IO3, including all instructions. This non-volatile QPI configuration bit enables the device to start immediately (boot) in QPI mode rather than the legacy serial instruction mode. The recommended procedure for moving to QPI mode is to first use the QPIEN (38h) command, the WRR or WRAR command can also set CR2V[3] = 1, QPI mode. The volatile register write for QPI mode has a short and well defined time (t_{QEN}) to switch the device interface into QPI mode and (t_{QEX}) to switch the device back to SPI mode Following commands can then be immediately sent in QPI protocol. The WRAR command can be used to program CR2NV[3] = 1, followed by polling of SR1V[0] to know when the programming operation is completed. Similarly, to exit QPI mode use the QPIEX (F5h) command. The WRR or WRAR command can also be used to clear CR2V[3] = 0.

Write Protect Selection Non-volatile CR2NV[2]: This bit controls the POR, hardware reset, or software reset state of the Write Protect Method. This non-volatile configuration bit enables the device to start immediately (boot) with Individual Block Lock protection rather than Legacy Block protection.

Address Length at Power-up Non-volatile CR2NV[1]: This bit controls the POR, hardware reset, or software reset state of the expected address length for all commands that require address and are not fixed 3 byte or 4 byte only address. Most commands that need an address are legacy SPI commands that traditionally used 3 byte (24 bit) address. For device densities greater than 128 Mb a 4 byte (32 bit) address is required to access the entire memory array. The address length configuration bit is used to change all 3 byte address commands to expect 4 byte address. See **Table 41** for command address length. This non-volatile Address Length configuration bit enables the device to start immediately (boot) in 4 byte address mode rather than the legacy 3 byte address mode.

6.6.4.2 Configuration Register 2 Volatile (CR2V)

Related Commands: Read Configuration Register 2 (RDCR2 15h), Read Any Register (RDAR 65h), Write Enable for Volatile (WRENV 50h), Write Register (WRR 01h), Write Any Register (WRAR 71h), Enter 4 byte address mode (4BEN B7h), Exit 4 byte address mode (4BEX E9h), Enter QPI (38h), Exit QPI (F5h). This is the register displayed by the RDCR2 command.

Table 16 Configuration Register 2 Volatile (CR2V)

Bits	Field name	Function	Type	Default state	Description
7	IO3R	IO3_Reset	Volatile	CR2NV	1 = Enabled -- IO3 is used as RESET# input when CS# is high or Quad Mode is disabled CR1V[1] = 0 or QPI is disabled (CR3V[3] = 0). 0 = Disabled -- IO3 has no alternate function, hardware reset through IO3 / RESET# input is disabled.
6	OI	Output Impedance			See **Table 15**.
5					
4	RFU	Reserved			Reserved for Future Use
3	QPI	QPI			1 = Enabled -- QPI (4-4-4) protocol in use 0 = Disabled -- Legacy SPI protocols in use, instruction is always serial on SI
2	WPS	Write Protect Selection			0 = Legacy Block Protection 1 = Individual Block Lock
1	ADP	Address Length at Power-up	Volatile Read Only		Read Status Only Bit 1 = 4 byte address 0 = 3 byte address
0	ADS	Address Length Status	Volatile	CR2NV[1]	Current Address Mode 1 = 4 byte address 0 = 3 byte address

IO3 Reset CR2V[7]: This bit controls the IO3 / RESET# signal behavior. This volatile IO3 Reset configuration bit enables the use of IO3 as a RESET# input during normal operation when CS# is high or Quad Mode is disabled (CR1V[1] = 0) or QPI is disabled (CR3V[3] = 0).

Output Impedance CR2V[6:5]: These bits control the IO signal output impedance (drive strength). This volatile output impedance configuration bit enables the user to adjust the drive strength during normal operation.

QPI CR2V[3]: This bit controls the expected instruction width for all commands. This volatile QPI configuration bit enables the device to enter and exit QPI mode during normal operation. When this bit is set to QPI mode, the QUAD mode is active, independent of the setting of QIO mode (CR1V[1]). When this bit is cleared to legacy SPI mode, the QUAD bit is not affected. The QPI CR2V[3] bit can also be set to '1' by the QPIEN (38h) command and set to '0' by the QPIEX (F5h) command.

Table 17 QPI and QIO mode control bits

QPI CR2V[3]	QUAD CR1V[1]	Description
0	0	SIO mode: Single and Dual Read, WP#/IO2 input is in use as WP# pin and IO3 / RESET# input is in use as RESET# pin
0	1	QIO mode: Single, Dual, and Quad Read, WP#/IO2 input is in use as IO2 and IO3 / RESET# input is in use as IO3 or RESET# pin
1	X	QPI mode: Quad Read, WP#/IO2 input is in use as IO2 and IO3 / RESET# input is in use as IO3 or RESET# pin

Write Protect Selection CR2V[2]: This bit selects which Array protection method is used; see **"Legacy block protection"** on page 59 or **"Individual block lock (IBL) protection"** on page 63. These volatile configuration bits enable the user to change Protection method during normal operation.

Address Length at Power-on (ADP) CR2V[1]: This bit is read only and shows what the address length will be after power-on reset, hardware reset, or software reset for all commands that require address and are not fixed 3 byte or 4 byte address.

Address Length Status (ADS) CR2V[0]: This bit controls the expected address length for all commands that require address and are not fixed 3 Byte or 4 Byte address. See **Table 41** for command address length. This volatile Address Length configuration bit enables the address length to be changed during normal operation. The four byte address mode (4BEN) command directly sets this bit into 4 byte address mode and the (4BEX) command exits sets this bit back into 3 byte address mode. This bit is also updated when the Address Length Non-volatile CR2NV[1] bit is updated.

6.6.5 Configuration Register 3

Configuration Register 3 controls the main Flash array read commands burst wrap behavior and read latency. The burst wrap configuration does not affect commands reading from areas other than the main Flash array e.g. read commands for registers or Security Regions. The non-volatile version of the register provides the ability to set the start up (boot) state of the controls as the contents are copied to the volatile version of the register during the POR, hardware reset, or software reset. The volatile version of the register controls the feature behavior during normal operation.

The register bits can be read and changed using the, Read Configuration 3 (RDCR3 33h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h). The volatile version of the register can also be written by the Set Burst Length (77h) command.

6.6.5.1 Configuration Register 3 Non-Volatile (CR3NV)

Related Commands: Non-volatile Write Enable (WREN 06h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 19 Configuration Register 3 Non-Volatile (CR3NV)

Bits	Field name	Function	Type	Default state	Description
7	RFU	Reserved	Non-volatile	0	Reserved for Future Use
6	WL_NV	Wrap Length Default		1	00 = 8-byte wrap 01 = 16-byte wrap 10 = 32-byte wrap 11 = 64-byte wrap
5				1	
4	WE_NV	Wrap Enable Default		1	0 = Wrap Enabled 1 = Wrap Disabled
3	RL_NV	Read Latency Default		1	0 to 15 latency (dummy) cycles following read address or continuous mode bits.
2				0	
1				0	
0				0	

Wrap Length Non-volatile CR3NV[6:5]: These bits controls the POR, hardware reset, or software reset state of the wrapped read length and alignment.

Wrap Enable Non-volatile CR3NV[4]: This bit controls the POR, hardware reset, or software reset state of the wrap enable. The commands affected by Wrap Enable are: Quad I/O Read, QPI Read, DDR Quad I/O Read and DDR QPI Read. This configuration bit enables the device to start immediately (boot) in wrapped burst read mode rather than the legacy sequential read mode.

Read Latency Non-volatile CR3NV[3:0]: These bits control the POR, hardware reset, or software reset state of the read latency (dummy cycle) delay in all variable latency read commands. The following read commands have a variable latency period between the end of address or mode and the beginning of read data returning to the host:

- The latency delay per clock frequency for the following commands are: One dummy cycle for all clock frequency's. The default latency code of '0' is one dummy cycle.
  - Data Learning pattern Read DLPRD (1-1-1) or (4-4-4)
  - IRP Read IRPRD (1-1-1) or (4-4-4))
  - Protect Register Read PRRD (1-1-1) or (4-4-4)
  - Password Read PASSRD (1-1-1) or (4-4-4)
- The latency delay per clock frequency for the following commands are shown in **Table 20** and **Table 21**. The default latency code of '0' is 8 dummy cycles.
  - Fast Read FAST_READ (1-1-1)
  - Quad-O Read QOR, 4QOR (1-1-4)
  - Dual-O Read DOR, 4DOR (1-1-2)
  - Dual I/O Read DIOR, 4DIOR (1-2-2)
  - Quad I/O Read QIOR, 4QIOR (1-4-4) or (4-4-4)
  - DDR Quad I/O Read DDRQIOR, 4DDRQIOR(1-4-4)
  - Security Regions Read SECRR (1-1-1) or (4-4-4)
  - Read Any Register RDAR (1-1-1) or (4-4-4)
  - Read Serial Flash Discoverable Parameters RSFDP (1-1-1) or (4-4-4)

The non-volatile read latency configuration bits set the number of read latency (dummy cycles) in use so the device can start immediately (boot) with an appropriate read latency for the host system.

Table 20 Latency code (Cycles) versus frequency

Latency code	Read command maximum frequency (MHz)						
	Fast read (1-1-1)	Dual-O read (1-1-2)	Dual I/O read (1-2-2)	Quad-O read (1-1-4)	Quad I/O read (1-4-4)	Quad I/O read QPI (4-4-4)	DDR quad I/O (1-4-4) QPI (4-4-4)
0	Mode cycles = 0	Mode cycles = 0	Mode cycles = 4	Mode cycles = 0	Mode cycles = 2	Mode cycles = 2	Mode cycles = 1
	Dummy cycles = 8	Dummy cycles = 8	Dummy cycles = 8	Dummy cycles = 8	Dummy cycles = 8	Dummy cycles = 8	Dummy cycles = 8
1	50	50	75	35	35	35	20
2	65	65	85	45	45	45	25
3	75	75	95	55	55	55	35
4	85	85	108	65	65	65	45
5	95	95	108	75	75	75	55
6	108	105	108	85	85	85	60
7	108	108	133	95	95	95	66
8	108	108	133	108	108	108	66
9	133	133	133	115	115	115	66
10	133	133	133	115	115	115	66
11	133	133	133	120	120	120	66
12	133	133	133	120	120	120	66
13	133	133	133	133	133	133	66
14	133	133	133	133	133	133	66
15	133	133	133	133	133	133	66

Table 21 Latency code (Cycles) versus frequency

Latency code 0	Read command maximum frequency (MHz)					
	Read Any Register (1-1-1)	Read Any Register QPI (4-4-4)	Security Region Read (1-1-1)	Security Region Read QPI (4-4-4)	Read SFDP RSFDP (1-1-1)	Read SFDP RSFDP QPI (4-4-4)
	Mode cycles = 0	Mode cycles = 0	Mode cycles = 0	Mode cycles = 0	Mode cycles = 0	Mode cycles = 0
	Dummy cycles = 8	Dummy cycles = 8	Dummy cycles = 8	Dummy cycles = 8	Dummy cycles = 8	Dummy cycles = 8
1	50	15	50	15	50	15
2	65	25	65	25	65	25
3	75	35	75	35	75	35
4	85	45	85	45	85	45
5	95	55	95	55	95	55
6	108	65	108	65	108	65
7	108	75	108	75	108	75
8	108	85	108	85	108	85
9	133	95	133	95	133	95
10	133	108	133	108	133	108
11	133	115	133	115	133	115
12	133	115	133	115	133	115
13	133	120	133	120	133	120
14	133	120	133	120	133	120
15	133	133	133	133	133	133

Notes

9. SCK frequency > 133 MHz SDR, or 66 MHz DDR is not supported by this family of devices.
10. The Dual I/O, Quad I/O, QPI, DDR Quad I/O, and DDR QPI command protocols include Continuous Read Mode bits following the address. The clock cycles for these bits are not counted as part of the latency cycles shown in the table. Example: the legacy Quad I/O command has 2 Continuous Read Mode cycles following the address. Therefore, the legacy Quad I/O command without additional read latency is supported only up to the frequency shown in the table for a read latency of 0 cycles. By increasing the variable read latency the frequency of the Quad I/O command can be increased to allow operation up to the maximum supported 133 MHz frequency and QPI maximum supported 133 MHz.
11. Other commands have fixed latency, e.g. Read always has zero read latency, Read Unique ID has 32 dummy cycles and release from Deep Power-Down has 24 dummy cycles.

6.6.5.2 Configuration Register 3 Volatile (CR3V)

Related Commands: Read Configuration 3 (RDCR3 33h), Write Enable for Volatile (WRENV 50h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h), Set Burst Length (SBL 77h). This is the register displayed by the RDCR3 command.

Table 22 Configuration Register 3 Volatile (CR3V)

Bits	Field name	Function	Type	Default state	Description
7	RFU	Reserved	Volatile	CR3NV	Reserved for Future Use
6	WL	Wrap Length			00 = 8-byte wrap 01 = 16 byte wrap 10 = 32 byte wrap 11 = 64 byte wrap
5					
4	WE	Wrap Enable			0 = Wrap Enabled 1 = Wrap Disabled
3	RL	Read Latency			0 to 15 latency (dummy) cycles following read address or continuous mode bits.
2					
1					
0					

Wrap Length CR3V[6:5]: These bits controls the wrapped read length and alignment during normal operation. These volatile configuration bits enable the user to adjust the burst wrapped read length during normal operation.

Wrap Enable CR3V[4]: This bit controls the burst wrap feature. This volatile configuration bit enables the device to enter and exit burst wrapped read mode during normal operation.

When CR3V[4] = 1, the wrap mode is not enabled and unlimited length sequential read is performed.

When CR3V[4] = 0, the wrap mode is enabled and a fixed length and aligned group of 8, 16, 32, or 64 bytes is read starting at the byte address provided by the read command and wrapping around at the group alignment boundary.

Read Latency CR3V[3:0]: These bits set the read latency (dummy cycle) delay in variable latency read commands. These volatile configuration bits enable the user to adjust the read latency during normal operation to optimize the latency for different commands or, at different operating frequencies, as needed.

6.6.6 Individual and Region Protection Register (IRP)

Related Commands: IRP Read (IRPRD 2Bh) and IRP Program (IRPP 2Fh), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

The IRP register is a 16 bit OTP memory location used to permanently configure the behavior of Individual and Region Protection (IRP) features. IRP does not have user programmable volatile bits, all defined bits are OTP.

The default state of the IRP bits are programmed by Infineon.

Table 23 IRP Register (IRP)

Bits	Field name	Function	Type	Default state	Description
15 to 7	RFU	Reserved	OTP	All bits are 1	Reserved for Future Use
6	SECRRP	Security Region 3 Read Password Mode Enable Bit		1	0 = Security Region 3 Read password mode selected 1 = Security Region 3 Read Password not selected IRP[6] is programmable if IRP[2:0] = 111
5	RFU	Reserved			Reserved for Future Use
4	IBLLBB	IBL Lock Boot Bit			0 = All individual IBL bits are set to '1' at power-up in the unprotected state 1 = All individual IBL bits are set to '0' at power-up in the protected state IRP[4] is programmable if IRP[2:0] = 111
3	RFU	Reserved			Reserved for Future Use
2	PWDMLB	Password Protection Mode Lock Bit			0 = Password Protection Mode permanently enabled. 1 = Password Protection Mode not permanently enabled. IRP[2] is programmable if IRP[2:0] = 111
1	PSLMLB	Power Supply Lock-down protection Mode Lock Bit			0 = Power Supply Lock-down protection Mode permanently enabled. 1 = Power Supply Lock-down protection Mode not permanently enabled. IRP[1] is programmable if this is enabled by IRP[2:0] = 111
0	PERMLB	Permanent Protection Lock			0 = Permanent Protection Mode permanently enabled. 1 = Permanent Protection Mode not permanently enabled. IRP[0] is programmable if IRP[2:0] = 111

Security Regions Read Password Mode Enable (SECRRP) IRP[6]: When programmed to '0', SECRRP enables the Security Region 3 read password mode when PWDMLB bit IRP[2] is program at same time or later. The SECRRP bit can only be programmed when IRP[2:0] = 111, if not programming will fail with P_ERR set to '1'. See **"Security Region read password protection"** on page 69.

IBL Lock Boot Bit (IBLLBB) IRP[4]: The default state is '1', all individual IBL bits are set to '0' in the protected state, following power-up, hardware reset, or software reset. In order to Program or Erase the Array the Global IBL Unlock or the Sector / Block IBL Unlock command must be given before the Program or Erase commands. When programmed to '0', all the individual IBL bits are in the un-protected state following power-up, hardware reset, or software reset. The IBLLBB bit can only be programmed when IRP[2:0] = 111, if not programming will fail with P_ERR set to '1'. See **"Individual block lock (IBL) protection"** on page 63.

Password Protection Mode Lock Bit (PWDMLB) IRP[2]: When programmed to '0', the Password Protection Mode is permanently selected to protect the Security Regions 2 and 3 and Pointer Region. The PWDMLB bit can only be programmed when IRP[2:0] = 111, if not programming will fail with P_ERR set to '1'. See **"Password protection mode"** on page 68.

After the Password protection mode is selected by programming IRP[2] = 0, the state of all IRP bits are locked and permanently protected from further programming. Attempting to program any IRP bits will result in a programming error with P_ERR set to '1'.

The Password must be programmed and verified, before the Password Mode (IRP[2] = 0) is set.

Power Supply Lock-down protection Mode Lock Bit (PSLMLB) IRP[1]: When programmed to '0', the Power Supply Lock-down protection Mode is permanently selected. The PSLMLB bit can only be programmed when IRP[2:0] = 111, if not programming will fail with P_ERR set to '1'.

After the Power Supply Lock-down protection mode is selected by programming IRP[1] = 0, the state of all IRP bits are locked and permanently protected from further programming. Attempting to program any IRP bits will result in a programming error with P_ERR set to '1'. See **"IRP register"** on page 67.

Permanent Protection Lock Bit (PERMLB) IRP[0]: When programmed to 0, the Permanent Protection Lock Bit permanently protects the Pointer Region and Security Regions 2 and 3, This bit provides a simple way to permanently protect the Pointer Region and Security Regions 2 and 3 without the use of a password or the PRL command. See **"IRP register"** on page 67.

PWDMLB (IRP[2]), PSLMLB (IRP[1]) and PERMLB(IRP[0]) are mutually exclusive, only one may be programmed to zero. IRP bits may only be programmed while IRP[2:0] = 111. Attempting to program IRP bits when IRP[2:0] is not equal to '111' will result in a programming error with P_ERR set to '1'. The IRP protection mode should be selected during system configuration to ensure that a malicious program does not select an undesired protection mode at a later time. By locking all the protection configuration via the IRP mode selection, later alteration of the protection methods by malicious programs is prevented.

6.6.7 Password Register (PASS)

Related Commands: Password Read (PASSRD E7h) and Password Program (PASSP E8h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h). The PASS register is a 64-bit OTP memory location used to permanently define a password for the Individual and Region Protection (IRP) feature. PASS does not have user programmable volatile bits, all defined bits are OTP. A volatile copy of PASS is used to satisfy read latency requirements but the volatile register is not user writable or further described. The Password can not be read or programmed after IRP[2] is programmed to '0' (see **Table 23**.)

Table 24 Password Register (PASS)

Bits	Field name	Function	Type	Default state	Description
63 to 0	PWD	Hidden Password	OTP	FFFFFFFF–FFFFFFFFh	Non-volatile OTP storage of 64-bit password. The password is no longer readable after the password protection mode is selected by programming IRP register bit 2 to zero.

6.6.8 Protection Register (PR)

Related Commands: Protection Register Read (PRRD A7h) Protection Register Lock (PRL A6h), Read Any Register (RDAR 65h).

PR does not have separate user programmable non-volatile bits, all defined bits are volatile read only status. The default state of the RFU bits is set by hardware. There is no non-volatile version of the PR register.

The NVLOCK bit is used to protect the Security Regions 2 and 3 and Pointer Region Protection. When NVLOCK[0] = 0, the Security Regions 2 and 3 and Pointer Region Protection can not be changed.

Table 25 Protection Status Register (PR)

Bits	Field name	Function	Type	Default state	Description
7	RFU	Reserved	Volatile Read Only	00h	Reserved for Future Use
6	SECRRP	Security Regions Read Password		IRP[6]	0 = Security Region 3 password protected from read when NVLOCK = 0 1 = Security Region 3 not password protected from read
5	RFU	Reserved		0	Reserved for Future Use
4					
3					
2					
1					
0	NVLOCK	Protect Non-volatile configuration		IRP[2] and IRP[0]	0 = Security Regions 2 and 3 and Pointer Region write protected 1 = Security Regions 2 and 3 and Pointer Region may be written[12].

6.6.9 Individual Block Lock Access Register (IBLAR)

Related Commands: IBL Read (IBLRD 3Dh or 4IBLRD E0h), IBL Lock (IBL 36h or 4IBL E1h), IBL Unlock (IBLUL 39h or 4IBUL E2h), Global IBL lock (GBL 7Eh), Global IBL unlock (GBUL 98h).

IBLAR does not have user programmable non-volatile bits, all bits are a representation of the volatile bits in the IBL array. The default state of the IBL array bits is set by hardware. There is no non-volatile version of the IBLAR register.

Table 26 IBL Access Register (IBLAR)

Bits	Field name	Function	Type	Default state	Description
7 to 0	IBL	Read or write IBL for individual sectors / blocks	Volatile	IRP[4] = 1 then 00h else FFh	00h = IBL for the sector / block addressed is set to ‘0’ by the IBL, 4IBL and GBL commands protecting that sector from program or erase operations. FFh = IBL for the sector / block addressed is cleared to ‘1’ by the IBUL, 4IBUL and GBUL commands not protecting that sector from program or erase operations.

Notes
12. The Command Protection Register Lock (PRL), sets the NVLOCK = 1.
13. See **Figure 25**.
14. The IBL bits maybe read by the IBLRD and 4IBLRD commands.

6.6.10 Pointer Region Protection Register (PRPR)

Related Commands: Set Pointer Region (SPRP FBh or 4SPRP E3h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

PRPR contains user programmable non-volatile bits. The default state of the PRPR bits is set by hardware. There is no volatile version of the PRPR register. See **"Pointer Region Protection (PRP)"** on page 64 for additional details.

Table 27 PRP Register (PRPR)

Bits	Field name	Function	Type	Default state	Description
A31 to A25	RFU	Reserved	Non-volatile	11111111b	Reserved for Future Use
A24	PRPAD	PRP Address		1	Pointer Address A24 in S25FL256L RFU in S25FL128L
A23 to A16				FFh	Pointer Address A23 to A16
A15 to A12				Fh	Pointer Address A15 to A12
A11	PRPALL	PRP Protect All		1	0 = Protect Pointer Region selected sectors 1 = Protect All sectors
A10	PRPEN	PRP Enable		1	0 = Enable Pointer Region Protection 1 = Disable Pointer Region Protection
A9	PRPTB	PRP Top/Bottom		1	0 = Pointer Region Protection starts from the top (high address) 1 = Pointer Region Protection starts from the bottom (low address)
A8	RFU	Reserved		1	Reserved for Future Use
A7 to A0				FFh	

6.6.11 DDR Data Learning Registers

Related Commands: Program DLRNV (PDLRNV 43h), Write DLRV (WDLRV 4Ah), Data Learning Pattern Read (DLPRD 41h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

The Data Learning Pattern (DLP) resides in an 8-bit Non-Volatile Data Learning Register (DLRNV) as well as an 8-bit Volatile Data Learning Register (DLRV). When shipped from Infineon, the DLRNV value is 00h. Once programmed, the DLRNV cannot be reprogrammed or erased; a copy of the data pattern in the DLRNV will also be written to the DLRV. The DLRV can be written to at any time, but on hardware and software reset or power cycles the data pattern will revert back to what is in the DLRNV. During the learning phase described in the SPI DDR modes, the DLP will come from the DLRV. Each IO will output the same DLP value for every clock edge. For example, if the DLP is 34h (or binary 00110100) then during the first clock edge all IO's will output 0; subsequently, the 2nd clock edge all I/O's will output 0, the 3rd will output 1, and so on.

When the DLRV value is 00h, no preamble data pattern is presented during the dummy phase in the DDR commands.

Table 28 Non-volatile Data Learning Register (DLRNV)

Bits	Field name	Function	Type	Default state	Description
7 to 0	NVDLP	Non-Volatile Data Learning Pattern	OTP	00h	OTP value that may be transferred to the host during DDR read command latency (dummy) cycles to provide a training pattern to help the host more accurately center the data capture point in the received data bits.

Table 29 Volatile Data Learning Register (DLRV)

Bits	Field name	Function	Type	Default state	Description
7 to 0	VDLP	Volatile Data Learning Pattern	Volatile	Takes the value of DLRNV during POR or Reset	Volatile copy of the NVDLP used to enable and deliver the Data Learning Pattern (DLP) to the outputs. The VDLP may be changed by the host during system operation.

7 Data protection

7.1 Security Regions

The device has a 1024 byte address space that is separate from the main flash array. This area is divided into 4, individually lockable, 256 byte length regions (see **"Security Regions address space"** on page 31).

The Security Region memory space is intended for increased system security. The data values can "mate" a flash component with the system CPU/ASIC to prevent device substitution. The Security Region address space is protected by the Security Region Lock bits or the Protection Register NVLOCK bit (PR[0]) (see **"Security Region Lock Bits (LB3, LB2, LB1, LB0)"** on page 54).

7.1.1 Reading Security Region Memory Regions

The Security Region Read command (SECRR) uses the same protocol as Fast Read. Read operations outside the valid 1024 byte Security Region address range will yield indeterminate data (see **"Security Regions Read (SECRR 48h)"** on page 118).

Security Region 3 may be password protected from read by setting the PWDMLB bit IRP[2] = 0 and SECRRP bit IRP[6] = 0 when NVLOCK = 0.

7.1.2 Programming the Security Regions

The protocol of the Security Region programming command (SECRP) is the same as page program (see **"Security Region Program (SECRP 42h)"** on page 117).

The valid address range for Security Region Program is depicted in **Table 6**. Security Region Program operations outside the valid Security Region address range will be ignored, without P_ERR in SR2V[5] set to '1'.

Security Regions 2 and 3 may be password protected from programming by setting the PWDMLB bit IRP[2] = 0.

7.1.3 Erasing the Security Regions

The protocol of the Security Region erasing command (SECRE) is the same as Sector erase (see **"Security Region Erase (SECRE 44h)"** on page 117).

The valid address range for Security Region Erase is depicted in **Table 6**. Security Region Erase operations outside the valid Security Region address range will be ignored, without E_ERR in SR2V set to '1'.

Security Regions 2 and 3 may be password protected from erasing by setting the PWDMLB bit IRP[2] = 0.

7.1.4 Security Region Lock Bits (LB3, LB2, LB1, LB0)

The Security Region Lock Bits (LB3, LB2, LB1, LB0) are non-volatile one time program (OTP) bits in Configuration Register 1(CR1NV[5:2]) that provide the write protect control and status to the Security Regions. The default state of Security Regions 0 to 3 are unlocked. LB[3:0] can be set to 1 individually using the Write Status Registers or Write Any Register command. LB[3:0] are One Time Programmable (OTP), once it's set to 1, the corresponding 256 Byte Security Region will become read-only permanently.

7.2 Deep Power Down

The Deep Power Down (DPD) command offers an alternative means of data protection as all commands are ignored during the DPD state, except for the Release from Deep Power Down (RES ABh) command and hardware reset. Thus, preventing any program or erase during the DPD state.

7.3 Write Enable commands

7.3.1 Write Enable (WREN)

The Write Enable (WREN) command must be written prior to any command that modifies non-volatile data. The WREN command sets the Write Enable Latch (WEL) bit. The WEL bit is cleared to '0' (disables writes) during power-up, hardware and software reset, or after the device completes the following commands:

- Reset
- Page Program (PP or 4PP)
- Quad Page Program (QPP or 4QPP)
- Sector Erase (SE or 4SE)
- Half Block Erase (HBE or 4HBE)
- Block Erase (BE or 4BE)
- Chip Erase (CE)
- Write Disable (WRDI)
- Write Registers (WRR)
- Write Any Register (WRAR)
- Security Region Erase (SECRE)
- Security Region Byte Programming (SECRP)
- Individual and Region Protection Register Program (IRPP)
- Password Program (PASSP)
- Clear Status Register (CLSR)
- Set Pointer Region Protection (SPRP or 4SPRP)
- Program Non-Volatile Data Learning Register (PDLRNV)
- Write Volatile Data Learning Register (WDLRV)
- Write Enable for Volatile Registers (WRENV)

The Write Enable Volatile (WRENV) command must be written prior to Write Register (WRR) command that modifies volatile registers data.

7.4 Write protect signal

When not in Quad mode (CR1V[1] = 0) or QPI mode (CR2V[3] = 0), the Write Protect (WP#) input in combination with the Status Register Protect 0 (SRP0) bit (SR1NV[7]) provide hardware input signal controlled protection. When WP# is Low and SRP0 is set to '1'; Status Register 1 (SR1NV and SR1V), Configuration register (CR1NV, CR1V, CR2NV, CR2V, CR2NV and CR3NV) and DDR Data Learning Registers (DLRNV and DLRV) are protected from alteration. This prevents disabling or changing the protection defined by the Legacy Block Protect bits or Security Region Lock Bits. See **"Status Register 1"** on page 32.

7.5 Status Register Protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are volatile bits in the configuration and status registers (CR1V[0] and SR1V[7]). The SRP bits control the method of write protection for SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV: software protection, hardware protection, or power supply lock-down.

Table 31 Status Register Protection Bits (High Security)

SRP1_D CR1NV[0]	SRP1 CR1V[0]	SRP0 SR1V[7]	WP#	Status Register	Description
0	0	0	X	Software Protection	WP# pin has no control. SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV can be written. [Factory Default]
0	0	1	0	Hardware Protected	When WP# pin is low SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV are locked and can not be written[15, 18].
0	0	1	1	Hardware Unprotected	When WP# pin is high SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV are unlocked and can be written[15].
0	1	X	X	Power Supply Lock-Down	SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV are protected and can not be written to again until the next power-down, power-up cycle[16].
1	1	X	X	One Time Program	SRP1_D CR1NV[0]= 1 SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV are permanently protected and can not be written[17].

Notes

15. SRP0 is reloaded from SRP0_NV (SR1NV[7]) default state after a power-down, power-up cycle, software or hardware reset. To enable hardware protection mode by the WP# pin at power-up set the SRP0_NV bit to '1'.
16. When SRP1 = 1, a power-down, power-up cycle, or hardware reset, will change SRP1 to 0 as SRP1 is reloaded from SRP1_D.
17. SRP1_D can be written only when IRP[2:0] = 111. When SRP1_D CR1NV[0] = 1; a power-down, power-up cycle, or hardware reset, will reload SRP1 from SRP1_D = 1 the volatile bit SRP1 is not writable, thus providing OTP protection. When SRP1_D is programmed to 1, Recommended that SRP0_NV should also be programmed to 1 as an indication that OTP protection is in use.
18. When QPI or QIO mode is enabled (CR2V[3] or CR1V[1] = 1) the internal WP# signal level is equal to '1' because the WP# external input is used as IO2 when either mode is active. This effectively turns off hardware protection when SRP1-SRP0 = 01b. The Register SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV are unlocked and can be written.
19. WIP, WEL, and SUS (SR1[1:0] and CR1[7]) are volatile read only status bits that are never affected by the Write Status Registers command.
20. The non-volatile version of SR1NV, CR1NV, CR2NV and CR3NV are not writable when protected by the SRP bits and WP# as shown in the table. The non-volatile version of these status register bits are selected for writing when the Write Enable (06h) command precedes the Write Status Registers (01h) command or the Write Any Register (71h) command.
21. The volatile version of registers SR1V, CR1V and CR2V are not writable when protected by the SRP bits and WP# as shown in the table. The volatile version of these status register bits are selected for writing when the Write Enable for volatile Status Register (50h) command precedes the Write Status Registers (01h) command or the Write Enable (06h) command precedes the Write Any Register (71h) command.
22. The volatile CR3V bits are not protected by the SRP bits and may be written at any time by volatile (50h) Write Enable command preceding the Write Status Registers (01h) command. The WRAR (71h) and SBL (77h) commands are alternative ways to write bits in the CR3V register.
23. During system power up and boot code execution: Trusted boot code can determine whether there is any need to change SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV values. If no changes are needed the SRP1 bit (CR1V[0]) can be set to 1 to protect the SR1NV, SR1V, CR1NV, CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV registers from changes during the remainder of normal system operation while power remains on.

7.6 Array protection

There are three types of memory array protection: Legacy Block (LBP), Individual Block Lock (IBL) and Pointer Region (PRP). The Write Protect Selection (WPS) bit is used by the user to enable one of two protection mechanisms: Legacy Block (LBP) protection (WPS CR2V[2] = 0)or Individual Block Lock (IBL) protection (WPS CR2V[2] = 1) (see **"Configuration Register 2 Volatile (CR2V)"** on page 43). Only one protection mechanism can be enabled at one time. The Legacy Block Protection is the default protection and is mutually exclusive with the IBL protection scheme. The Pointer Region Protection is enabled by the Set Pointer Region Protection command or the WRAR command by the value of A10 = 0 (see **"Pointer Region command"** on page 124). When the Pointer Region Protection is enabled it is logically ORed with the Legacy Block Protection or Individual Block Lock protection.

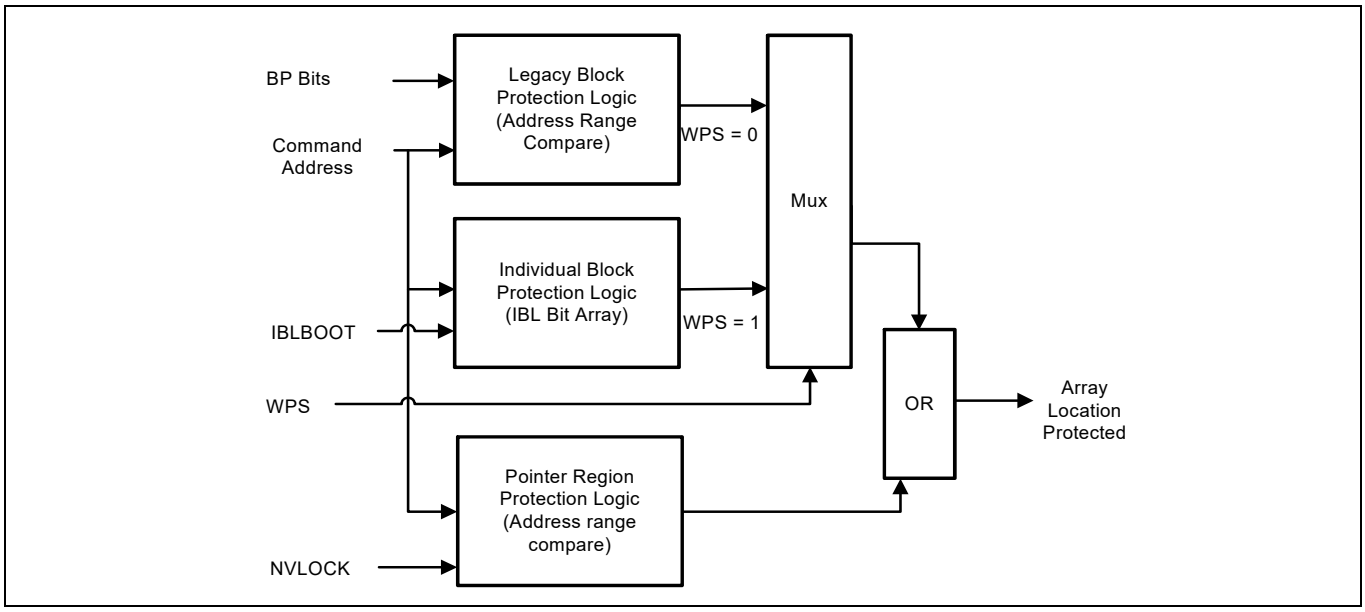


Figure 24 WPS selection of LBP or IBL and PRP array protection

7.6.1 Legacy block protection

The Legacy Block Protect bits (S25FL256L)Status Register bits BP3, BP2, BP1, BP0 -- SR1V[5:2]) (S25FL128L,) Status Register bits BP2, BP1, BP0 -- SR1V[4:2]) in combination with the Configuration Register TBPROT (SR1V[6] S25FL256L) (SR1V[5] S25FL128L)bit, CMP (CR1V[6] bit and SEC (SR1V[5] S25FL128L) can be used to protect an address range of the main Flash array from program and erase operations. The size of the range is determined by the value of the BP bits and the upper or lower starting point of the range is selected by the TBPROT bit of the configuration register (SR1V[6] S25FL256L) (SR1V[5] S25FL128L,). The protection is complemented when the CMP bit (CR1V[6]) is set to '1'.

If the Pointer Region Protection is enabled this region protection is logically ORed with the Legacy Block protection region.

Table 32 S25FL128L block protection (CMP = 0)

Status Register					128L (128 Mb) block protection (CMP = 0)			
SEC	**TBPROT**	**BP2**	**BP1**	**BP0**	**Protected block(s)**	**Protected addresses**	**Protected density**	**Protected portion**
X	X	0	0	0	None	None	None	None
0	0	0	0	1	252 thru 255	FC0000h–FFFFFFh	256 kB	Upper 1/64
0	0	0	1	0	248 thru 255	F80000h–FFFFFFh	512 kB	Upper 1/32
0	0	0	1	1	240 thru 255	F00000h–FFFFFFh	1 MB	Upper 1/16
0	0	1	0	0	224 thru 255	E00000h–FFFFFFh	2 MB	Upper 1/8
0	0	1	0	1	192 thru 255	C00000h–FFFFFFh	4 MB	Upper 1/4
0	0	1	1	0	128 thru 255	800000h–FFFFFFh	8 MB	Upper 1/2
0	1	0	0	1	0 thru 3	000000h–03FFFFh	256 kB	Lower 1/64
0	1	0	1	0	0 thru 7	000000h–07FFFFh	512 kB	Lower 1/32
0	1	0	1	1	0 thru 15	000000h–0FFFFFh	1 MB	Lower 1/16
0	1	1	0	0	0 thru 31	000000h–1FFFFFh	2 MB	Lower 1/8
0	1	1	0	1	0 thru 63	000000h–3FFFFFh	4 MB	Lower 1/4
0	1	1	1	0	0 thru 127	000000h–7FFFFFh	8 MB	Lower 1/2
X	X	1	1	1	0 thru 255	000000h–FFFFFFh	16 MB	ALL
1	0	0	0	1	255	FFF000h–FFFFFFh	4 kB	Upper 1/4096
1	0	0	1	0	255	FFE000h–FFFFFFh	8 kB	Upper 1/2048
1	0	0	1	1	255	FFC000h–FFFFFFh	16 kB	Upper 1/1024
1	0	1	0	X	255	FF8000h–FFFFFFh	32 kB	Upper 1/512
1	0	1	1	0				
1	1	0	0	1	0	000000h–000FFFh	4 kB	Lower 1/4096
1	1	0	1	0	0	000000h–001FFFh	8 kB	Lower 1/2048
1	1	0	1	1	0	000000h–003FFFh	16 kB	Lower 1/1024
1	1	1	0	X	0	000000h–007FFFh	32 kB	Lower 1/512
1	1	1	1	0				

Note
24.X = don't care.

Table 33 S25FL128L (128 Mb) block protection (CMP = 1)

Status Register					128L legacy block protection (CMP = 1)			
SEC	**TBPORT**	**BP2**	**BP1**	**BP0**	**Protected block(s)**	**Protected addresses**	**Protected density**	**Protected portion**
X	X	0	0	0	0 thru 255	000000h–FFFFFFh	16 MB	ALL
0	0	0	0	1	0 thru 251	000000h–FBFFFFh	16,128 kB	Lower 63/64
0	0	0	1	0	0 thru 247	000000h–F7FFFFh	15,872 kB	Lower 31/32
0	0	0	1	1	0 thru 239	000000h–EFFFFFh	15 MB	Lower 15/16
0	0	1	0	0	0 thru 223	000000h–DFFFFFh	14 MB	Lower 7/8
0	0	1	0	1	0 thru 191	000000h–BFFFFFh	12 MB	Lower 3/4
0	0	1	1	0	0 thru 127	000000h–7FFFFFh	8 MB	Lower 1/2
0	1	0	0	1	4 thru 255	040000h–FFFFFFh	16,128 kB	Upper 63/64
0	1	0	1	0	8 thru 255	080000h–FFFFFFh	15,872 kB	Upper 31/32
0	1	0	1	1	16 thru 255	100000h–FFFFFFh	15 MB	Upper 15/16
0	1	1	0	0	32 thru 255	200000h–FFFFFFh	14 MB	Upper 7/8
0	1	1	0	1	64 thru 255	400000h–FFFFFFh	12 MB	Upper 3/4
0	1	1	1	0	128 thru 255	800000h–FFFFFFh	8 MB	Upper 1/2
X	X	1	1	1	None	None	None	None
1	0	0	0	1	0 thru 255	000000h–FFEFFFh	16,380 kB	Lower 4095/4096
1	0	0	1	0	0 thru 255	000000h–FFDFFFh	16,376 kB	Lower 2047/2048
1	0	0	1	1	0 thru 255	000000h–FFBFFFh	16,368 kB	Lower 1023/1024
1	0	1	0	X	0 thru 255	000000h–FF7FFFh	16,352	Lower 511/512
1	0	1	1	0				
1	1	0	0	1	0 thru 255	001000h–FFFFFFh	16,380 kB	Upper 4095/4096
1	1	0	1	0	0 thru 255	002000h–FFFFFFh	16,376 kB	Upper 2047/2048
1	1	0	1	1	0 thru 255	004000h–FFFFFFh	16,368 kB	Upper 1023/1024
1	1	1	0	X	0 thru 255	008000h–FFFFFFh	16,352 kB	Upper 511/512
1	1	1	1	0				

Note
25.X = don’t care.

Table 34 S25FL256L (256Mb) upper array complement legacy block protection (TBPROT = 0, CMP = 1)

Status Register content				S25FL256L legacy block protection (TBPROT = 0, CMP = 1)			
BP3	BP2	BP1	BP0	Number protected blocks	Protected blocks	Protected density (KB)	Protected portion
0	0	0	0	512	0–511	32768	All
0	0	0	1	511	0–510	32704	Lower 511/512
0	0	1	0	510	0–509	32640	Lower 255/256
0	0	1	1	508	0–507	32512	Lower 127/128
0	1	0	0	504	0–503	32256	Lower 63/64
0	1	0	1	496	0–495	31744	Lower 31/32
0	1	1	0	480	0–479	30720	Lower 15/16
0	1	1	1	448	0–447	28672	Lower 7/8
1	0	0	0	384	0–383	24576	Lower 3/4
1	0	0	1	256	0–255	16384	Lower 1/2
1	0	1	0	0	None	0	None
1	0	1	1	0	None	0	None
1	1	0	0	0	None	0	None
1	1	0	1	0	None	0	None
1	1	1	0	0	None	0	None
1	1	1	1	0	None	0	None

Table 35 S25FL256L (256Mb) lower array complement legacy block protection (TBPROT = 1, CMP = 1)

Status Register content				S25FL256L legacy block protection (TBPROT = 1, CMP = 1)			
BP3	BP2	BP1	BP0	Number protected blocks	Protected blocks	Protected density (KB)	Protected portion
0	0	0	0	512	0–511	32768	All
0	0	0	1	511	1–511	32704	Upper 511/512
0	0	1	0	510	2–511	32640	Upper 255/256
0	0	1	1	508	4–511	32512	Upper 127/128
0	1	0	0	504	8–511	32256	Upper 63/64
0	1	0	1	496	16–511	31744	Upper 31/32
0	1	1	0	480	32–511	30720	Upper 15/16
0	1	1	1	448	64–511	28672	Upper 7/8
1	0	0	0	384	128–511	24576	Upper 3/4
1	0	0	1	256	256–511	16384	Upper 1/2
1	0	1	0	0	None	0	None
1	0	1	1	0	None	0	None
1	1	0	0	0	None	0	None
1	1	0	1	0	None	0	None
1	1	1	0	0	None	0	None
1	1	1	1	0	None	0	None

Table 36 S25FL256L (256Mb) upper array legacy block protection (TBPROT = 0, CMP = 0)

Status Register content				S25FL256L legacy block protection (TBPROT = 0, CMP = 0)			
BP3	BP2	BP1	BP0	Number Protected blocks	Protected blocks	Protected density (KB)	Protected portion
0	0	0	0	0	None	0	None
0	0	0	1	1	511	64	Upper 1/512
0	0	1	0	2	510–511	128	Upper 1/256
0	0	1	1	4	508–511	256	Upper 1/128
0	1	0	0	8	504–511	512	Upper 1/64
0	1	0	1	16	496–511	1024	Upper 1/32
0	1	1	0	32	480–511	2048	Upper 1/16
0	1	1	1	64	448–511	4096	Upper 1/8
1	0	0	0	128	384–511	8192	Upper 1/4
1	0	0	1	256	256–511	16384	Upper 1/2
1	0	1	0	512	0–511	32768	ALL
1	0	1	1	512	0–511	32768	ALL
1	1	0	0	512	0–511	32768	ALL
1	1	0	1	512	0–511	32768	ALL
1	1	1	0	512	0–511	32768	ALL
1	1	1	1	512	0–511	32768	ALL

Table 37 S25FL256L (256Mb) lower array legacy block protection (TBPROT = 1, CMP = 0)

Status Register content				S25FL256L legacy block protection (TBPROT = 0, CMP = 0)			
BP3	BP2	BP1	BP0	Number protected blocks	Protected blocks	Protected density (KB)	Protected portion
0	0	0	0	0	None	0	None
0	0	0	1	1	0	64	Lower 1/512
0	0	1	0	2	0–1	128	Lower 1/256
0	0	1	1	4	0–3	256	Lower 1/128
0	1	0	0	8	0–7	512	Lower 1/64
0	1	0	1	16	0–15	1024	Lower 1/32
0	1	1	0	32	0–31	2048	Lower 1/16
0	1	1	1	64	0–63	4096	Lower 1/8
1	0	0	0	128	0–127	8192	Lower 1/4
1	0	0	1	256	0–255	16384	Lower 1/2
1	0	1	0	512	0–511	32768	ALL
1	0	1	1	512	0–511	32768	ALL
1	1	0	0	512	0–511	32768	ALL
1	1	0	1	512	0–511	32768	ALL
1	1	1	0	512	0–511	32768	ALL
1	1	1	1	512	0–511	32768	ALL

7.6.2 Individual block lock (IBL) protection

Individual Block Lock Bits (IBL) are volatile, with one bit for each sector / block, and each bit can be individually modified. By issuing the IBL or GBL commands, a IBL bit is set to '0' protecting each related sector / block. By issuing the IBUL or GUL commands, a IBL bit is cleared to '1' unprotecting each related sector or block. By issuing the IBLRD command the state of each IBL bit can be read. This feature allows software to easily protect individual sectors / blocks against inadvertent changes, yet does not prevent the easy removal of protection when changes are needed. The IBL's can be set or cleared as often as needed as they are volatile bits.

Every main 64KB Block and the 4KB Sectors in bottom and top blocks has a volatile Individual Block Lock Bit (IBL) associated with it. When a sector / block IBL bit is '0', the related sector/block is protected from program and erase operations.

If the Pointer Region Protection is enabled this protected region is logically ORed with the IBL bits.

Following power-up, hardware reset, or software reset the default state [IBLLBB = 1] (see **Table 23**) all individual IBL bits are set to '0' in the protected state. In order to Program or Erase the Array the Global IBL Unlock or the Sector / Block IBL Unlock command must be given before the Program or Erase commands. When [IBLLBB = 0], all the individual IBL bits are set to '1' in the un-protected state following power-up, hardware reset, or software reset.

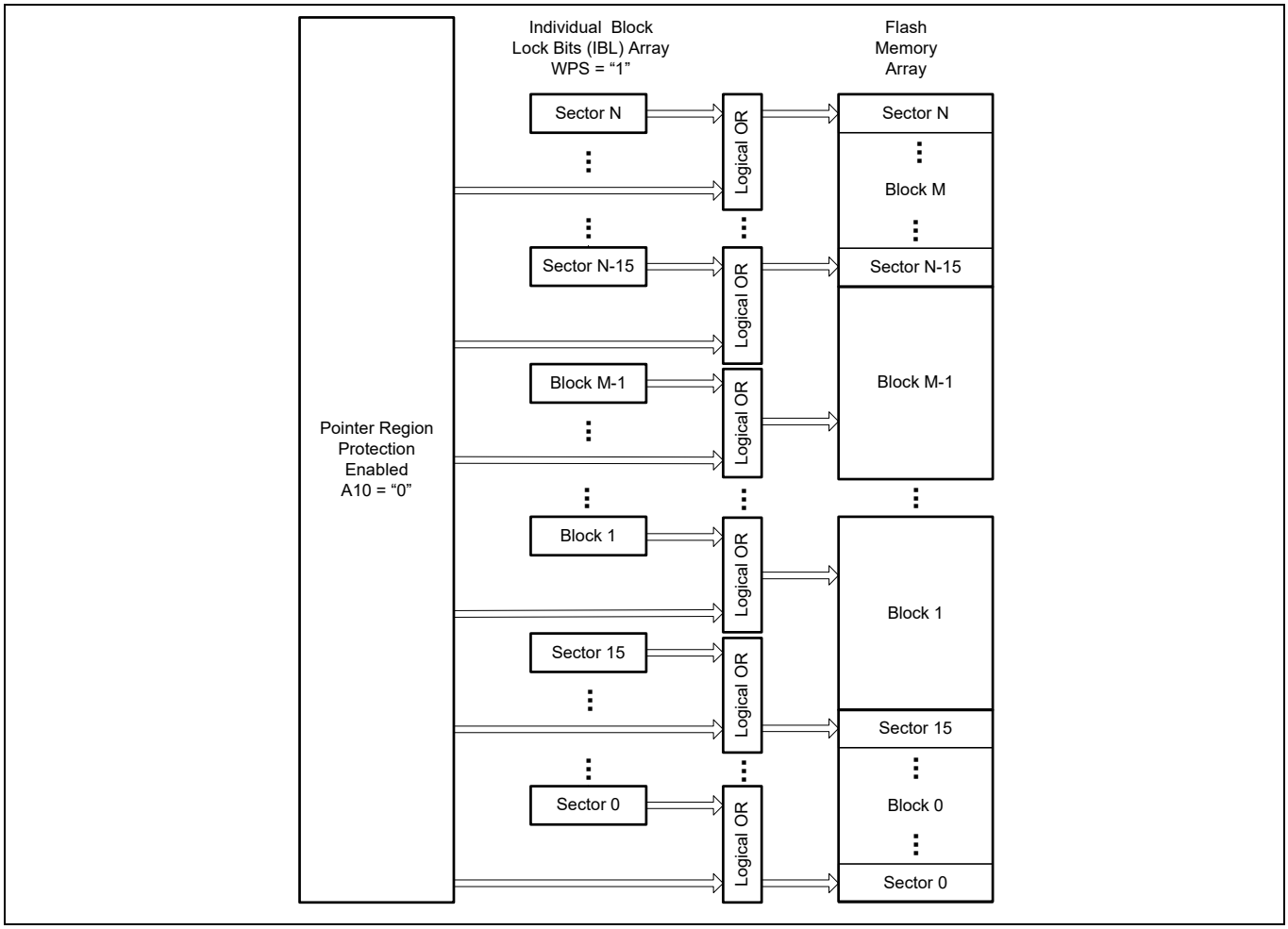


Figure 25 Individual block lock / pointer region protection control

Notes
26.The 'M' is the top 64KB block.
27.The 'N' is the top 4KB sector.

7.6.3 Pointer Region Protection (PRP)

The Pointer Region Protection is defined by a non-volatile address pointer that selects any 4KB sector as the boundary between protected and unprotected regions in the memory. This provides a protection scheme with individual sector granularity that remains in effect across power cycles and reset operations. PRP settings can also be protected from modification until the next power cycle, until a password is supplied, or can be permanently locked. PRP can be used in combination with either the Legacy Block Protection or Individual Block Lock protection methods. When enabled, PRP protection is logically ORed with the protection method selected by the WPS bit (CR2V[2]).

The Set Pointer Region Protection (SPRP FBh or 4SPRP E3h) command (see **"Pointer Region command"** on page 124) or Write Any Register (WRAR 71h) command to write the PRPR register (see **"Write Any Register (WRAR 71h)"** on page 93) is used to enable or disable PRP, and set the pointer value.

The S25FL256L device must have 4 Byte addressing enabled (CR2V[0] = 1) to set the Pointer Region Protection register PRPR (see **"Pointer Region Protection Register (PRPR)"** on page 52) this insures that A24 and A25 are set correctly.

After the Set Block/Pointer Protection command is given or Write Any Register (WRAR 71h) command to write the PRPR register, the value of A10 enables or disables the pointer protection mechanism. If A10 = 1, then the pointer protection region is disabled. This is the default state, and the rest of pointer values are don't care. If A10 = 0, then the pointer protection region is enabled. The value of A10 is written in the non-volatile pointer bit in the PRPR. The pointer address values for RFU bits are don't care but these bit locations will read back as ones. See **"Pointer Region Protection Register (PRPR)"** on page 52 for additional information on the PRPR.

If the pointer protection mechanism is enabled, the pointer value determines the block boundary between the protected and the unprotected regions in the memory. The pointer boundary is set by the three (A23–A12) or four (A31–A12) address bytes written to the non-volatile pointer value in the PRPR. The area that is unprotected will be inclusive of the 4KB sector selected by the pointer value.

The value of A9 is used to determine whether the region that is unprotected will start from the top (highest address) or bottom (lowest address) of the memory array to the location of the pointer. If A9 = 0 when the SPRP or 4SPRP command is issued followed by a the address, then the 4-kB sector which includes that address and all the sectors from the bottom up (zero to higher address) will be unprotected. If A9 = 1 when the SPRP or 4SPRP-command is issued followed by address then the 4-kB sector which includes that address and all the sectors from the Top down (max to lower address) will be unprotected. The value of A9 is in the non-volatile pointer value in the PRPR.

The A11 bit can be used to protect all sectors. If A11 = 1, then all sectors are protected. If A11 = 0, then the unprotected range will be determined by Amax–A12. The value of A11 is in the non-volatile pointer value in the PRPR.

The SPRP or 4SPRP command is ignored during a suspend operation because the pointer value cannot be erased and re-programmed during a suspend.

The SPRP or 4SPRP command is ignored if NVLOCK PR[0] = 0.

The Read Any Register 65h command (see **"Read Any Register (RDAR 65h)"** on page 90) reads the contents of PRP access register. This allows the contents of the pointer to be read out for test and verification.

Table 38 PRP table

A11	A10	A9	Protect address range	Unprotect address range	Comment
x	1	x	None	All	A10 = 1 is PRP disabled (this is the default state and the rest of pointer value is don't care).
0	0	0	1FFFFFF to (A[31:12] + 1)	A[31:12] to 0000000	The 4-KB sector which includes that address and all the sectors from the bottom up (zero to higher address) will be unprotected.
0	0	1	(A[31;12] – 1) to 0000000	1FFFFFF to A[31:12]	The 4-KB sector which includes that address and all the sectors from the Top down (max to lower address) will be unprotected.
1	0	x	1FFFFFF to 000000	Not Applicable	A10 = 0 and A11 = 1 means protect all sectors and Amax–A12 are don't care.

If the pointer protect scheme is active (A10 = 0), and the pointer protects any portion of the address space to which an erase command is applied, the erase command fails. For example, if the pointer protection is protecting 4KB of the array that would be affected by a Block erase command, that erase command fails. Chip Erase CEh command is ignored if PRP is enabled (A10 = 0) and this will set the E_ERR status bit.

If the Pointer Region Protection is enabled this protection is logically ORed with either the Legacy Block protection region if WPS CR2V[2] = 0 or Individual Block Lock protection if WPS CR2V[2] = 1 (See **Figure 24**).

7.7 Individual and Region protection

Individual and Region Protection (IRP) is the name used for a set of independent hardware and software methods used to disable or enable programming or erase operations on Security Regions 2 and 3 and the Pointer Region Protection Register.

Each method manages the state of the NVLOCK bit (PR[0]). When NVLOCK = 1, the Security Regions 2 and 3 and the Pointer Region Protection Register (PRPR) may be programmed and erased. When NVLOCK = 0, the Security Regions 2 and 3 and PRPR can not be programmed or erased. Note, the Security Regions 2 and 3 are also protected respectively by LB2 or LB3 = 1 (CR1NV[4:5]).

Power Supply Lock-down protection is the default method. This method sets the NVLOCK bit to ‘1’ during POR or Hardware Reset so that the NVLOCK related areas and registers are unprotected by a device reset. The PRL (A6h) command clears the NVLOCK bit to ‘0’ to protect the NVLOCK related areas and registers. There is no command in the Power Supply Lock-down method to set the NVLOCK bit to ‘1’, therefore the NVLOCK bit will remain at ‘0’ until the next power-off or hardware reset. The Power Supply Lock-down method allows boot code the option of changing Security Regions 2 and 3 or the value in PRPR, by programming or erasing these non-volatile areas, then protecting these non-volatile areas from further change for the remainder of normal system operation by clearing the NVLOCK bit to ‘0’. This is sometimes called Boot-code controlled protection.

The Password method clears the Protection Register NVLOCK bit to 0 and sets the SECRRP bit = IRP[6] during POR or Hardware Reset to protect the NVLOCK related areas and registers. The SECRRP bit determines whether Security Region 3 is readable. A 64-bit password may be permanently programmed and hidden for the password method. The PASSU (EAh) command can be used to provide a password for comparison with the hidden password. If the password matches, the NVLOCK bit is set to ‘1’ to unprotect the NVLOCK related areas and registers. The PRL (A6h) command can be used to clear the NVLOCK bit to ‘0’ to turn on protection again.

The Permanent method permanently sets the SECRRP bit = 1 and clears NVLOCK to 0. This permanently protects the Security Regions 2 and 3 and the PRPR.

The selection of the NVLOCK bit management method is made by programming OTP bits in the IRP Register (IRP[2 or 1 or 0] so as to permanently select the method used.

An overview of all methods is shown in **Figure 26**.

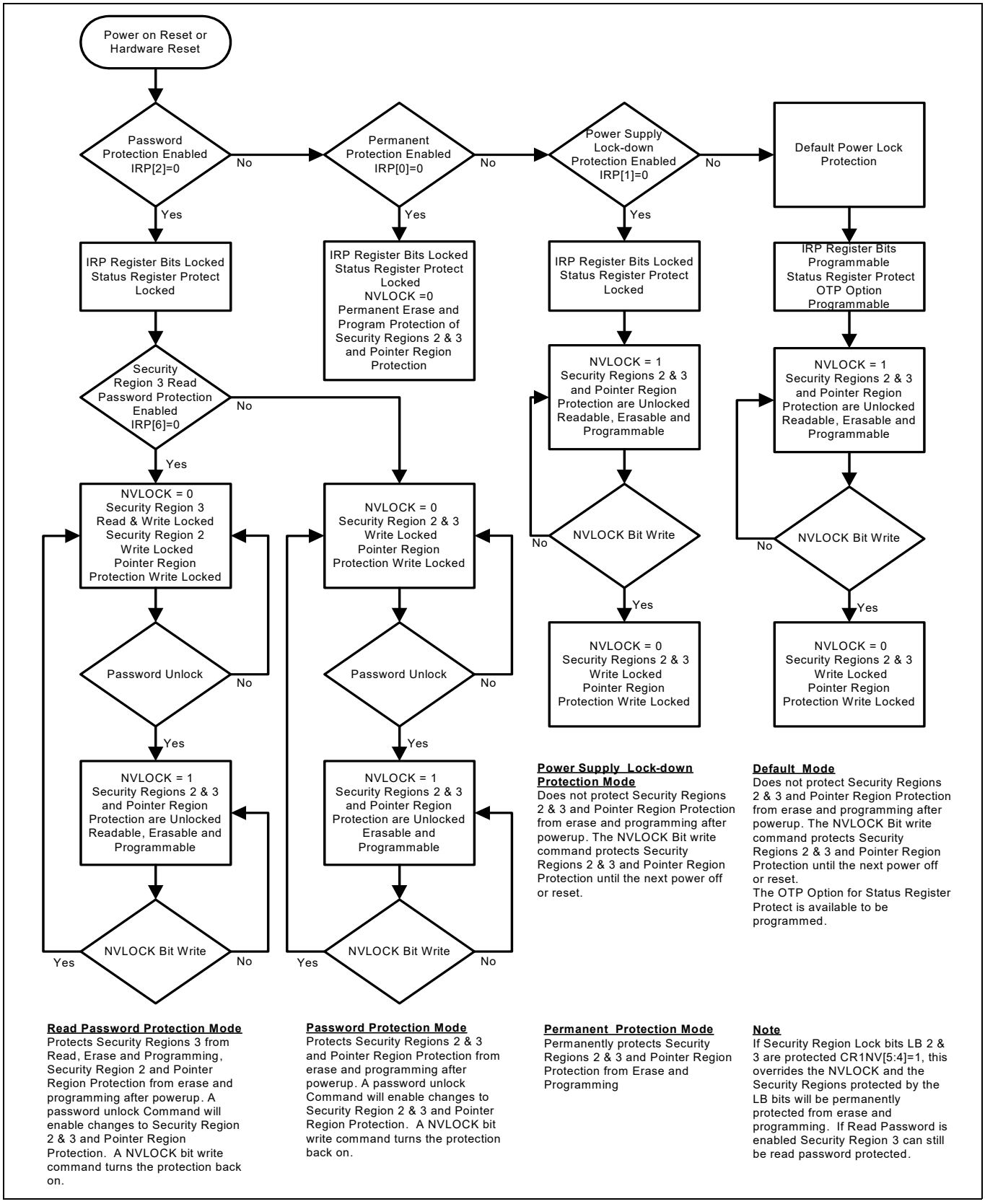


Figure 26 Permanent, password and power supply lock-down protection overview

7.7.1 IRP register

The IRP register is used to permanently configure the behavior of Individual and Region Protection (IRP) features (see **Table 23**).

As shipped from the factory, all devices default to the power supply lock-down protection mode, with all regions unprotected.

The device programmer or host system must then choose which protection method to use by programming one of the, one-time programmable bits, Permanent, Power Supply Lock-down or Password Protection Mode. Programming one of these bits locks the part permanently in the selected mode:

Factory Defaults IRP register

- IRP[6] = 1 = Read Password Protection Mode not enabled.
- IRP[4] = 1 = IBL bits power-up in protected state.
- IRP[2] = 1 = Password Protection Mode not enabled.
- IRP[1] = 1 = Power Supply Lock-down protection Mode not enabled but is the default mode.
- IRP[0] = 1 = Permanent Protection Mode not enabled.

IRP register programming rules:

- If the Read Password mode is chosen, the SECRRP bit must be programmed prior or at the same time as setting the Password Protection mode Lock Bits IRP[2].
- If the IBL bits power-up in unprotected mode is chosen, the IBLLBB bit must be programmed prior or at the same time as setting one of the Protection mode Lock Bits IRP[2:0].
- If the password mode is chosen, the password must be programmed prior to setting the Password Protection mode Lock Bits IRP[2].
- The protection modes are mutually exclusive, only one may be selected. Once one of the Protection Modes is selected IPRP[2:0], the IRP Register bits are permanently protected from programming and no further changes to the OTP register bits is allowed. If an attempt to change any of the register bits above, after the Protection mode is selected, the operation will fail and P_ERR (SR2V[5]) will be set to 1.

The programming time of the IRP Register is the same as the typical page programming time. The system can determine the status of the IRP register programming operation by reading the WIP bit in the Status Register. See **“Status Register 1”** on page 32 for information on WIP. See **“Password protection mode”** on page 68.

7.7.1.1 IBL Lock Boot bit

The default IBL Lock Bit IRP[4] = 1, all the IBL bits on power-up or reset (after a hardware reset or software reset) to the “protected state.” If the IBL Lock Bit IRP[4] = 0 (programmed), the IBL power-up or reset to the “unprotected state.”

7.7.2 Protection Register (PR)

7.7.2.1 NVLOCK bit (PR[0])

The NVLOCK bit is a volatile bit for protecting:

- Pointer Region Protection Register
- Security Regions 2 and 3

When cleared to '0', NVLOCK locks the related regions. When set to '1', it allows the related regions to be changed. See **"Protection Register (PR)"** on page 51 for more information.

The PRL command is used to clear the NVLOCK bit to '0'. The NVLOCK Bit should be cleared to '0' only after all the related regions are configured to the desired settings.

In Power Supply Lock-down protection mode, the NVLOCK is set to '1' during POR or a hardware reset. A software reset command does not affect the NVLOCK bit. When cleared to '0', no software command sequence can set the NVLOCK bit to '1', only another hardware reset or power-up can set the NVLOCK bit.

In the Password Protection mode, the NVLOCK bit is cleared to '0' during POR, or a hardware reset. The NVLOCK bit can only be set to '1' by the Password Unlock command.

The Permanent method permanently clears NVLOCK to 0. This permanently protects the Security Regons 2 and 3 and the PRPR.

7.7.2.2 Security Region Read Password Lock bit (SECRRP, PR[6])

The SECRRP Bit is a volatile bit for read protecting Security Region 3. When SECRRP[6] = 0 the Security Region 3 can not be read, See **"Protection Register (PR)"** on page 51 for more information.

In the Password Protection mode, the SECRRP bit is set equal to IRP[6] during POR or software or hardware reset. The NVLOCK bit can only be set to '1' by the Password Unlock command. A software reset does not affect the NVLOCK bit.

The Permanent method permanently sets the SECRRP bit = 1. This permanently leaves Security Region 3 readable.

7.7.3 Password protection mode

Password Protection Mode allows an even higher level of security than the Power Supply Lock-down protection Mode, by requiring a 64-bit password for unlocking the NVLOCK bit. In addition to this password requirement, after power up, hardware reset, the NVLOCK bit is cleared to '0' to ensure protection after power-up or reset. Successful execution of the Password Unlock command by entering the entire password sets the NVLOCK bit to 1, allowing for sector NVLOCK related areas and registers modifications.

Password Protection Notes:

- Once the Password is programmed and verified, the Password Mode (IRP[2] = 0) must be set in order to prevent reading the password.
- The Password Program Command is only capable of programming '0's. Programming a '1' after a cell is programmed as a '0' results in the cell left as a '0' with no programming error set.
- The password is all '1's when shipped from Infineon. It is located in its own memory space and is accessible through the use of the Password Program, Password Read, RDAR, and WRAR commands.
- All 64-bit password combinations are valid as a password.
- The Password Mode, once programmed, prevents reading the 64-bit password and further password programming. All further program and read commands to the password region are disabled and these commands are ignored or return undefined data. There is no means to verify what the password is after the Password Mode Lock Bit is selected. Password verification is only allowed before selecting the Password Protection mode.
- The Protection Mode Lock Bits are not erasable.

- The exact password must be entered in order for the unlocking function to occur. If the password unlock command provided password does not match the hidden internal password, the unlock operation fails in the same manner as a programming operation on a protected sector. The P_ERR bit is set to one, the WIP Bit remains set, and the NVLOCK bit remains cleared to 0.
- The Password Unlock command cannot be accepted any faster than once every 100 µs ± 20 µs. This makes it take an unreasonably long time (58 million years) for a hacker to run through all the 64-bit combinations in an attempt to correctly match a password. The Read Status Register 1 command may be used to read the WIP bit to determine when the device has completed the password unlock command or is ready to accept a new password command. When a valid password is provided the password unlock command does not insert the 100 µs delay before returning the WIP bit to zero.
- If the password is lost after selecting the Password Mode, there is no way to set the NVLOCK bit = 1.

7.7.4 Security Region read password protection

The Security Region Read Password Protection enables protecting Security Region 3 from read, program and erase.

- Security Region Read Password Protection is an optional addition to the Password Protection Mode (described above). The Security Regions Read Password Protection is enabled when the user programs SECRRP bit 'IRP[6] = 0'. The SECRRP bit IRP[6] must be programmed prior or at the same time as setting the Password Protection mode Lock Bits IRP[2].

The Security Regions Read Password Protection is not active until the password is programmed, IRP[2] is programmed to 0.

When the SECRRP (PR[6]) bit is set to 0 the Security Region 3 is not readable. If these regions are read the resulting data is invalid and undefined.

7.7.5 Recommended IRP protection process

During system manufacture, the Flash device configuration should be defined by:

1. Programming the Security Regions as desired.
2. Set Pointer Region Protection Register as desired.
3. Program the Password register (PASS) if password protection will be used.
4. Program the IRP Register as desired, including the selection of Permanent, Power Supply Lock-down or password IRP protection mode in IRP[2:0]. It is very important to explicitly select a protection mode so that later accidental or malicious programming of the IRP register is prevented. This is to ensure that only the intended protection features are enabled.
   Before or while programming the IRP register:
   a. The IBLLBB bit (IRP[4]) may be used to cause all the IBL bits to power up in the unprotected state.
   b. The SECRRP bit (IRP[6]) may be programmed to select Security Regions Read Password Protection to use the password to control read access to the Security Region 3.

During system power up and boot code execution: If the Power Supply Lock-down protection mode is in use, trusted boot code can determine whether there is any need to modify the NVLOCK related areas or registers. If no changes are needed the NVLOCK bit can be cleared to 0 via the PRL command to protect the NVLOCK related areas or registers from changes during the remainder of normal system operation while power remains on.

8 Commands

All communication between the host system and FL-L family memory devices is in the form of units called commands. See **"Command protocol"** on page 19 for details on command protocols.

Although host software in some cases is used to directly control the SPI interface signals, the hardware interfaces of the host system and the memory device generally handle the details of signal relationships and timing. For this reason, signal relationships and timing are not covered in detail within this software interface focused section of the document. Instead, the focus is on the logical sequence of bits transferred in each command rather than the signal timing and relationships. Following are some general signal relationship descriptions to keep in mind. For additional information on the bit level format and signal timing relationships of commands, see **"Command protocol"** on page 19.

- The host always controls the Chip Select (CS#), Serial Clock (SCK), and Serial Input (SI) - SI for single bit wide transfers. The memory drives Serial Output (SO) for single bit read transfers. The host and memory alternately drive the IO0–IO3 signals during Dual and Quad transfers.
- All commands begin with the host selecting the memory by driving CS# low before the first rising edge of SCK. CS# is kept low throughout a command and when CS# is returned high the command ends. Generally, CS# remains low for eight bit transfer multiples to transfer byte granularity information. No commands will be accepted if CS# is returned high not at an 8 bit boundary.

8.1 Command set summary

8.1.1 Extended addressing

To accommodate addressing above 128 Mb, there are two options:

1. Instructions that always require a 4-Byte address, used to access up to 32 Gb of memory:

Table 39 Extended address 4-byte address commands

Command name	Function	Instruction (Hex)
4READ	Read	13
4FAST_READ	Read Fast	0C
4DOR	Dual Output Read	3C
4QOR	Quad Output Read	6C
4DIOR	Dual I/O Read	BC
4QIOR	Quad I/O Read	EC
4DDRQIOR	DDR Quad I/O Read	EE
4PP	Page Program	12
4QPP	Quad Page Program	34
4SE	Sector Erase	21
4HBE	Half Block Erase	53
4BE	Block Erase	DC
4IBLRD	IBL Read	E0
4IBL	IBL Lock	E1
4IBUL	IBL Unlock	E2
4SPRP	Set Pointer Region Protection	E3

2. A 4 Byte address mode for backward compatibility to the 3 Byte address instructions. The standard 3 Byte instructions can be used in conjunction with a 4 Byte address mode controlled by the Address Length configuration bit (CR2V[0]). The default value of CR2V[0] is loaded from CR2NV[1] (following power up, hardware reset, or software reset), to enable default 3-Byte (24-bit) or 4 Byte (32 bit) addressing. When the address length (CR2V[0]) set to 1, the legacy commands are changed to require 4-Bytes (32-bits) for the address field. The following instructions can be used in conjunction with the 4 Byte address mode configuration to switch from 3-Bytes to 4-Bytes of address field.

Table 40 Extended address 4-byte address mode with 3-byte address commands

Command name	Function	Instruction (Hex)
RSFDP	Read SFDP	5A
READ	Read	03
FAST_READ	Read Fast	0B
DOR	Dual Output Read	3B
QOR	Quad Output Read	6B
DIOR	Dual I/O Read	BB
QIOR	Quad I/O Read	EB
DDRQIOR	DDR Quad I/O Read)	ED
PP	Page Program	02
QPP	Quad Page Program	32
SE	Sector Erase	20
HBE	Half Block Erase	52
BE	Block Erase	D8
RDAR	Read Any Register	65
WRAR	Write Any Register	71
SECRE	Security Region Erase	44
SECRP	Security Region Program	42
SECRR	Security Region Read	48
IBLRD	IBL Read	3D
IBL	IBL Lock	36
IBUL	IBL Unlock	39
SPRP	Set Pointer Region Protection	FB

8.1.2 Command summary by function

Table 41 FL-L family command set (Sorted by function)

Function	Command name	Command description	Instruction value (Hex)	Maximum frequency (MHz)	Address length (Bytes)	QPI
Read Device ID	RDID	Read ID (JEDEC Manufacturer ID)	9F	108	0	Yes
	RSFDP	Read JEDEC Serial Flash Discoverable Parameters	5A	133	3 or 4	
	RDQID	Read Quad ID	AF	108	0	
	RUID	Read Unique ID	4B	133		
Register Access	RDSR1	Read Status Register 1	05	108		
	RDSR2	Read Status Register 2	07			No
	RDCR1	Read Configuration Register 1	35			
	RDCR2	Read Configuration Register 2	15			
	RDCR3	Read Configuration Register 3	33			
	RDAR	Read Any Register	65	133	3 or 4	Yes
	WRR	Write Register (Status-1 and Configuration-1,2,3)	01		0	
	WRDI	Write Disable	04			
	WREN	Write Enable for Non-volatile data change	06			
	WRENV	Write Enable for Volatile Status and Configuration Registers	50			
	WRAR	Write Any Register	71		3 or 4	
	CLSR	Clear Status Register	30		0	
	4BEN	Enter 4 Byte Address Mode	B7			
	4BEX	Exit 4 Byte Address Mode	E9			
	SBL	Set Burst Length	77			
	QPIEN	Enter QPI	38			No
	QPIEX	Exit QPI	F5			Yes
	DLPRD	Data Learning Pattern Read	41			
	PDLRNV	Program NV Data Learning Register	43			
	WDLRV	Write Volatile Data Learning Register	4A			

Table 41 FL-L family command set (Sorted by function) (Continued)

Function	Command name	Command description	Instruction value (Hex)	Maximum frequency (MHz)	Address length (Bytes)	QPI
Read Flash Array	READ	Read	03	50	3 or 4	No
	4READ	Read	13	50	4	
	FAST_READ	Fast Read	0B	133	3 or 4	
	4FAST_READ		0C		4	
	DOR	Dual Output Read	3B		3 or 4	
	4DOR		3C		4	
	QOR	Quad Output Read	6B		3 or 4	
	4QOR		6C		4	
	DIOR	Dual I/O Read	BB		3 or 4	
	4DIOR		BC		4	

Table 41 FL-L family command set (Sorted by function) (Continued)

Function	Command name	Command description	Instruction value (Hex)	Maximum frequency (MHz)	Address length (Bytes)	QPI
Read Flash Array	QIOR	Quad I/O Read (CR1V[1] = 1) or CR2V[3] = 1	EB	133	3 or 4	Yes
	4QIOR		EC		4	
	DDRQIOR	DDR Quad I/O Read (CR1V[1] = 1 or CR2V[3] = 1)	ED	66	3 or 4	
	4DDRQIOR	DDR Quad I/O Read (CR1V[1] = 1 or CR2V[3] = 1)	EE		4	
Program Flash Array	PP	Page Program	02	133	3 or 4	
	4PP		12		4	
	QPP	Quad Page Program	32		3 or 4	No
	4QPP		34		4	
Erase Flash Array	SE	Sector Erase	20		3 or 4	Yes
	4SE		21		4	
	HBE	Half Block Erase	52		3 or 4	
	4HBE		53		4	
	BE	Block Erase	D8		3 or 4	
	4BE		DC		4	
	CE	Chip Erase	60		0	
	CE	Chip Erase (alternate instruction)	C7			
Erase /Program Suspend /Resume	EPS	Erase / Program Suspend	75			
	EPR	Erase / Program Resume	7A			
Security Region Array	SECRE	Security Region Erase	44		3 or 4	
	SECRP	Security Region Program	42			
	SECRR	Security Region Read	48			
Array Protection	IBLRD	IBL Read	3D			
	4IBLRD	IBL Read	E0		4	
	IBL	IBL Lock	36		3 or 4	
	4IBL		E1		4	
	IBUL	IBL Unlock	39		3 or 4	
	4IBUL		E2		4	
	GBL	Global IBL Lock0	7E		0	
	GBUL	Global IBL Unlock	98			
	SPRP	Set Pointer Region Protection	FB		3 or 4[29]	
	4SPRP	Set Pointer Region Protection	E3		4	
Individual and Region Protection	IRPRD	IRP Register Read	2B		0	
	IRPP	IRP Register Program	2F			
	PRRD	Protection Register Read	A7			
	PRL	Protection Register Lock (NVLOCK Bit Write)	A6			

Table 41 FL-L family command set (Sorted by function) (Continued)

Function	Command name	Command description	Instruction value (Hex)	Maximum frequency (MHz)	Address length (Bytes)	QPI
Reset	RSTEN	Software Reset Enable	66	133	0	Yes
	RST	Software Reset	99			
	MBR	Mode Bit Reset	FF			
Deep Power Down	DPD	Deep Power Down	B9			
	RES	Release from Deep Power Down / Device ID	AB			
RFU	Reserved-18	Reserved	18	–	–	
	Reserved-41		41			
	Reserved-43		43			
	Reserved-4A		4A			
	Reserved-ED		ED			
	Reserved-EE		EE			

8.1.3 Read device identification

There are multiple commands to read information about the device manufacturer, device type, and device features. SPI memories from different vendors have used different commands and formats for reading information about the memories. The FL-L family supports the three device information commands.

8.1.4 Register read or write

There are multiple registers for reporting embedded operation status or controlling device configuration options. There are commands for reading or writing these registers. Registers contain both volatile and non-volatile bits. Non-volatile bits in registers are automatically erased and programmed as a single (write) operation.

8.1.4.1 Monitoring operation status

The host system can determine when a write, program, erase, suspend or other embedded operation is complete by monitoring the Write in Progress (WIP) bit in the Status Register. The Read from Status Register 1 command or Read Any Register command provides the state of the WIP bit. The Read from Status Register 2 or Read Any Register command provides the state of the program error (P_ERR) and erase error (E_ERR) bits in the status register indicate whether the most recent program or erase command has not completed successfully. When P_ERR or E_ERR bits are set to one, the WIP bit will remain set to one indicating the device remains busy and unable to receive most new operation commands. Only status reads (RDSR1 05h, RDSR2 07h), Read Any Register (RDAR 65h), Read Configuration RDCR1 and RDCR3, status clear (CLSR 30h), and software reset (RSTEN 66h followed by RST 99h) are valid commands when P_ERR or E_ERR is set to 1. A Clear Status Register (CLSR) command must be sent to return the device to standby state. Alternatively, Hardware Reset, or Software Reset (RSTEN 66h followed by RST 99h) may be used to return the device to standby state.

8.1.4.2 Configuration

There are commands to read, write, and protect registers that control interface path width, interface timing, interface address length, and some aspects of data protection.

Notes

28.Commands not supported in QPI mode have undefined behavior if sent when the device is in QPI mode.
29.For S25FL256L device, the SPRP command must be in 4 byte address mode with CR2V[0] = 1.

8.1.5 Read flash array

Data may be read from the memory starting at any byte boundary. Data bytes are sequentially read from incrementally higher byte addresses until the host ends the data transfer by driving CS# input High. If the byte address reaches the maximum address of the memory array, the read will continue at address zero of the array.

Burst Wrap read can be enabled by the Set Burst Length (SBL 77h) command with the requested wrapped read length and alignment, see **"Set Burst Length (SBL 77h)"** on page 94. Burst Wrap read is only for Quad I/O and QPI modes.

There are several different read commands to specify different access latency and data path widths. Double Data Rate (DDR) commands also define the address and data bit relationship to both SCK edges:

- The Read command provides a single address bit per SCK rising edge on the SI/IO0 signal with read data returning a single bit per SCK falling edge on the SO/IO1 signal. This command has zero latency between the address and the returning data but is limited to a maximum SCK rate of 50 MHz.
- Other read commands have a latency period between the address and returning data but can operate at higher SCK frequencies. The latency depends on a configuration register read latency value.
- The Fast Read command provides a single address bit per SCK rising edge on the SI/IO0 signal with read data returning a single bit per SCK falling edge on the SO/IO1 signal.
- Dual or Quad Output Read commands provide address on SI/IO0 pin on the SCK rising edge with read data returning two bits, or four bits of data per SCK falling edge on the IO0–IO3 signals.
- Dual or Quad I/O Read commands provide address two bits or four bits per SCK rising edge with read data returning two bits, or four bits of data per SCK falling edge on the IO0–IO3 signals. Continuous read feature is enabled if the mode bits value is Axh.
- Quad Double Data Rate read commands provide address four bits per every SCK edge with read data returning four bits of data per every SCK edge on the IO0–IO3 signals. Continuous read feature is enabled if the mode bits value is Axh.

8.1.6 Program flash array

Programming data requires two commands: Write Enable (WREN), and Page Program (PP, 4PP, QPP, 4QPP). The Page Program command accepts from 1 byte up to 256 consecutive bytes of data (page) to be programmed in one operation. Programming means that bits can either be left at 1, or programmed from 1 to 0. Changing bits from 0 to 1 requires an erase operation.

8.1.7 Erase flash array

The Sector Erase, Half Block Erase, Block Erase, or Chip Erase commands set all the bits in a sector or the entire memory array to 1. A bit needs to be first erased to 1 before programming can change it to a 0. While bits can be individually programmed from a 1 to 0, erasing bits from 0 to 1 must be done on a sector-wide, half block-wide, block-wide or array-wide (Chip) level. The Write Enable (WREN) command must precede an erase command.

8.1.8 Security Regions, legacy block protection, and individual and region protection

There are commands to read and program a separate One Time Protection (OTP) array for permanently protected data such as a serial number. There are commands to control a contiguous group (block) of Flash memory array sectors that are protected from program and erase operations.There are commands to control which individual Flash memory array sectors are protected from program and erase operations. There is a mode to limit read access of Security Region 3 until a password is supplied.

8.1.9 Reset

There are commands to reset to the default conditions present after power on to the device. However, the software reset commands do not affect the current state of the SRP1 or NVLOCK Bits. In all other respects a software reset is the same as a hardware reset.

There is a command to reset (exit from) the Continuous Read Mode.

8.1.10 Reserved

Some instructions are reserved for future use. In this generation of the FL-L family some of these command instructions may be unused and not affect device operation, some may have undefined results.

Some commands are reserved to ensure that a legacy or alternate source device command is allowed without effect. This allows legacy software to issue some commands that are not relevant for the current generation FL-L family with the assurance these commands do not cause some unexpected action.

Some commands are reserved for use in special versions of the FL-L not addressed by this document or for a future generation. This allows new host memory controller designs to plan the flexibility to issue these command instructions. The command format is defined if known at the time this document revision is published.

8.2 Identification commands

8.2.1 Read Identification (RDID 9Fh)

The Read Identification (RDID) command provides read access to manufacturer identification, device identification. The manufacturer identification is assigned by JEDEC. The device identification values are assigned by Infineon.

Any RDID command issued while a program, erase, or write cycle is in progress is ignored and has no effect on execution of the program, erase, or write cycle that is in progress.

The RDID instruction is shifted on SI / IO0. After the last bit of the RDID instruction is shifted into the device, a byte of manufacturer identification, two bytes of device identification, will be shifted sequentially out on SO / IO1, As a whole this information is referred to as ID. See **“Device ID address map”** on page 147 for the detail description of the ID contents.

Continued shifting of output beyond the end of the defined ID address space will provide undefined data. The RDID command sequence is terminated by driving CS# to the logic high state anytime during data output. The RDID command is supported up to 108 MHz.

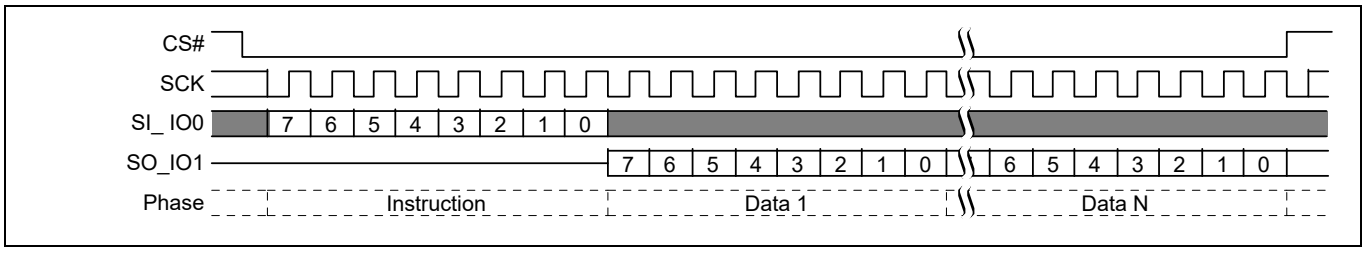


Figure 27 Read Identification (RDID) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 and the returning data is shifted out on IO0–IO3.

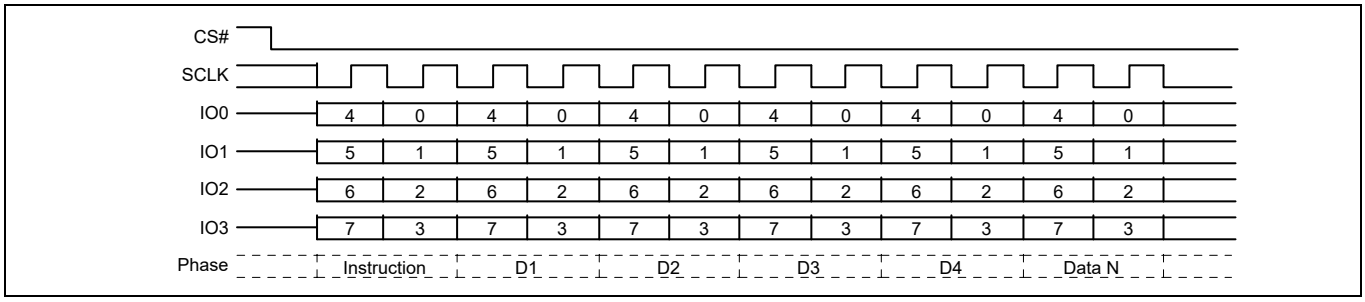


Figure 28 Read Identification (RDID) QPI mode command

8.2.2 Read Quad Identification (RDQID AFh)

The Read Quad Identification (RDQID) command provides read access to manufacturer identification, device identification. This command is an alternate way of reading the same information provided by the RDID command while in QPI mode. In all other respects the command behaves the same as the RDID command.

The command is recognized only when the device is in QPI Mode (CR2V[3] = 1) or Quad Mode (CR1V[1] = 1). The instruction is shifted in on IO0–IO3 for QPI Mode and IO0 for Quad Mode. After the last bit of the instruction is shifted into the device, a byte of manufacturer identification, two bytes of device identification will be shifted sequentially out on IO0–IO3. As a whole this information is referred to as ID. See **“Device ID address map”** on page 147 for the detail description of the ID contents.

Continued shifting of output beyond the end of the defined ID address space will provide undefined data. The command sequence is terminated by driving CS# to the logic high state anytime during data output.

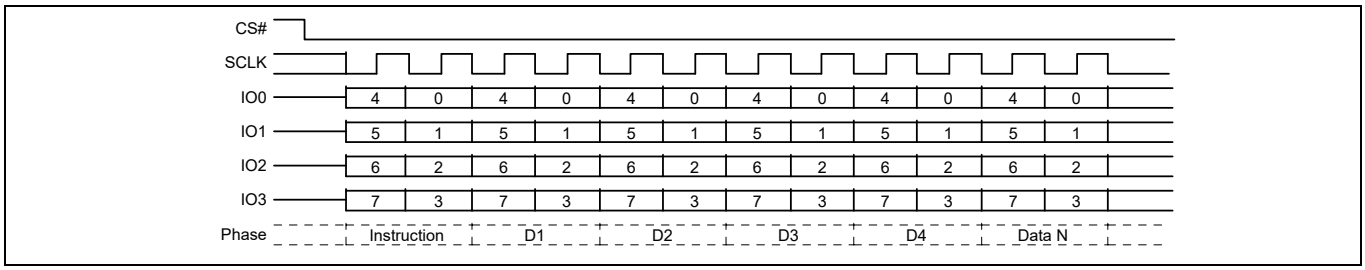


Figure 29 Read Quad Identification (RDQID) command sequence QPI mode

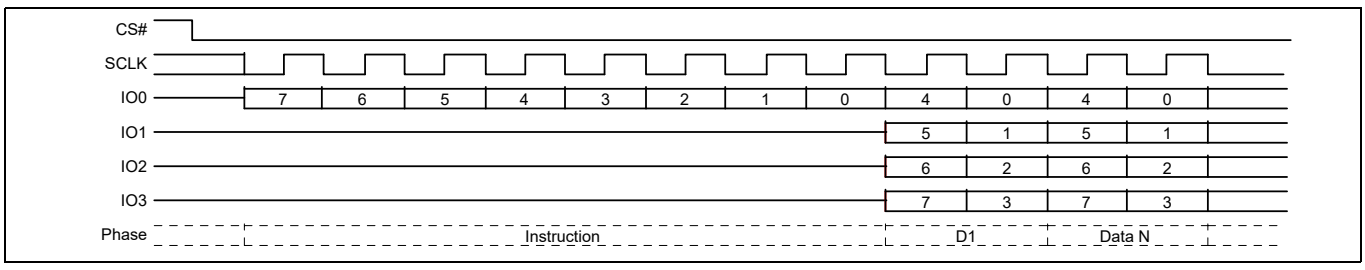


Figure 30 Read Quad Identification (RDQID) command sequence quad mode

8.2.3 Read serial flash discoverable parameters (RSFDP 5Ah)

The command is initiated by shifting on SI the instruction code “5Ah”, followed by a 24-bit (3 byte) address or 32-bit (4 byte) address (depending on the current Address Length configuration of CR2V[0]), followed by the number of read latency (dummy cycles) set by the Variable Read Latency configuration in CR3V[3:0].

The SFDP bytes are then shifted out on SO/IO1 starting at the falling edge of SCK after the dummy cycles. The SFDP bytes are always shifted out with the MSb first. If the 24-bit (3 byte) address or 32-bit (4 byte) address is set to any non-zero value, the selected location in the SFDP space is the starting point of the data read. This enables random access to any parameter in the SFDP space. In SPI mode the RSFDP command is supported up to 133 MHz.

The Variable Read Latency should be set to 8 cycles for compliance with the JEDEC JESD216 SFDP standard. The non-volatile default Variable Read Latency in CR3NV is set to 8 dummy cycles when the device is shipped from Infineon. However, because the RSFDP command uses the same implementation as other variable address length and latency read commands, users are free to modify the address length and latency of the command if desired.

Continuous (sequential) read is supported with the Read SFDP command.

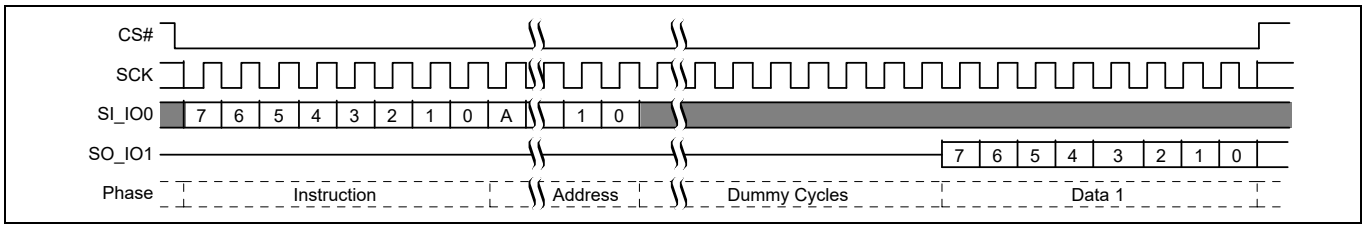


Figure 31 RSFDP command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 and the returning data is shifted out on IO0–IO3.

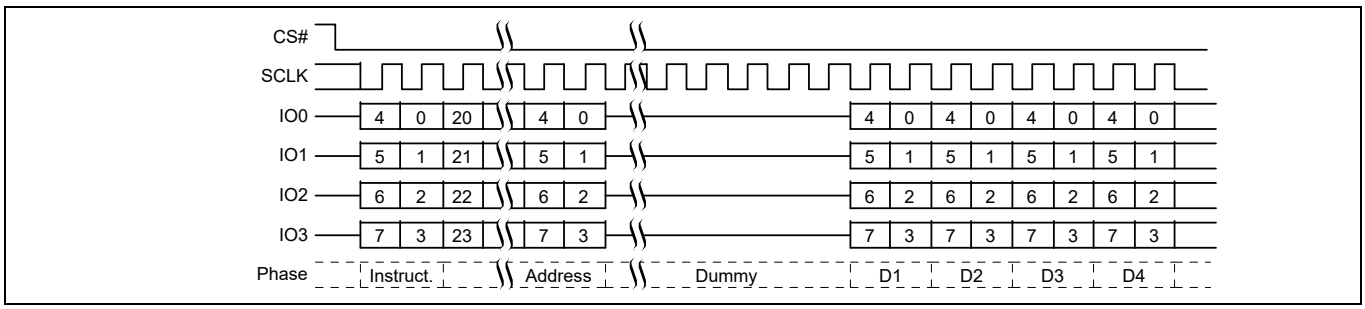


Figure 32 RSFDP QPI mode command sequence

Note
30.A = MSb of address = 23 for CR2V[0] = 0, or 31 for CR2V[0] = 1 or command 13h.

8.2.4 Read Unique ID (RUID 4Bh)

The Read Identification (RUID) command provides read access to factory set read only 64-bit number that is unique to each device.

The RUID instruction is shifted on SI followed by four dummy bytes or 16 dummy bytes QPI (32 clock cycles). This latency period (i.e., dummy bytes) allows the device's internal circuitry enough time to access data at the initial address. During latency cycles, the data value on IO0–IO3 are "don't care" and may be high impedance.

Then the 8 bytes of Unique ID will be shifted sequentially out on SO / IO1.

Continued shifting of output beyond the end of the defined Unique ID address space will provide undefined data. The RUID command sequence is terminated by driving CS# to the logic high state anytime during data output.

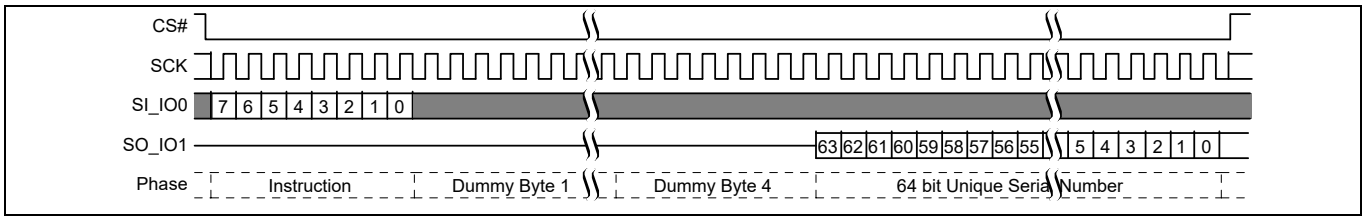


Figure 33 Read Unique ID (RUID) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 and the returning data is shifted out on IO0–IO3.

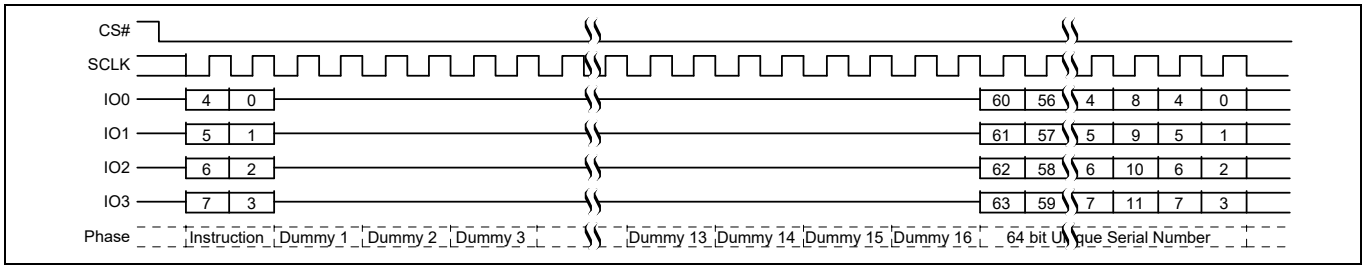


Figure 34 Read Unique ID (RUID) QPI mode command

8.3 Register access commands

8.3.1 Read Status Register 1 (RDSR1 05h)

The Read Status Register 1 (RDSR1) command allows the Status Register 1 contents to be read from SO/IO1.

The volatile version of Status Register 1 (SR1V) contents may be read at any time, even while a program, erase, or write operation is in progress. It is possible to read Status Register 1 continuously by providing multiples of eight clock cycles. The status is updated for each eight cycle read.

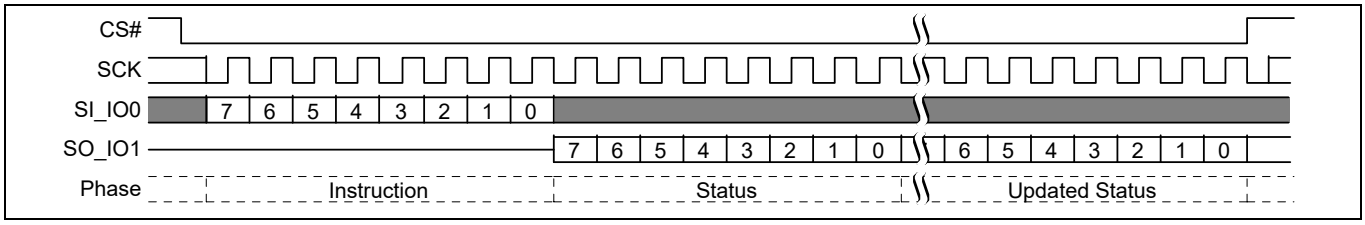


Figure 35 Read Status Register 1 (RDSR1) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 and the returning data is shifted out on IO0–IO3. In QPI mode, the read status register can be supported up to 108 MHz clock frequency. To read Status Register 1 above 108 MHz use the Read Any Register command, see **"Read Any Register (RDAR 65h)"** on page 90.

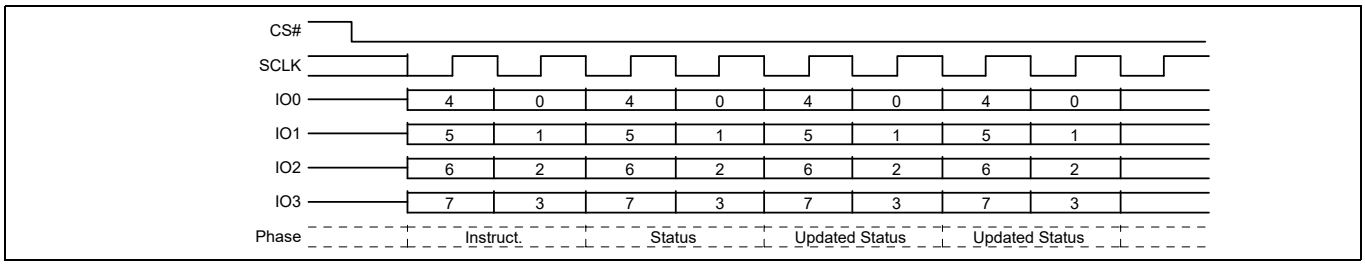


Figure 36 Read Status Register 1 (RDSR1) QPI Mode Command

8.3.2 Read Status Register 2 (RDSR2 07h)

The Read Status Register 2 (RDSR2) command allows the Status Register 2 contents to be read from SO/IO1.

The volatile Status Register 2 SR2V contents may be read at any time, even while a program, erase, or write operation is in progress. It is possible to read the Status Register 2 continuously by providing multiples of eight clock cycles. The status is updated for each eight cycle read.

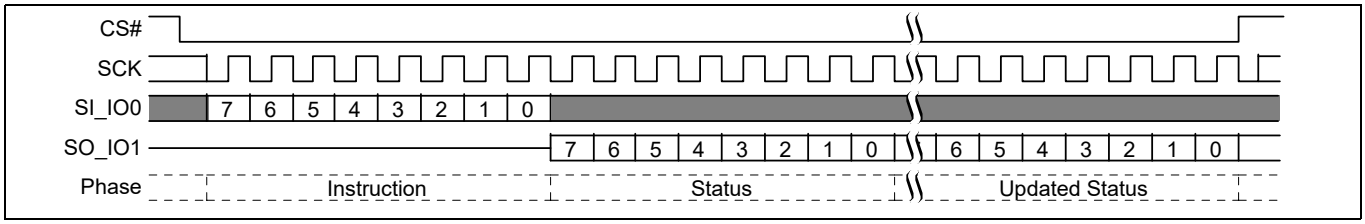


Figure 37 Read Status Register 2 (RDSR2) Command

In QPI mode, status register 2 may be read via the Read Any Register command, see **"Read Any Register (RDAR 65h)"** on page 90.

8.3.3 Read Configuration Registers (RDCR1 35h) (RDCR2 15h) (RDCR3 33h)

The Read Configuration Register (RDCR1, RDCR2, RDCR3) commands allows the volatile Configuration Registers (CR1V, CR2V, CR3V) contents to be read from SO/IO1.

It is possible to read CR1V, CR2V and CR3V continuously by providing multiples of eight clock cycles. The Configuration Registers contents may be read at any time, even while a program, erase, or write operation is in progress. To read the Configuration Register 1, 2 and 3 at higher frequencies use the read any register command, see **"Read Any Register (RDAR 65h)"** on page 90.

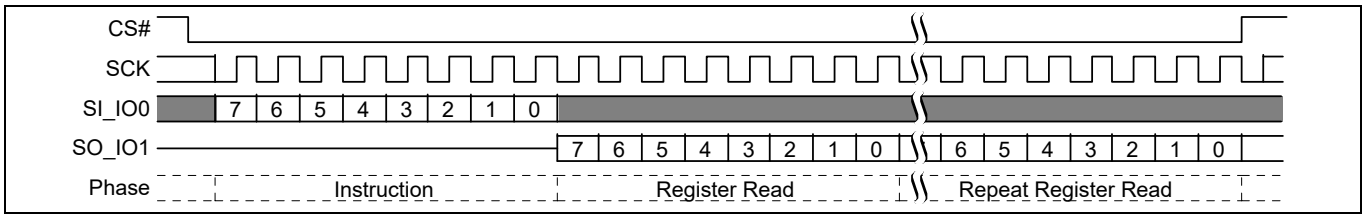


Figure 38 Read Configuration Register (RDCR1) (RDCR2) (RDCR3) command sequence

In QPI mode, configuration register 1, 2 and 3 may be read via the Read Any Register command, see **"Read Any Register (RDAR 65h)"** on page 90.

8.3.4 Write Registers (WRR 01h)

The Write Registers (WRR) command allows new values to be written to the Status Register 1, Configuration Register 1, Configuration Register 2 and Configuration Register 3. Before the Write Registers (WRR) command can be accepted by the device, a Write Enable (WREN) or Write Enable for Volatile Registers (WRENV) command must be received. After the Write Enable (WREN) command has been decoded successfully, the device will set the Write Enable Latch (WEL) in the Status Register to enable non-volatile write operations and direct the values in the following WRR command to the non-volatile SR1NV, CR1NV, CR2NV and CR3NV registers. After the Write Enable for Volatile Registers (WRENV) command has been decoded successfully, the device directs the values in the following WRR command to the volatile SR1V, CR1V, CR2V and CRV3 registers.

The Write Registers (WRR) command is entered by shifting the instruction and the data bytes on SI/IO0. The Status Register is one data byte in length.

A WRR operation directed to non-volatile registers by a preceding WREN command, first erases non-volatile registers then programs the new value as a single operation, then copies the new non-volatile values to the volatile version of the registers. A WRR operation directed to volatile registers by a preceding WRENV command, updates the volatile registers without affecting the related non-volatile register values. The Write Registers (WRR) command will set the P_ERR or E_ERR bits if there is a failure in the WRR operation. See **"Status Register 2 Volatile (SR2V)"** on page 38 for a description of the error bits. The device hangs busy until clear status register (CLSR) is used to clear the error and WIP for return to standby. Any Status or Configuration Register bit reserved for the future must be written as a '0'.

CS# must be driven to the logic high state after the eighth, sixteenth, twenty-fourth, or thirty-second bit of data has been latched. If not, the Write Registers (WRR) command is not executed. If CS# is driven high after the:

- eighth cycle then only the Status Register 1 is written
- sixteenth cycle both the Status 1 and Configuration 1 Registers are written;
- twenty-fourth cycle Status 1 and Configuration 1 and 2 Registers are written;
- thirty-second cycle Status 1and Configuration 1, 2 and 3 Registers are written.

As soon as CS# is driven to the logic high state, the self-timed Write Registers (WRR) operation is initiated. While the Write Registers (WRR) operation is in progress, the Status Register may still be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a '1' during the self-timed Write Registers (WRR) operation, and is a '0' when it is completed. When the Write Registers (WRR) operation is completed, the Write Enable Latch (WEL) is set to a '0'.

The WRR command is protected from a hardware and software reset, the hardware reset and software reset command are ignored and have no effect on the execution of the WRR command.

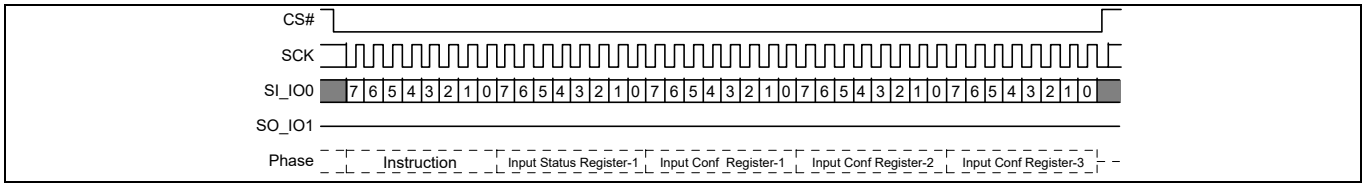


Figure 39 Write Registers (WRR) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction and data is shifted in on IO0–IO3.

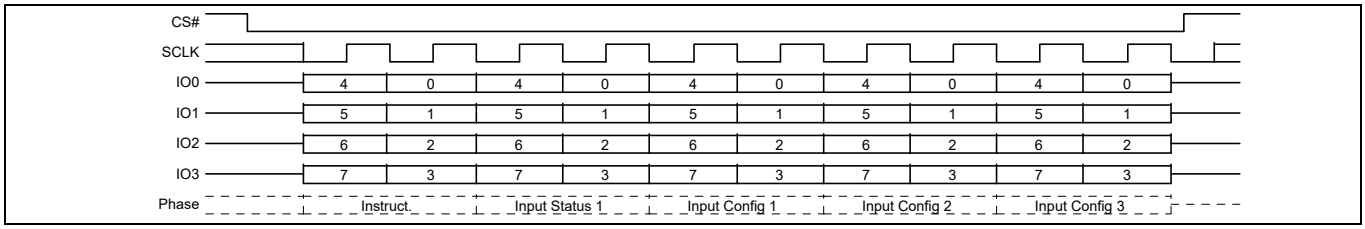


Figure 40 Write Register (WRR) command sequence QPI mode

The Write Registers (WRR) command allows the user to change the values of the Legacy Block Protection bits in either the non-volatile Status Register 1 or in the volatile Status Register 1, to define the size of the area that is to be treated as read-only.

The Write Registers (WRR) command also allows the user to set the Status Register Protect 0 (SRP0) bit to a ‘1’ or a ‘0’. The Status Register Protect 0 (SRP0) bit and Write Protect (WP#) signal allow the BP bits to be hardware protected.

When the Status Register Protect 0 (SRP0 SR1V[7]) bit is a ‘0’, it is possible to write to the Status Register provided that the WREN or WRENV command has previously been sent, regardless of whether Write Protect (WP#) signal is driven to the logic high or logic low state.

When the Status Register Protect 0 (SRP0) bit is set to a ‘1’, two cases need to be considered, depending on the state of Write Protect (WP#):

- If Write Protect (WP#) signal is driven to the logic high state, it is possible to write to the Status and Configuration Registers provided that the WREN or WRENV command has previously been sent before the WRR command.
- If Write Protect (WP#) signal is driven to the logic low state, it is not possible to write to the Status and Configuration Registers even if the WREN or WRENV command has previously been sent before the WRR command. Attempts to write to the Status and Configuration Registers are rejected, not accepted for execution, and no error indication is provided. As a consequence, all the data bytes in the memory area that are protected by the Legacy Block Protection bits of the Status Register, are also hardware protected by WP#.

The WP# hardware protection can be provided:

- by setting the Status Register Protect 0 (SRP0) bit after driving Write Protect (WP#) signal to the logic low state;
- or by driving Write Protect (WP#) signal to the logic low state after setting the Status Register Protect 0 (SRP0) bit to a ‘1’.

The only way to release the hardware protection is to pull the Write Protect (WP#) signal to the logic high state. If WP# is permanently tied high, hardware protection of the BP bits can never be activated.

Hardware protection is disabled when Quad Mode is enabled (CR1V[1] = 1) or QPI mode is enabled (CR2V[3] = 1) because WP# becomes IO2; therefore, it cannot be utilized.

See **“Status Register Protect (SRP1, SRP0)”** on page 56 for a table showing the SRP and WP# control of Status and Configuration protection.

8.3.5 Write Enable (WREN 06h)

The Write Enable (WREN) command sets the Write Enable Latch (WEL) bit of the Status Register 1 (SR1V[1]) to a '1'. The Write Enable Latch (WEL) bit must be set to a '1' by issuing the Write Enable (WREN) command to enable write, program and erase commands.

CS# must be driven into the logic high state after the eighth bit of the instruction byte has been latched in on SI/IO0. Without CS# being driven to the logic high state after the eighth bit of the instruction byte has been latched in on SI/IO0, the write enable operation will not be executed.

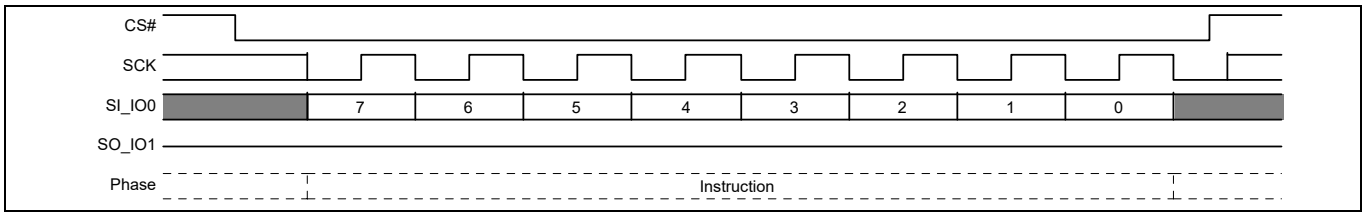


Figure 41 Write Enable (WREN) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

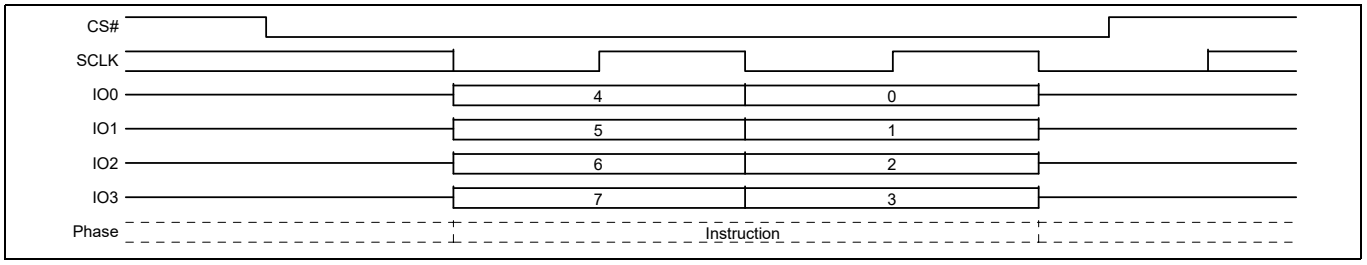


Figure 42 Write Enable (WREN) command sequence QPI mode

8.3.6 Write Disable (WRDI 04h)

The Write Disable (WRDI) command clears the Write Enable Latch (WEL) bit of the Status Register 1 (SR1V[1]) to a '0'.

The Write Enable Latch (WEL) bit may be cleared to a '0' by issuing the Write Disable (WRDI) command to disable Page Program (PP, 4PP, QPP, 4QPP), Sector Erase (SE), Half Block Erase (HBE), Block Erase (BE), Chip Erase (CE), Write Registers (WRR or WRAR), Security Region Erase (SECRE), Security Region Program (SECRP), and other commands, that require WEL be set to '1' for execution. The WRDI command can be used by the user to protect memory areas against inadvertent writes that can possibly corrupt the contents of the memory. The WRDI command is ignored during an embedded operation while WIP bit = 1.

CS# must be driven into the logic high state after the eighth bit of the instruction byte has been latched in on SI/IO0. Without CS# being driven to the logic high state after the eighth bit of the instruction byte has been latched in on SI/IO0, the write disable operation will not be executed.

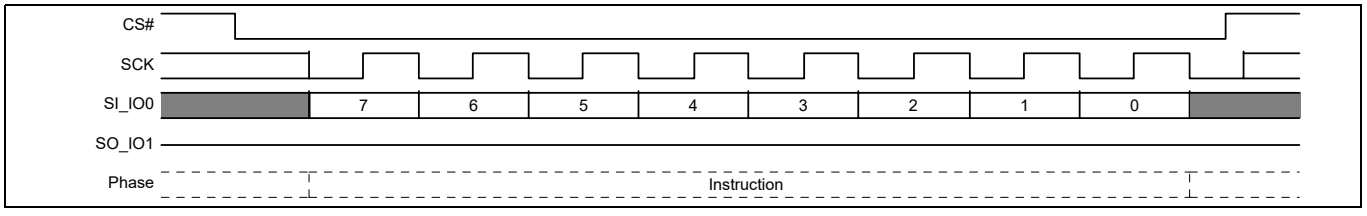


Figure 43 Write Disable (WRDI) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

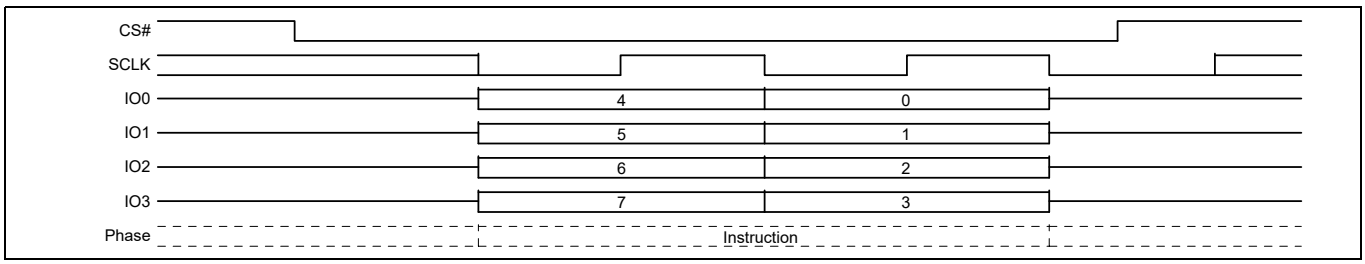


Figure 44 Write Disable (WRDI) command sequence QPI mode

8.3.7 Write Enable for Volatile Registers (WRENV 50h)

The volatile SR1V, CR1V, CR2V and CR3V registers described in **"Registers"** on page 32, can be written by sending the WRENV command followed by the WRR command. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the status or configuration non-volatile register bits. The WRENV command will not set the Write Enable Latch (WEL) bit, WRENV is used only to direct the following WRR command to change the volatile status and configuration register bit values.

CS# must be driven into the logic high state after the eighth bit of the instruction byte has been latched in on SI/IO0. Without CS# being driven to the logic high state after the eighth bit of the instruction byte has been latched in on SI/IO0, the write enable operation will not be executed.

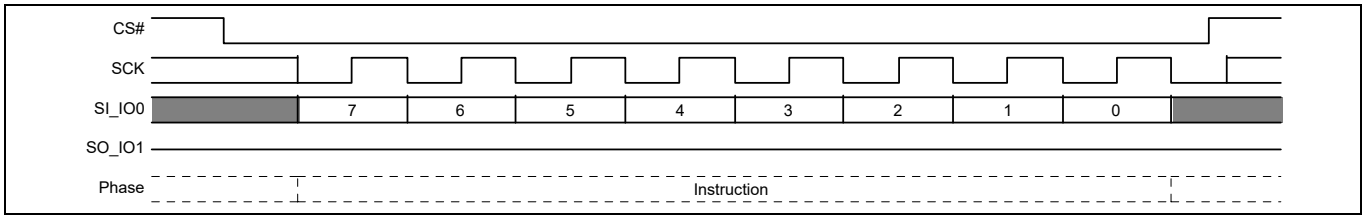


Figure 45 Write Enable for Volatile Registers (WRENV) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

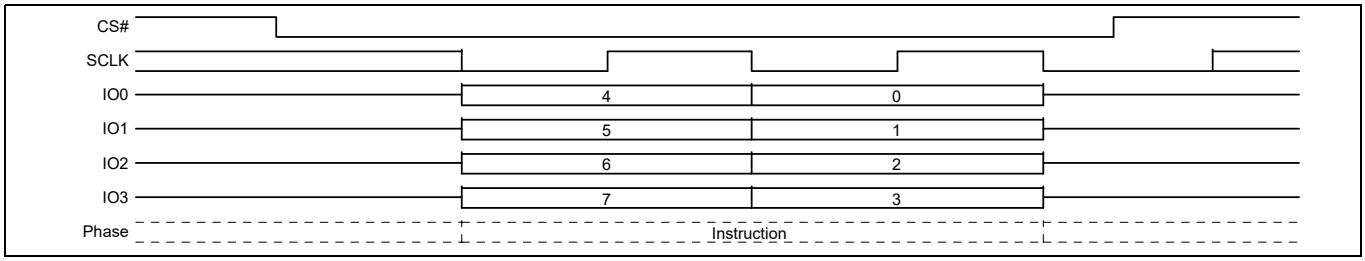


Figure 46 Write Enable for Volatile Registers (WRENV) command sequence QPI mode

8.3.8 Clear Status Register (CLSR 30h)

The Clear Status Register command clears the WIP (SR1V[0]), WEL (SR1V[1]), P_ERR (SR2V[5]), and E_ERR (SR2V[6]) bits to '0'. It is not necessary to set the WEL bit before a Clear Status Register command is executed. The Clear Status Register command will be accepted even when the device remains busy with WIP set to 1, as the device does remain busy when either error bit is set.

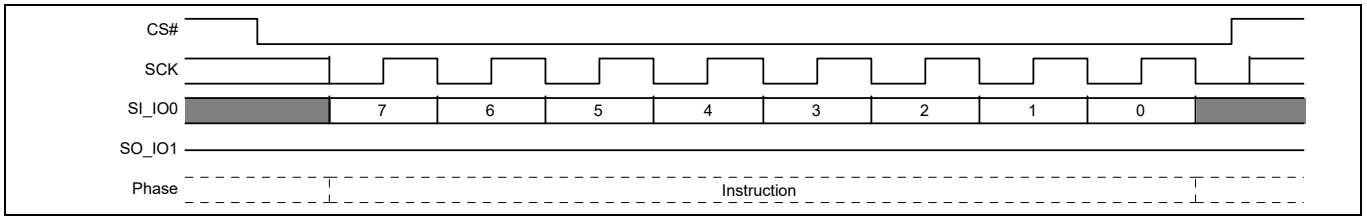


Figure 47 Clear Status Register (CLSR) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

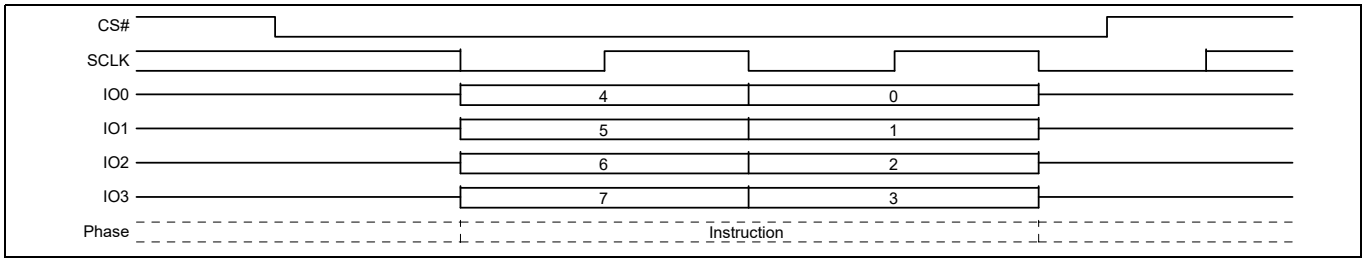


Figure 48 Clear Status Register (CLSR) QPI mode

8.3.9 Program DLRNV (PDLRNV 43h)

Before the Program DLRNV (PDLRNV) command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device. After the Write Enable (WREN) command has been decoded successfully, the device will set the Write Enable Latch (WEL) to enable the PDLRNV operation.

The PDLRNV command is entered by shifting the instruction and the data byte on SI/IO0.

CS# must be driven to the logic high state after the eighth (8th) bit of data has been latched. If not, the PDLRNV command is not executed. As soon as CS# is driven to the logic high state, the self-timed PDLRNV operation is initiated. While the PDLRNV operation is in progress, the Status Register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a '1' during the self-timed PDLRNV cycle, and a is 0 when it is completed. The PDLRNV operation can report a program error in the P_ERR bit of the status register. When the PDLRNV operation is completed, the Write Enable Latch (WEL) is set to a '0'. The maximum clock frequency for the PDLRNV command is 133 MHz.

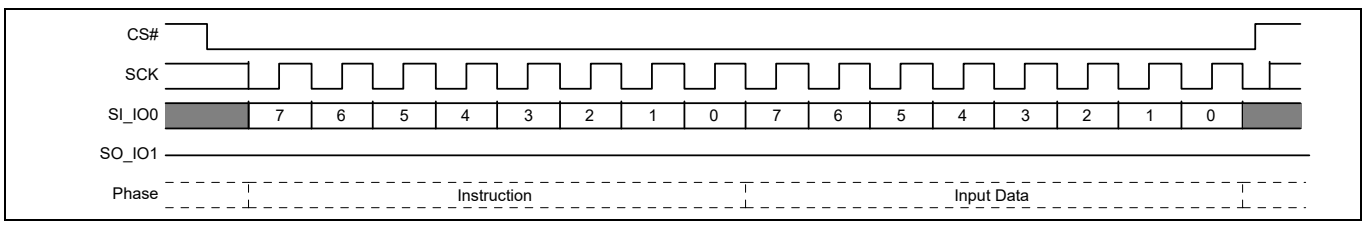


Figure 49 Program DLRNV (PDLRNV) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction and data is shifted in on IO0–IO3.

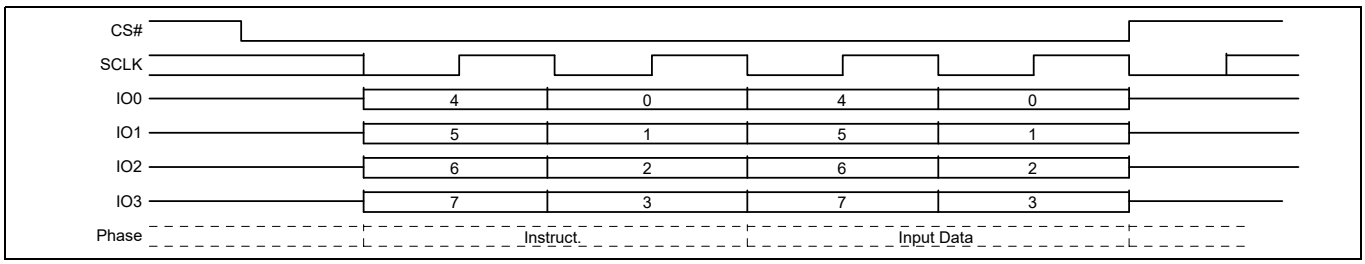


Figure 50 Program DLRNV (PDLRNV) command sequence – QPI mode

8.3.10 Write DLRV (WDLRV 4Ah)

Before the Write DLRV (WDLRV) command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device. After the Write Enable (WREN) command has been decoded successfully, the device will set the Write Enable Latch (WEL) to enable WDLRV operation.

The WDLRV command is entered by shifting the instruction and the data byte on SI/IO0.

CS# must be driven to the logic high state after the eighth (8th) bit of data has been latched. If not, the WDLRV command is not executed. As soon as CS# is driven to the logic high state, the WDLRV operation is initiated with no delays. The maximum clock frequency for the WDLRV command is 133 MHz.

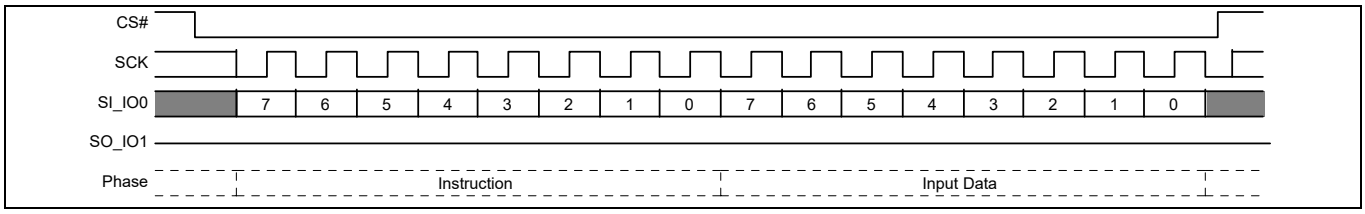


Figure 51 Write DLRV (WDLRV) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction and data is shifted in on IO0–IO3.

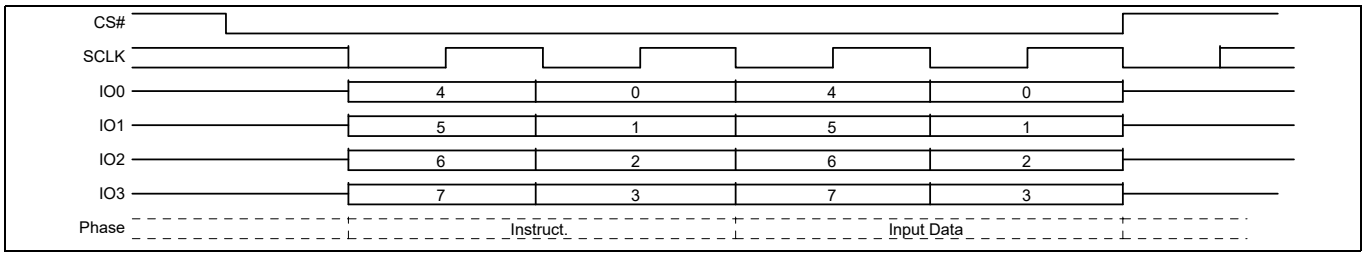


Figure 52 Write DLRV (WDLRV) command sequence – QPI mode

8.3.11 Data Learning Pattern Read (DLPRD 41h)

The instruction 41h is shifted into SI/IO0 by the rising edge of the SCK signal followed by one dummy cycle. This latency period allows the device's internal circuitry enough time to access data at the initial address. During latency cycles, the data value on IO0–IO3 are "don't care" and may be high impedance. Then the 8-bit DLP is shifted out on SO/IO1. It is possible to read the DLP continuously by providing multiples of eight clock cycles. The maximum operating clock frequency for the DLPRD command is 133 MHz.

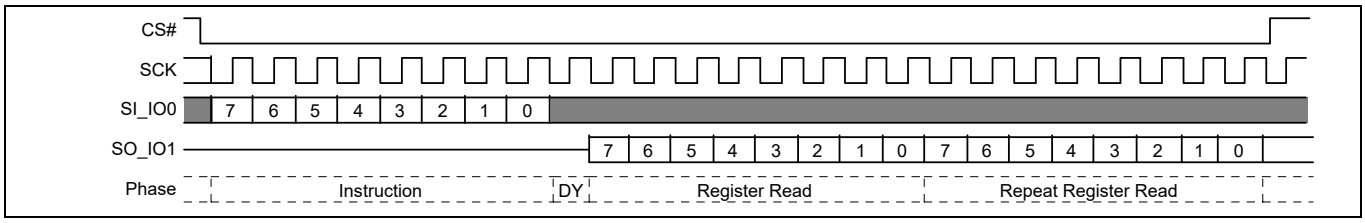


Figure 53 DLP Read (DLPRD) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in and returning data out on IO0–IO3.

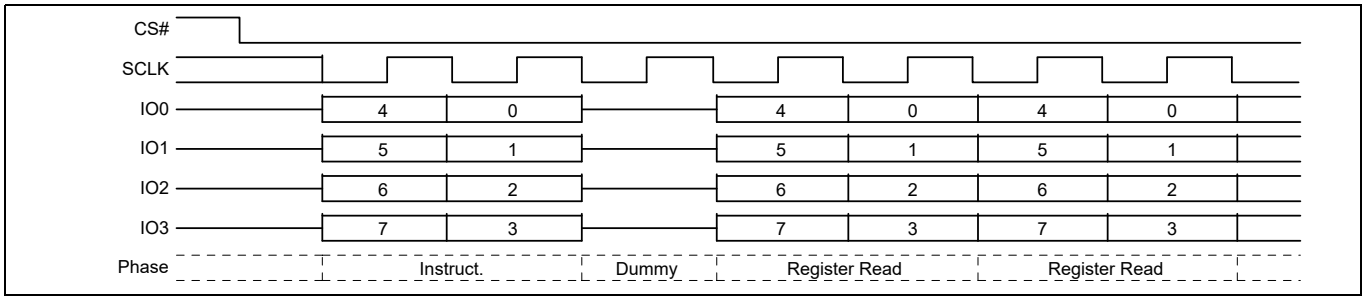


Figure 54 DLP Read (DLPRD) command sequence – QPI mode

8.3.12 Enter 4 Byte Address Mode (4BEN B7h)

The enter 4 Byte Address Mode (4BEN) command sets the volatile Address Length status (ADS) bit (CR2V[0]) to 1 to change all 3 Byte address commands to require 4 Bytes of address. This command will not affect 4 Byte only commands which will still continue to expect 4 Bytes of address.

To return to 3 Byte Address mode the 4BEX command clears the volatile Address Length bit CR2V[0] = 0). The WRAR command can also clear the volatile Address Length bit CR2V[0] = 0). Also, a hardware or software reset may be used to return to the 3 byte address mode if the non-volatile Address Length bit CR2NV[1] = 0.

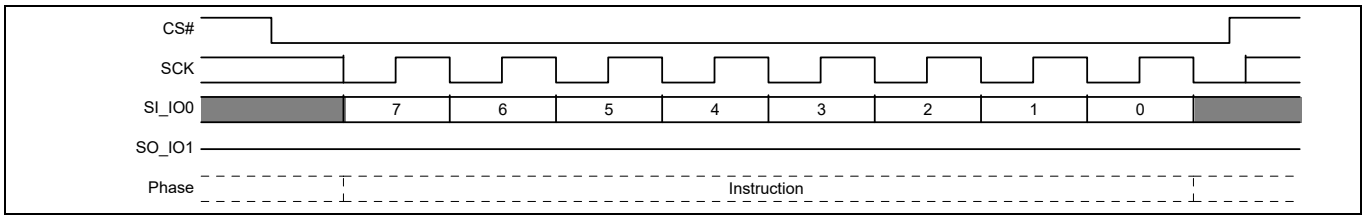


Figure 55 Enter 4 Byte Address Mode (4BEN B7h) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

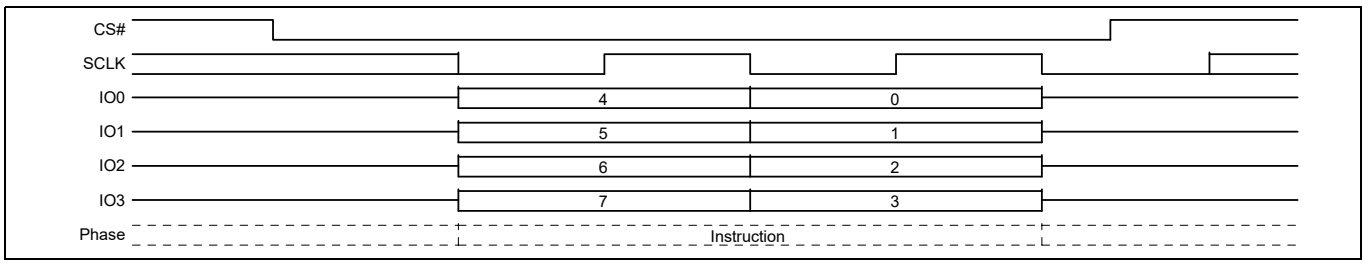


Figure 56 Enter 4 Byte Address QPI mode

8.3.13 Exit 4 Byte Address Mode (4BEX E9h)

The exit 4 Byte Address Mode (4BEX) command sets the volatile Address Length Status (ADS) bit (CR2V[0]) to 0 to change most 4 Byte address commands to require 3 Bytes of address. This command will not affect 4 Byte only commands which will still continue to expect 4 Bytes of address.

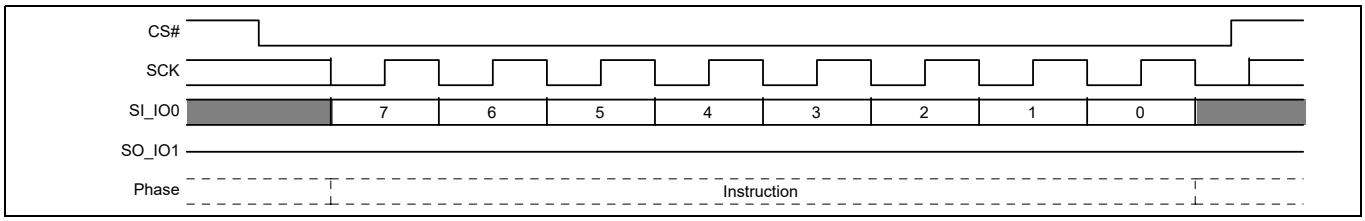


Figure 57 Exit 4 Byte Address Mode (4BEX E9h) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

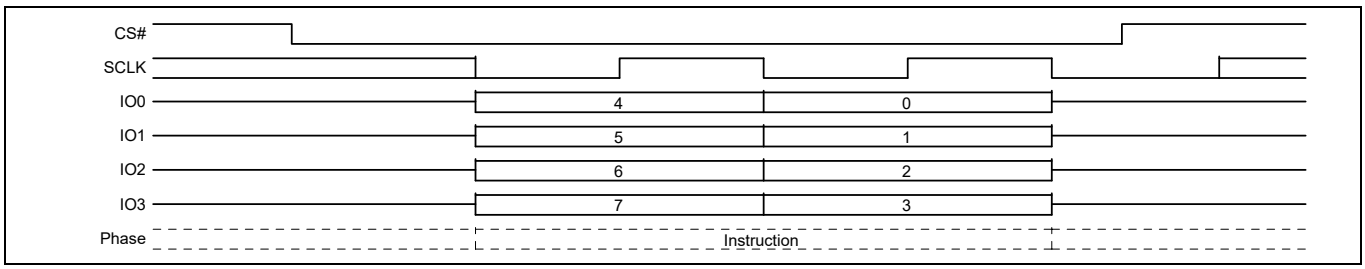


Figure 58 Exit 4 Byte Address QPI mode

8.3.14 Read Any Register (RDAR 65h)

The Read Any Register (RDAR) command provides a way to read device registers. The instruction is followed by a 3 or 4 Byte address (depending on the address length configuration CR2V[0]), followed by a number of latency (dummy) cycles set by CR3V[3:0]. Then the selected register contents are returned. If the read access is continued the same addressed register contents are returned until the command is terminated - only one register is read by each RDAR command.

Reading undefined locations provides undefined data.

The RDAR command may be used during embedded operations to read Status Register 1 (SR1V).

The RDAR command is not used for reading registers that act as a window into a larger array: IBLAR. There are separate commands required to select and read the location in the array accessed.

The RDAR command will read invalid data from the PASS register locations if the IRP Password protection mode is selected by programming IRP[2] to 0.

Table 42 Register address map

Byte address (Hex)	Register name	Description
000000	SR1NV	Non-volatile Status and Configuration Registers Reading of Non-volatile Status and Configuration Registers actually reads the volatile registers
000001	N/A	
000002	CR1NV	
000003	CR2NV	
000004	CR3NV	
000005	NVDLP	
...	N/A	N/A
000020	PASS[7:0]	Non-volatile Password Register
000021	PASS[15:8]	
000022	PASS[23:16]	
000023	PASS[31:24]	
000024	PASS[39:32]	
000025	PASS[47:40]	
000026	PASS[55:48]	
000027	PASS[63:56]	
...	N/A	N/A
000030	IRP[7:0]	Non-volatile
000031	IRP[15:8]	IRP Register
...	N/A	
000039	PRPR[A15:A8]	Pointer Region Protection Register A15:A8
00003A	PRPR[A23:A16]	Pointer Region Protection Register A23:A16
00003B	PRPR[A31:A24]	Pointer Region Protection Register A31:A24
...	N/A	N/A
800000	SR1V	Volatile Status and Configuration Registers
800001	SR2V	
800002	CR1V	
800003	CR2V	
800004	CR3V	
800005	VDLP	
...	N/A	N/A
800040	PR	Volatile Protection Register
...	N/A	N/A

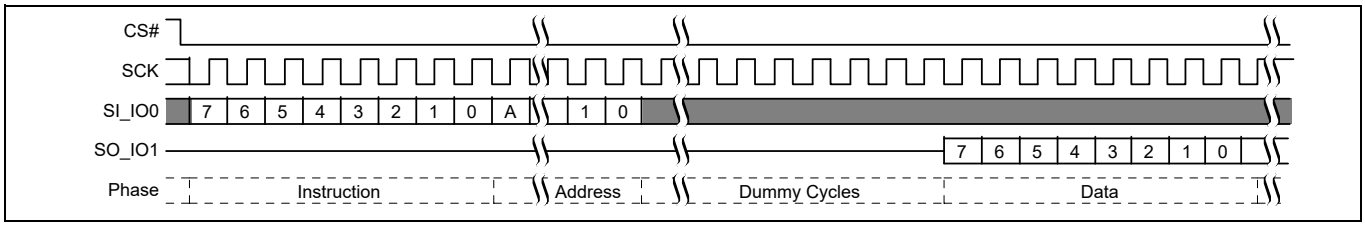


Figure 59 Read Any Register Read command sequence[31]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted in and returning data out on IO0–IO3.

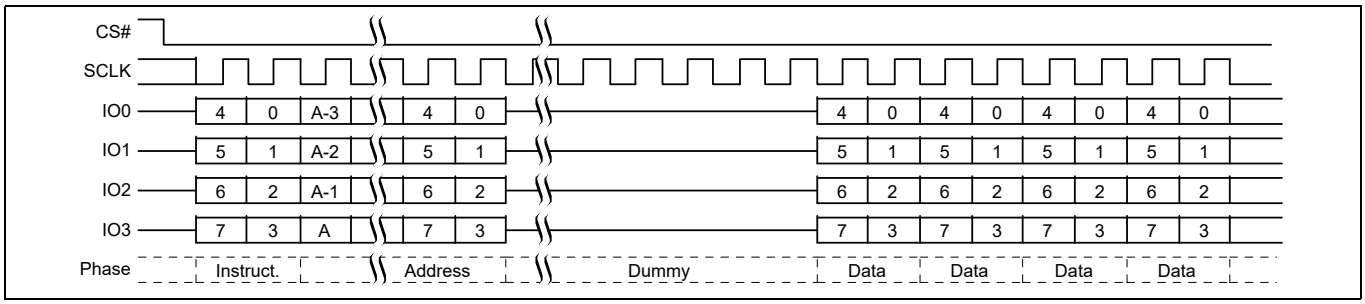


Figure 60 Read Any Register, QPI mode, command sequence[31]

Note
31.A = MSb of address = 23 for Address length CR2V[0] = 0, or 31 for CR2V[0] = 1.

8.3.15 Write Any Register (WRAR 71h)

The Write Any Register (WRAR) command provides a way to write any device register - non-volatile or volatile. The instruction is followed by a 3 or 4 Byte address (depending on the address length configuration CR2V[0]), followed by one byte of data to write in the address selected register.

The S25FL256L device must have 4 Byte addressing enabled (CR2V[0] = 1) to set the Pointer Region Protection register PRPR (see **"Pointer Region Protection Register (PRPR)"** on page 52).

Before the WRAR command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations. The WIP bit in SR1V may be checked to determine when the operation is completed. The P_ERR and E_ERR bits in SR2V may be checked to determine if any error occurred during the operation.

Some registers have a mixture of bit types and individual rules controlling which bits may be modified. Some bits are read only, some are OTP.

Read only bits are never modified and the related bits in the WRAR command data byte are ignored without setting a program or erase error indication (P_ERR or E_ERR in SR2V). Hence, the value of these bits in the WRAR data byte do not matter.

OTP bits may only be programmed to the level opposite of their default state. Writing of OTP bits back to their default state is ignored and no error is set.

Non-volatile bits which are changed by the WRAR data, require non-volatile register write time (t_W) to be updated. The update process involves an erase and a program operation on the non-volatile register bits. If either the erase or program portion of the update fails the related error bit in SR2V and WIP in SR1V will be set to 1.

Volatile bits which are changed by the WRAR data, require the volatile register write time (t_{CS}) to be updated.

Status Register 1 may be repeatedly read (polled) to monitor the Write-In-Progress (WIP) bit (SR1V[0]) to determine when the register write is completed and Status Register 2 for the error bits (SR2V[6,5]) to determine if there is write failure. If there is a write failure, the clear status command is used to clear the error status and enable the device to return to standby state. When the WRAR operation is completed, the Write Enable Latch (WEL) is set to a '0'.

However, the PR register can not be written by the WRAR command. The PR register contents are treated as read only bits. Only the NVLOCK Bit Write (PRL) command can write the PR register.

The WRAR command to write the SR1NV, CR1NV CR2NV and CR3NV is protected from a hardware and software reset, the WRAR command to all other register are reset from a hardware or software reset.

The WRAR command sequence and behavior is the same as the PP or 4PP command with only a single byte of data provided. See **"Page Program (PP 02h or 4PP 12H)"** on page 106.

The address map of the registers is the same as shown for **Table 42**.

8.3.16 Set Burst Length (SBL 77h)

The Set Burst Length (SBL) command is used to configure the Burst Wrap feature. Burst Wrap is used in conjunction with Quad I/O Read and DDR Quad I/O Read, in QIO or QPI modes, to access a fixed length and alignment of data. Certain applications can benefit from this feature by improving the overall system code execution performance. The Burst Wrap feature allows applications that use cache, to start filling a cache line with instruction or data from a critical address first, then fill the remainder of the cache line afterwards within a fixed length (8/16/32/64-bytes) of data, without issuing multiple read commands.

The Set Burst Length command is initiated by driving the CS# pin low and then shifting the instruction code “77h” followed by 24 dummy bits and 8 “Wrap Length Bits (WL[7]–WL[0])”. The command sequence is shown in **Figure 61** and **Figure 62**. Wrap Length bit WL[7] and the lower nibble WL[3:0] are not used. See Configuration Register 3 (CR3V[6:4]) for the encoding of WL[6]–WL[4] in **“Configuration Register 3”** on page 44.

Once WL[6:4] is set by a Set Burst Length command, all the following “Quad I/O Read” commands will use the WL[6:4] setting to access the 8/16/32/64-byte section of data. Note, Configuration Register 1 Quad bit CR1V[1] or Configuration Register 2 QPI bit CR2V[3] must be set to 1 in order to use the Quad I/O read and Set Burst Length commands. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap command should be issued to set WL4 = 1. The default value of WL[6:4] upon power on, hardware or software reset as set in the CR2NV[6:5]. Use WRR or WRAR command to set the default wrap length in CR2NV[6;2].

The Set Burst Length (SBL) command writes only to CR3V[6:4] bits to enable or disable the wrapped read feature and set the wrap boundary. The SBL command cannot be used to set the read latency in CR3V[3:0]. The WRAR command must be used to set the read latency in CR3V or CR3NV.

See **Table 43** for CR3V[6:5] values for wrap boundary’s and start address. When enabled the wrapped read feature changes the related read commands from sequentially reading until the command ends, to reading sequentially wrapped within a group of bytes.

When the wrap mode is not enabled (**Table 19** and **Table 22**), an unlimited length sequential read is performed.

When the wrap mode is enabled (**Table 19** and **Table 22**) a fixed length and aligned group of 8, 16, 32, or 64 bytes is read starting at the byte address provided by the read command and wrapping around at the group alignment boundary.

The group of bytes is of length and aligned on an 8, 16, 32, or 64 byte boundary. CR3V[6:5] selects the boundary. See **“Configuration Register 3 Volatile (CR3V)”** on page 48.

The starting address of the read command selects the group of bytes and the first data returned is the addressed byte. Bytes are then read sequentially until the end of the group boundary is reached. If the read continues the address wraps to the beginning of the group and continues to read sequentially. This wrapped read sequence continues until the command is ended by CS# returning high.

Table 43 Example burst wrap sequences

CR3V value (Hex)	Wrap boundary (Bytes)	Start address (Hex)	Address sequence (Hex)
1X	Sequential	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, ...
00	8	XXXXXX00	00, 01, 02, 03, 04, 05, 06, 07, 00, 01, 02, ...
00	8	XXXXXX07	07, 00, 01, 02, 03, 04, 05, 06, 07, 00, 01, ...
01	16	XXXXXX02	02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03, ...
01	16	XXXXXX0C	0C, 0D, 0E, 0F, 00, 01, 02, 03, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, ...
02	32	XXXXXX0A	0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, ...
02	32	XXXXXX1E	1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, ...
03	64	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02, ...
03	64	XXXXXX2E	2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D,, ...

The power-on reset, hardware reset, or software reset default burst length can be changed by programming CR3NV with the desired value using the WRAR command.

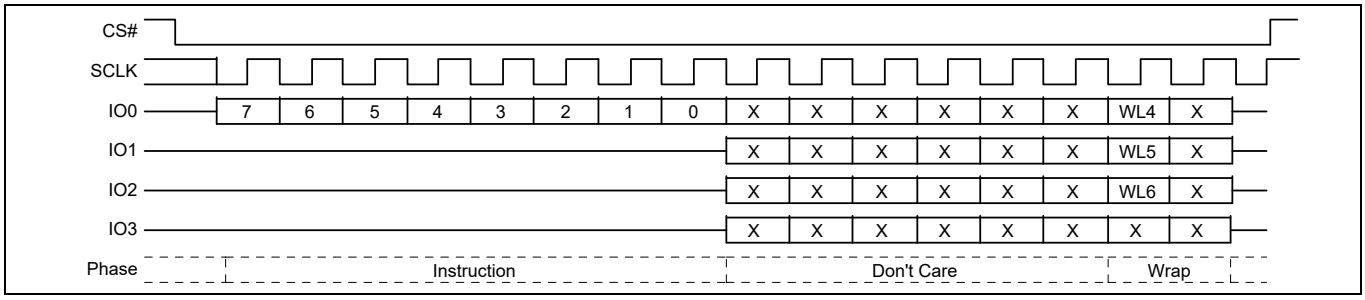


Figure 61 Set Burst Length command sequence quad I/O mode

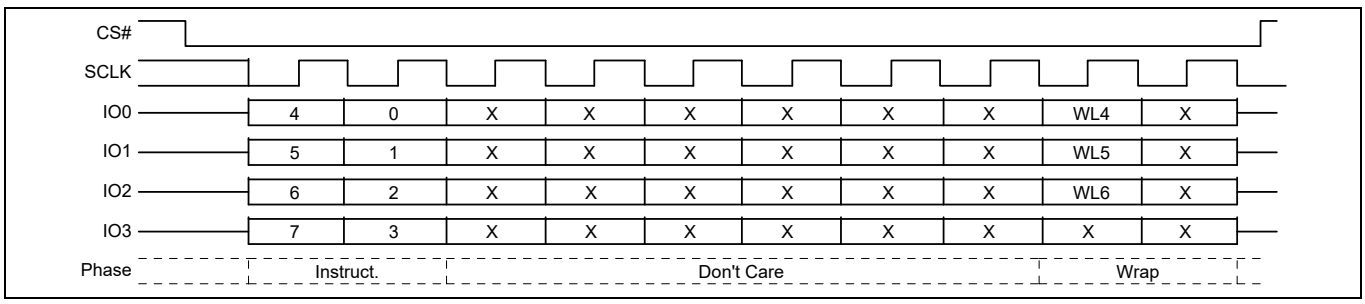


Figure 62 Set Burst Length command sequence QPI mode

8.3.17 Enter QPI Mode (QPIEN 38h)

The enter QPI Mode (QPIEN) command enables the QPI mode by setting the volatile QPI bit (CR2V[3] = 1). See **Table 16**. The time required to enter QPI Mode is t_{QEN}, see **Table 64**, no other commands are allowed during the t_{QEN} transition time to QPI mode.

To return to SPI mode the QPIEX command or a write to register (CR2V[3] = 0) is required. A power on reset, hardware, or software reset will also return the part to SPI mode if the Non-volatile QPI (CR2NV[3] = 0). See **Table 14**.

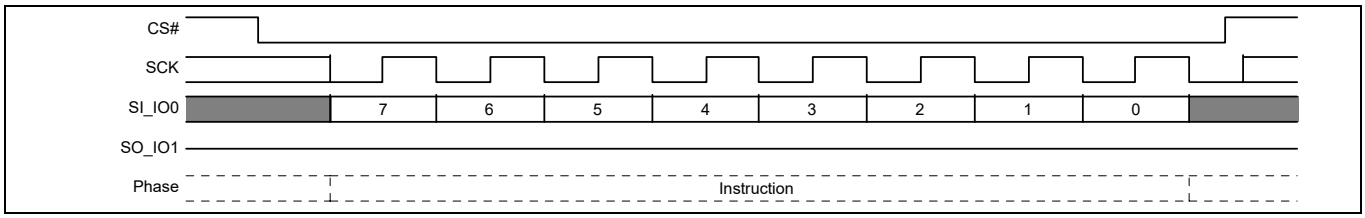


Figure 63 Enter QPI Mode (QPIEN 38h) command sequence

8.3.18 Exit QPI Mode (QPIEX F5h)

The exit QPI Mode (QPIEX) command disables the QPI mode by setting the volatile QPI bit (CR2V[3] = 0) and returning to SPI mode. See **Table 16**. The time required to exit QPI Mode is t_{QEX}, see **Table 64**, no other commands are allowed during the t_{QEX} transition time to exit the QPI mode.

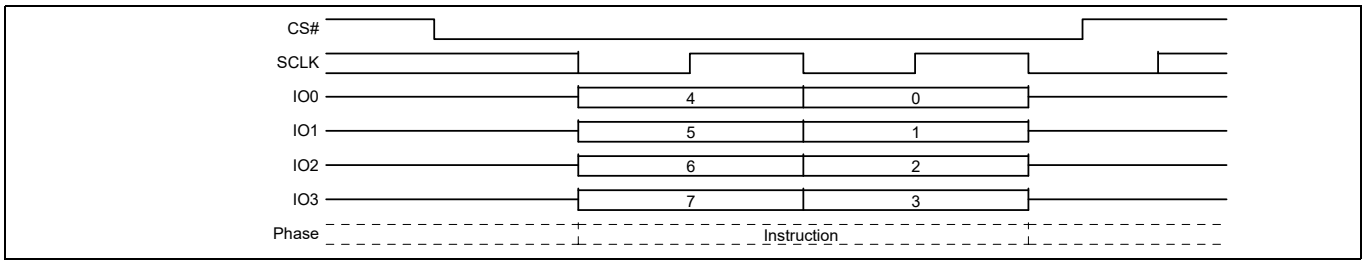


Figure 64 Exit QPI (QPIEX F5h) command sequence

8.4 Read Memory Array commands

Read commands for the main Flash array provide many options for prior generation SPI compatibility or enhanced performance SPI:

- Some commands transfer address or data on each rising edge of SCK. These are called Single Data Rate commands (SDR).
- Some SDR commands transfer address one bit per falling edge of SCK and return data 1-bit of data per rising edge of SCK. These are called Single width commands.
- Some SDR commands transfer both address and data 2- or 4-bits per rising edge of SCK. These are called Dual I/O for 2-bit, Quad I/O, and QPI for 4-bit. QPI also transfers instructions 4-bits per rising edge.
- Some commands transfer address and data on both the rising edge and falling edge of SCK. These are called Double Data Rate (DDR) commands.
- There are DDR commands for 4-bits of address or data per SCK edge. These are called Quad I/O DDR and QPI DDR for 4-bit per edge transfer.

All of these commands, except QPI Read, begin with an instruction code that is transferred one bit per SCK rising edge. QPI Read transfers the instruction 4-bits per SCK rising edge.The instruction is followed by either a 3 or 4 byte address transferred at SDR or DDR. Commands transferring address or data 2- or 4-bits per clock edge are called Multiple I/O (MIO) commands. For FL-L family devices at 256 Mb or higher density, the traditional SPI 3 byte addresses are unable to directly address all locations in the memory array. Separate 4 byte address read commands are provided for access to the entire address space. These devices may be configured to take a 4 byte address from the host system with the traditional 3 byte address commands. The 4 byte address mode for traditional commands is activated by setting the Address Length bit in configuration register 2 to ‘1’. In the S25FL128L higher order address bits above A23 in the 4 byte address commands, or commands using 4 byte Address mode are not relevant and are ignored because the Flash array is only 128 Mb in size.

The Dual I/O, Quad I/O and QPI commands provide a performance improvement option controlled by mode bits that are sent following the address bits. The mode bits indicate whether the command following the end of the current read will be another read of the same type, without an instruction at the beginning of the read. These mode bits give the option to eliminate the instruction cycles when doing a series of Dual or Quad read accesses.

Some commands require delay cycles following the address or mode bits to allow time to access the memory array - read latency. The delay or read latency cycles are traditionally called dummy cycles. The dummy cycles are ignored by the memory thus any data provided by the host during these cycles is “don’t care” and the host may also leave the SI signal at high impedance during the dummy cycles. When MIO commands are used the host must stop driving the IO signals (outputs are high impedance) before the end of last dummy cycle. When DDR commands are used the host must not drive the I/O signals during any dummy cycle. The number of dummy cycles varies with the SCK frequency or performance option selected via the Configuration Register 2 (CR3V[3:0]) Latency Code. Dummy cycles are measured from SCK falling edge to next SCK falling edge. SPI outputs are traditionally driven to a new value on the falling edge of each SCK. Zero dummy cycles means the returning data is driven by the memory on the same falling edge of SCK that the host stops driving address or mode bits.

The DDR commands may optionally have an 8 edge Data Learning Pattern (DLP) driven by the memory, on all data outputs, in the dummy cycles immediately before the start of data. The DLP can help the host memory controller determine the phase shift from SCK to data edges so that the memory controller can capture data at the center of the data eye.

When using SDR I/O commands at higher SCK frequencies (>50 MHz), an LC that provides 1 or more dummy cycles should be selected to allow additional time for the host to stop driving before the memory starts driving data, to minimize I/O driver conflict. When using DDR I/O commands with the DLP enabled, an LC that provides 5 or more dummy cycles should be selected to allow 1 cycle of additional time for the host to stop driving before the memory starts driving the 4 cycle DLP.

Each read command ends when CS# is returned High at any point during data return. CS# must not be returned High during the mode or dummy cycles before data returns as this may cause mode bits to be captured incorrectly; making it indeterminate as to whether the device remains in continuous read mode.

8.4.1 Read (Read 03h or 4READ 13h)

The instruction

- 03h (CR2V[0] = 0) is followed by a 3-byte address (A23–A0) or
- 03h (CR2V[0] = 1) is followed by a 4-byte address (A31–A0) or
- 13h is followed by a 4-byte address (A31–A0)

Then the memory contents, at the address given, are shifted out on SO/IO1.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

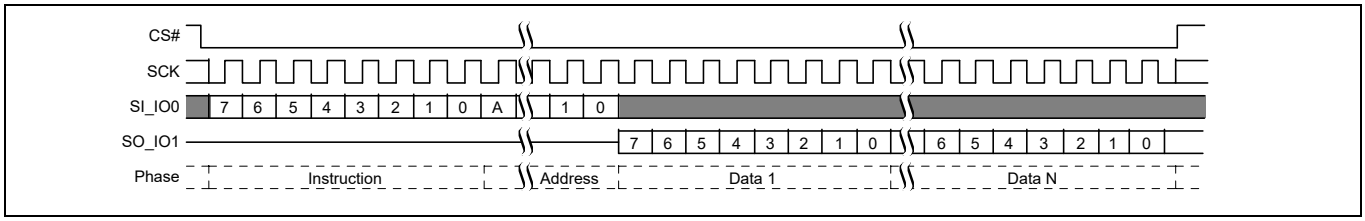


Figure 65 Read command sequence[32]

8.4.2 Fast Read (FAST_READ 0Bh or 4FAST_READ 0Ch)

The instruction

- 0Bh (CR2V[0] = 0) is followed by a 3-byte address (A23–A0) or
- 0Bh (CR2V[0] = 1) is followed by a 4-byte address (A31–A0) or
- 0Ch is followed by a 4-byte address (A31–A0)

The address is followed by dummy cycles depending on the latency code set in the Configuration Register CR3V[3:0]. The dummy cycles allow the device internal circuits additional time for accessing the initial address location. During the dummy cycles the data value on SO/IO1 is “don’t care” and may be high impedance. Then the memory contents, at the address given, are shifted out on SO/IO1.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

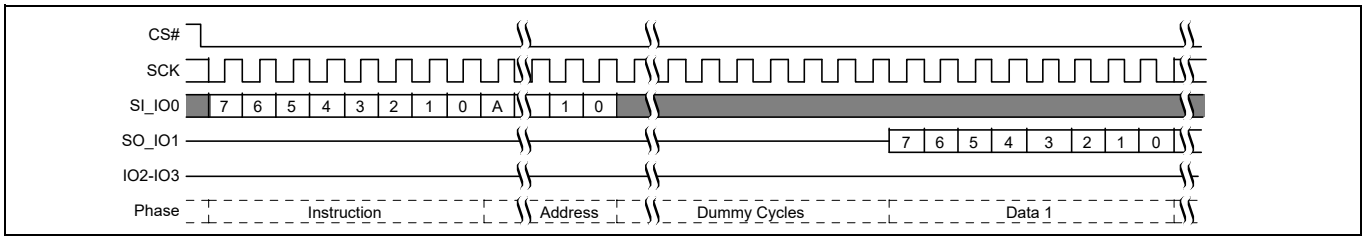


Figure 66 Fast Read (FAST_READ) command sequence[33]

Notes
32.A = MSb of address = 23 for CR2V[0] = 0, or 31 for CR2V[0] = 1 or command 13h.
33.A = MSb of address = 23 for CR2V[0] = 0, or 31 for CR2V[0] = 1 or command 0Ch.

8.4.3 Dual Output Read (DOR 3Bh or 4DOR 3Ch)

The instruction

- 3Bh (CR2V[0] = 0) is followed by a 3-byte address (A23–A0) or
- 3Bh (CR2V[0] = 1) is followed by a 4-byte address (A31–A0) or
- 3Ch is followed by a 4-byte address (A31–A0)

The address is followed by dummy cycles depending on the latency code set in the Configuration Register CR3V[3:0]. The dummy cycles allow the device internal circuits additional time for accessing the initial address location. During the dummy cycles the data value on IO0 (SI) and IO1 (S0) is “don’t care” and may be high impedance.

Then the memory contents, at the address given, is shifted out two bits at a time through IO0 (SI) and IO1 (SO). Two bits are shifted out at the SCK frequency by the falling edge of the SCK signal.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

For Dual Output Read commands, there are dummy cycles required after the last address bit is shifted into IO0 (SI) before data begins shifting out of IO0 and IO1.

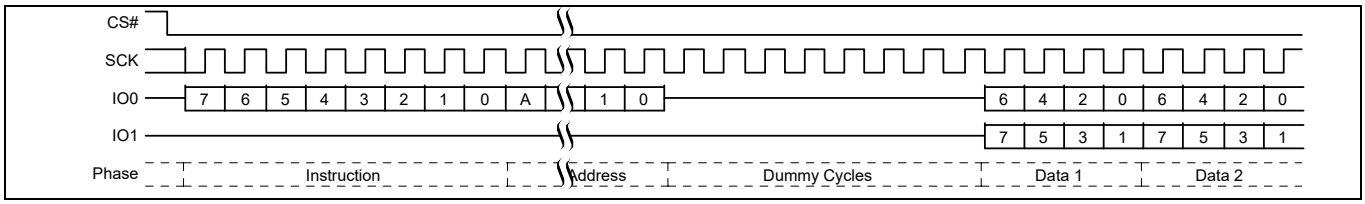


Figure 67 Dual Output Read command sequence[34]

8.4.4 Quad Output Read (QOR 6Bh or 4QOR 6Ch)

The instruction

- 6Bh (CR2V[0] = 0) is followed by a 3-byte address (A23–A0) or
- 6Bh (CR2V[0] = 1) is followed by a 4-byte address (A31–A0) or
- 6Ch is followed by a 4-byte address (A31–A0)

The address is followed by dummy cycles depending on the latency code set in the Configuration Register CR3V[3:0]. The dummy cycles allow the device internal circuits additional time for accessing the initial address location. During the dummy cycles the data value on IO0–IO3 is “don’t care” and may be high impedance.

Then the memory contents, at the address given, is shifted out four bits at a time through IO0–IO3. Each nibble (4 bits) is shifted out at the SCK frequency by the falling edge of the SCK signal.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

For Quad Output Read commands, there are dummy cycles required after the last address bit is shifted into IO0 before data begins shifting out of IO0–IO3.

Note
34.A = MSb of address = 23 for CR2V[0] = 0, or 31 for CR2V[0] = 1 or command 3Ch.

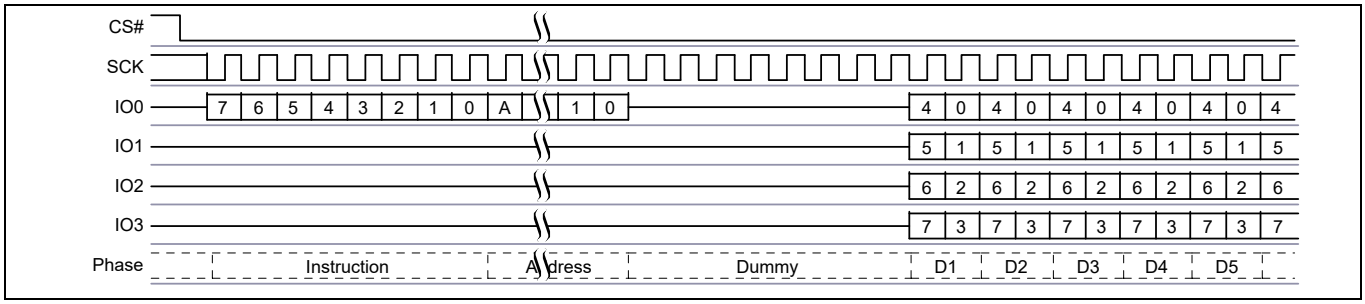


Figure 68 Quad Output Read command sequence[35]

8.4.5 Dual I/O Read (DIOR BBh or 4DIOR BCh)

The instruction

- BBh (CR2V[0] = 0) is followed by a 3-byte address (A23–A0) or
- BBh (CR2V[0] = 1) is followed by a 4-byte address (A31–A0) or
- BCh is followed by a 4-byte address (A31–A0)

The Dual I/O Read commands improve throughput with two I/O signals — IO0 (SI) and IO1 (SO). This command takes input of the address and returns read data two bits per SCK rising edge. In some applications, the reduced address input and data output time might allow for code execution in place (XIP) i.e. directly from the memory device.

The Dual I/O Read command has continuous read mode bits that follow the address so, a series of Dual I/O Read commands may eliminate the 8 bit instruction after the first Dual I/O Read command sends a mode bit pattern of Axh that indicates the following command will also be a Dual I/O Read command. The first Dual I/O Read command in a series starts with the 8 bit instruction, followed by address, followed by four cycles of mode bits, followed by an optional latency period. If the mode bit pattern is Axh the next command is assumed to be an additional Dual I/O Read command that does not provide instruction bits. That command starts with address, followed by mode bits, followed by optional latency.

Variable latency may be added after the mode bits are shifted into SI and SO before data begins shifting out of IO0 and IO1. This latency period (dummy cycles) allows the device internal circuitry enough time to access data at the initial address. During the dummy cycles, the data value on SI and SO are “don’t care” and may be high impedance. The number of dummy cycles is determined by the frequency of SCK. The latency is configured in CR3V[3:0].

The continuous read feature removes the need for the instruction bits in a sequence of read accesses and greatly improves code execution (XIP) performance. The upper nibble (bits 7–4) of the Mode bits control the length of the next Dual I/O Read command through the inclusion or exclusion of the first byte instruction code. The lower nibble (bits 3-0) of the Mode bits are “don’t care” (“x”) and may be high impedance. If the Mode bits equal Axh, then the device remains in Dual I/O Continuous Read Mode and the next address can be entered (after CS# is raised high and then asserted low) without the BBh or BCh instruction, as shown in **Figure 70**; thus, eliminating eight cycles of the command sequence. The following sequences will release the device from Dual I/O Continuous Read mode; after which, the device can accept standard SPI commands:

1. During the Dual I/O continuous read command sequence, if the Mode bits are any value other than Axh, then the next time CS# is raised high the device will be released from Dual I/O continuous read mode.
2. Send the Mode Reset command.

Note that the four mode bit cycles are part of the device’s internal circuitry latency time to access the initial address after the last address cycle that is clocked into IO0 (SI) and IO1 (SO).

Note
35.A = MSb of address = 23 for CR2V[0] = 0, or 31 for CR2V[0] = 1 or command 6Ch.

It is important that the I/O signals be set to high-impedance at or before the falling edge of the first data out clock. At higher clock speeds the time available to turn off the host outputs before the memory device begins to drive (bus turn around) is diminished. It is allowed and may be helpful in preventing I/O signal contention, for the host system to turn off the I/O signal outputs (make them high impedance) during the last two “don’t care” mode cycles or during any dummy cycles.

Following the latency period the memory content, at the address given, is shifted out two bits at a time through IO0 (SI) and IO1 (SO). Two bits are shifted out at the SCK frequency at the falling edge of SCK signal.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

CS# should not be driven high during mode or dummy bits as this may make the mode bits indeterminate.

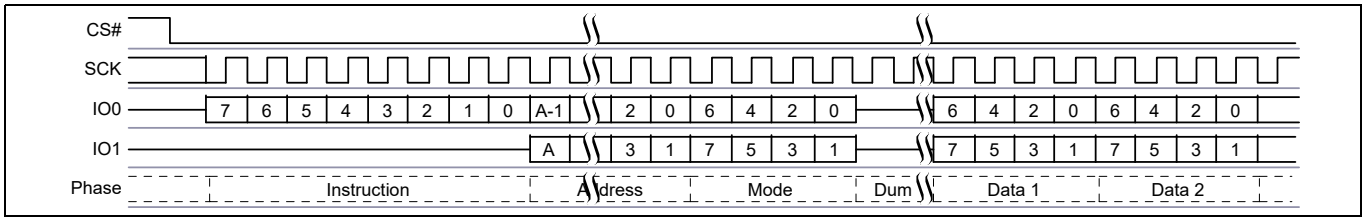


Figure 69 Dual I/O Read command sequence[36, 37]

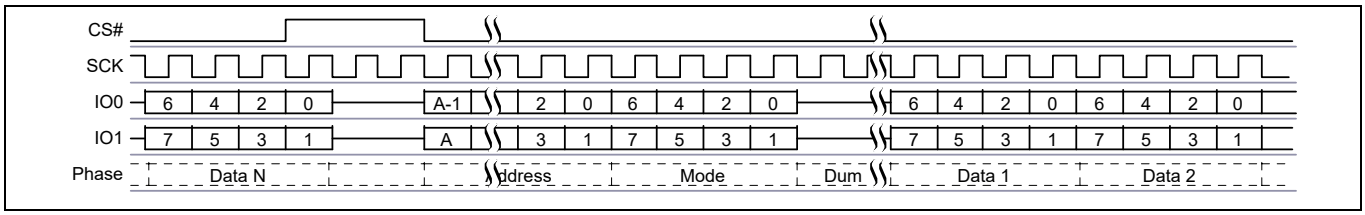


Figure 70 Dual I/O Continuous Read command sequence[36]

Notes

36.A = MSb of address = 23 for CR2V[0] = 0, or 31 for CR2V[0] = 1 or command BCh.

37.Least significant 4 bits of Mode are don’t care and it is optional for the host to drive these bits. The host may turn off drive during these cycles to increase bus turn around time between Mode bits from host and returning data from the memory.

8.4.6 Quad I/O Read (QIOR EBh or 4QIOR ECh)

The instruction,

- EBh (CR2V[0] = 0) is followed by a 3-byte address (A23–A0) or
- EBh (CR2V[0] = 1) is followed by a 4-byte address (A31–A0) or
- ECh is followed by a 4-byte address (A31–A0)

The Quad I/O Read command improves throughput with four I/O signals IO0-IO3. It allows input of the address bits four bits per serial SCK clock. In some applications, the reduced instruction overhead might allow for code execution (XIP) directly from FL-L family devices. The QUAD bit of the Configuration Register 1 must be set (CR1V[1] = 1) or the QPI bit of Configuration Register 2 must be set (CR2V[1] = 1 to enable the Quad capability of FL-L family devices.

For the Quad I/O Read command, there is a latency required after the mode bits (described below) before data begins shifting out of IO0–IO3. This latency period (i.e., dummy cycles) allows the device's internal circuitry enough time to access data at the initial address. During latency cycles, the data value on IO0–IO3 are "don't care" and may be high impedance. The number of dummy cycles is determined by the frequency of SCK. The latency is configured in CR3V[3:0].

Following the latency period, the memory contents at the address given, is shifted out four bits at a time through IO0–IO3. Each nibble (4 bits) is shifted out at the SCK frequency by the falling edge of the SCK signal.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

Address jumps can be done without the need for additional Quad I/O Read instructions. This is controlled through the setting of the Mode bits (after the address sequence, as shown in **Figure 71**. This added feature removes the need for the instruction sequence and greatly improves code execution (XIP). The upper nibble (bits 7–4) of the Mode bits control the length of the next Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble (bits 3-0) of the Mode bits are "don't care" ("x"). If the Mode bits equal Axh, then the device remains in Quad I/O High Performance Read Mode and the next address can be entered (after CS# is raised high and then asserted low) without requiring the EBh or ECh instruction, as shown in **Figure 73**; thus, eliminating eight cycles for the command sequence. The following sequences will release the device from Quad I/O High Performance Read mode; after which, the device can accept standard SPI commands:

1. During the Quad I/O Read Command Sequence, if the Mode bits are any value other than Axh, then the next time CS# is raised high the device will be released from Quad I/O High Performance Read mode.
2. Send the Mode Reset command.

Note that the two mode bit clock cycles and additional wait states (i.e., dummy cycles) allow the device's internal circuitry latency time to access the initial address after the last address cycle that is clocked into IO0–IO3.

It is important that the IO0–IO3 signals be set to high-impedance at or before the falling edge of the first data out clock. At higher clock speeds the time available to turn off the host outputs before the memory device begins to drive (bus turn around) is diminished. It is allowed and may be helpful in preventing IO0–IO3 signal contention, for the host system to turn off the IO0–IO3 signal outputs (make them high impedance) during the last "don't care" mode cycle or during any dummy cycles.

CS# should not be driven high during mode or dummy bits as this may make the mode bits indeterminate.

In QPI mode (CR2V[3] = 1), the Quad I/O instructions are sent 4-bits per SCK rising edge. The remainder of the command protocol is identical to the Quad I/O commands.

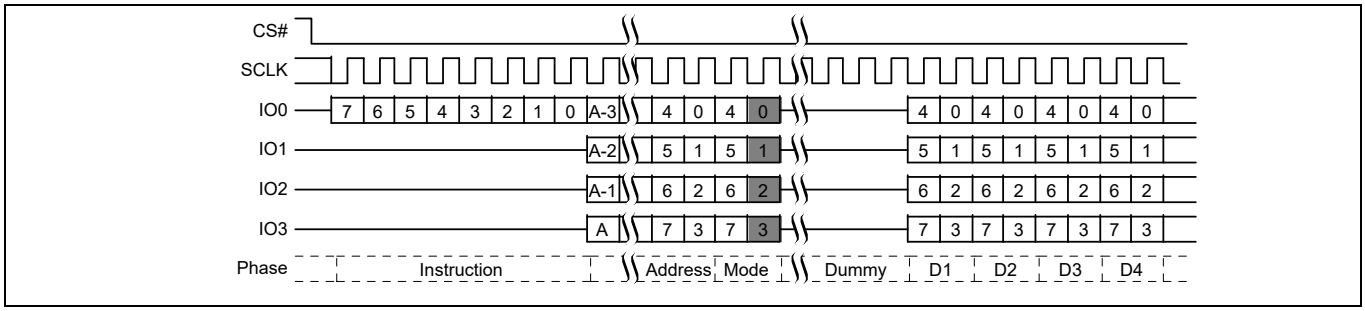


Figure 71 Quad I/O Read initial access command sequence[38]

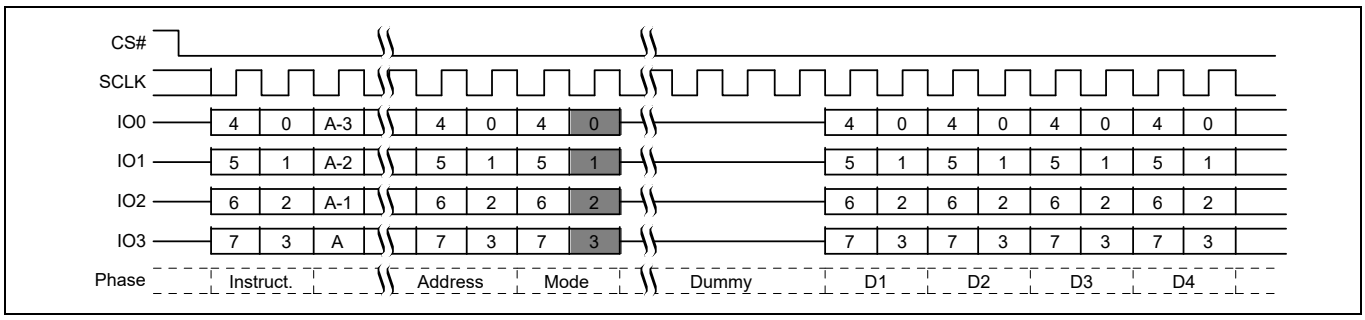


Figure 72 Quad I/O Read initial access command sequence QPI mode[38]

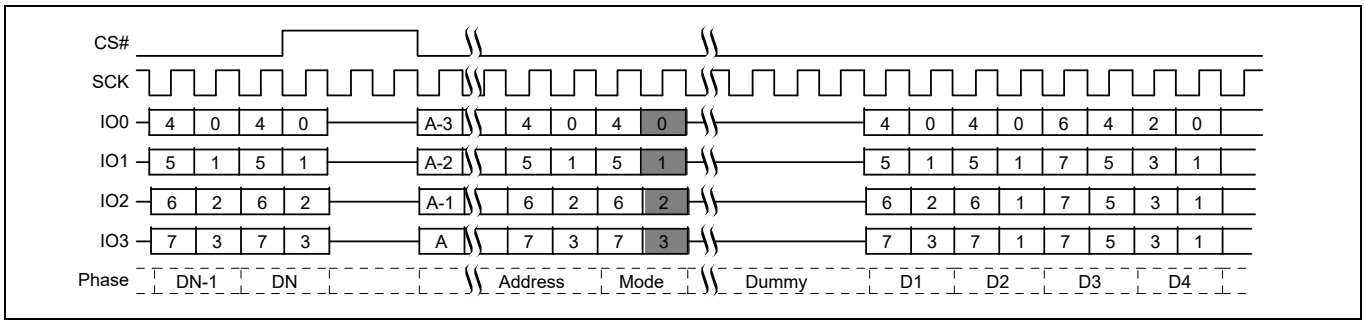


Figure 73 Continuous Quad I/O Read command sequence[38, 39]

Notes
38.A = MSb of address = 23 for CR2V[0] = 0, or 31 for CR2V[0] = 1 or command ECh.
39.The same sequence is used in QPI mode.

8.4.7 DDR Quad I/O Read (EDh, EEh)

The DDR Quad I/O Read command improves throughput with four I/O signals IO0-IO3. It is similar to the Quad I/O Read command but allows input of the address four bits on every edge of the clock. In some applications, the reduced instruction overhead might allow for code execution (XIP) directly from FL-L Family devices. The QUAD bit of the Configuration Register 1 must be set (CR1V[1] = 1) or the QPI bit of Configuration Register 2 must be set (CR2V[1] = 1 to enable the Quad capability of FL-L family devices.

The instruction

- EDh (CR2V[0] = 0) is followed by a 3-byte address (A23–A0) or
- EDh (CR2V[0] = 1) is followed by a 4-byte address (A31–A0) or
- EEh is followed by a 4-byte address (A31–A0)

The address is followed by mode bits. Then the memory contents, at the address given, is shifted out, in a DDR fashion, with four bits at a time on each clock edge through IO0–IO3.

The maximum operating clock frequency for DDR Quad I/O Read command is 66 MHz.

For DDR Quad I/O Read, there is a latency required after the last address and mode bits are shifted into the IO0–IO3 signals before data begins shifting out of IO0–IO3. This latency period (dummy cycles) allows the device's internal circuitry enough time to access the initial address. During these latency cycles, the data value on IO0–IO3 are "don't care" and may be high impedance. When the Data Learning Pattern (DLP) is enabled the host system must not drive the IO signals during the dummy cycles. The IO signals must be left high impedance by the host so that the memory device can drive the DLP during the dummy cycles.

The number of dummy cycles is determined by the frequency of SCK. The latency is configured in CR3V[3:0].

Mode bits allow a series of Quad I/O DDR commands to eliminate the 8 bit instruction after the first command sends a complementary mode bit pattern. This feature removes the need for the eight bit SDR instruction sequence and dramatically reduces initial access times (improves XIP performance). The Mode bits control the length of the next DDR Quad I/O Read operation through the inclusion or exclusion of the first byte instruction code. If the upper nibble (IO[7:4]) and lower nibble (IO[3:0]) of the Mode bits are complementary (i.e. 5h and Ah) the device transitions to Continuous DDR Quad I/O Read Mode and the next address can be entered (after CS# is raised high and then asserted low) without requiring the EDh or EEh instruction, thus eliminating eight cycles from the command sequence. The following sequences will release the device from Continuous DDR Quad I/O Read mode; after which, the device can accept standard SPI commands:

1. During the DDR Quad I/O Read Command Sequence, if the Mode bits are not complementary the next time CS# is raised high and then asserted low the device will be released from DDR Quad I/O Read mode.
2. Send the Mode Reset command.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

CS# should not be driven high during mode or dummy bits as this may make the mode bits indeterminate. Note that the memory devices may drive the IOs with a preamble prior to the first data value. The preamble is a Data Learning Pattern (DLP) that is used by the host controller to optimize data capture at higher frequencies. The preamble drives the IO bus for the four clock cycles immediately before data is output. The host must be sure to stop driving the IO bus prior to the time that the memory starts outputting the preamble.

The preamble is intended to give the host controller an indication about the round trip time from when the host drives a clock edge to when the corresponding data value returns from the memory device. The host controller will skew the data capture point during the preamble period to optimize timing margins and then use the same skew time to capture the data during the rest of the read operation. The optimized capture point will be determined during the preamble period of every read operation. This optimization strategy is intended to compensate for both the PVT (process, voltage, temperature) of both the memory device and the host controller as well as any system level delays caused by flight time on the PCB.

Although the data learning pattern (DLP) is programmable, the following example shows example of the DLP of 34h. The DLP 34h (or 00110100) will be driven on each of the active outputs (i.e. all four IOs). This pattern was chosen to cover both “DC” and “AC” data transition scenarios. The two DC transition scenarios include data low for a long period of time (two half clocks) followed by a high going transition (001) and the complementary low going transition (110). The two AC transition scenarios include data low for a short period of time (one half clock) followed by a high going transition (101) and the complementary low going transition (010). The DC transitions will typically occur with a starting point closer to the supply rail than the AC transitions that may not have fully settled to their steady state (DC) levels. In many cases the DC transitions will bound the beginning of the data valid period and the AC transitions will bound the ending of the data valid period. These transitions will allow the host controller to identify the beginning and ending of the valid data eye. Once the data eye has been characterized the optimal data capture point can be chosen. In QPI mode (CR2V[3] = 1) the DDR Quad I/O instructions are sent 4-bits at SCK rising edge. The remainder of the command protocol is identical to the DDR Quad I/O commands.

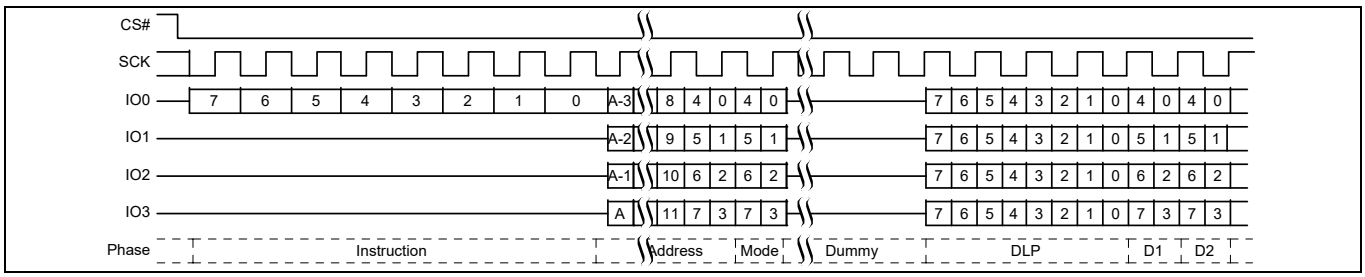


Figure 74 DDR Quad I/O Read initial access[40, 42]

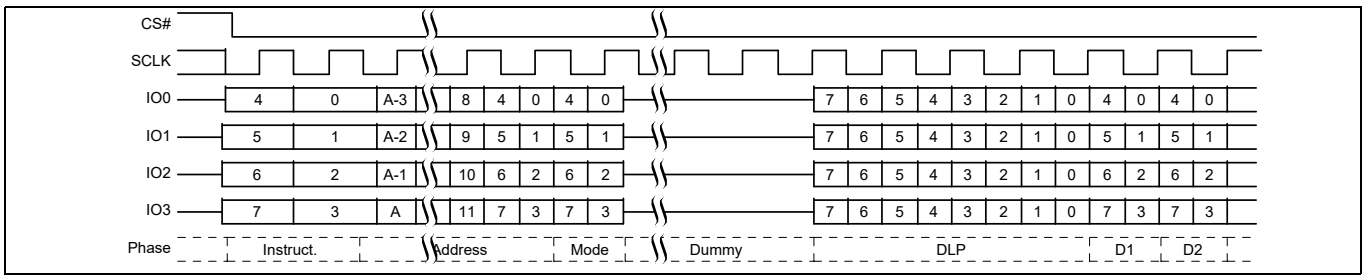


Figure 75 DDR Quad I/O Read initial access QPI mode[40, 42]

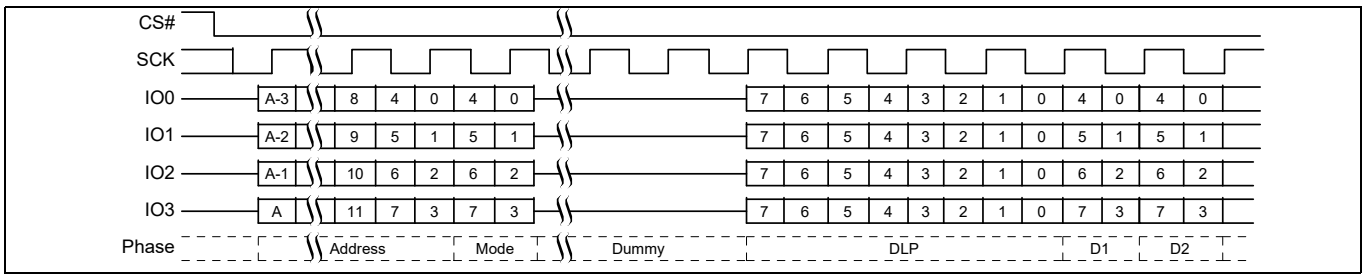


Figure 76 Continuous DDR Quad I/O Read subsequent access[40, 41, 42]

Notes
40.A = MSb of address = 23 for CR2V[0] = 0, or 31 for CR2V[0] = 1 or command EEh.
41.The same sequence is used in QPI mode.
42.Example DLP of 34h (or 00110100).

8.5 Program Flash Array commands

8.5.1 Program granularity

8.5.1.1 Page programming

Page Programming is done by loading a Page Buffer with data to be programmed and issuing a programming command to move data from the buffer to the memory array. This sets an upper limit on the amount of data that can be programmed with a single programming command. Page Programming allows up to a page size 256 bytes to be programmed in one operation. The page is aligned on the page size address boundary. It is possible to program from one bit up to a page size in each Page programming operation. For the very best performance, programming should be done in full pages of 256 bytes aligned on 256 byte boundaries with each Page being programmed only once.

8.5.1.2 Single byte programming

Single Byte Programming allows full backward compatibility to the legacy standard SPI Page Programming (PP) command by allowing a single byte to be programmed anywhere in the memory array.

8.5.2 Page Program (PP 02h or 4PP 12H)

The Page Program (PP) command allows bytes to be programmed in the memory (changing bits from 1 to 0). Before the Page Program (PP) commands can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device. After the Write Enable (WREN) command has been decoded successfully, the device sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The instruction

- 02h (CR2V[0] = 0) is followed by a 3-byte address (A23–A0) or
- 02h (CR2V[0] = 1) is followed by a 4-byte address (A31–A0) or
- 12h is followed by a 4-byte address (A31–A0)

and at least one data byte on SI/IO0. Up to a page can be provided on SI/IO0 after the 3-byte address with instruction 02h or 4-byte address with instruction 12h has been provided. As with the write and erase commands, the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program command will not be executed. After CS# is driven high, the self-timed Page Program command will commence for a time duration of t_{PP}.

Using the Page Program (PP) command to load an entire page, within the page boundary, will save overall programming time versus loading less than a page into the program buffer.

The programming process is managed by the Flash memory device internal control logic. After a programming command is issued, the programming operation status can be checked using the Read Status Register 1 command. The WIP bit (SR1V[0]) will indicate when the programming operation is completed. The P_ERR bit (SR2V[5]) will indicate if an error occurs in the programming operation that prevents successful completion of programming. This includes attempted programming of a protected area.

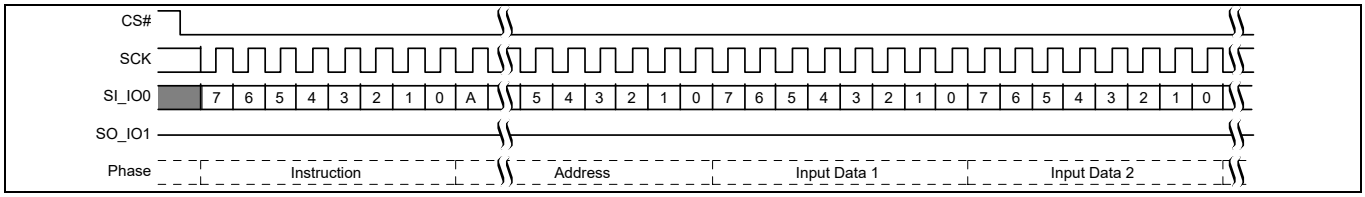


Figure 77 Page Program (PP 02h or 4PP 12h) command sequence[43]

Note
43.A = MSb of address = A23 for PP 02h with CR2V[0] = 0, or A31 for PP 02h with CR2V[0] = 1, or for 4PP 12h.

This command is also supported in QPI mode. In QPI mode, the instruction, address and data is shifted in on IO0–IO3.

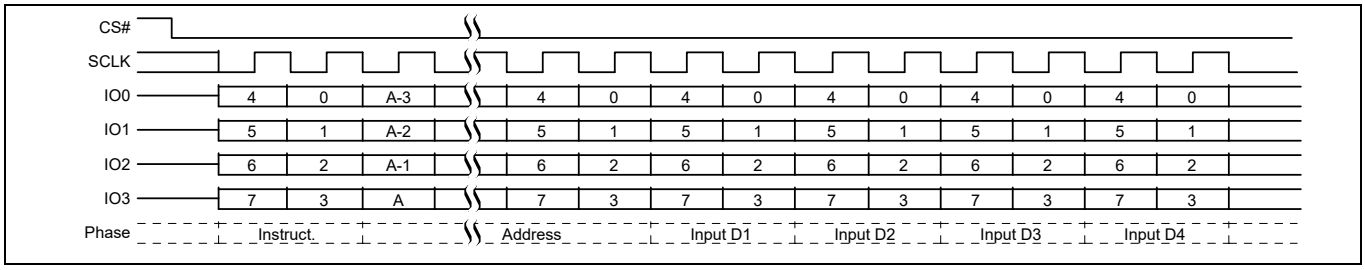


Figure 78 Page Program (PP 02h or 4PP 12h) QPI mode command sequence[44]

8.5.3 Quad Page Program (QPP 32h or 4QPP 34h)

The Quad-input Page Program (QPP) command allows bytes to be programmed in the memory (changing bits from 1 to 0). The Quad-input Page Program (QPP) command allows up to a page of data to be loaded into the Page Buffer using four signals: IO0–IO3. QPP can improve performance for PROM Programmer and applications that have slower clock speeds (< 12 MHz) by loading 4 bits of data per clock cycle. Systems with faster clock speeds do not realize as much benefit for the QPP command since the inherent page program time becomes greater than the time it takes to clock-in the data. The maximum frequency for the QPP command is 133 MHz.

To use Quad Page Program the Quad Enable Bit in the Configuration Register must be set (QUAD = 1). A Write Enable command must be executed before the device will accept the QPP command (Status Register 1, WEL = 1).

The instruction

- 32h (CR2V[0] = 0) is followed by a 3-byte address (A23–A0) or
- 32h (CR2V[0] = 1) is followed by a 4-byte address (A31–A0) or
- 34h is followed by a 4-byte address (A31–A0)

and at least one data byte, into the IO signals. Data must be programmed at previously erased (FFh) memory locations.

All other functions of QPP are identical to Page Program. The QPP command sequence is shown in the figure below.

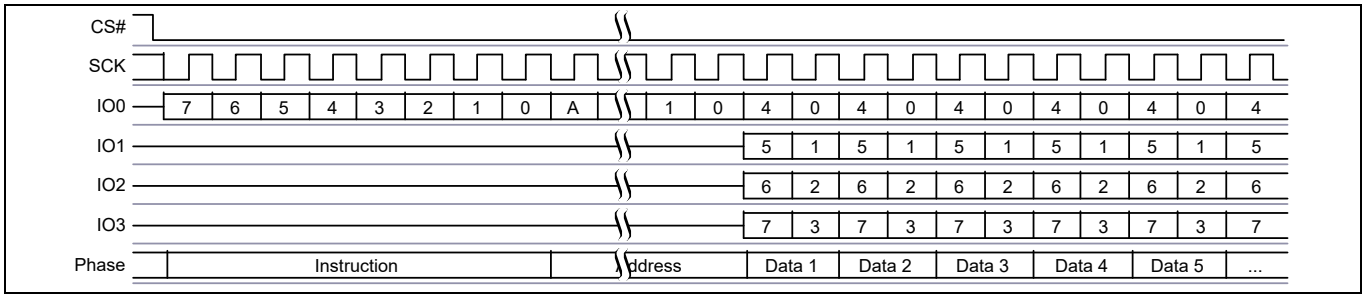


Figure 79 Quad page program command sequence[45]

Notes
44.A = MSb of address = A23 for PP 02h with CR2V[0] = 0, or A31 for PP 02h with CR2V[0] = 1, or for 4PP 12h.
45.A = MSb of address = A23 for QPP 32h with CR2V[0] = 0, or A31 for QPP 32h with CR2V[0] = 1, or for 4QPP 34h.

8.6 Erase Flash Array commands

8.6.1 Sector Erase (SE 20h or 4SE 21h)

The Sector Erase (SE) command sets all bits in the addressed sector to 1 (all bytes are FFh). Before the Sector Erase (SE) command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The instruction

- 20h [CR2V[0] = 0] is followed by a 3-byte address (A23–A0), or
- 20h [CR2V[0] = 1] is followed by a 4-byte address (A31–A0), or
- 21h is followed by a 4-byte address (A31–A0)

CS# must be driven into the logic high state after the twenty-fourth or thirty-second bit of the address has been latched in on SI/IO0. This will initiate the beginning of internal erase cycle, which involves the pre-programming and erase of the chosen sector of the flash memory array. If CS# is not driven high after the last bit of address, the sector erase operation will not be executed.

As soon as CS# is driven high, the internal erase cycle will be initiated. With the internal erase cycle in progress, the user can read the value of the Write-In Progress (WIP) bit to determine when the operation has been completed. The WIP bit will indicate a '1'. when the erase cycle is in progress and a '0' when the erase cycle has been completed.

A SE or 4SE command applied to a sector that has been write protected through the Legacy Block Protection, Individual Block Lock or Pointer Region Protection will not be executed and will set the E_ERR status.

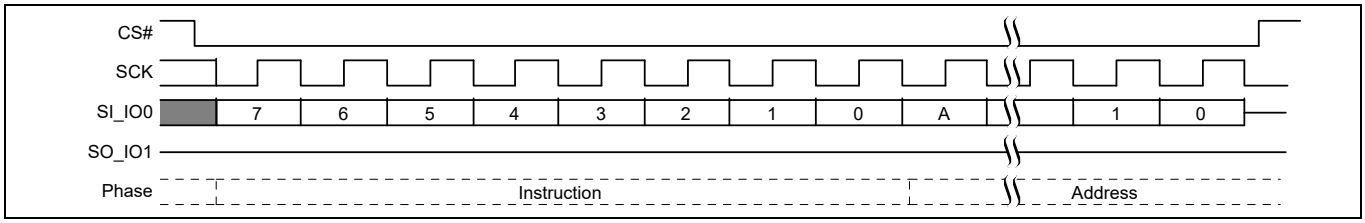


Figure 80 Sector Erase (SE 20h or 4SE 21h) command sequence[46]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted in on IO0–IO3.

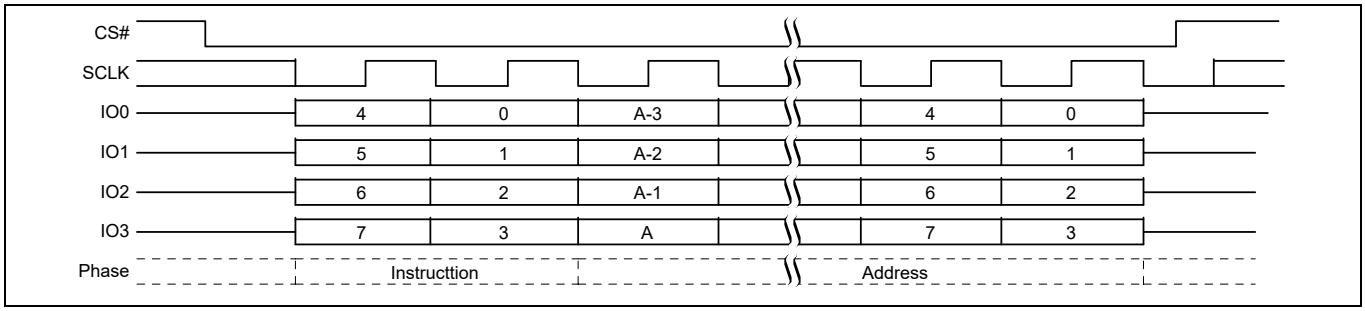


Figure 81 Sector Erase (SE 20h or 4SE 21h) QPI mode command sequence[46]

Note
46.A = MSb of address = A23 for SE 20h with CR2V[0] = 0, or A31 for SE 20h with CR2V[0] = 1 or for 4SE 21h.

8.6.2 Half Block Erase (HBE 52h or 4HBE 53h)

The Half Block Erase (HBE) command sets all bits in the addressed half block to 1 (all bytes are FFh). Before the Half Block Erase (HBE) command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The instruction

- 52h [CR2V[0] = 0] is followed by a 3-byte address (A23–A0), or
- 52h [CR2V[0] = 1] is followed by a 4-byte address (A31–A0), or
- 53h is followed by a 4-byte address (A31–A0)

CS# must be driven into the logic high state after the twenty-fourth or thirty-second bit of address has been latched in on SI/IO0. This will initiate the erase cycle, which involves the pre-programming and erase of each sector of the chose block. If CS# is not driven high after the last bit of address, the half block erase operation will not be executed.

As soon as CS# is driven into the logic high state, the internal erase cycle will be initiated. With the internal erase cycle in progress, the user can read the value of the Write-In Progress (WIP) bit to check if the operation has been completed. The WIP bit will indicate a '1' when the erase cycle is in progress and a '0' when the erase cycle has been completed.

A Half Block Erase (HBE) command applied to a Block that has been Write Protected through the Legacy Block Protection, Individual Block Lock or Pointer Region Protection will not be executed and will set the E_ERR status.

If a half block erase command is applied and if any region, sector or block in the half block erase area is protected the erase will not be executed on the 32 KB range and will set the E_ERR status.

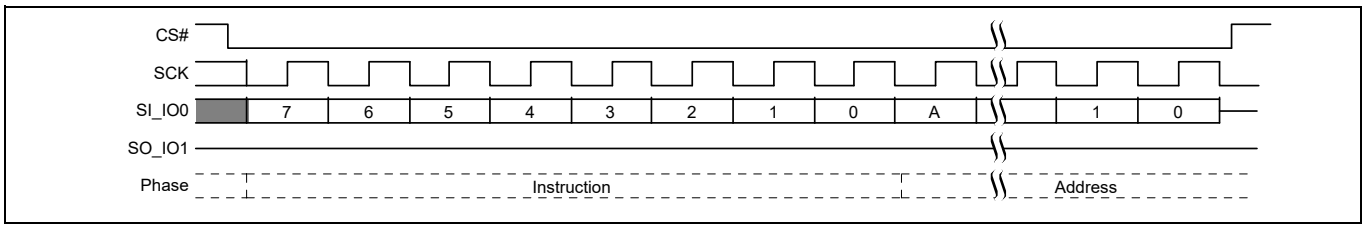


Figure 82 Half Block Erase (HBE 52h or 4HBE 53h) command sequence[47, 48]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted in on IO0–IO3.

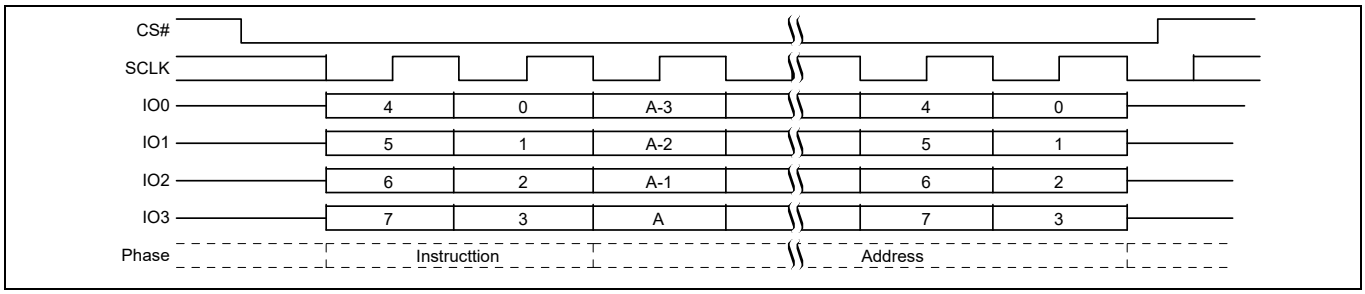


Figure 83 Half Block Erase (HBE 52h or 4HBE 53h) QPI mode command sequence[47, 48]

Notes
47.A = MSb of address = A23 for HBE 52h with CR2V[0] = 0, or A31 for HBE 52h with CR2V[0] = 1 or 4HBE 53h.
48.When A[15] = 0, the sectors 0–7 of Block are erased and A[15] = 1 then sectors 8-15 of Block are erased.

8.6.3 Block Erase (BE D8h or 4BE DCh)

The Block Erase (BE) command sets all bits in the addressed block to 1 (all bytes are FFh). Before the Block Erase (BE) command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The instruction

- D8h [CR2V[0] = 0] is followed by a 3-byte address (A23–A0), or
- D8h [CR2V[0] = 1] is followed by a 4-byte address (A31–A0), or
- DCh is followed by a 4-byte address (A31–A0)

CS# must be driven into the logic high state after the twenty-fourth or thirty-second bit of address has been latched in on SI/IO0. This will initiate the erase cycle, which involves the pre-programming and erase of each sector of the chosen block. If CS# is not driven high after the last bit of address, the block erase operation will not be executed.

As soon as CS# is driven into the logic high state, the internal erase cycle will be initiated. With the internal erase cycle in progress, the user can read the value of the Write-In Progress (WIP) bit to check if the operation has been completed. The WIP bit will indicate a '1' when the erase cycle is in progress and a '0' when the erase cycle has been completed.

A Block Erase (BE) command applied to a Block that has been Write Protected through the Legacy Block Protection, Individual Block Lock or Pointer Region Protection will not be executed and will set the E_ERR status.

If a block erase command is applied and if any region or sector area is protected the erase will not be executed on the 64 KB range and will set the E_ERR status.

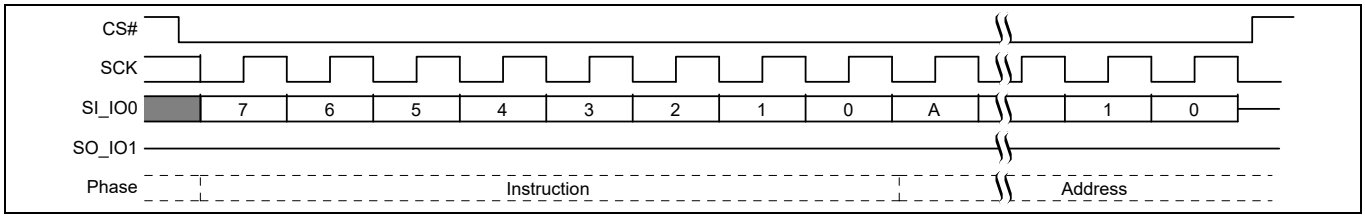


Figure 84 Block Erase (BE D8h or 4BE DCh) command sequence[49]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted in on IO0–IO3.

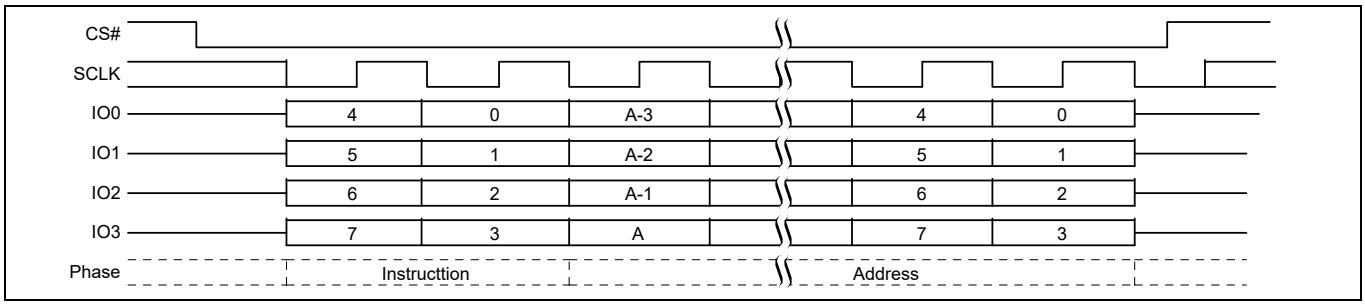


Figure 85 Block Erase (BE D8h or 4BE DCh) QPI mode command sequence[49]

Note
49.A = MSb of address = A23 for BE D8h with CR2V[0] = 0, or A31 for BE D8h with CR2V[0] = 1 or 4BE DCh.

8.6.4 Chip Erase (CE 60h or C7h)

The Chip Erase (CE) command sets all bits to 1 (all bytes are FFh) inside the entire flash memory array. Before the CE command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

CS# must be driven into the logic high state after the eighth bit of the instruction byte has been latched in on SI/IO0. This will initiate the erase cycle, which involves the pre-programming and erase of the entire flash memory array. If CS# is not driven high after the last bit of instruction, the CE operation will not be executed.

As soon as CS# is driven into the logic high state, the erase cycle will be initiated. With the erase cycle in progress, the user can read the value of the Write-In Progress (WIP) bit to determine when the operation has been completed. The WIP bit will indicate a '1' when the erase cycle is in progress and a '0' when the erase cycle has been completed.

A CE command will not be executed when the Legacy Block Protection, Individual Block Lock or Pointer Region Protection set to protect any sector or block and this will set the E_ERR status bit.

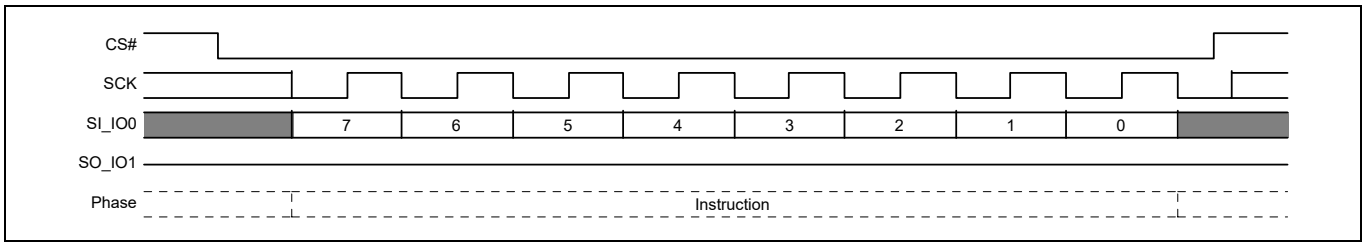


Figure 86 Chip Erase command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

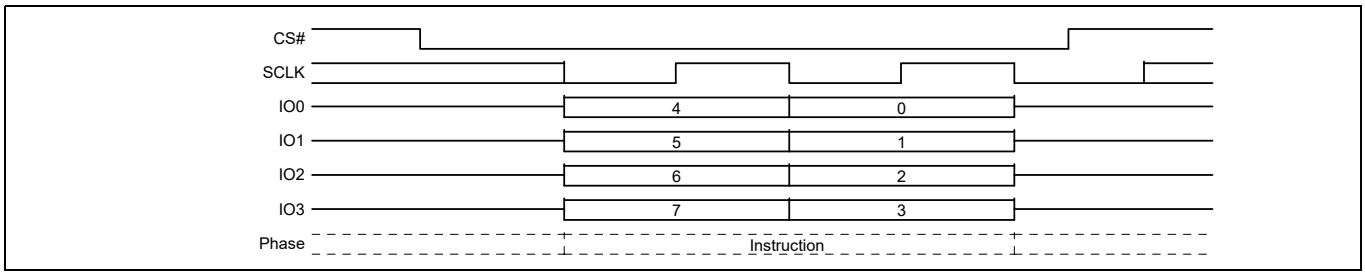


Figure 87 Chip Erase command sequence QPI mode

8.6.5 Program or Erase Suspend (PES 75h)

The PES command allows the system to interrupt a programming or erase operation and then read from any other non-erase-suspended sector or non-program-suspended-page. Program or Erase Suspend is valid only during a programming or sector erase, half block erase or block erase operation. A Chip Erase operation cannot be suspended.

The Write in Progress (WIP) bit in Status Register 1 (SR1V[0]) must be checked to know when the programming or erase operation has stopped. The Program Suspend Status bit in the Status Register 2 (SR2[0]) can be used to determine if a programming operation has been suspended or was completed at the time WIP changes to 0. The Erase Suspend Status bit in the Status Register 2 (SR2[1]) can be used to determine if an erase operation has been suspended or was completed at the time WIP changes to 0. The time required for the suspend operation to complete is t_{SL}, see **Table 67**.

An Erase can be suspended to allow a program operation or a read operation. During an erase suspend, the IBL array may be read to examine sector protection and written to remove or restore protection on a sector to be programmed. The protection bits will not be rechecked when the operation is resumed so any changes made will not impact current in progress operation.

A program operation may be suspended to allow a read operation.

A new suspend operation is not allowed with-in an already suspended erase or program operation. The suspend command is ignored in this situation.

Table 44 Commands allowed during program or erase suspend

Instruction name	Instruction code (Hex)	Allowed during Erase Suspend	Allowed during Program Suspend	Comment
READ	03	X	X	All array reads allowed in suspend
RDSR1	05			Needed to read WIP to determine end of suspend process
RDAR	65			Alternate way to read WIP to determine end of suspend process
RDSR2	07			Needed to read suspend status to determine whether the operation is suspended or complete.
RDCR1	35			Needed to read Configuration Register 1
RDCR2	15			Needed to read Configuration Register 2
RDCR3	33			Needed to read Configuration Register 3
RUID	4B			Needed to read Unique Id
RDID	9F			Needed to read Device Id
RDQID	AF			Needed to read Quad Device Id
RSFDP	5A			Needed to read SFDP
SBL	77			Needed to set Burst Length
WREN	06			Required for program command within erase suspend
WRDI	04			
PP	02			Required for array program during erase suspend. Only allowed if there is no other program suspended program operation (SR2V[0] = 0). A program command will be ignored while there is a suspended program. If a program command is sent for a location within an erase suspended sector the program operation will fail with the P_ERR bit set.
4PP	12			Required for array program during erase suspend. Only allowed if there is no other program suspended program operation (SR2V[0] = 0). A program command will be ignored while there is a suspended program. If a program command is sent for a location within an erase suspended sector the program operation will fail with the P_ERR bit set.
QPP	32			Required for array program during erase suspend. Only allowed if there is no other program suspended program operation (SR2V[0] = 0). A program command will be ignored while there is a suspended program. If a program command is sent for a location within an erase suspended sector the program operation will fail with the P_ERR bit set.
4QPP	34			Required for array program during erase suspend. Only allowed if there is no other program suspended program operation (SR2V[0] = 0). A program command will be ignored while there is a suspended program. If a program command is sent for a location within an erase suspended sector the program operation will fail with the P_ERR bit set.

Table 44 Commands allowed during program or erase suspend (Continued)

Instruction name	Instruction code (Hex)	Allowed during Erase Suspend	Allowed during Program Suspend	Comment
4READ	13	X	X	All array reads allowed in suspend
CLSR	30			Clear status may be used if a program operation fails during erase suspend.
EPR	7A			Required to resume from erase or program suspend.
RSTEN	66			Reset allowed anytime
RST	99			
FAST_READ	0B			All array reads allowed in suspend
4FAST_READ	0C			
DOR	3B			
4DOR	3C			
DIOR	BB			
4DIOR	BC			
IBLRD	3D			It may be necessary to remove and restore Individual Block Lock during erase suspend to allow programming during erase suspend.
4IBLRD	E0			
IBL	36			
4IBL	E1			
IBUL	39			
4IBUL	E2			
QOR	6B			Read Quad Output (3 or 4 Byte Address)[50]
4QOR	6C			Read Quad Output (4 Byte Address)[50]
QIOR	EB			All array reads allowed in suspend[50]
4QIOR	EC			
DDRQIOR	ED			
DDR4QIOR	ED			
MBR	FF			May need to reset a read operation during suspend
SECRP	42			All Security Regions program allowed in erase suspend
SECRR	48			All Security Regions reads allowed in suspend

All command not included in **Table 44** are not allowed during Erase or Program Suspend. The WRR, WRAR, or SPRP commands are not allowed during Erase or Program Suspend, it is therefore not possible to alter the Legacy Block Protection bits or Pointer Region Protection during Erase Suspend.

Reading at any address within an erase-suspended sector or program-suspended page produces undetermined data.

After an erase-suspended program operation is complete, the device returns to the erase-suspend mode. The system can determine the status of the program operation by reading the WIP bit in the Status Register, just as in the standard program operation.

Note

50.For all Quad commands the Quad Enable CR1V[1] bit (see **Figure 13**) needs to be set to '1' before initial program or erase, since the WRR/WRAR commands are not allowed inside of the suspend state.

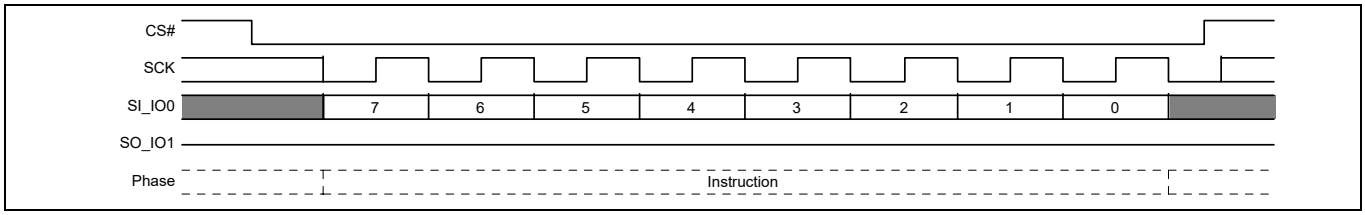


Figure 88 Program or Erase Suspend command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

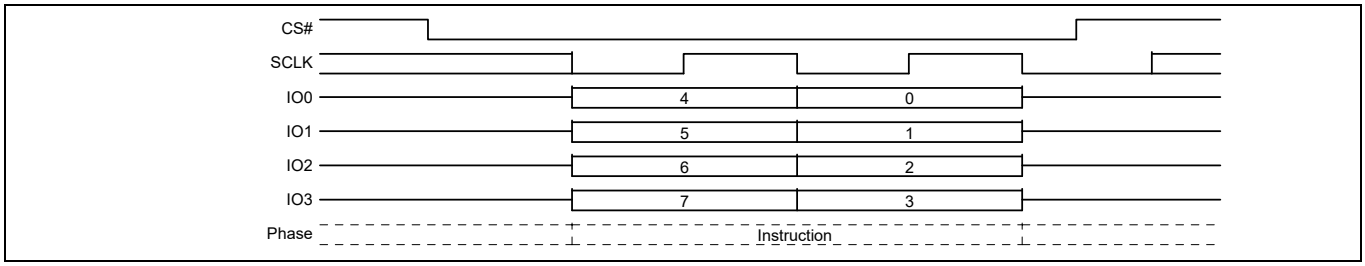


Figure 89 Program or Erase Suspend command sequence QPI mode

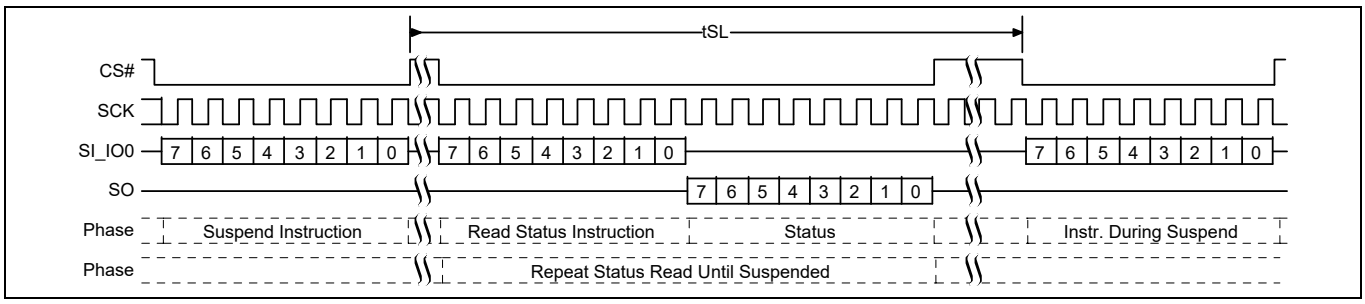


Figure 90 Program or Erase Suspend command with continuing instruction commands sequence

8.6.6 Erase or Program Resume (EPR 7Ah)

After program or read operations are completed during a program or erase suspend the Erase or Program Resume command is sent to continue the suspended operation.

After an Erase or Program Resume command is issued, the WIP bit in the Status Register 1 will be set to a 1 and the suspended operation will resume if one is suspended. If there is no suspended program or erase operation the resume command is ignored.

Program or erase operations may be interrupted as often as necessary e.g. a program suspend command could immediately follow a program resume command but, but in order for a program or erase operation to progress to completion there must be some periods of time between resume and the next suspend command greater than or equal to t_{RNS}. See **Table 67**.

The Program Suspend Status bit in the Status Register 2 (SR2[0]) can be used to determine if a programming operation has been suspended or was completed at the time WIP changes to 0. The Erase Suspend Status bit in the Status Register 2 (SR2[1]) can be used to determine if an erase operation has been suspended or was completed at the time WIP changes to 0. See **"Status Register 2 Volatile (SR2V)"** on page 38.

An Erase or Program Resume command must be written to resume a suspended operation.

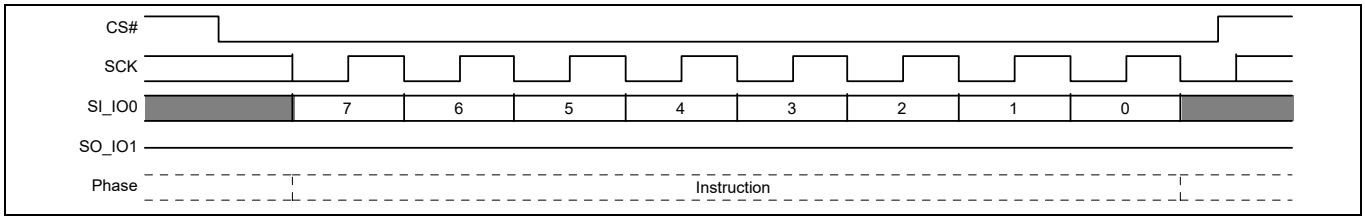


Figure 91 Erase or Program Resume command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

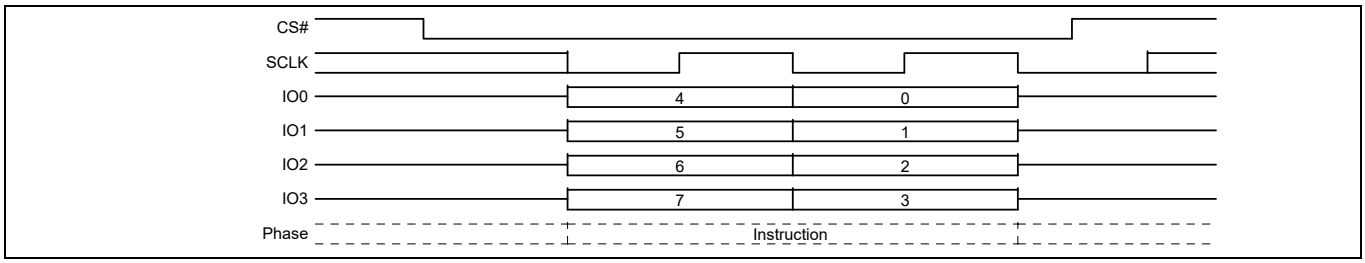


Figure 92 Erase or Program Resume command sequence QPI mode

8.7 Security Regions array commands

The Security Regions commands select which region to use by address A15 to A8 as shown below.

- Security Region 0: A23–16 = 00h; A15–8 = 00h; A7–0 = byte address
- Security Region 1: A23–16 = 00h; A15–8 = 01h; A7–0 = byte address
- Security Region 2: A23–16 = 00h; A15–8 = 02h; A7–0 = byte address
- Security Region 3: A23–16 = 00h; A15–8 = 03h; A7–0 = byte address

8.7.1 Security Region Erase (SECRE 44h)

The Security Region Erase command erases data in the Security Region, which is in a different address space from the main array data. The Security Region is 1024 bytes so, the address bits for S25FL128L (A23 to A10) and S25FL256L (A24 to A10) must be zero for this command. Each region can be individually erased. Refer to **"Security Regions address space"** on page 31 for details on the Security Region.

Before the Security Region Erase command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations. The WIP bit in SR1V may be checked to determine when the operation is completed. The E_ERR bit in SR2V may be checked to determine if any error occurred during the operation.

The Security Region Lock Bits (CR1NV[2-5]) in the Configuration Register 1 can be used to protect the Security Regions for erase. Once a lock bit is set to 1, the corresponding Security Region will be permanently locked, Attempting to erase a region that is locked will fail with the E_ERR bit in SR2V[6] set to '1'.

When the Protection Register NVLOCK Bit = 0, Security Regions 2 and 3 are protected from program or erase. Attempting to erase in a region that locked will fail with the E_ERR bits in SR2V[6] set to '1'. See **"NVLOCK bit (PR[0])"** on page 68.

The Password Protection Mode Lock Bit (IRP[2]) allows regions 2 and 3 to be protected from erase operations until the correct password is provided to enable erasing of these Security Regions. Attempting to erase in a region that is password locked will fail with the E_ERR bit in SR2V[6] set to '1'. See **"Security Region read password protection"** on page 69.

The protocol of the Security Region Erase command is the same as the Sector Erase command. See **"Sector Erase (SE 20h or 4SE 21h)"** on page 108 for the command sequence. QPI Mode is supported.

8.7.2 Security Region Program (SECRP 42h)

The Security Region Program command programs data in the Security Region, which is in a different address space from the main array data. The Security Region is 1024 bytes so, the address bits for S25FL128L (A23 to A10) and S25FL256L (A24 to A10) must be zero for this command. Refer to **"Security Regions address space"** on page 31 for details on the Security Region.

Before the Security Region Program command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations. The WIP bit in SR1V may be checked to determine when the operation is completed. The P_ERR bit in SR2V may be checked to determine if any error occurred during the operation.

To program the Security Region array in bit granularity, the rest of the bits within a data byte can be set to '1'.

Each region in the Security Region memory space can be programmed one or more times, provided that the region is not locked. However, for the best data integrity, it is recommended that one or more 16 byte length and aligned groups of bytes be programed together and programmed only once between erase operations within each region.

The Security Region Lock Bits (CR1NV[2-5]) in the Configuration Register 1 can be used to protect the Security Regions for Programming. Once a lock bit is set to 1, the corresponding Security Region will be permanently locked. Attempting to program zeros or ones in a region that is locked (protected) will fail with the P_ERR bit in SR2V[5] set to '1'. Programming ones in a un-protected area does not cause an error and does not set P_ERR. (see **"Configuration Register 1"** on page 39 for detail descriptions).

When the Protection Register NVLOCK Bit = 0, Security Regions 2 and 3 are protected from program or erase. Attempting to program in a region that locked will fail with the P_ERR bit in SR2V[5] set to '1'. See **"NVLOCK bit (PR[0])"** on page 68.

The Password Protection Mode Lock Bit (IRP[2]) allows regions 2 and 3 to be protected from programming operations until the correct password is provided to enable programming of these Security Regions 2 and 3. Attempting to program in a region that is password locked will fail with the P_ERR bit in SR2V[5] set to '1'. See **"Password protection mode"** on page 68.

The protocol of the Security Region Program command is the same as the Page Program command. See **"Page programming"** on page 106 for the command sequence. QPI Mode is supported.

8.7.3 Security Regions Read (SECRR 48h)

The Security Region Read (SECRR) command provides a way to read data from the Security Regions. The Security Region is 1024 bytes so, the address bits for S25FL128L (A23 to A10) and S25FL256L (A24 to A10) must be zero for this command. Refer to **"Security Regions address space"** on page 31 for details on the Security Regions.

The instruction is followed by a 3 or 4 Byte address (depending on the address length configuration CR2V[0], followed by a number of latency (dummy) cycles set by CR3V[3:0]. Then the selected register data are returned. The protocol of the Security Region Read command will not wrap to the starting address after the Security Region address is at its maximum; instead, the data beyond the maximum address will be undefined. The Security Region Read command read latency is set by the latency value in CR3V[3:0].

The Security Region Read Password Mode Enable Bit (IRP[6]) allows regions 3 to be protected from read operations until the correct password is provided to enable reading of this Security Region. Attempting to read in region 3 that is password locked will return invalid and undefined data. See **"Security Region read password protection"** on page 69.

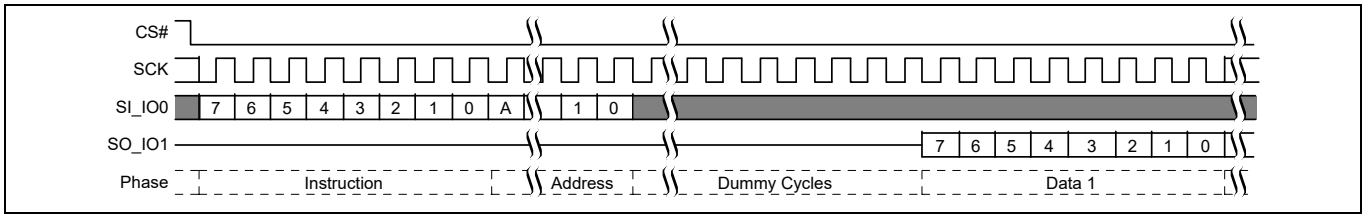


Figure 93 Security Regions Read command sequence[51]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted in and returning data out on IO0–IO3.

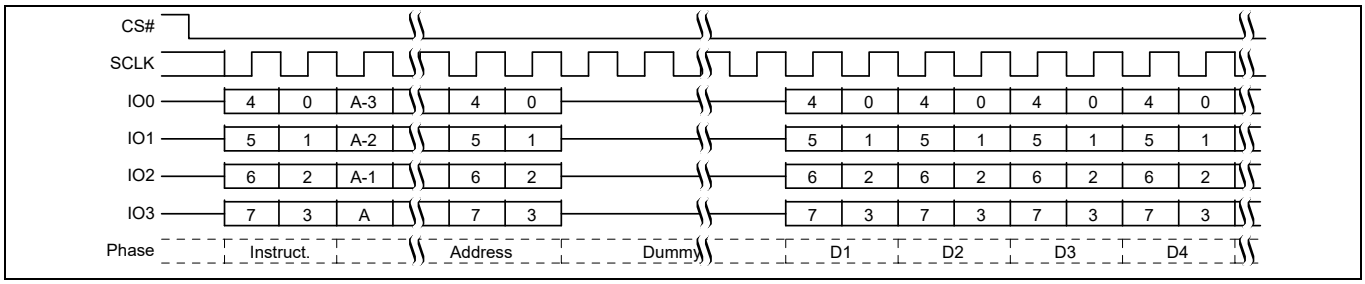


Figure 94 Security Regions Read command sequence QPI mode[52]

Notes
51.A = MSb of address = 23 for Address length CR2V[0] = 0, or 31 for CR2V[0] = 1.
52.A = MSb of address = 23 for CR2V[0] = 0, or 31 for CR2V[0] = 1.

8.8 Individual Block Lock commands

In order to use Individual Block Lock, the IBL protection scheme must be selected by the WPS bit in Configuration Register 2 CR2V[2] = 1. If if IBL protection scheme is not selected CR2V[2] = 0 the IBL commands are ignored.

Individual Block Lock Bits (IBL) are volatile, with one for each sector / block, and can be individually modified. By issuing the IBL or GBL commands, a IBL bit is set to '0' protecting each related sector / block. By issuing the IBUL or GUL commands, a IBL bit is cleared to '1' unprotecting each related sector or block. By issuing the IBLRD command the state of each IBL bit protection can be read.

8.8.1 IBL Read (IBLRD 3Dh or 4IBLRD E0h)

The IBLRD/4IBLRD command allows reading the state of each IBL bit protection.

The instruction is latched into SI by the rising edge of the SCK signal. The instruction is followed by the 24- or 32-Bit address, depending on the address length configuration CR2V[0], selecting location zero within the desired sector.

Then the 8-bit IBL access register contents are shifted out on the serial output SO/IO1. Each bit is shifted out at the SCK frequency by the falling edge of the SCK signal. It is possible to read the same IBL access register continuously by providing multiples of eight clock cycles. The address of the IBL register does not increment so this is not a means to read the entire IBL array. Each location must be read with a separate IBL Read command.

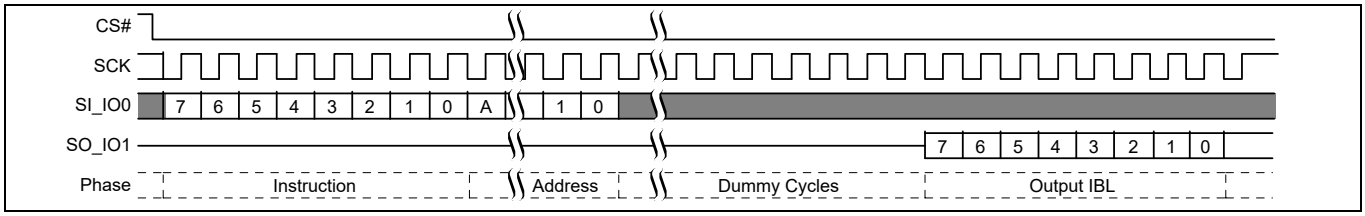


Figure 95 IBLRD command sequence[53, 54]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted in and returning data out on IO0–IO3.

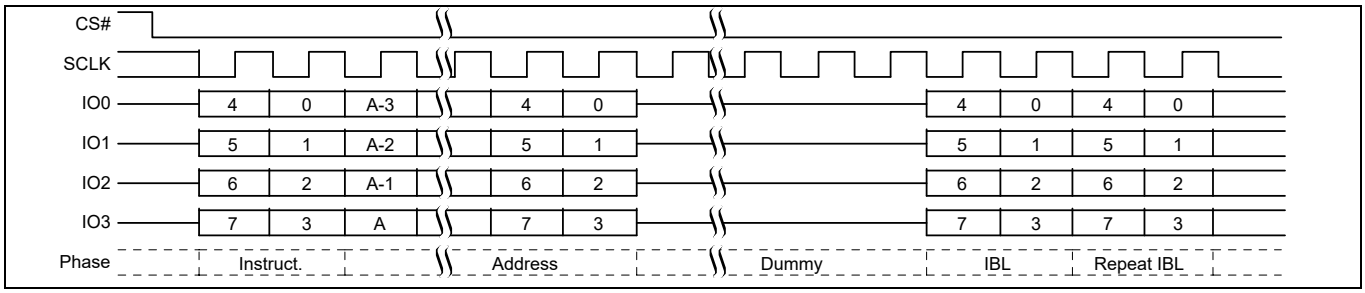


Figure 96 IBLRD command sequence QPI[53, 54]

Notes
53.A = MSb of address = 23 for Address length (CR2V[0] = 0, or 31 for CR2V[0] = 1 with command 3Dh.
54.A = MSb of address = 31 with command E0h.

8.8.2 IBL Lock (IBL 36h or 4IBL E1h)

The IBL/4IBL commands sets the selected IBL bit to '0' protecting each related sector / block.

The IBL command is entered by driving CS# to the logic low state, followed by the instruction, followed by the 24- or 32-Bit address, depending on the address length configuration CR2V[0]. The IBL command affects the WIP bits of the Status and Configuration Registers in the same manner as any other programming operation.

CS# must be driven to the logic high state after the 24- or 32-Bit address (depending on the address length configuration CR2V[0]) has been latched in. As soon as CS# is driven to the logic high state, the self-timed IBL operation is initiated. While the IBL operation is in progress, the Status Register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a '1' during the self-timed IBL operation, and is a '0' when it is completed.

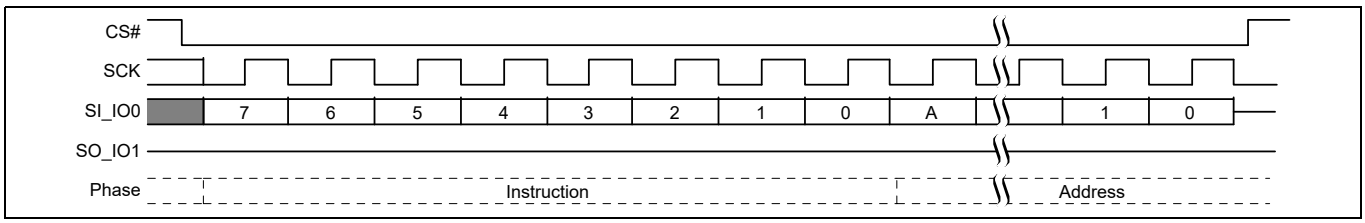


Figure 97 IBL command sequence[55, 56]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted in on IO0–IO3.

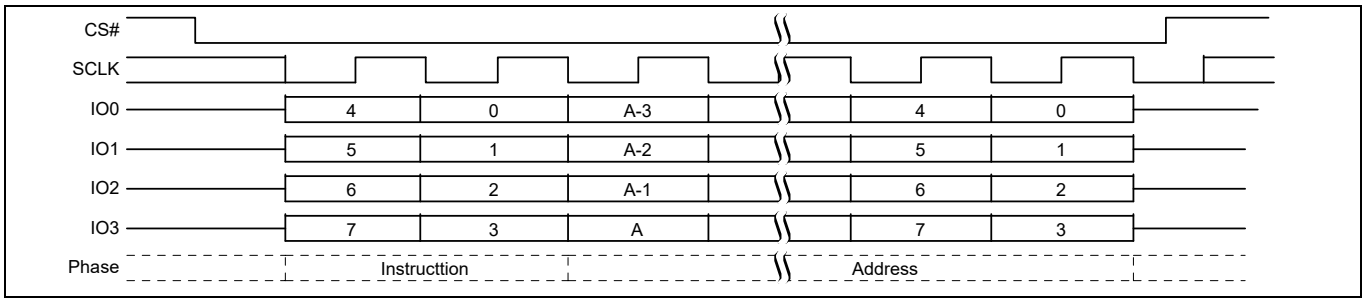


Figure 98 IBL command sequence QPI mode[55, 56]

Notes
55.A = MSb of address = 23 for Address length (CR2V[0] = 0, or 31 for CR2V[0] = 1 with command 36h.
56.A = MSb of address = 31 with command E1h.

8.8.3 IBL Unlock (IBUL 39h or 4IBUL E2h)

The IBUL/4IBULcommands clears the selected IBL bit to ‘1’ unprotecting each related sector / block.

The IBUL command is entered by driving CS# to the logic low state, followed by the instruction, followed by the 24- or 32-Bit address, depending on the address length configuration CR2V[0]. The IBUL command affects the WIP bits of the Status and Configuration Registers in the same manner as any other programming operation.

CS# must be driven to the logic high state after the 24- or 32-Bit address (depending on the address length configuration CR2V[0]) has been latched in. As soon as CS# is driven to the logic high state, the self-timed IBL operation is initiated. While the IBUL operation is in progress, the Status Register may be read to check the value of the Write-In Progress (WIP) bit. The WIP bit is a ‘1’ during the self-timed IBUL operation, and is a ‘0’ when it is completed.

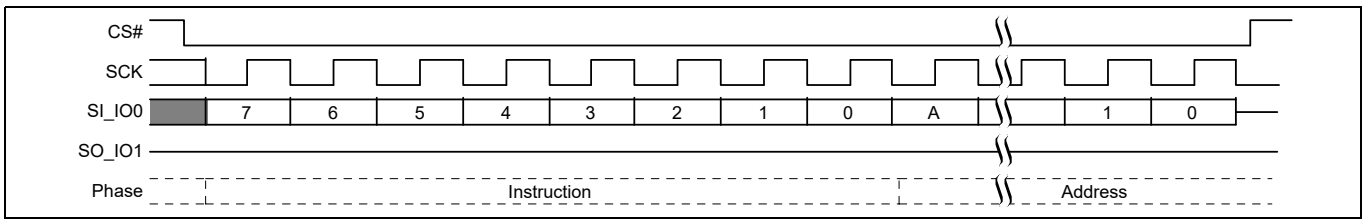


Figure 99 IBUL command sequence[57, 58]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted in on IO0–IO3.

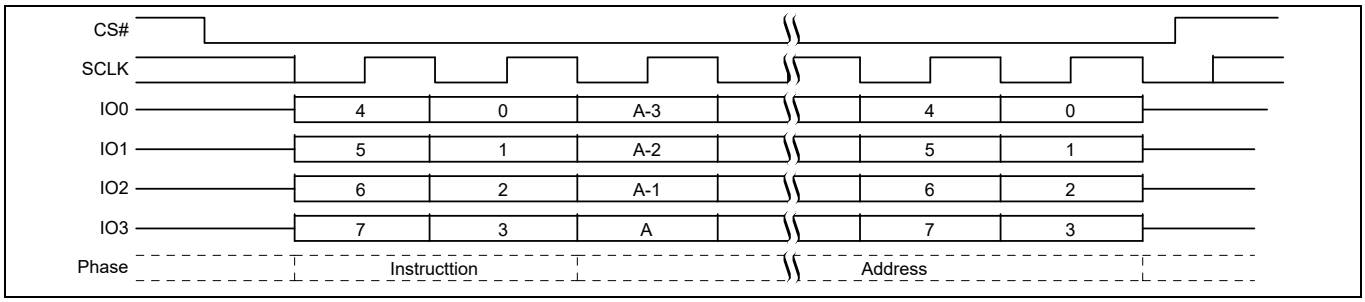


Figure 100 IBUL command sequence QPI mode[57, 58]

Notes
57.A = MSb of address = 23 for Address length (CR2V[0] = 0, or 31 for CR2V[0] = 1 with command 39h.
58.A = MSb of address = 31 with command E2h.

8.8.4 Global IBL Lock (GBL 7Eh)

The GBL commands sets all the IBL bits to ‘0’ protecting all sectors / blocks.

CS# must be driven into the logic high state after the eighth bit of the instruction byte has been latched in on SI. This will initiate the GBL. If CS# is not driven high after the last bit of instruction, the GBL operation will not be executed.

As soon as CS# is driven into the logic high state, the GBL will be initiated. With the GBL in progress, the user can read the value of the Write-In Progress (WIP) bit to determine when the operation has been completed. The WIP bit will indicate a ‘1’ when the GBL is in progress and a ‘0’ when the GBL has been completed.

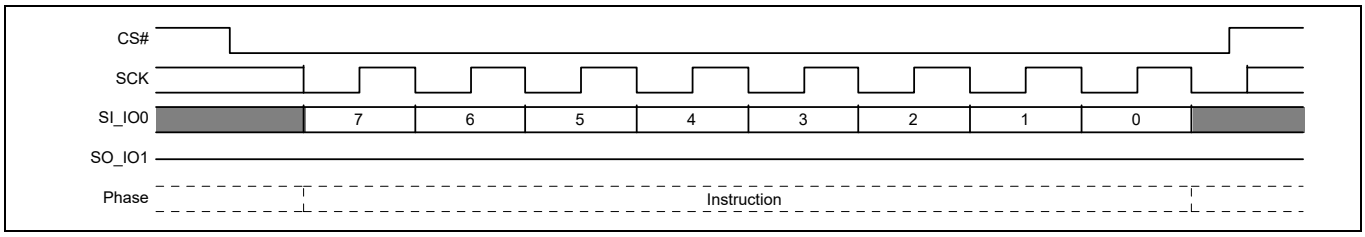


Figure 101 Global IBL Lock (GBL) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

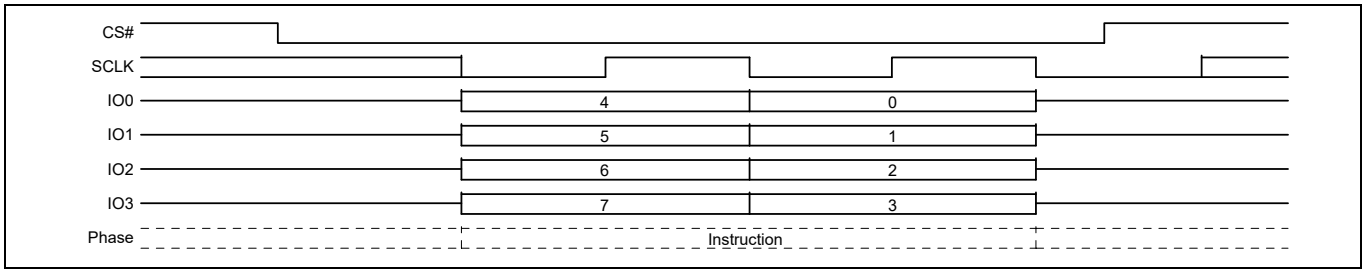


Figure 102 Global IBL Lock (GBL) command sequence QPI mode

8.8.5 Global IBL Unlock (GBUL 98h)

The GBUL commands clears all the IBL bits to ‘1’ unprotecting all sectors / blocks.

CS# must be driven into the logic high state after the eighth bit of the instruction byte has been latched in on SI. This will initiate the GBUL If CS# is not driven high after the last bit of instruction, the GBUL operation will not be executed.

As soon as CS# is driven into the logic high state, the GBL will be initiated. With the GBL in progress, the user can read the value of the Write-In Progress (WIP) bit to determine when the operation has been completed. The WIP bit will indicate a ‘1’ when the GBUL is in progress and a ‘0’ when the GBUL has been completed.

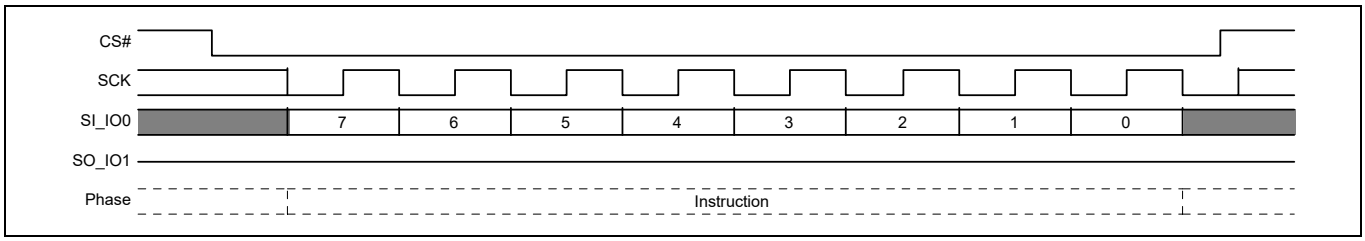


Figure 103 Global IBL Unlock (GBUL) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

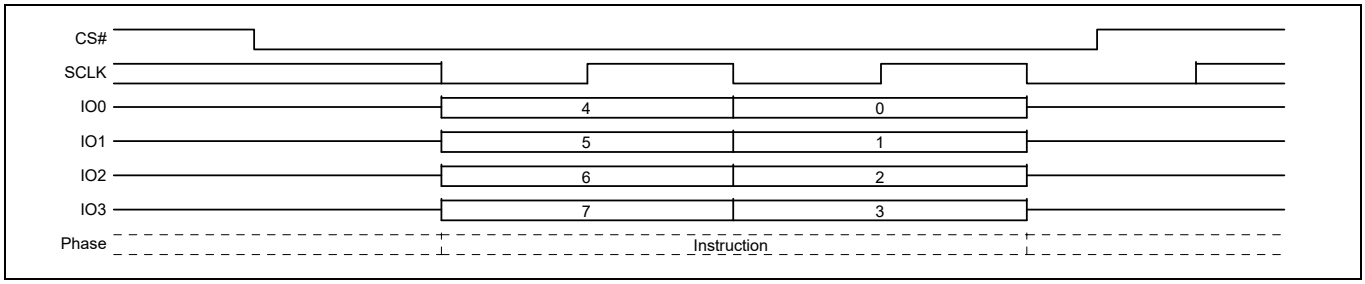


Figure 104 Global IBL Unlock (GBUL) command sequence QPI mode

8.9 Pointer Region command

8.9.1 Set Pointer Region Protection (SPRP FBh or 4SPRP E3h)

The SPRP or 4SPRP command is ignored during a suspend operation because the pointer value cannot be erased and re-programmed during a suspend.

The SPRP or 4SPRP command is ignored if default Power Supply Lock-down protection NVLOCK PR[0] = 0 or Power Supply Lock-down protection enabled IRP[1] = 0 or Password Protection enabled IRP[2] = 0 and NVLOCK PR[0] = 0.

The S25FL256L device must have 4 Byte addressing enabled (CR2V[0] = 1) to set the Pointer Region Protection register PRPR (see **"Pointer Region Protection Register (PRPR)"** on page 52) this ensures that A24 and A25 are set correctly. The S25FL128L device can have 4 Byte addressing enabled (CR2V[0] = 1) or 3 Byte addressing enabled (CR2V[0] = 0).

Before the SPRP or 4SPRP command can be accepted by the device, a Write Enable (WREN) command must be issued. After the Write Enable (WREN) command has been decoded, the device will set the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The SPRP or 4SPRP command is entered by driving CS# to the logic low state, followed by the instruction, followed by the 24- or 32-Bit address, depending on the address length configuration CR2V[0], see **"Pointer Region Protection (PRP)"** on page 64 for details on address values to select protection options.

CS# must be driven to the logic high state after the last bit of address has been latched in. If not, the SPRP command is not executed. As soon as CS# is driven to the logic high state, the self-timed SPRP operation is initiated. While the SPRP operation is in progress, the Status Register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a '1' during the self-timed SPRP operation, and is a '0' when it is completed. When the SPRP operation is completed, the Write Enable Latch (WEL) is set to a '0'. The SPRP or 4SPRP command will set the P_ERR or E_ERR bits if there is a failure in the Set Pointer Region Protection operation.

For details on the address pointer defining a sector boundary between protected and unprotected regions in the memory, see **"Pointer Region Protection (PRP)"** on page 64.

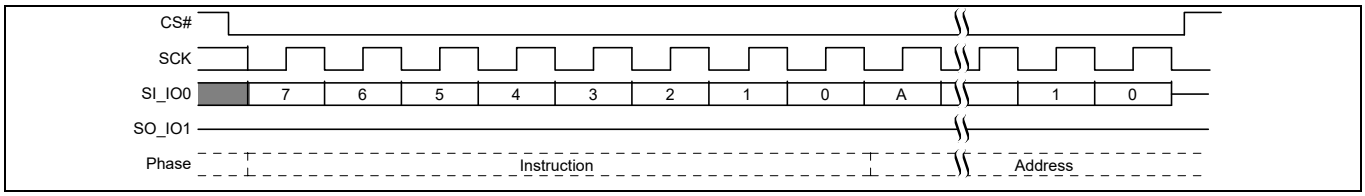


Figure 105 SPRP command sequence[59, 60]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted in on IO0–IO3.

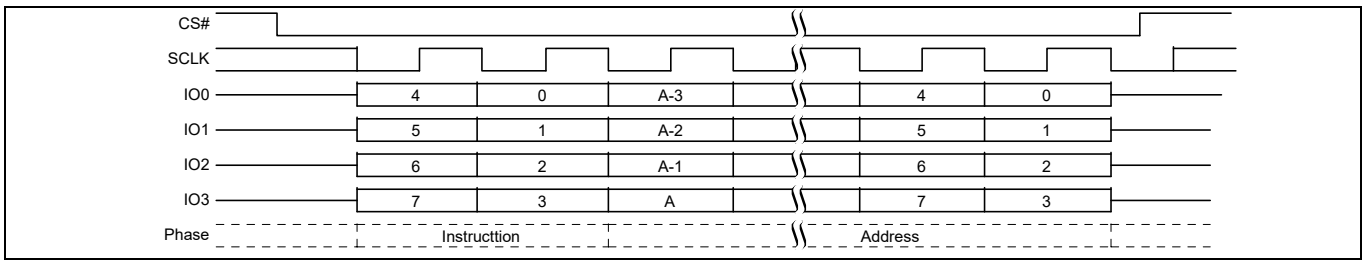


Figure 106 SPRP command sequence QPI mode[59, 60]

Notes
59.A = MSb of address = 23 for Address length (CR2V[0] = 0, or 31 for CR2V[0] = 1 with command FDh.
60.A = MSb of address = 31 with command E3h.

8.10 Individual and Region Protection (IRP) commands

8.10.1 IRP Register Read (IRPRD 2Bh)

The IRP Register Read instruction 2Bh is shifted into SI/IO0 by the rising edge of the SCK signal followed by one dummy cycle. This latency period allows the device's internal circuitry enough time to access data at the initial address. During latency cycles, the data value on IO0–IO3 are "don't care" and may be high impedance.

Then the 16-bit IRP register contents are shifted out on the serial output S0/IO1, LSB first. Each bit is shifted out at the SCK frequency by the falling edge of the SCK signal. It is possible to read the IRP register continuously by providing multiples of 16 clock cycles.

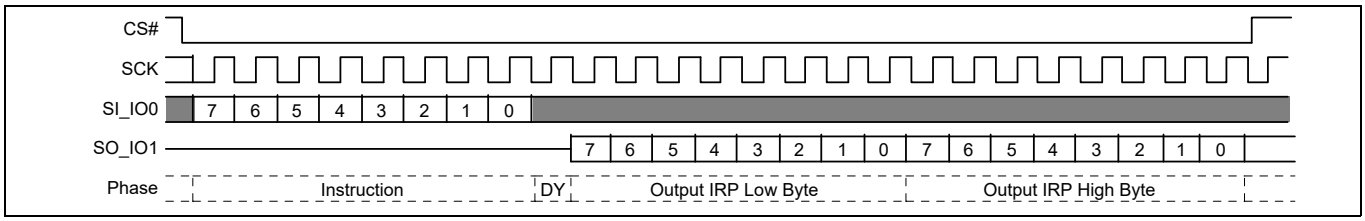


Figure 107 IRPRD command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in and returning data out on IO0–IO3.

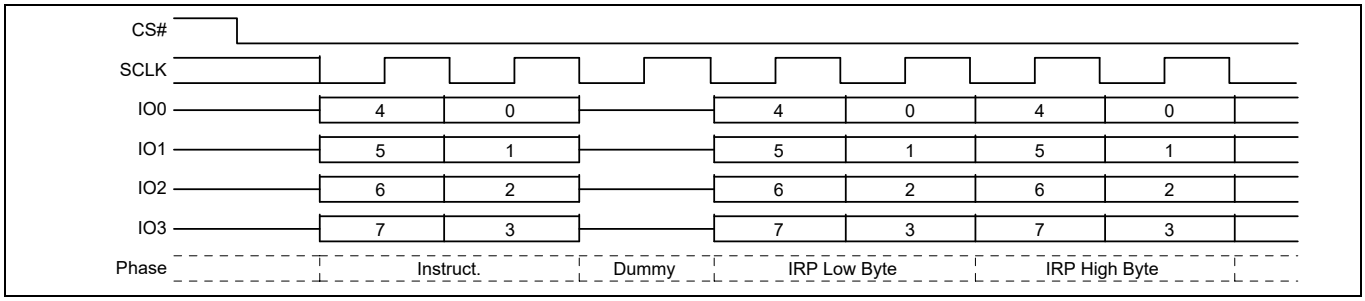


Figure 108 IRPRD command sequence – QPI mode

8.10.2 IRP Program (IRPP 2Fh)

Before the IRP Program (IRPP) command can be accepted by the device, a Write Enable (WREN) command must be issued. After the Write Enable (WREN) command has been decoded, the device will set the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The IRPP command is entered by driving CS# to the logic low state, followed by the instruction and two data bytes on SI, LSB first. The IRP Register is two data bytes in length.

The IRPP command affects the P_ERR and WIP bits of the Status and Configuration Registers in the same manner as any other programming operation.

CS# input must be driven to the logic high state after the sixteenth bit of data has been latched in. If not, the IRPP command is not executed. As soon as CS# is driven to the logic high state, the self-timed IRPP operation is initiated. While the IRPP operation is in progress, the Status Register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a '1' during the self-timed IRPP operation, and is a '0' when it is completed. When the IRPP operation is completed, the Write Enable Latch (WEL) is set to a '0'.

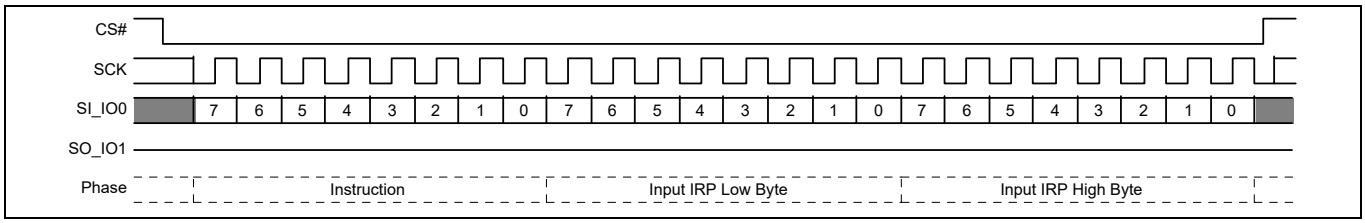


Figure 109 IRP Program (IRPP) command

This command is also supported in QPI mode. In QPI mode, the instruction and data is shifted in on IO0–IO3.

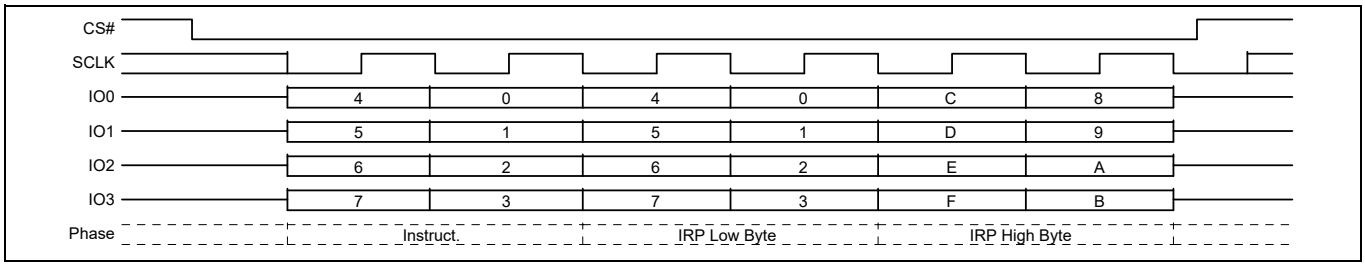


Figure 110 IRP Program (IRPP) command QPI

8.10.3 Protection Register Read (PRRD A7h)

The Protection Register Read (PRRD) command allows the Protection Register contents to be read out of SO/IO1. The Read instruction A7h is shifted into SI by the rising edge of the SCK signal followed by one dummy cycle. This latency period allows the device's internal circuitry enough time to access data at the initial address. During latency cycles, the data value on IO0–IO3 are "don't care" and may be high impedance.

Then the 8-bit Protection Register contents are shifted out on the serial output SO/IO1. Each bit is shifted out at the SCK frequency by the falling edge of the SCK signal. It is possible to read the Protection register continuously by providing multiples of eight clock cycles.

The Protection Register contents may only be read when the device is in standby state with no other operation in progress.

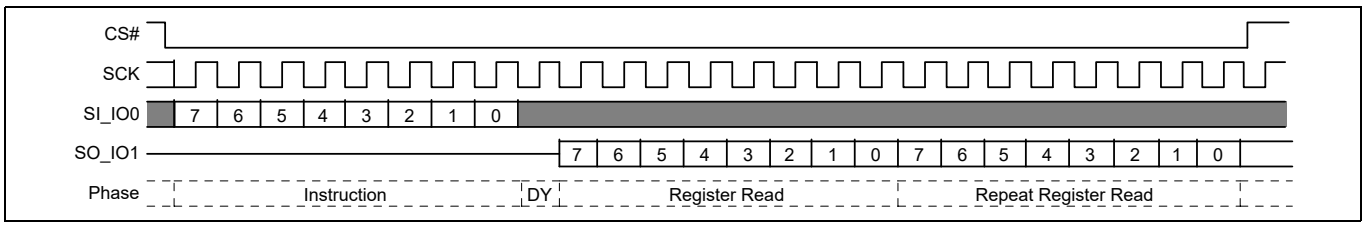


Figure 111 Protection Register Read (PRRD) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in and returning data out on IO0–IO3.

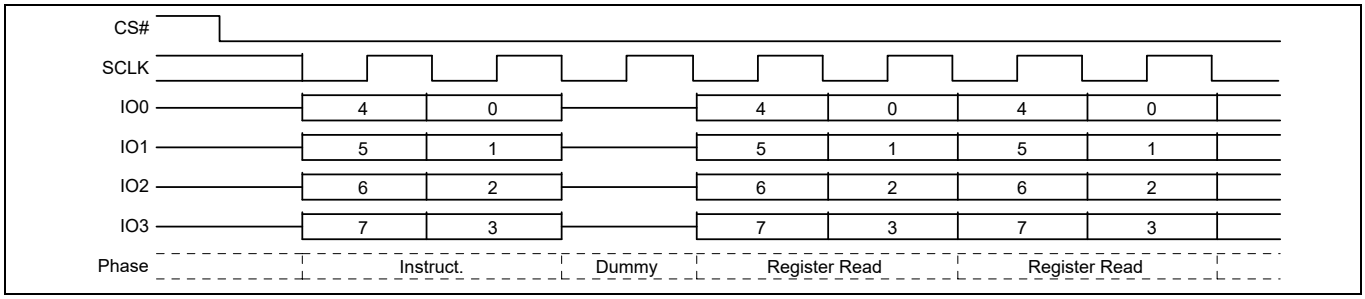


Figure 112 Protection Register Read (PRRD) command sequence – QPI mode

8.10.4 Protection Register Lock (PRL A6h)

The Protection Register Lock (PRL) command clears the NVLOCK bit (PR[0]) to zero and loads the IRP[6] value in to SECRRP (PR[6]). See **"Protection Register (PR)"** on page 51. Before the PRL command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The PRL command is entered by driving CS# to the logic low state, followed by the instruction.

CS# must be driven to the logic high state after the eighth bit of instruction has been latched in. If not, the PRL command is not executed. As soon as CS# is driven to the logic high state, the self-timed PRL operation is initiated. While the PRL operation is in progress, the Status Register may still be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a '1' during the self-timed PRL operation, and is a '0' when it is completed. When the PRL operation is completed, the Write Enable Latch (WEL) is set to a '0'.

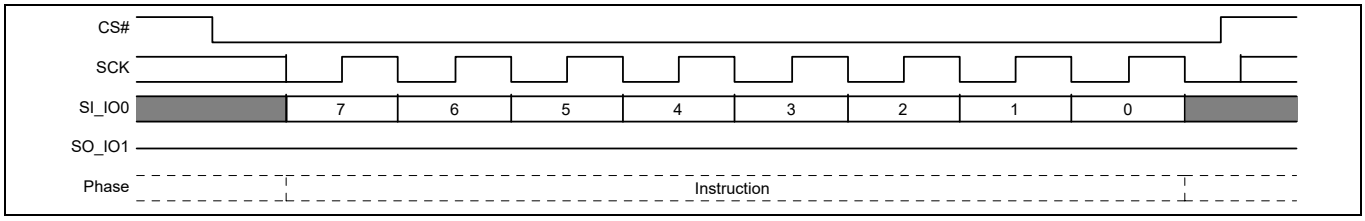


Figure 113 Protection Register Lock (PRL) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

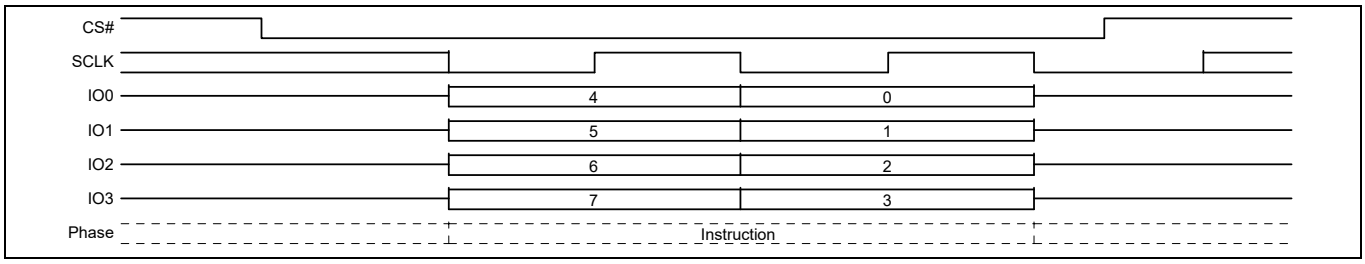


Figure 114 Protection Register Lock (PRL) command sequence – QPI mode

8.10.5 Password Read (PASSRD E7h)

The correct password value may be read only after it is programmed and before the Password Mode has been selected by programming the Password Protection Mode bit to 0 in the IRP Register (IRP[2]). After the Password Protection Mode is selected the password is no longer readable, the PASSRD command will output undefined data.

The PASSRD command is shifted into SI followed by one dummy cycle. This latency period allows the device's internal circuitry enough time to access data at the initial address. During latency cycles, the data value on are "don't care" and may be high impedance.

Then the 64-bit Password is shifted out on the serial output, LSB first, MSb of each byte first. Each bit is shifted out at the SCK frequency by the falling edge of the SCK signal. It is possible to read the Password continuously by providing multiples of 64 clock cycles.

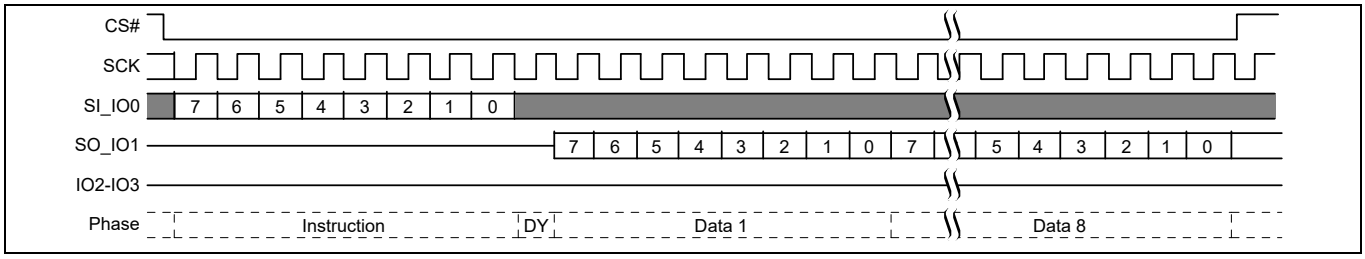


Figure 115 Password Read (PASSRD) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in and returning data out on IO0–IO3.

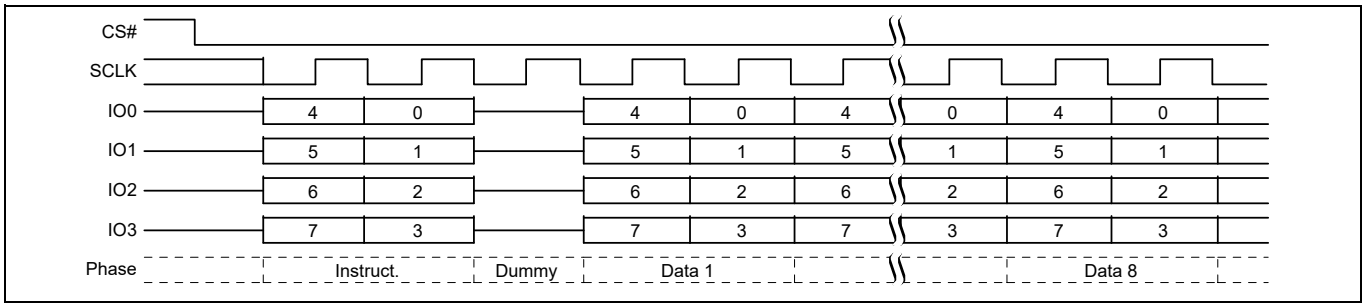


Figure 116 Password Read (PASSRD) command sequence – QPI mode

8.10.6 Password Program (PASSP E8h)

Before the Password Program (PASSP) command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device. After the Write Enable (WREN) command has been decoded, the device sets the Write Enable Latch (WEL) to enable the PASSP operation.

The password can only be programmed before the Password Mode is selected by programming the Password Protection Mode bit to 0 in the IRP Register (IRP[2]). After the Password Protection Mode is selected the PASSP command is ignored.

The PASSP command is entered by driving CS# to the logic low state, followed by the instruction and the password data bytes on SI/IO0, LSB first, MSb of each byte first. The password is sixty-four (64) bits in length.

CS# must be driven to the logic high state after the sixty-fourth (64^{th}) bit of data has been latched. If not, the PASSP command is not executed. As soon as CS# is driven to the logic high state, the self-timed PASSP operation is initiated. While the PASSP operation is in progress, the Status Register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a '1' during the self-timed PASSP cycle, and is a '0' when it is completed. The PASSP command can report a program error in the P_ERR bit of the status register. When the PASSP operation is completed, the Write Enable Latch (WEL) is set to a '0'.

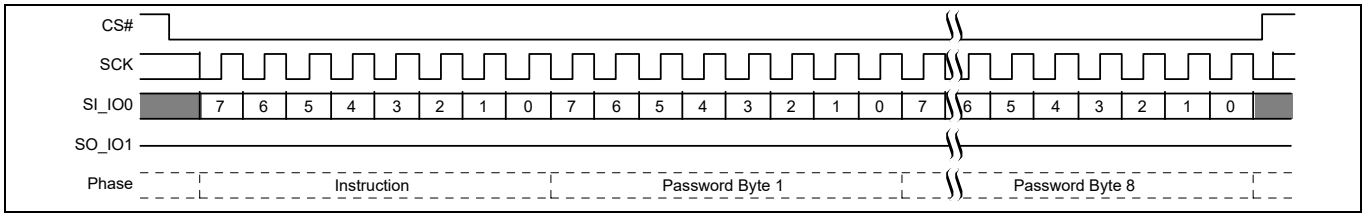


Figure 117 Password Program (PASSP) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction and data is shifted in on IO0–IO3.

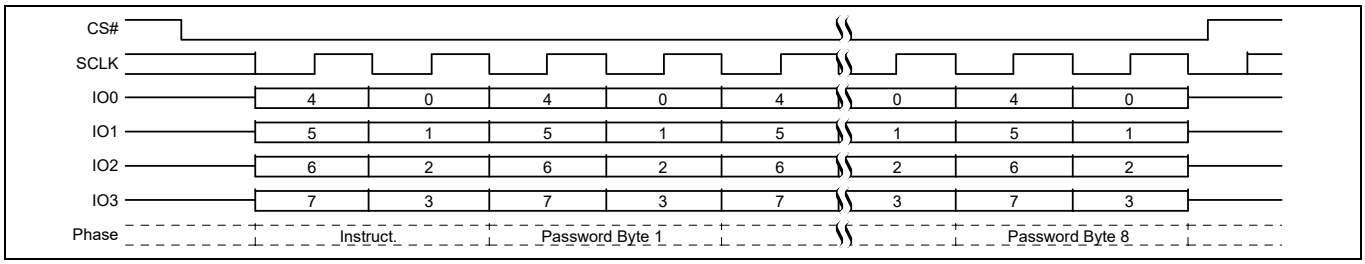


Figure 118 Password Program (PASSP) command sequence QPI mode

8.10.7 Password Unlock (PASSU EAh)

The PASSU command is entered by driving CS# to the logic low state, followed by the instruction and the password data bytes on SI, LSB first, MSb of each byte first. The password is sixty-four (64) bits in length.

CS# must be driven to the logic high state after the sixty-fourth (64^{th}) bit of data has been latched. If not, the PASSU command is not executed. As soon as CS# is driven to the logic high state, the self-timed PASSU operation is initiated. While the PASSU operation is in progress, the Status Register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a '1' during the self-timed PASSU cycle, and is a '0' when it is completed.

If the PASSU command supplied password does not match the hidden password in the Password Register, an error is reported by setting the P_ERR bit to '1'. The WIP bit of the status register also remains set to '1'. It is necessary to use the CLSR command to clear the status register, the software reset command (RSTEN 66h followed by RST 99h) to reset the device, or drive the RESET# and IO3 / RESET# input to initiate a hardware reset, in order to return the P_ERR and WIP bits to '0'. This returns the device to standby state, ready for new commands such as a retry of the PASSU command.

If the password does match, the NVLOCK bit is set to '1'.

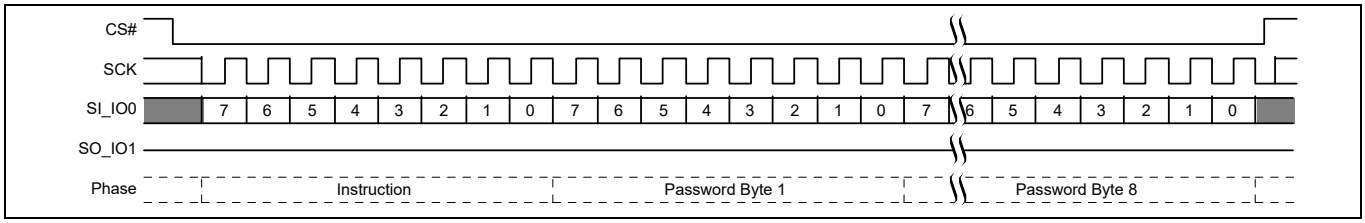


Figure 119 Password Unlock (PASSU) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction and data is shifted in on IO0–IO3.

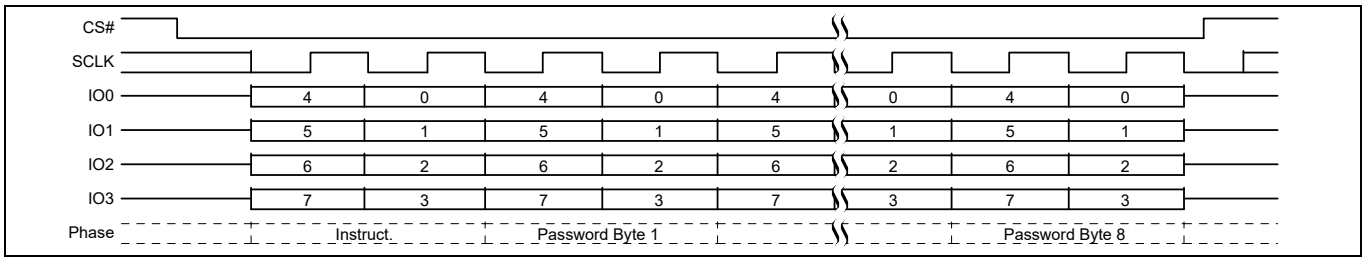


Figure 120 Password Unlock (PASSU) command sequence QPI mode

8.11 Reset commands

Software controlled Reset commands restore the device to its initial power up state, by reloading volatile registers from non-volatile default values. If a software reset is initiated during a Erase, Program or writing of a Register operation the data in that Sector, Page or Register is not stable, the operation that was interrupted needs to be initiated again.

However, the volatile SRP1 bit in the Configuration register CR1V[0] and the volatile NVLOCK bit in the Protection Register are not changed by a software reset. The software reset cannot be used to circumvent the SRP1 or NVLOCK bit protection mechanisms for the other security configuration bits.

The SRP1 bit and the NVLOCK bit will remain set at their last value prior to the software reset. To clear the SRP1 bit and set the NVLOCK bit to its protection mode selected power on state, a full power-on-reset sequence or hardware reset must be done.

A software reset command (RSTEN 66h followed by RST 99h) is executed when CS# is brought high at the end of the instruction and requires t_{RPH} time to execute.

In the case of a previous Power-up Reset (POR) failure to complete, a reset command triggers a full power up sequence requiring t_{PU} to complete.

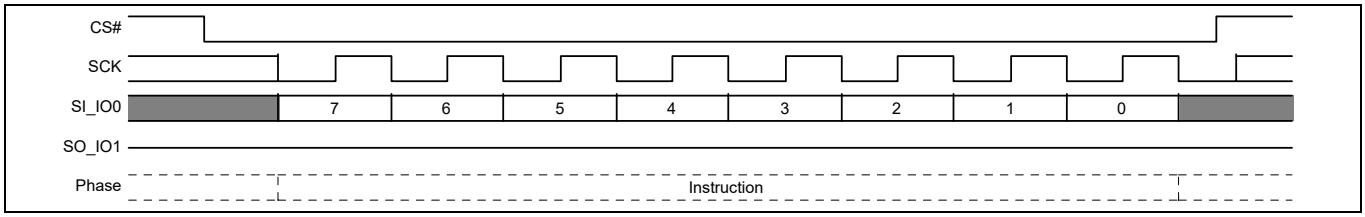


Figure 121 Software / Mode Bit Reset command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

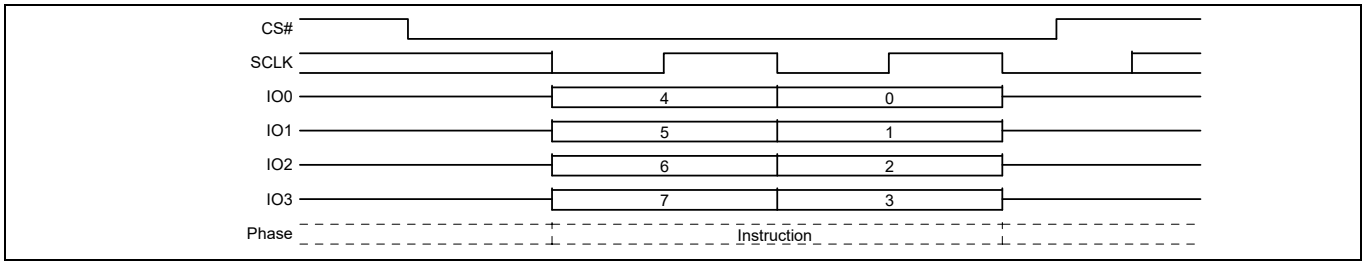


Figure 122 Software reset / Mode Bit command sequence – QPI mode

8.11.1 Software Reset Enable (RSTEN 66h)

The Reset Enable (RSTEN) command is required immediately before a software reset command (RST 99h) such that a software reset is a sequence of the two commands. Any command other than RST following the RSTEN command, will clear the reset enable condition and prevent a later RST command from being recognized.

8.11.2 Software Reset (RST 99h)

The Reset (RST) command immediately following a RSTEN command, initiates the software reset process. Any command other than RST following the RSTEN command, will clear the reset enable condition and prevent a later RST command from being recognized.

8.11.3 Mode Bit Reset (MBR FFh)

The Mode Bit Reset (MBR) command is used to return the device from continuous high performance read mode back to normal standby awaiting any new command. Because the hardware RESET# input may be disabled and a device that is in a continuous high performance read mode may not recognize any normal SPI command, a system hardware reset or software reset command may not be recognized by the device. It is recommended to use the MBR command after a system reset when the RESET# signal is not available or, before sending a software reset, to ensure the device is released from continuous high performance read mode.

The MBR command sends Ones on SI/IO0for eight SCK cycles. IO1–IO3 are “don’t care” during these cycles.

8.12 Deep Power Down commands

8.12.1 Deep Power-Down (DPD B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-Down command. The lower power consumption makes the Deep Power-down (DPD) command especially useful for battery powered applications (see I_{CC1} and I_{CC2} in **“DC characteristics”** on page 152). The command is initiated by driving the CS# pin low and shifting the instruction code “B9h”.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Deep Power-Down command will not be executed. After CS# is driven high, the power-down state will be entered within the time duration of t_{DP} (**Table 64**). While in the power-down state only the Release from Deep Power-Down / Device ID command, which restores the device to normal operation, will be recognized. All other commands are ignored. This includes the Read Status Register command, which is always available during normal operation. Ignoring all but one command also makes the Power Down state a useful condition for securing maximum write protection.

While in the deep power-down mode the device will only accept a hardware reset which will initiate a Power on Reset that will restore the device to normal operation. The device always powers-up in the normal operation with the standby current of I_{CC1}.

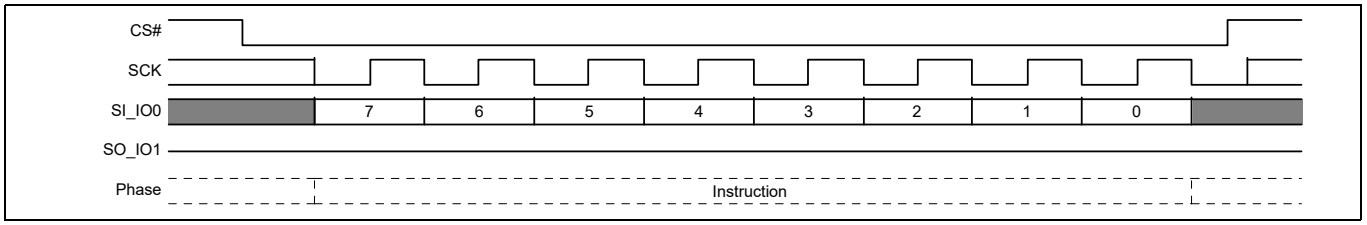


Figure 123 Deep Power Down (DPD) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

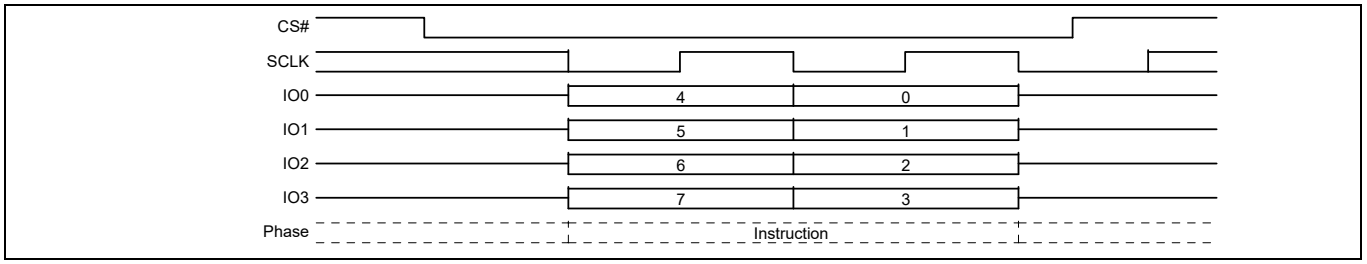


Figure 124 Deep Power Down (DPD) command sequence – QPI mode

8.12.2 Release from Deep Power-Down / Device ID (RES ABh)

The Release from Deep Power-Down /Device ID command is a multi-purpose command. It can be used to release the device from the Deep Power-Down state, or obtain the devices electronic identification (ID) number.

To release the device from the Deep Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code “ABh” and driving CS# high. Release from Deep Power-Down will take the time duration of t_{RES} (**Table 64**) before the device will resume normal operation and other commands are accepted. The CS# pin must remain high during the t_{RES} time duration.

When used only to obtain the Device ID while not in the Deep Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with MSb first. The Device ID values for the S25FL-L Family is listed in and **Table 51**. Continued shifting of output beyond the end of the defined ID address space will provide undefined data. The command is completed by driving CS# high.

When used to release the device from the Deep Power-Down state and obtain the Device ID, the command is the same as previously described, and shown in **Figure 127** and **Figure 128**, except that after CS# is driven high it must remain high for a time duration of t_{RES}. After this time duration the device will resume normal operation and other commands will be accepted. If the Release from Deep Power-Down / Device ID command is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the command is ignored and will not have any effects on the current cycle.

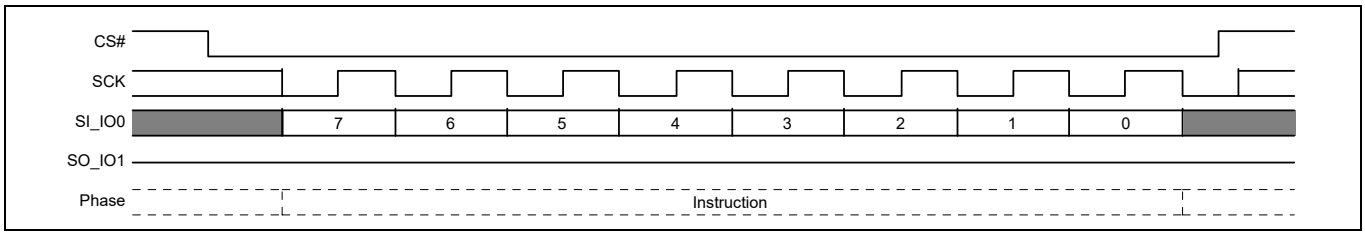


Figure 125 Release from Deep Power Down (RES) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3.

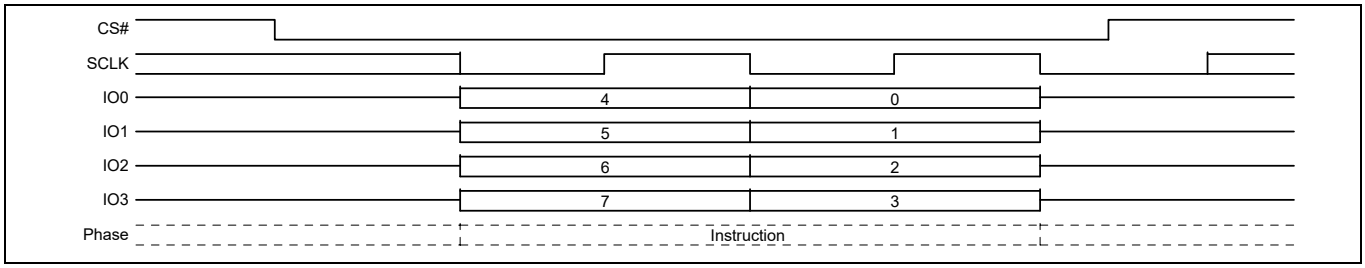


Figure 126 Release from Deep Power Down (RES) command sequence – QPI mode

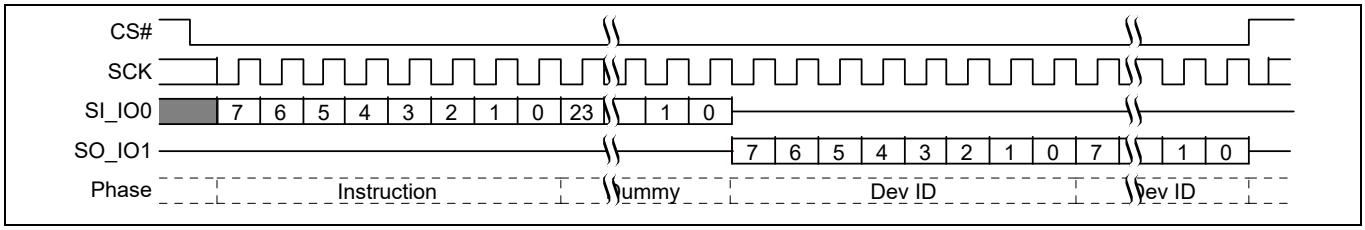


Figure 127 Read Identification (RES) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0–IO3 and the returning data is shifted out on IO0–IO3.

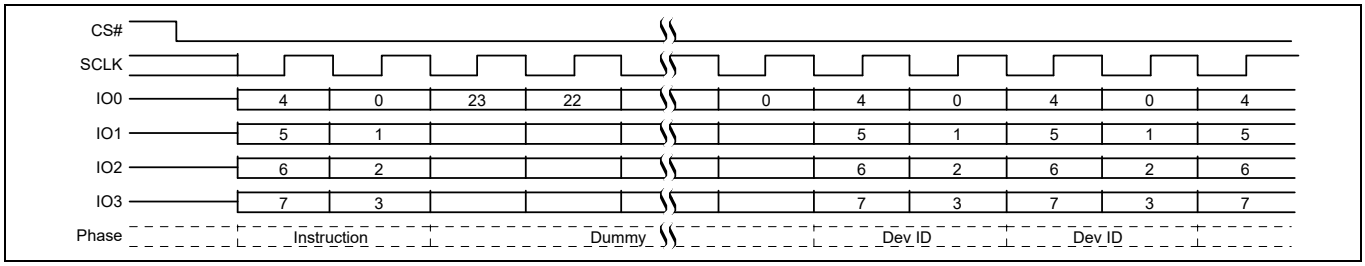


Figure 128 Read Identification (RES) QPI mode command

9 Data integrity

9.1 Erase endurance

Table 45 Erase endurance

Parameter	Min	Unit
Program/Erase cycles per main Flash array sectors	100K	P/E cycle
Program/Erase cycles per Security Registers or non-volatile register array[61]	1K	

9.2 Data retention

Table 46 Data retention

Parameter	Test conditions	Minimum time	Unit
Data retention time	10K program/erase cycles	20	Years
	100K program/erase cycles	2	

Contact Infineon Sales or an FAE representative for additional information regarding data integrity.

Note
61.Each write command to a non-volatile register causes a P/E cycle on the entire non-volatile register array.

10 Software interface reference

10.1 JEDEC JESD216B serial flash discoverable parameters

This document defines the serial flash discoverable parameters (SFDP) revision B data structure used in the following Infineon Serial Flash Devices:

- S25FL-L Family

These data structure values are an update to the earlier revision SFDP data structure currently existing in the above devices.

The Read SFDP (RSFDP) command (5Ah) reads information from a separate Flash memory address space for device identification, feature, and configuration information, in accord with the JEDEC JESD216B standard for Serial Flash Discoverable Parameters.

The SFDP data structure consists of a header table that identifies the revision of the JESD216 header format that is supported and provides a revision number and pointer for each of the SFDP parameter tables that are provided. The parameter tables follow the SFDP header. However, the parameter tables may be placed in any physical location and order within the SFDP address space. The tables are not necessarily adjacent nor in the same order as their header table entries.

The SFDP header points to the following parameter tables:

- Basic Flash
  - This is the original SFDP table. It has a few modified fields and new additional field added at the end of the table.
- 4 Byte Address Instruction
  - This is the original SFDP table. It has a few modified fields and new additional field added at the end of the table.

The physical order of the tables in the SFDP address space is: SFDP Header, Basic Flash Sector Map, 4 Byte Instruction.

The SFDP address space is programmed by Infineon and read-only for the host system.

10.1.1 SFDP address map

The SFDP address space has a header starting at address zero that identifies the SFDP data structure and provides a pointer to each parameter. One basic flash parameter is mandated by the JEDEC JESD216B standard. Optional parameter tables for 4 Byte Address Instructions follow the Basic Flash table.

Table 47 SFDP overview map

Byte address	Description
0000h	Location zero within JEDEC JESD216B SFDP space - start of SFDP header
,,,	Remainder of SFDP header followed by undefined space
0300h	Start of SFDP parameter
...	Remainder of SFDP JEDEC parameter followed by undefined space

10.1.2 SFDP header field definitions

Table 48 SFDP header

SFDP Byte address	SFDP Dword name	Data	Description
00h	SFDP Header 1st DWORD	53h	This is the entry point for Read SFDP (5Ah) command i.e. location zero within SFDP space ASCII “S”
01h		46h	ASCII “F”
02h		44h	ASCII “D”
03h		50h	ASCII “P”
04h	SFDP Header 2nd DWORD	06h	SFDP Minor Revision (06h = JEDEC JESD216 Revision B) This revision is backward compatible with all prior minor revisions. SFDP reading and parsing software will work with higher minor revision numbers than the software was designed to handle. Software designed for a higher revisions must know how to handle earlier revisions. Example: SFDP reading and parsing software for minor revision 0 will still work with minor revision 6. SFDP reading and parsing software for minor revision 6 must be designed to also read minor revision 0 or 5. Do not do a simple compare on the minor revision number, looking only for a match with the revision number that the software is designed to handle. There is no problem with using a higher number minor revision.
05h		01h	SFDP Major Revision This is the original major revision. This major revision is compatible with all SFDP reading and parsing software.
06h		01h	Number of Parameter Headers (zero based, 01h = 2 parameters)
07h		FFh	Unused
08h	Parameter Header 0 1st DWORD	00h	Parameter ID LSB (00h = JEDEC SFDP Basic SPI Flash Parameter)
09h		06h	Parameter Minor Revision (06h = JESD216 Revision B)
0Ah		01h	Parameter Major Revision (01h = The original major revision - all SFDP software is compatible with this major revision.
0Bh		10h	Parameter Table Length (in double words = Dwords = 4 byte units) 10h = 16 Dwords
0Ch	Parameter Header 0 2nd DWORD	00h	Parameter Table Pointer Byte 0 (Dword = 4 byte aligned) JEDEC Basic SPI Flash parameter byte offset = 0300h address
0Dh		03h	Parameter Table Pointer Byte 1
0Eh		00h	Parameter Table Pointer Byte 2
0Fh		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
10h	Parameter Header 1 1st DWORD	84h	Parameter ID LSB (84h = SFDP 4 Byte Address Instructions Parameter)
11h		00h	Parameter Minor Revision (00h = Initial version as defined in JESD216 Revision B)
12h		01h	Parameter Major Revision (01h = The original major revision - all SFDP software that recognizes this parameter’s ID is compatible with this major revision.
13h		02h	Parameter Table Length (in double words = Dwords = 4 byte units) (2h = 2 Dwords)

Table 48 SFDP header (Continued)

SFDP Byte address	SFDP Dword name	Data	Description
14h	Parameter Header 1 2nd DWORD	40h	Parameter Table Pointer Byte 0 (Dword = 4 byte aligned) JEDEC parameter byte offset = 0340h
15h		03h	Parameter Table Pointer Byte 1
16h		00h	Parameter Table Pointer Byte 2
17h		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)

10.1.3 JEDEC SFDP basic SPI flash parameter

Table 49 Basic SPI flash parameter, JEDEC SFDP Rev B

SFDP parameter relative byte address	SFDP Dword name	Data	Description
00h	JEDEC Basic Flash Parameter Dword-1	E5h	Start of SFDP JEDEC parameter Bits 7:5 = unused = 111b Bit 4:3 = 05h is volatile status register write instruction and status register is default non-volatile = 00b Bit 2 = Program Buffer > 64 Bytes = 1 Bits 1:0 = Uniform 4KB erase is supported through out the device = 01b
01h		20h	Bits 15:8 = Uniform 4KB erase instruction = 20h
02h		FBh	Bit 23 = Unused = 1b Bit 22 = Supports QOR (1-1-4) Read, Yes = 1b Bit 21 = Supports QIO (1-4-4) Read, Yes =1b Bit 20 = Supports DIO (1-2-2) Read, Yes = 1b Bit19 = Supports DDR, Yes = 1b Bit 18:17 = Number of Address Bytes, 3 or 4 = 01b Bit 16 = Supports Fast Read SIO and DIO Yes = 1b
03h		FFh	Bits 31:24 = Unused = FFh
04h	JEDEC Basic Flash Parameter Dword-2	FFh	Density in bits, zero based, 128Mb = 07FFFFFFh256Mb = 0FFFFFFFh512Mb = 1FFFFFFFh
05h		FFh	
06h		FFh	
07h		07h 128Mb0Fh 256Mb1Fh 512Mb	
08h	JEDEC Basic Flash Parameter Dword-3	48h	Bits 7:5 = number of QIO Mode cycles = 010b Bits 4:0 = number of Fast Read QIO Dummy cycles = 01000b for default latency code
09h		EBh	Fast Read QIO instruction code
0Ah		08h	Bits 23:21 = number of Quad Out Mode cycles = 000b Bits 20:16 = number of Quad Out Dummy cycles = 01000b for default latency code
0Bh		6Bh	Quad Out instruction code

Table 49 Basic SPI flash parameter, JEDEC SFDP Rev B (Continued)

SFDP parameter relative byte address	SFDP Dword name	Data	Description
0Ch	JEDEC Basic Flash Parameter Dword-4	08h	Bits 7:5 = number of Dual Out Mode cycles = 000b Bits 4:0 = number of Dual Out Dummy cycles = 01000b for default latency code
0Dh		3Bh	Dual Out instruction code
0Eh		88h	Bits 23:21 = number of Dual I/O Mode cycles = 100b Bits 20:16 = number of Dual I/O Dummy cycles = 01000b for default latency code
0Fh		BBh	Dual I/O instruction code
10h	JEDEC Basic Flash Parameter Dword-5	FEh	Bits 7:5 RFU = 111b Bit 4 = QPI supported = 1b Bits 3:1 RFU = 111b Bit 0 = Dual All not supported = 0b
11h		FFh	Bits 15:8 = RFU = FFh
12h		FFh	Bits 23:16 = RFU = FFh
13h		FFh	Bits 31:24 = RFU = FFh
14h	JEDEC Basic Flash Parameter Dword-6	FFh	Bits 7:0 = RFU = FFh
15h		FFh	Bits 15:8 = RFU = FFh
16h		FFh	Bits 23:21 = number of Dual All Mode cycles = 111b Bits 20:16 = number of Dual All Dummy cycles = 11111b
17h		FFh	Dual All instruction code
18h	JEDEC Basic Flash Parameter Dword-7	FFh	Bits 7:0 = RFU = FFh
19h		FFh	Bits 15:8 = RFU = FFh
1Ah		48h	Bits 23:21 = number of QPI Mode cycles = 010b Bits 20:16 = number of QPI Dummy cycles = 01000b for default latency code
1Bh		EBh	QPI Fast Read instruction code (Same as QIO when QPI is enabled)
1Ch	JEDEC Basic Flash Parameter Dword-8	0Ch	Sector type 1 size 2^N Bytes = 4KB = 0Ch (for Uniform 4KB)
1Dh		20h	Sector type 1 instruction
1Eh		0Fh	Sector type 2 size 2^N Bytes = 32KB = 0Fh (for Uniform 32KB)
1Fh		52h	Sector type 2 instruction
20h	JEDEC Basic Flash Parameter Dword-9	10h	Sector type 3 size 2^N Bytes = 64KB = 10h (for Uniform 64KB)
21h		D8h	Sector type 3 instruction
22h		00h	Sector type 4 size 2^N Bytes = not supported = 00h
23h		FFh	Sector type 4 instruction = not supported = FFh

Table 49 Basic SPI flash parameter, JEDEC SFDP Rev B (Continued)

SFDP parameter relative byte address	SFDP Dword name	Data	Description
24h	JEDEC Basic Flash Parameter Dword-10	21h	Bits 31:30 = Sector Type 4 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = RFU = 11b Bits 29:25 = Sector Type 4 Erase, Typical time count = RFU = 1_1111b (typ erase time = count +1 * units = RFU =11111) Bits 24:23 = Sector Type 3 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 16ms = 01b Bits 22:18 = Sector Type 3 Erase, Typical time count = 1_0000b (typ erase time = count +1 * units = 17 * 16 ms = 272 ms) Bits 17:16 = Sector Type 2 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 16 ms = 01b Bits 15:11 = Sector Type 2 Erase, Typical time count = 0_1011b (typ erase time = count +1 * units = 12 * 16 ms = 192 ms) Bits 10:9 = Sector Type 1 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 16 ms = 01b Bits 8:4 = Sector Type 1 Erase, Typical time count = 0_0010b (typ erase time = count +1 * units = 3 * 16 ms = 48 ms) Bits 3:0 = Count = (Max Erase time / (2 * Typical Erase time)) – 1 = 0001b Multiplier from typical erase time to maximum erase time = 4x multiplier Max Erase time = 2 * (Count + 1) * Typ Erase time Binary Fields: 11-11111-01-10000-01-01011-01-00010-0001 Nibble Format: 1111_1110_1100_0001_0101_1010_0010_0001 Hex Format: FE_C1_5A_21
25h		5Ah	
26h		C1h	
27h		FEh	
28h	JEDEC Basic Flash Parameter Dword-11	81h	Bits 23 = Byte Program Typical time, additional byte units (0b:1 µs, 1b:8 µs) = 1 µs = 0b Bits 22:19 = Byte Program Typical time, additional byte count, (count + 1) * units, count = 0101b, (typ Program time = count + 1 * units = 6 * 1 µs = 6 µs Bits 18 = Byte Program Typical time, first byte units (0b:1 µs, 1b:8 µs) = 1 µs = 0b Bits 17:14 = Byte Program Typical time, first byte count, (count + 1) * units, count = 0111b, (typ Program time = count + 1 * units = 8 * 1 µs = 8 µs Bits 13 = Page Program Typical time units (0b:8 µs, 1b:64 µs) = 64 µs = 1b Bits 12:8 = Page Program Typical time count, (count + 1) * units, count = 00100b, (typ Program time = count + 1 * units = 5 * 64 µs = 320 µs) Bits 7:4 = N = 1000b, Page size= 2^N = 256B page Bits 3:0 = Count = 0001b = (Max Page Program time / (2 * Typ Page Program time)) – 1 Multiplier from typical Page Program time to maximum Page Program time = 4x multiplier Max Page Program time = 2 * (Count + 1) * Typ Page Program time Binary Fields: 0-0101-0-0111-1-00100-1000-0001 Nibble Format: 0010_1001_1110_0100_1000_0001 Hex Format: 29_74_81
29h		E4h	
2Ah		29h	

Table 49 Basic SPI flash parameter, JEDEC SFDP Rev B (Continued)

SFDP parameter relative byte address	SFDP Dword name	Data	Description
2Bh	JEDEC Basic Flash Parameter Dword-11	D1h 128Mb E2h 256Mb	128Mb = 1101_0001b = D1h Bit 31 Reserved = 1b Bits 30:29 = Chip Erase, Typical time units (00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s) = 4s = 10b Bits 28:24 = Chip Erase, Typical time count, (count+1)*units, count = 10001b, (typ Program time = count +1 * units = 18 * 4s = 72 s 256Mb = 1110_0010b = E2h Bit 31 Reserved = 1b Bits 30:29 = Chip Erase, Typical time units (00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s) = 64s = 11b Bits 28:24 = Chip Erase, Typical time count, (count + 1) * units, count = 00010b, (typ Program time = count + 1 * units = 3 * 64 s = 192 s

Table 49 Basic SPI flash parameter, JEDEC SFDP Rev B (Continued)

SFDP parameter relative byte address	SFDP Dword name	Data	Description
2Ch	JEDEC Basic Flash Parameter Dword-12	CCh	Bit 31 = Suspend and Resume supported = 0b Bits 30:29 = Suspend in-progress erase max latency units (00b: 128 ns, 01b: 1µs, 10b: 8 µs, 11b: 64 µs) = 8 µs = 10b Bits 28:24 = Suspend in-progress erase max latency count = 00100b, max erase suspend latency = count +1 * units = 5 * 8 µs = 40 µs Bits 23:20 = Erase resume to suspend interval count = 0001b, interval = count +1 * 64 µs = 2 * 64 µs = 128 µs Bits 19:18 = Suspend in-progress program max latency units (00b: 128 ns, 01b: 1 µs, 10b: 8 µs, 11b: 64 µs) = 8 µs = 10b Bits 17:13 = Suspend in-progress program max latency count = 00100b, max erase suspend latency = count +1 * units = 5 * 8 µs = 40 µs Bits 12:9 = Program resume to suspend interval count = 0001b, interval = count +1 * 64 µs = 2 * 64 µs = 128 µs Bit 8 = RFU = 1b Bits 7:4 = Prohibited operations during erase suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx0xb: May not initiate a page program anywhere + x1xxb: May not initiate a read in the erase suspended sector size + 1xxxb: The erase and program restrictions in bits 5:4 are sufficient = 1100b Bits 3:0 = Prohibited Operations During Program Suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx0xb: May not initiate a new page program anywhere (program nesting not permitted) + x1xxb: May not initiate a read in the program suspended page size + 1xxxb: The erase and program restrictions in bits 1:0 are sufficient = 1100b Binary Fields: 0-10-00100-0001-10-00100-0001-1-1100-1100 Nibble Format: 0100_0100_0001_1000_1000_0011_1100_1100 Hex Format: 44_18_83_CC
2Dh		83h	
2Eh		18h	
2Fh		44h	
30h	JEDEC Basic Flash Parameter Dword-13	7Ah	Bits 31:24 = Erase Suspend Instruction = 75h Bits 23:16 = Erase Resume Instruction = 7Ah Bits 15:8 = Program Suspend Instruction = 75h Bits 7:0 = Program Resume Instruction = 7Ah
31h		75h	
32h		7Ah	
33h		75h	

Table 49 Basic SPI flash parameter, JEDEC SFDP Rev B (Continued)

SFDP parameter relative byte address	SFDP Dword name	Data	Description
34h	JEDEC Basic Flash Parameter Dword-14	F7h	Bit 31 = Deep Power Down Supported = supported = 0 Bits 30:23 = Enter Deep Power Down Instruction = B9h = 1011_1001b Bits 22:15 = Exit Deep Power Down Instruction = ABh = 1010_1011b Bits 14:13 = Exit Deep Power Down to next operation delay units = (00b: 128 ns, 01b: 1 µs, 10b: 8 µs, 11b: 64 µs) = 1 µs = 01b Bits 12:8 = Exit Deep Power Down to next operation delay count = 00010b, Exit Deep Power Down to next operation delay = (count + 1) * units = 3 * 1 µs = 3 µs Bits 7:4 = RFU = Fh Bit 3:2 = Status Register Polling Device Busy = 01b: Legacy status polling supported = Use legacy polling by reading the Status Register with 05h instruction and checking WIP bit[0] (0=ready; 1=busy). Bits 1:0 = RFU = 11b Binary Fields: 0-10111001-10101011-01-00010-1111-01-11 Nibble Format: 0101_1100_1101_0101_1010_0010_1111_0111 Hex Format: 5C_D5_A2_F7
35h		A2h	
36h		D5h	
37h		5Ch	
38h	JEDEC Basic Flash Parameter Dword-15	22h	Bits 31:24 = RFU = FFh Bit 23 = Hold and WP Disable = not supported = 0b Bits 22:20 = Quad Enable Requirements = 101b: QE is bit 1 of the status register 2. Status register 1 is read using Read Status instruction 05h. Status register 2 is read using instruction 35h. QE is set via Write Status instruction 01h with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. Bits 19:16 0-4-4 Mode Entry Method = xxx1b: Mode Bits[7:0] = A5h Note: QE must be set prior to using this mode + x1xxb: Mode Bits[7:0] = Axh + 1xxxb: RFU = 1101b Bits 15:10 0-4-4 Mode Exit Method = xx_xxx1b: Mode Bits[7:0] = 00h will terminate this mode at the end of the current read operation + xx_1xxxb: Input Fh (mode bit reset) on DQ0-DQ3 for 8 clocks. This will terminate the mode prior to the next read operation. + 11_x1xx: RFU = 111101 Bit 9 = 0-4-4 mode supported = 1 Bits 8:4 = 4-4-4 mode enable sequences = 0_0010b: issue instruction 38h Bits 3:0 = 4-4-4 mode disable sequences = 0010b: 4-4-4 issues F5h instruction Binary Fields: 11111111-0-101-1101-111101-1-00010-0010 Nibble Format: 1111_1111_0101_1101_1111_0110_0010_0010 Hex Format: FF_5D_F6_22
39h		F6h	
3Ah		5Dh	
3Bh		FFh	

Table 49 Basic SPI flash parameter, JEDEC SFDP Rev B (Continued)

SFDP parameter relative byte address	SFDP Dword name	Data	Description
3Ch	JEDEC Basic Flash Parameter Dword-16	E8h	Bits 31:24 = Enter 4-Byte Addressing = xxxx_xxx1b:issue instruction B7 (preceding write enable not required = xxxx_1xxxb: 8-bit volatile bank register used to define A[30:24] bits. MSb (bit[7]) is used to enable/disable 4-byte address mode. When MSb is set to '1', 4-byte address mode is active and A[30:24] bits are don't care. Read with instruction 16h. Write instruction is 17h with 1 byte of data. When MSb is cleared to '0', select the active 128 Mb segment by setting the appropriate A[30:24] bits and use 3-Byte addressing. + xx1x_xxxxb: Supports dedicated 4-Byte address instruction set. Consult vendor data sheet for the instruction set definition or look for 4 Byte Address Parameter Table. + 1xxx_xxxxb: Reserved = 10100001b Bits 23:14 = Exit 4-Byte Addressing = xx_xxxx_xxx1b:issue instruction E9h to exit 4-Byte address mode (Write enable instruction 06h is not required) = xx_xxxx_1xxxb: 8-bit volatile bank register used to define A[30:24] bits. MSb (bit[7]) is used to enable/disable 4-byte address mode. When MSb is cleared to '0', 3-byte address mode is active and A30:A24 are used to select the active 128 Mb memory segment. Read with instruction 16h. Write instruction is 17h, data length is 1 byte. + xx_xx1x_xxxxb: Hardware reset + xx_x1xx_xxxxb: Software reset (see bits 13:8 in this DWORD) + xx_1xxx_xxxxb: Power cycle + x1_xxxx_xxxxb: Reserved + 1x_xxxx_xxxxb: Reserved = 1111100001b Bits 13:8 = Soft Reset and Rescue Sequence Support = x1_xxxxb: issue reset enable instruction 66h, then issue reset instruction 99h. The reset enable, reset sequence may be issued on 1,2, or 4 wires depending on the device operating mode = 010000b Bit 7 = RFU = 1 Bits 6:0 = Volatile or Non-Volatile Register and Write Enable Instruction for Status Register 1 = xxx_1xxxb: Non-Volatile/Volatile status register 1 powers-up to last written value in the non-volatile status register, use instruction 06h to enable write to non-volatile status register. Volatile status register may be activated after power-up to override the non-volatile status register, use instruction 50h to enable write and activate the volatile status register. + x1x_xxxxb: Reserved + 1xx_xxxxb: Reserved = 1101000b Binary Fields: 10100001-1111100001-010000-1-1101000 Nibble Format: 1010_0001_1111_1000_0101_0000_1110_1000 Hex Format: A1_F8_60_E8
3Dh		50h	
3Eh		F8h	
3Fh		A1h	

10.1.4 JEDEC SFDP 4-byte address instruction table

Table 50 4-byte address instruction, JEDEC SFDP Rev B

SFDP parameter relative byte address	SFDP Dword name	Data	Description
40h	JEDEC 4 Byte Address Instructions Parameter Dword-1h	FBh	Supported = 1, Not Supported = 0 Bits 31:20 = RFU = FFFh Bit 19 = Support for non-volatile individual sector lock write command, Instruction = E3h = 0 Bit 18 = Support for non-volatile individual sector lock read command, Instruction = E2h = 0 Bit 17 = Support for volatile individual sector lock Write command, Instruction = E1h = 1 Bit 16 = Support for volatile individual sector lock Read command, Instruction = E0h = 1 Bit 15 = Support for (1-4-4) DTR_Read Command, Instruction = EEh = 1 Bit 14 = Support for (1-2-2) DTR_Read Command, Instruction = BEh = 0 Bit 13 = Support for (1-1-1) DTR_Read Command, Instruction = 0Eh = 0 Bit 12 = Support for Erase Command – Type 4 = 0 Bit 11 = Support for Erase Command – Type 3 = 1 Bit 10 = Support for Erase Command – Type 2 = 1 Bit 9 = Support for Erase Command – Type 1 = 1 Bit 8 = Support for (1-4-4) Page Program Command, Instruction = 3Eh =0 Bit 7 = Support for (1-1-4) Page Program Command, Instruction = 34h = 1 Bit 6 = Support for (1-1-1) Page Program Command, Instruction = 12h = 1 Bit 5 = Support for (1-4-4) FAST_READ Command, Instruction = ECh = 1 Bit 4 = Support for (1-1-4) FAST_READ Command, Instruction = 6Ch = 1 Bit 3 = Support for (1-2-2) FAST_READ Command, Instruction = BCh = 1 Bit 2 = Support for (1-1-2) FAST_READ Command, Instruction = 3Ch = 0 Bit 1 = Support for (1-1-1) FAST_READ Command, Instruction = 0Ch = 1 Bit 0 = Support for (1-1-1) READ Command, Instruction = 13h = 1 Nibble Format: 1111_1111_1111_0011_1000_1110_1111_1011 Hex Format: FF_F3_8E_FB
41h		8Eh	
42h		F3h	
43h		FFh	
44h	JEDEC 4 Byte Address Instructions Parameter Dword-2h	21h	Bits 31:24 = FFh = Instruction for Erase Type 4: RFU Bits 23:16 = DCh = Instruction for Erase Type 3 Block Bits 15:8 = 52h = Instruction for Erase Type 2 Half Block Bits 7:0 = 21h = Instruction for Erase Type 1 Sector
45h		52h	
46h		DCh	
47h		FFh	

10.2 Device ID address map

10.2.1 Field definitions

Table 51 Manufacturer device type

Byte address	Data	Description
00h	01h	Manufacturer ID for Infineon
01h	60h	Device ID MSB - Memory Interface Type
02h	18h (128Mb) 19h (256Mb)	Device ID LSB - Density and Features
03h	Undefined	Reserved for Future Use

Table 52 Unique Device ID

Byte address	Data	Description
00h to 07	8 Byte Unique Device ID	64-bit unique ID number, see section **"Device Unique ID"** on page 31.

10.3 Initial delivery state

The device is shipped from Infineon with non-volatile bits set as follows:

- The entire memory array is erased: i.e. all bits are set to 1 (each byte contains FFh).
- The Security Region address space has all bytes erased to FFh.
- The SFDP address space contains the values as defined in the description of the SFDP address space.
- The ID address space contains the values as defined in the description of the ID address space.
- The Status Register 1 Non-volatile contains 00h (all SR1NV bits are cleared to 0's).
- The Configuration Register 1 Non-volatile contains 00h.
- The Configuration Register 2 Non-volatile contains 60h.
- The Configuration Register 3 Non-volatile contains 78h.
- The Password Register contains FFFFFFFF-FFFFFFFFh.
- The IRP Register bits are FFFDh for Standard Part and FFFFh for High Security Part.
- The PRPR Register bits are FFFFFFh.

11 Electrical specifications

11.1 Absolute maximum ratings

Description	Min
Storage temperature plastic packages	–65°C to +150°C
Ambient temperature with power applied	–65°C to +125°C
V_{CC}	–0.5 V to +4.0 V
Input voltage with respect to Ground (V_{SS})[62]	–0.5 V to V_{CC} + 0.5 V
Output short circuit current[63]	100 mA

11.2 Latchup characteristics

Table 53 Latchup specification[65]

Description	Min	Max	Unit
Input voltage with respect to V_{SS} on all input only connections	–1.0	V_{CC} + 1.0	V
Input voltage with respect to V_{SS} on all I/O connections			
V_{CC} current	–100	+100	mA

11.3 Thermal resistance

Table 54 Thermal resistance

Parameter	Description	Test conditions	Device	SO3016	SOC008	WND008	FAB024	FAC024	WNG008	Unit
Theta JA	Thermal resistance (Junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance in accordance with EIA/JESD51, with still air (0 m/s).	128 Mb	42	63	32	39	39	–	°C/W
			256 Mb	35.8	–	–	34.5	34.5	28	
Theta JB	Thermal resistance (Junction to board)		128 Mb	23	37	7.5	23.9	23.9	–	
			256 Mb	16.6	–	–	18.3	18.3	11.7	
Theta JC	Thermal resistance (Junction to case)		128 Mb	12	30.4	23.9	14	14	–	
			256 Mb	10.2	–	–	10.3	10.3	13.1	

Notes

62. See **"Input signal overshoot"** on page 149 for allowed maximums during signal transition.
63. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
64. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.
65. Excludes power supply V_{CC}. Test conditions: V_{CC} = 3.0 V, one connection at a time tested, connections not being tested are at V_{SS}.

11.4 Operating ranges

Operating ranges define those limits between which the functionality of the device is guaranteed.

11.4.1 Power supply voltages

Table 55 Power supply voltages

V_{CC}
2.7 V to 3.6 V

11.4.2 Temperature ranges

Table 56 Temperature ranges

Parameter	Symbol	Devices	Spec		Unit
			Min	Max	
Ambient temperature	T_A	Industrial (I)	–40	+85	°C
		Industrial Plus (V)		+105	
		Extended (N)		+125	
		Automotive, AEC-Q100 grade 3 (A)		+85	
		Automotive, AEC-Q100 grade 2 (B)		+105	
		Automotive, AEC-Q100 grade 1 (M)		+125	

11.4.3 Input signal overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{CC}. During voltage transitions, inputs or I/Os may overshoot V_{SS} to –1.0 V or overshoot to V_{CC} + 1.0 V, for periods up to 20 ns.

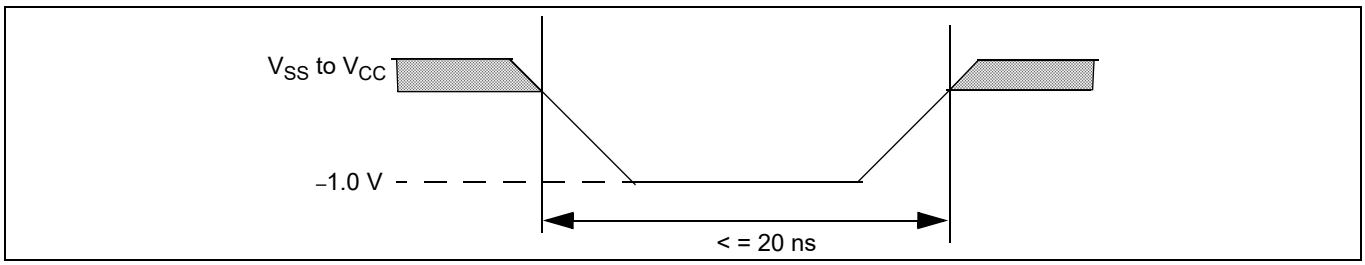


Figure 129 Maximum negative overshoot waveform

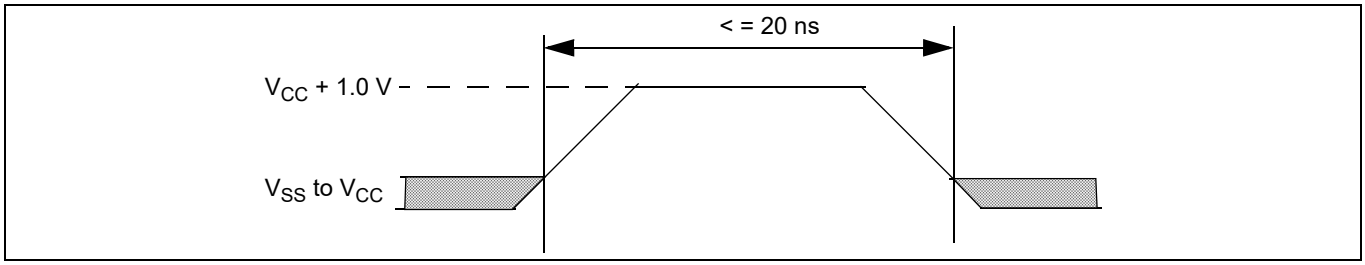


Figure 130 Maximum positive overshoot waveform

11.5 Power-up and power-down

The device must not be selected at power-up or power-down (that is, CS# must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value as follows:

- V_{CC} (min) at power-up, and then for a further delay of t_{PU}
- V_{SS} at power-down

User is not allowed to enter any command until a valid delay of t_{PU} has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold (see **Figure 131**). However, correct operation of the device is not guaranteed if V_{CC} returns below V_{CC} (min) during t_{PU}. No command should be sent to the device until the end of t_{PU}.

The device draws I_{POR} during t_{PU}. After power-up (t_{PU}), the device is in Standby mode, draws CMOS standby current (I_{SB}), and the WEL bit is reset.

During power-down or if supply voltage drops below V_{CC}(cut-off), the supply voltage must stay below V_{CC}(low) for a period of t_{PD} for the part to initialize correctly on power-up (see **Figure 132**). If during a voltage drop the V_{CC} stays above V_{CC} (cut-off), the part will stay initialized and will work correctly when V_{CC} is again above V_{CC} (min). In the event power-on reset (POR) did not complete correctly after power up, the assertion of the RESET# signal or receiving a software reset command (RSTEN 66h followed by RST 99h) will restart the POR process.

If V_{CC} drops below the $V_{CC\ (Cut\text{-}off)}$ during an embedded program or erase operation the embedded operation may be aborted and the data in that memory area may be incorrect.

Normal precautions must be taken for supply rail decoupling to stabilize the V_{CC} supply at the device. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package supply connection (this capacitor is generally of the order of 0.1 µF).

Table 57 Power-up / power-down voltage and timing

Symbol	Parameter	Min	Max	Unit
V_{CC} (min)	V_{CC} (minimum operation voltage)	2.7	–	V
V_{CC} (cut-off)	V_{CC} (Cut 0ff where re-initialization is needed)	2.4	–	
V_{CC} (low)	V_{CC} (low voltage for initialization to occur)	1.0	–	
t_{PU}	V_{CC} (min) to Read operation	–	300	µs
t_{PD}	V_{CC} (low) time	10.0	–	

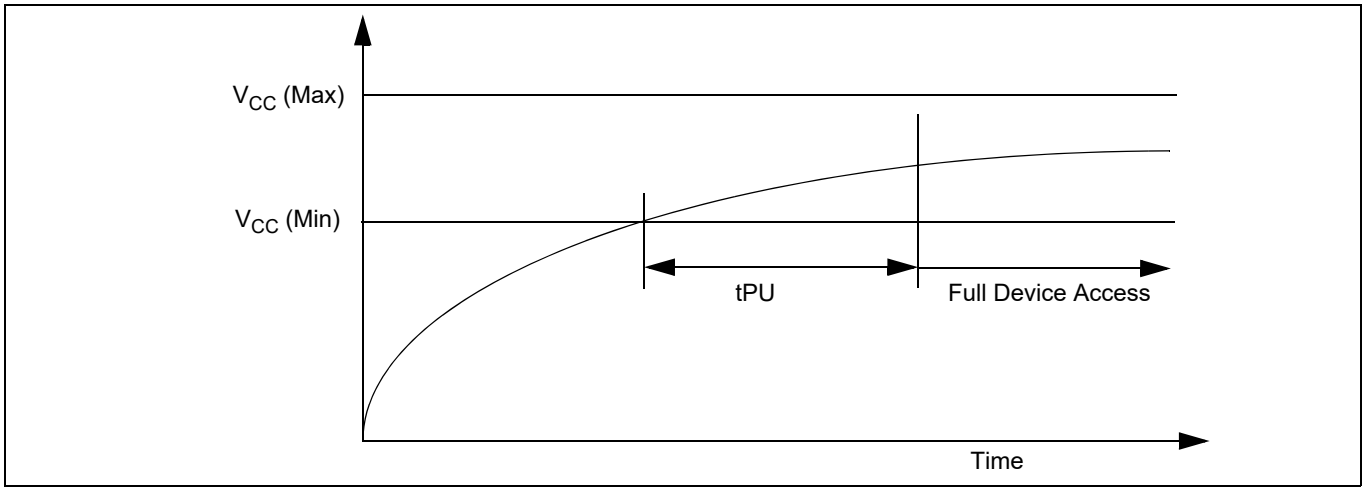


Figure 131 Power-up

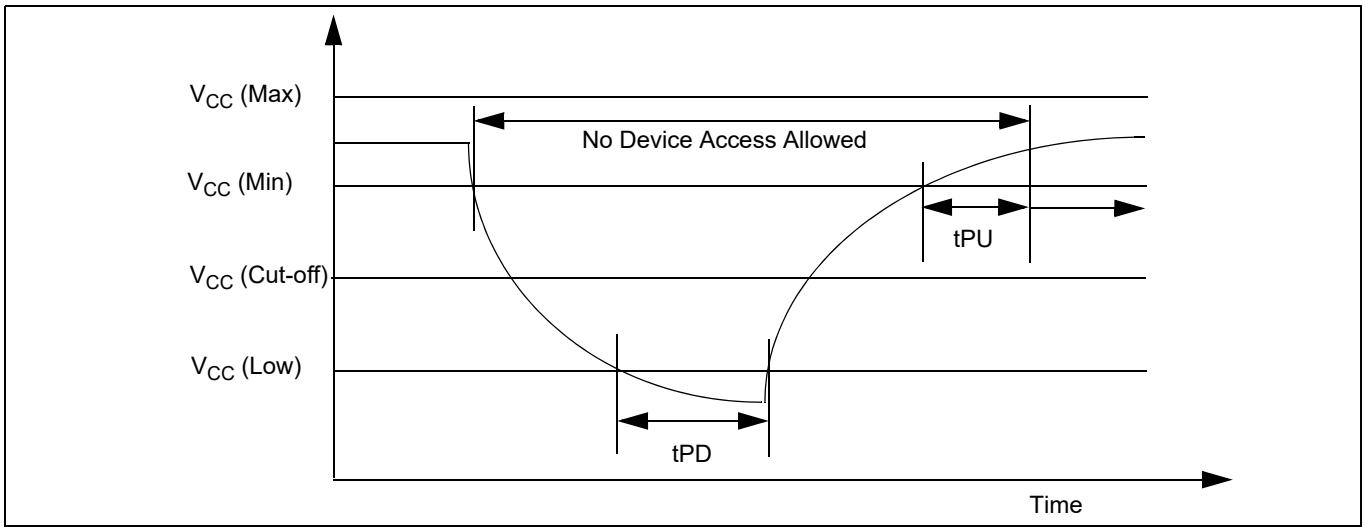


Figure 132 Power-down and voltage drop

11.6 DC characteristics

Table 58 DC characteristics — operating temperature range –40°C to +85°C

Symbol	Parameter	Test conditions	Min	Typ[66]	Max	Unit
V_{IL}	Input low voltage	–	–0.5		$0.3 \times V_{CC}$	V
V_{IH}	Input high voltage	–	$0.7 \times V_{CC}$		$V_{CC} + 0.4$	
V_{OL}	Output low voltage	I_{OL} = 0.1 mA, $V_{CC} = V_{CC}$ min	–		0.2	
V_{OH}	Output high voltage	I_{OH} = –0.1 mA	V_{CC} – 0.2		–	
I_{LI}	Input leakage current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{IH}$ or V_{SS}, CS# = V_{IH}		–	±2	µA
I_{LO}	Output leakage current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{IH}$ or V_{SS}, CS# = V_{IH}			±2	
I_{CC1}	Active power supply current (READ)[67]	Serial SDR @ 5 MHz	–	10	15	mA
		Serial SDR @ 10 MHz		10	15	
		Serial SDR @ 20 MHz		10	15	
		Serial SDR @ 50 MHz		15	20	
		Serial SDR @ 108 MHz		20	25	
		Serial SDR @ 133 MHz		22	30	
		QIO/QPI SDR @ 108 MHz		25	30	
		QIO/QPI SDR @ 133 MHz		30	35	
		QIO/QPI DDR @ 30 MHz		15	20	
		QIO/QPI DDR @ 66 MHz		22	25	
I_{CC2}	Active power supply current (Page Program)	CS# = V_{CC}		40	50	
I_{CC3}	Active power supply current (WRR or WRAR)			24	30	
I_{CC4}	Active power supply current (SE)			20	25	
I_{CC5}	Active power supply current (HBE, BE)			25	35	
I_{SB}	Standby current	RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}: SPI, Dual I/O and Quad I/O Modes		20	35	µA
		RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}: QPI Mode		40	60	
I_{DPD}	Deep power down current	RESET#, CS# = V_{CC}; V_{IN} = GND or V_{CC}		2	20	
I_{POR}	Power on reset current	RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}		15	30	mA

Notes
66. Typical values are at T_{AI} = 25°C and V_{CC} = 3.0 V.
67. Outputs unconnected during read data return. Output switching current is not included.

Table 59 DC characteristics — operating temperature range –40°C to +105°C

Symbol	Parameter	Test conditions	Min	Typ[68]	Max	Unit
V_{IL}	Input low voltage	–	–0.5		$0.3 \times V_{CC}$	V
V_{IH}	Input high voltage	–	$0.7 \times V_{CC}$		$V_{CC} + 0.4$	
V_{OL}	Output low voltage	I_{OL} = 0.1 mA, $V_{CC} = V_{CC}$ min	–		0.2	
V_{OH}	Output high voltage	I_{OH} = –0.1 mA	V_{CC} – 0.2		–	
I_{LI}	Input leakage current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{IH}$ or V_{SS}, CS# = V_{IH}		–	±4	µA
I_{LO}	Output leakage current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{IH}$ or V_{SS}, CS# = V_{IH}			±4	
I_{CC1}	Active power supply current (READ)[69]	Serial SDR @ 5 MHz Serial SDR @ 10MHz Serial SDR @ 20 MHz Serial SDR @ 50 MHz Serial SDR @ 108Mhz Serial SDR @133MHz QIO/QPI SDR @ 108MHz QIO/QPI SDR @ 133 MHz QIO/QPI DDR @ 30MHz QIO/QPI DDR @ 66 MHz	–	10 10 10 15 20 22 25 30 15 22	15 15 15 20 30 30 35 35 20 25	mA
I_{CC2}	Active power supply current (Page Program)	CS# = V_{CC}		40	50	
I_{CC3}	Active power supply current (WRR or WRAR)			24	35	
I_{CC4}	Active power supply current (SE)			20	30	
I_{CC5}	Active power supply current (HBE, BE)			25	35	
I_{SB}	Standby current	RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}: SPI, Dual I/O and Quad I/O Modes		20	45	µA
		RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}: QPI Mode		40	80	
I_{DPD}	Deep power down current	RESET#, CS# = V_{CC}; V_{IN} = GND or V_{CC}		2	30	
I_{POR}	Power on reset current	RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}		15	30	mA

Notes
68.Typical values are at T_{AI} = 25°C and V_{CC} = 3.0 V.
69.Outputs unconnected during read data return. Output switching current is not included.

Table 60 DC characteristics — Operating temperature range –40°C to +125°C

Symbol	Parameter	Test conditions	Min	Typ[70]	Max	Unit
V_{IL}	Input low voltage	–	–0.5		$0.3 \times V_{CC}$	V
V_{IH}	Input high voltage	–	$0.7 \times V_{CC}$		$V_{CC} + 0.4$	
V_{OL}	Output low voltage	I_{OL} = 0.1 mA, $V_{CC} = V_{CC}$ min	–		0.2	
V_{OH}	Output high voltage	I_{OH} = –0.1 mA	V_{CC} – 0.2		–	
I_{LI}	Input leakage current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{IH}$ or V_{SS}, CS# = V_{IH}		–	±4	µA
I_{LO}	Output leakage current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{IH}$ or V_{SS}, CS# = V_{IH}			±4	
I_{CC1}	Active power supply current (READ)[71]	Serial SDR @ 5 MHz Serial SDR @ 10MHz Serial SDR @ 20 MHz Serial SDR @ 50 MHz Serial SDR @ 108Mhz Serial SDR @ 133MHz QIO/QPI SDR @ 108MHz QIO/QPI SDR @ 133 MHz QIO/QPI DDR @ 30MHz QIO/QPI DDR @ 66 MHz		10 10 10 15 20 22 25 30 15 22	15 15 15 20 30 30 35 35 20 25	mA
I_{CC2}	Active power supply current (Page Program)	CS# = V_{CC}	–	40	50	
I_{CC3}	Active power supply current (WRR or WRAR)			24	35	
I_{CC4}	Active power supply current (SE)			20	30	
I_{CC5}	Active power supply current (HBE, BE)			25	35	
I_{SB}	Standby current	RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}: SPI, Dual I/O and Quad I/O Modes		20	70	µA
		RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}: QPI Mode		40	80	
I_{DPD}	Deep power down current	RESET#, CS# = V_{CC}; V_{IN} = GND or V_{CC}		2	50	
I_{POR}	Power on reset current	RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}		15	35	mA

Notes
70.Typical values are at T_{AI} = 25°C and V_{CC} = 1.8 V.
71.Outputs unconnected during read data return. Output switching current is not included.

11.6.1 Active power and standby power modes

The device is enabled and in the Active Power mode when Chip Select (CS#) is Low. When CS# is HIGH, the device is disabled, but may still be in an Active Power mode until all program, erase, and write operations have completed. The device then goes into the Standby Power mode, and power consumption drops to I_{SB}.

11.6.2 Deep power down power mode (DPD)

The Deep Power Down mode is enabled by inputing the command instruction code “B9h” and the power consumption drops to I_{DPD}. In DPD mode, the device responds only to the Resume from DPD command (RES ABh) or Hardware reset (RESET# and IO3 / RESET#). All other commands are ignored during DPD mode.

12 Timing specifications

12.1 Key to switching waveforms

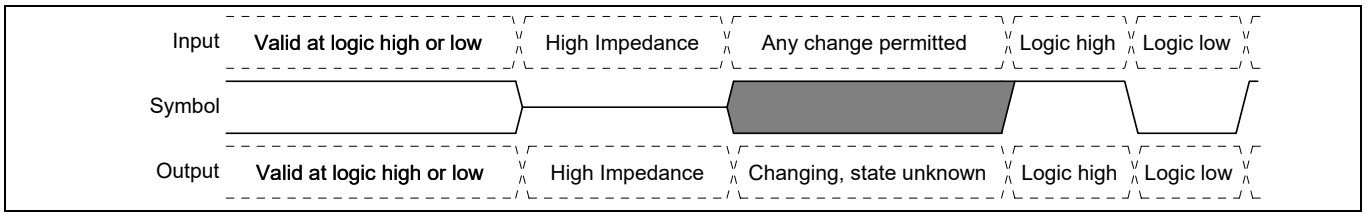


Figure 133 Waveform element meanings

12.2 AC test conditions

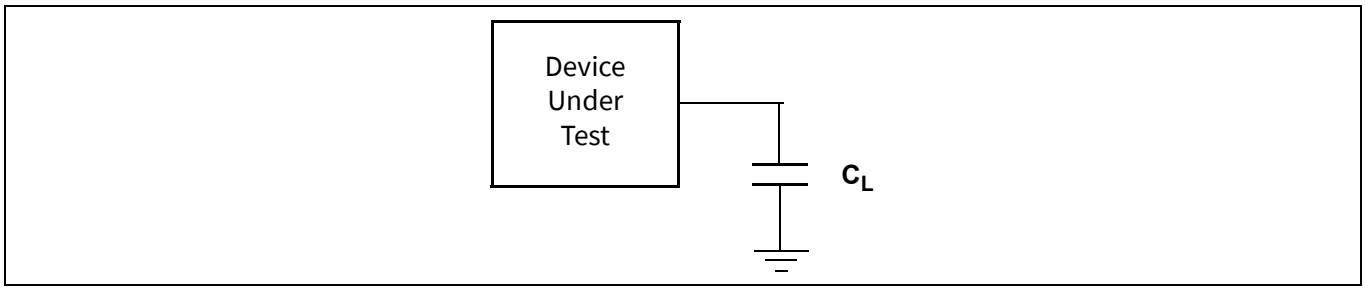


Figure 134 Test setup

Table 61 AC measurement conditions

Symbol	Parameter	Min	Max	Unit
C_L	Load capacitance	–	15 / 30[72]	pF
–	Input pulse voltage	0.2 × V_{CC}	0.8 × V_{CC}	V
–	Input timing ref voltage	0.5 × V_{CC}		
–	Output timing ref voltage			

Notes
72. Load capacitance depends on the operation frequency or mode of operation.
73. AC characteristics tables assume clock and data signals have the same slew rate (slope). See **"SDR AC characteristics"** on page 160 note [77] for slew rates at operating frequencies.

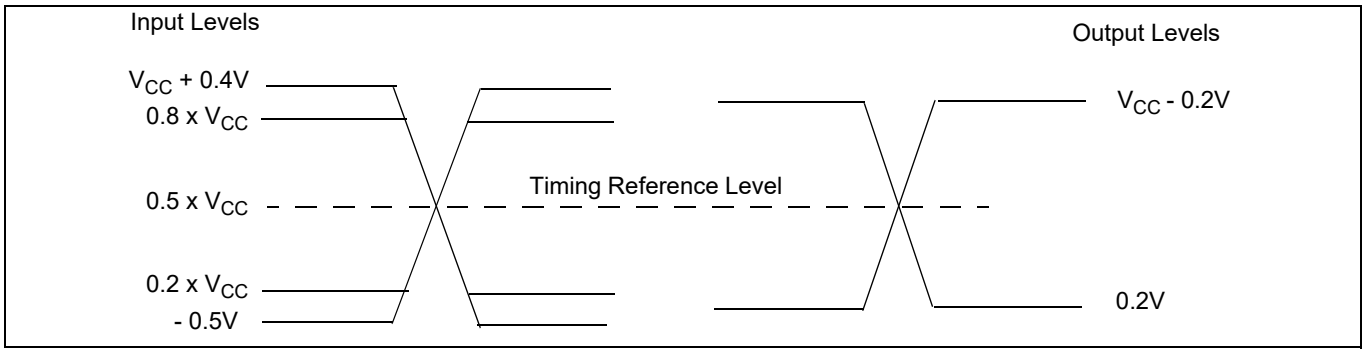


Figure 135 Input, output, and timing reference levels

12.2.1 Capacitance characteristics

Table 62 Capacitance

Symbol	Parameter	Test conditions	Min	Max	Unit
C_{IN}	Input capacitance (applies to SCK, CS#, RESET#, IO3 / RESET#)	1 MHz	–	8	pF
C_{OUT}	Output capacitance (applies to All I/O)				

12.3 Reset

If a Hardware Reset is initiated during a Erase, Program or writing of a Register operation the data in that Sector, Page or Register is not stable, the operation that was interrupted needs to be initiated again. If a Hardware Reset is initiated during a Software Reset operation, the Hardware Reset might be ignored.

12.3.1 Power-on (cold) reset

The device executes a POR process until a time delay of t_{PU} has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold. See **Figure 131** and **Table 57**. The device must not be selected (CS# to go high with V_{CC}) during power-up (t_{PU}), i.e. no commands may be sent to the device until the end of t_{PU}.

RESET# and IO3 / RESET# reset function is ignored during POR. If RESET# or IO3 / RESET# is low during POR and remains low through and beyond the end of t_{PU}, CS# must remain high until t_{RH} after RESET# and IO3 / RESET# returns high. RESET# and IO3 / RESET# must return high for greater than t_{RS} before returning low to initiate a hardware reset.

The IO3 / RESET# input functions as the RESET# signal when CS# is HIGH for more than t_{CS} time or when Quad or QPI mode is not enabled CR1V[1] = 0 or CR2V[3] = 0.

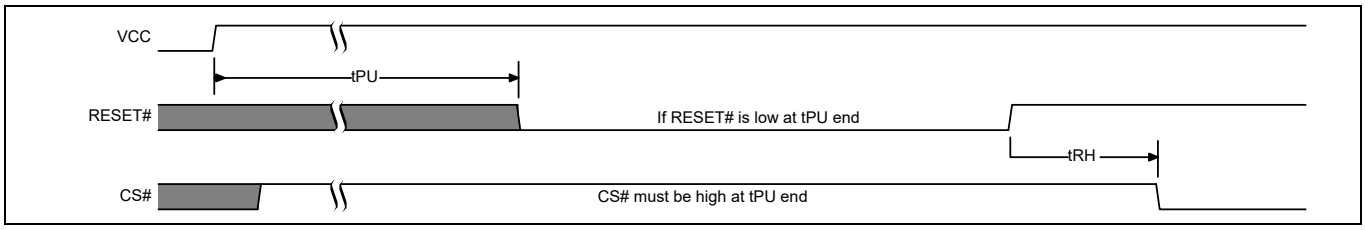


Figure 136 Reset low at the end of POR

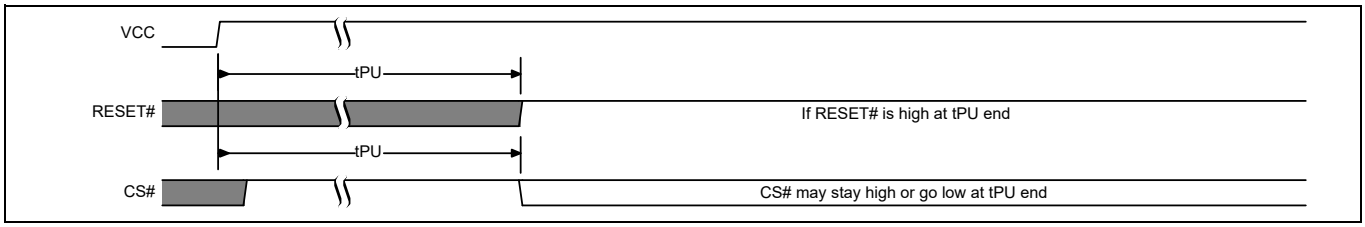


Figure 137 Reset high at the end of POR

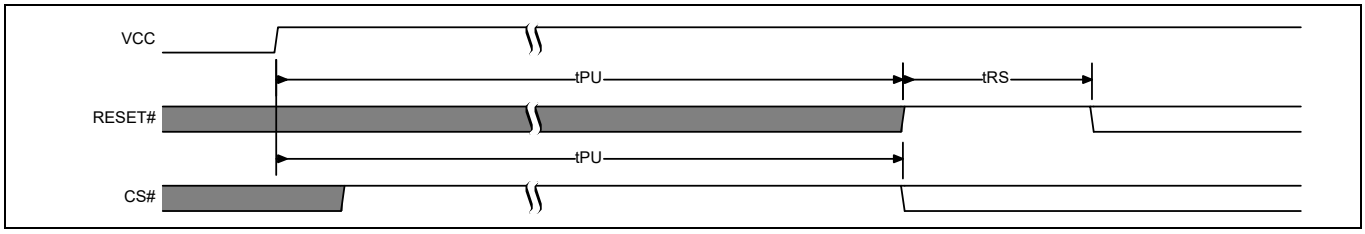


Figure 138 POR followed by hardware reset

12.3.2 RESET # and IO3 / RESET# input initiated hardware (warm) reset

The RESET# and IO3 / RESET# inputs can function as the RESET# signal. Both inputs can initiate the reset operation under conditions.

The RESET# input initiates the reset operation when transitions from V_{IH} to V_{IL} for > t_{RP}, the device will reset register states in the same manner as POR but, does not go through the full reset process that is performed during POR. The hardware reset process requires a period of t_{RPH} to complete. The RESET# input is available only on the SOIC 16 lead and BGA ball packages.

The IO3 / RESET# input initiates the reset operation under the following when CS# is HIGH for more than t_{CS} time or when Quad or QPI mode is not enabled CR1V[1] = 0 or CR2V[3] = 0. The IO3 / RESET# input has an internal pull-up to V_{CC} and may be left unconnected if Quad or QPI mode is not used. The t_{CS} delay after CS# goes HIGH gives the memory or host system time to drive IO3 high after its use as a Quad or QPI mode I/O signal while CS# was low. The internal pull-up to V_{CC} will then hold IO3 / RESET# HIGH until the host system begins driving IO3 / RESET#. The IO3 / RESET# input is ignored while CS# remains HIGH during t_{CS}, to avoid an unintended Reset operation. If CS# is driven LOW to start a new command, IO3 / RESET# is used as IO3.

When the device is not in Quad or QPI mode or, when CS# is HIGH, and IO3 / RESET# transitions from V_{IH} to V_{IL} for > t_{RP}, following t_{CS}, the device will reset register states in the same manner as power-on reset but, does not go through the full reset process that is performed during POR.

The hardware reset process requires a period of t_{RPH} to complete. If the POR process did not complete correctly for any reason during power-up (t_{PU}), RESET# going low will initiate the full POR process instead of the hardware reset process and will require t_{PU} to complete the POR process.

The software reset command (RSTEN 66h followed by RST 99h) is independent of the state of RESET # and IO3 / RESET#. If RESET# and IO3 / RESET# is high or unconnected, and the software reset instructions are issued, the device will perform software reset.

Additional notes:

- If both RESET# and IO3 / RESET# input options are available use only one reset option in your system. IO3 / RESET# input reset operation can be disable by setting CR2NV[7] = 0 (see **Table 14**) setting the IO3_RESET to only operate as IO3. The RESET# input can be disable by not connecting or tying the RESET# input to V_{IH}. RESET# and IO3 / RESET# must be high for t_{RS} following t_{PU} or t_{RPH}, before going low again to initiate a hardware reset.
- When IO3 / RESET# is driven low for at least a minimum period of time (t_{RP}), following t_{CS}, the device terminates any operation in progress, makes all outputs high impedance, and ignores all read/write commands for the duration of t_{RPH}. The device resets the interface to standby state.
- If Quad or QPI mode and the IO3 / RESET# feature are enabled, the host system should not drive IO3 low during $t_{CS,}$ to avoid driver contention on IO3. Immediately following commands that transfer data to the host in Quad or QPI mode, e.g. Quad I/O Read, the memory drives IO3 / RESET# high during $t_{CS,}$ to avoid an unintended Reset operation. Immediately following commands that transfer data to the memory in Quad mode, e.g. Page Program, the host system should drive IO3 / RESET# high during $t_{CS,}$ to avoid an unintended Reset operation.
- If Quad or QPI mode is not enabled, and if CS# is LOW at the time IO3 / RESET# is asserted LOW, CS# must return HIGH during t_{RPH} before it can be asserted low again after t_{RH}.

Table 63 Hardware reset parameters

Parameter	Description	Limit	Time	Unit
t_{RS}	Reset setup - Prior reset end and RESET# HIGH before RESET# LOW	Min	50	ns
t_{RPH}	Reset pulse hold - RESET# LOW to CS# LOW		100	µs
t_{RP}	RESET# pulse width		200	ns
t_{RH}	Reset hold - RESET# HIGH before CS# LOW		150	

Notes
74. RESET# and IO3 / RESET# LOW is ignored during power-up (t_{PU}). If Reset# is asserted during the end of t_{PU}, the device will remain in the reset state and t_{RH} will determine when CS# may go LOW.
75. If Quad or QPI mode is enabled, IO3 / RESET# LOW is ignored during t_{CS}.
76. Sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.

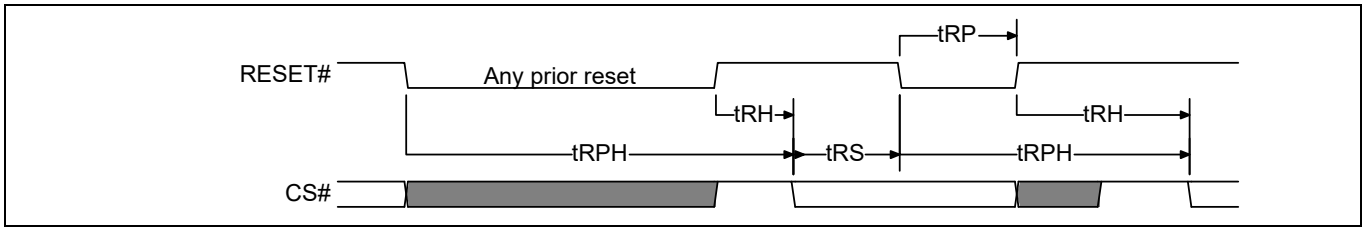


Figure 139 Hardware reset using RESET# input

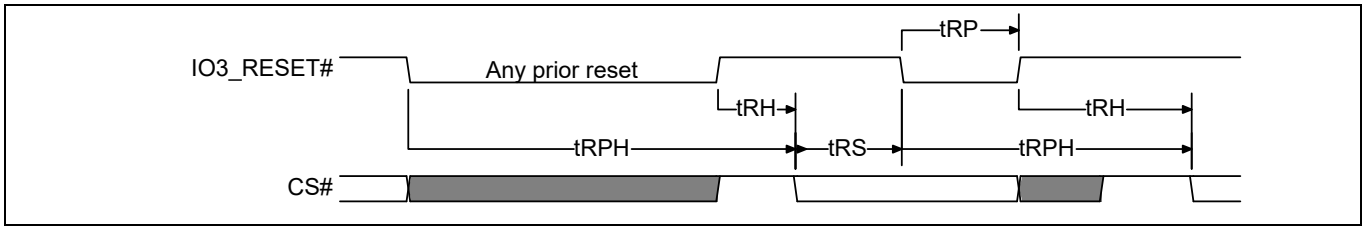


Figure 140 Hardware reset when quad or QPI mode is not enabled and IO3 / RESET# is enabled

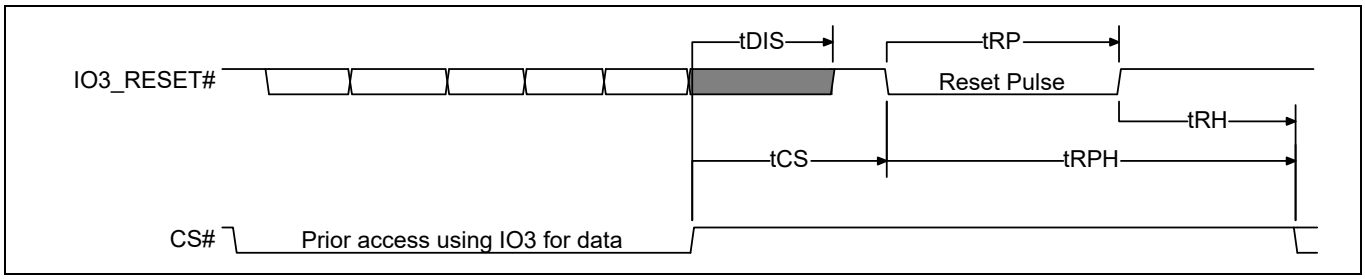


Figure 141 Hardware reset when quad or QPI mode and IO3 / RESET# are enabled

12.4 SDR AC characteristics

Table 64 SDR AC characteristics

Symbol	Parameter	Min	Max	Unit
$F_{SCK, R}$	SCK clock frequency for READ and 4READ instructions	DC	50	MHz
$F_{SCK, C}$	SCK clock frequency for the following dual and quad commands: QOR, 4QOR, DIOR, 4DIOR, QIOR, 4QIOR		133	
P_{SCK}	SCK clock period	1/ F_{SCK}	–	–
t_{WH}, t_{CH}	Clock high time	50% P_{SCK} ± 5%		ns
t_{WL}, t_{CL}	Clock low time			
t_{CRT}, t_{CLCH}	Clock rise time (slew rate)[77]	0.1		V/ns
t_{CFT}, t_{CHCL}	Clock fall time (slew rate)[77]	0.1		
t_{CS}	CS# high time (any read Instructions)	20	–	ns
	CS# high time (all other non-read instructions)	50		
t_{CSS}	CS# active setup time (relative to SCK)	3		
t_{CSH}	CS# active hold time (relative to SCK)	5		
t_{SU}	Data in setup time	3		
t_{HD}	Data in hold time	2		
t_V	Clock low to output valid	–	8[78] 6[79]	
t_{HO}	Output hold time	1	–	
t_{DIS}	Output disable time[80] Output disable time (when reset feature and quad mode are both enabled)	–	8 20[81]	
t_{WPS}	WP# setup time[82]	20	–	
t_{WPH}	WP# hold time[82]	100		
t_{DP}	CS# high to deep power down mode	–	3	µs
t_{RES}	CS# high to Release from deep power down mode		5	
t_{QEN}	QIO or QPI enter mode, time needed to issue next command		1.5	
t_{QEXN}	QIO or QPI exit mode, time needed to issue next command		1	

Notes
77. t_{CRT}, t_{CLCH} clock rise and fall slew rate for fast clock (108 MHz) min is 1.5 V/ns and for slow clock (50 MHz) min is 1.0 V/ns.
78. Full V_{CC} range and CL = 30 pF.
79. Full V_{CC} range and CL = 15 pF.
80. Output HI-Z is defined as the point where data is no longer driven.
81. t_{DIS} require additional time when the reset feature and quad mode are enabled (CR2V[7] = 1 and CR1V[1] = 1).
82. Only applicable as a constraint for WRR or WRAR instruction when SRP0 is set to a 1.

12.4.1 Clock timing

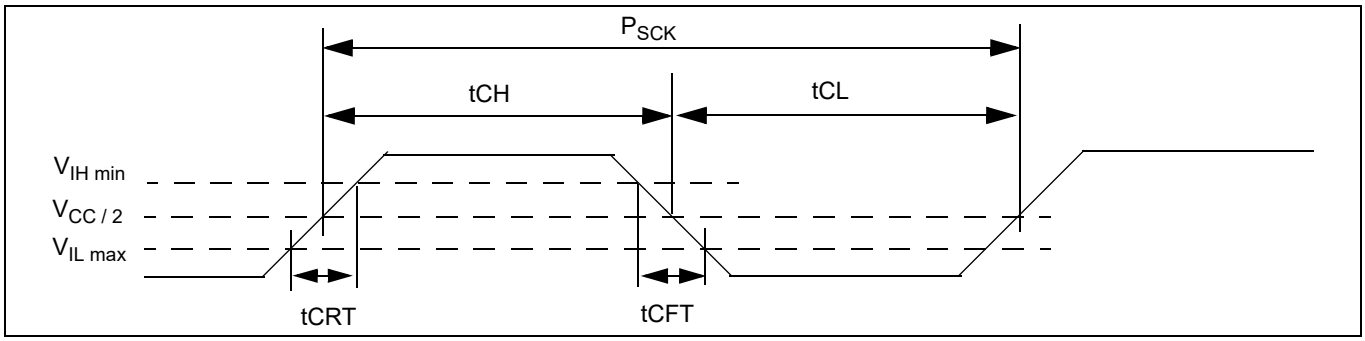


Figure 142 Clock timing

12.4.2 Input / Output timing

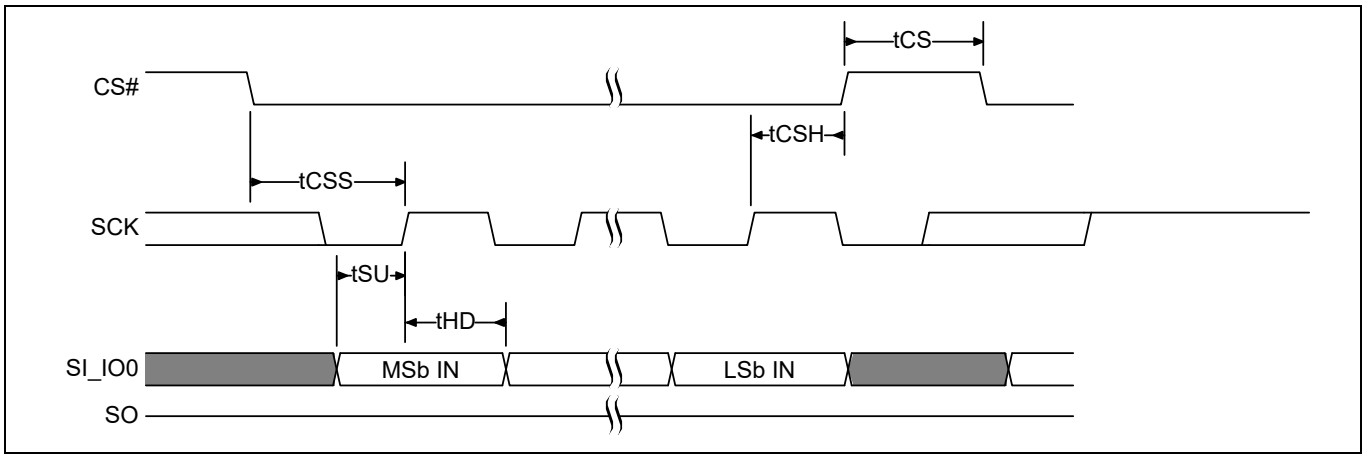


Figure 143 SPI single bit input timing

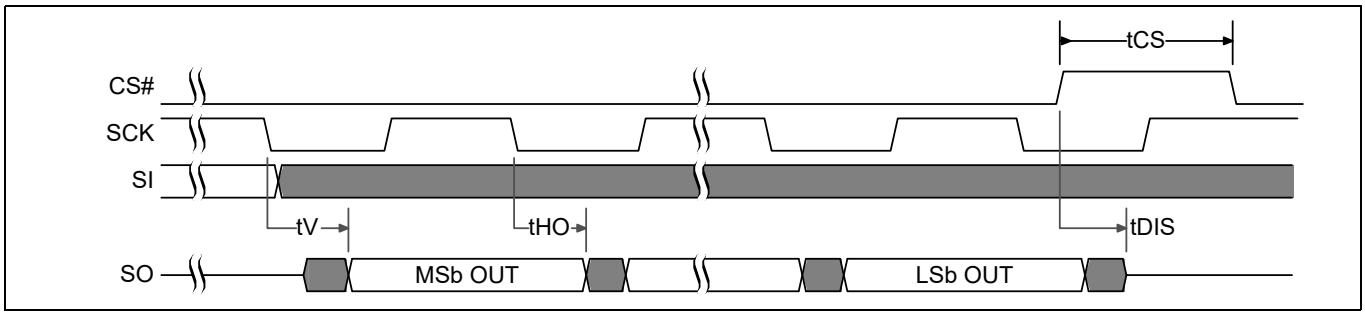


Figure 144 SPI single bit output timing

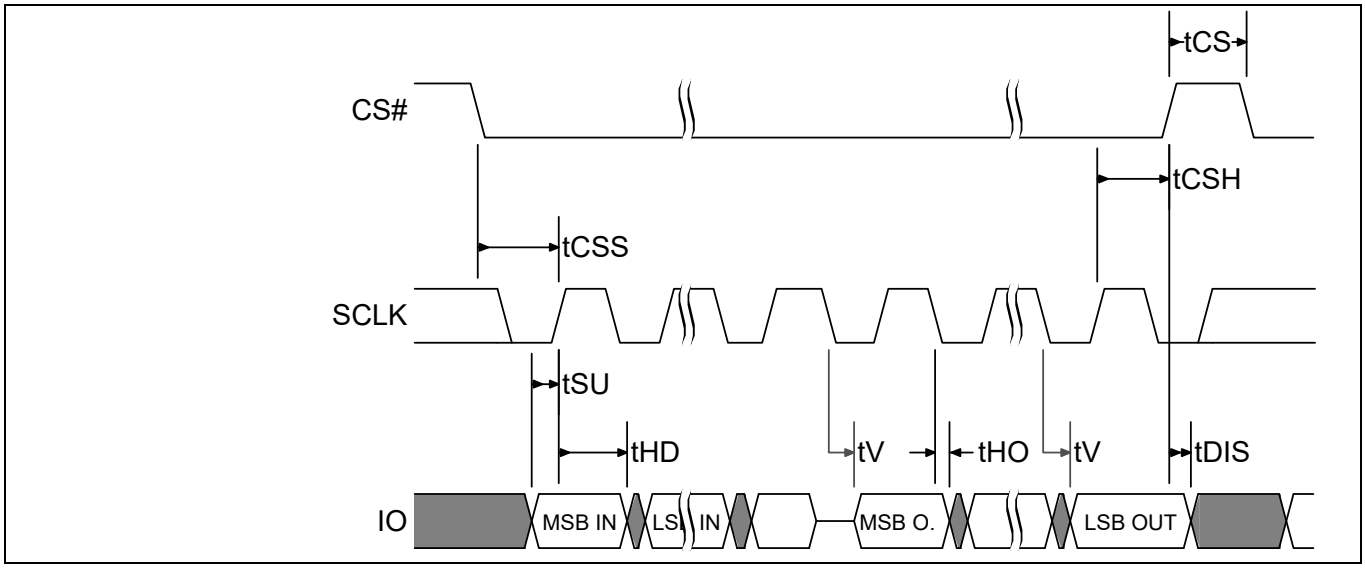


Figure 145 SDR MIO timing

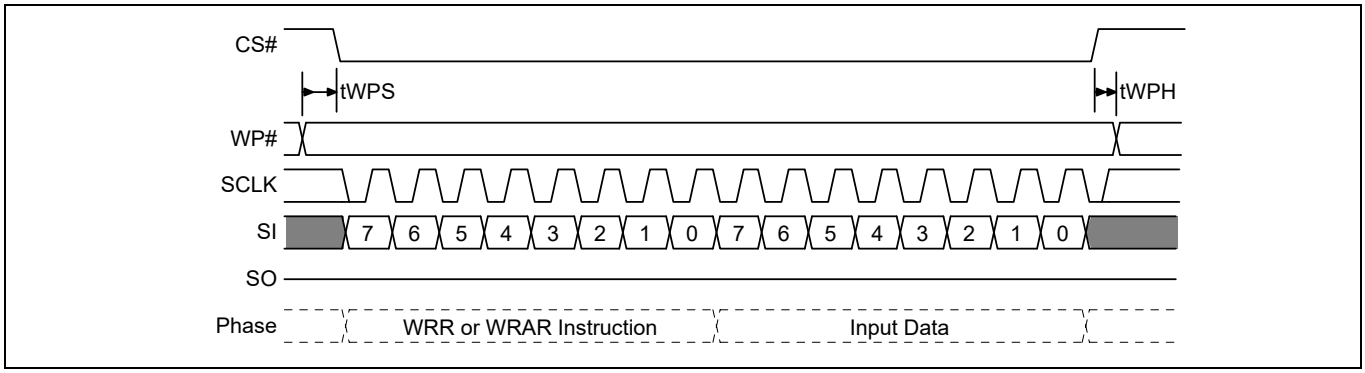


Figure 146 WP# input timing

12.5 DDR AC characteristics

Table 65 DDR AC characteristics 66 MHz operation

Symbol	Parameter	Min	Max	Unit
$F_{SCK, R}$	SCK clock frequency for DDR READ instruction	DC	66	MHz
$P_{SCK, R}$	SCK clock Period for DDR READ instruction	$1/F_{SCK}$	–	ns
t_{crt}	Clock rise time (slew rate)	1.5	–	V/ns
t_{cft}	Clock fall time (slew rate)			
t_{WH}, t_{CH}	Clock high time	50% P_{SCK} – 5%	–	ns
t_{WL}, t_{CL}	Clock low time			
t_{CS}	CS# high time (read instructions) CS# high time (Read instructions when Reset feature is enabled)	20 50	–	
t_{CSS}	CS# Active Setup Time (relative to SCK)	3	–	
t_{SU}	IO in Setup Time	3	–	
t_{HD}	IO in hold Time	2	–	
t_V	Clock Low to Output Valid	–	8[83] 6[84]	
t_{HO}	Output Hold Time	1	–	
t_{DIS}	Output Disable Time Output Disable Time (when Reset feature is enabled)	–	8 20	
t_{O_skew}	First IO to last IO data valid time	–	600[85]	ps

Notes
83.Full V_{CC} range and CL = 30 pF.
84.Full V_{CC} range and CL = 15 pF.
85.Not tested.

12.5.1 DDR input timing

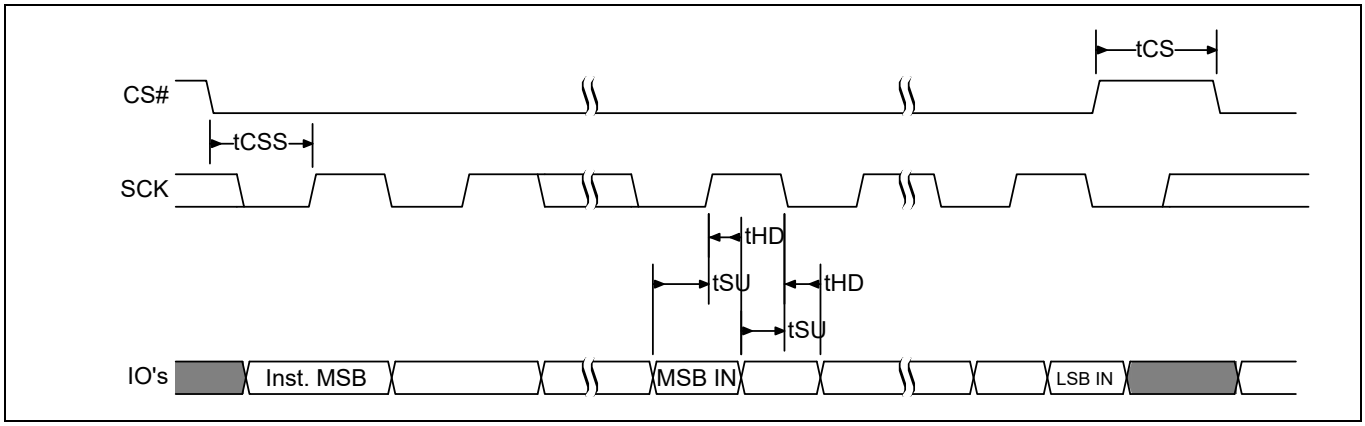


Figure 147 SPI DDR input timing

12.5.2 DDR output timing

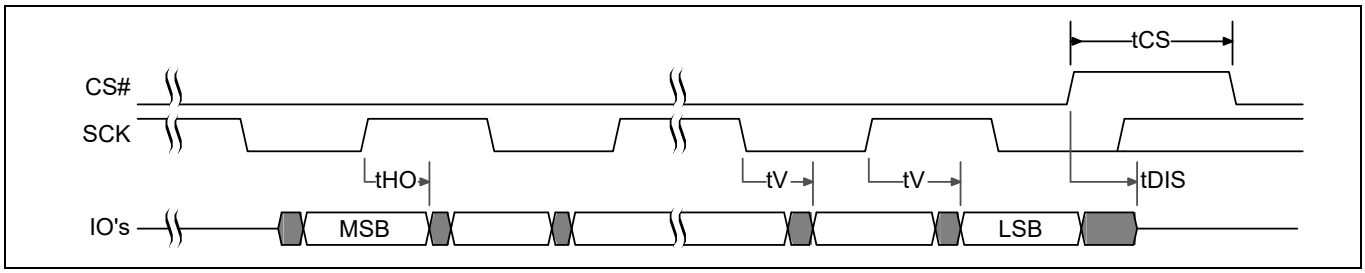


Figure 148 SPI DDR output timing

12.5.3 DDR data valid timing using DLP

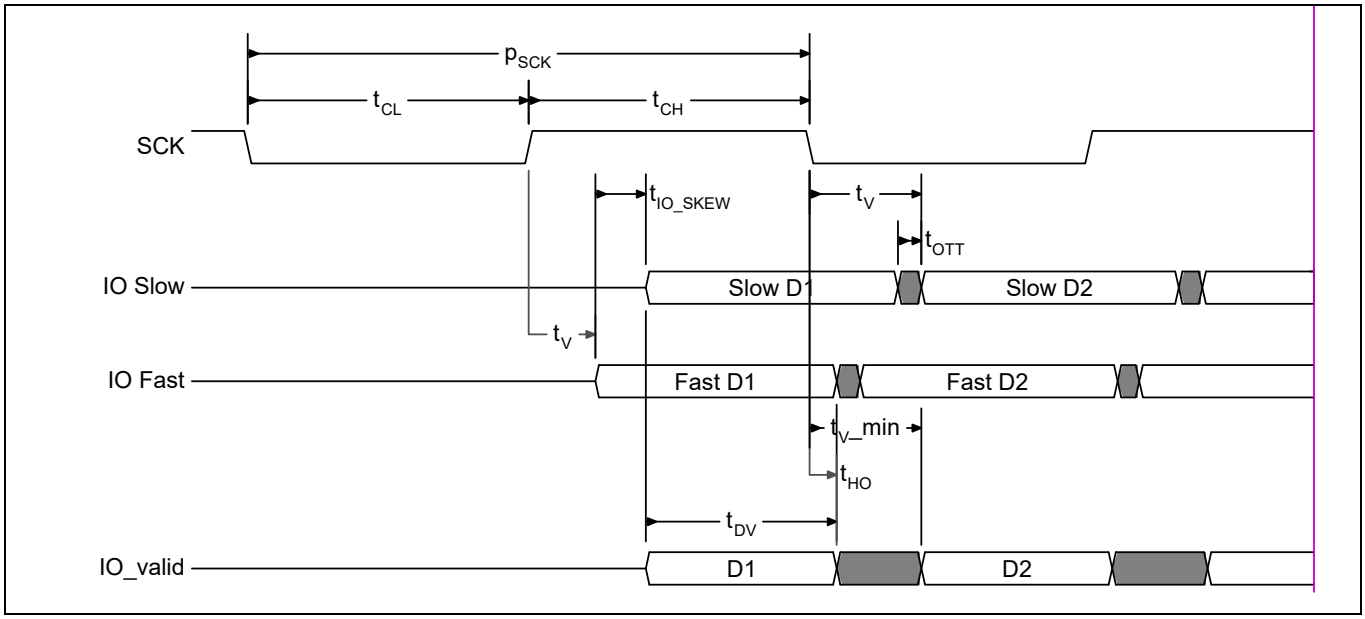


Figure 149 SPI DDR data valid window

The minimum data valid window (t_{DV}) and t_V minimum can be calculated as follows:

t_{DV} = Minimum half clock cycle time (t_{CLH}[86]) – t_{OTT}[88] – t_{IO_SKEW}[87]

t_V _min = t_{HO} + t_{IO_SKEW} + t_{OTT}

Example:

- 66 MHz clock frequency = 15 ns clock period, DDR operations and duty cycle of 45% or higher
  - t_{CLH} = 0.45 × PSCK = 0.45 × 15 ns = 6.75 ns
- t_{OTT} calculation[89] is bus impedance of 45 ohm and capacitance of 37 pf, with timing reference of 0.75 V_{CC}, the rise time from 0 to 1 or fall time 1 to 0 is 1.4[92] × RC time constant (Tau)[91] = 1.4 × 1.67 ns = 2.34 ns
  - t_{OTT} = rise time or fall time = 2.34 ns.
- Data Valid Window
  - t_{DV} = t_{CLH} – t_{IO_SKEW} – t_{OTT} = 6.75 ns – 600 ps – 2.34 ns = 3.81 ns
- t_V Minimum
  - t_V _min = t_{HO} + t_{IO_SKEW} + t_{OTT} = 1.0 ns + 600 ps + 2.34 ns = 3.94 ns

Notes

86. t_{CLH} is the shorter duration of t_{CL} or t_{CH}.
87. t_{IO_SKEW} is the maximum difference (delta) between the minimum and maximum t_V (output valid) across all IO signals.
88. t_{OTT} is the maximum Output Transition Time from one valid data value to the next valid data value on each IO.
89. t_{OTT} is dependent on system level considerations including:
    a. Memory device output impedance (drive strength).
    b. System level parasitics on the IOs (primarily bus capacitance).
    c. Host memory controller input V_{IH} and V_{IL} levels at which 0 to 1 and 1 to 0 transitions are recognized.
    d. t_{OTT} is not a specification tested by Infineon, it is system dependent and must be derived by the system designer based on the above considerations.
90. t_{DV} is the data valid window.
91. Tau = R (Output Impedance) x C (Load capacitance).
92. Multiplier of Tau time for voltage to rise to 75% of V_{CC}.

12.6 Embedded algorithm performance tables

Table 66 Dual quad program and erase performance

Symbol	Parameter	Min	Typ []	Max	Unit
t_W	Non-volatile register write time	–	145	750	ms
t_{PP}	Page programming (256 bytes)		300	1,200	µs
t_{BP1}	Byte programming (first byte)[95]		50	60	
t_{BP2}	Additional byte programming (after first byte)[95]		6	20	
t_{SE}	Sector erase time (4KB physical sectors)		50	250	ms
t_{HBE}	Half block erase time (32KB physical sectors)		190	363	
t_{BE}	Block erase time (64KB physical sectors)		270	725	
t_{CE}	Chip erase time (S25FL128L)		70	180	sec
t_{CE}	Chip erase time (S25FL256L)		140	360	

Notes
93. Typical program and erase times assume the following conditions: 25°C, V_{CC} = 3.0 V; 10,000 cycles; checker-board data pattern.
94. The programming time for any OTP programming command is the same as t_{PP}. This includes IRPP 2Fh, PASSP E8h and PDLRNV 43h.
95. For multiple bytes after firs byte within a page $t_{BPN} = t_{BP1} + t_{BP2} * N$ (typical and $t_{BPN} = t_{BP1} = t_{BP2} * N$ (max), where N = number of bytes programmed.

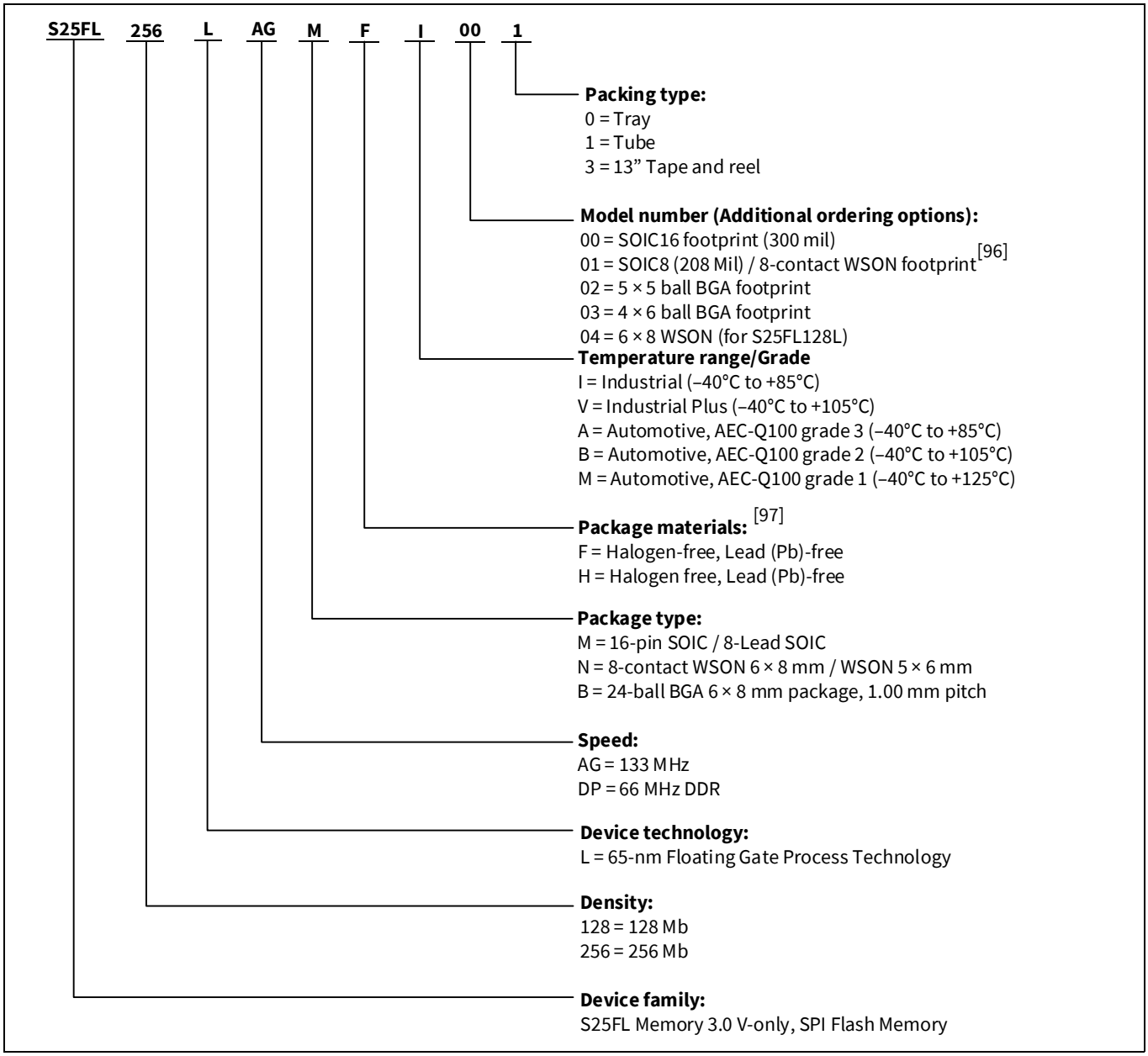
Table 67 Program or erase suspend AC parameters

Parameter	Typical	Max	Unit	Comments
Suspend latency (t_{SL})	–	40	µs	The time from Suspend command until the WIP bit is 0.
Resume to next suspend (t_{RNS})	100	–		Is the time needed to issue the next Suspend command.

13 Ordering information

13.1 Ordering part number

The ordering part number is formed by a valid combination of the following:



Notes
96.WSON 6 × 8 mm is for S25FL256L. WSON 5 × 6 mm is for S25FL128L only.
97.Halogen free definition is in accordance with IEC 61249-2-21 specifications.

13.2 Valid combinations — Standard

Valid Combinations list configurations planned to be supported in volume for this device. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 68 Valid combinations - standard

Product	Speed option	Package and temperature	Model number	Packing type	Package marking
S25FL128L	AG	MFI, MFV	00	0, 1, 3	(Base) + A + (temp) + F + (model number)
	AG	MFI, MFV	01	0, 1, 3	(Base) + A + (temp) + F + (model number)
	AG	NFI, NFV	01	0, 1, 3	(Base) + A + (temp) + F + (model number)
	AG	BHI, BHV	02, 03	0, 3	(Base) + A + (temp) + H + (model number)
	AG	NFI, NFV	04	0, 3	(Base) + A + (temp) + F + (model number)
	DP	MFI, MFV	00	0, 1, 3	(Base) + D + (temp) + F + (model number)
	DP	MFI, MFV	01	0, 1, 3	(Base) + D + (temp) + F + (model number)
	DP	NFI, NFV	01	0, 1, 3	(Base) + D + (temp) + F + (model number)
	DP	BHI, BHV	02, 03	0, 3	(Base) + D + (temp) + H + (model number)
	DP	NFI, NFV	04	0, 3	(Base) + D + (temp) + F + (model number)
S25FL256L	AG	MFI, MFV	00	0, 1, 3	(Base) + A + (temp) + F + (model number)
	AG	NFI, NFV	01	0, 1, 3	(Base) + A + (temp) + F + (model number)
	AG	BHI, BHV	02, 03	0, 3	(Base) + A + (temp) + H + (model number)
	DP	MFI, MFV	00	0, 1, 3	(Base) + D + (temp) + F + (model number)
	DP	NFI, NFV	01	0, 1, 3	(Base) + D + (temp) + F + (model number)
	DP	BHI, BHV	02, 03	0, 3	(Base) + D + (temp) + H + (model number)

13.3 Valid combinations — Automotive grade / AEC-Q100

Table 69 lists configurations that are Automotive Grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Contact your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products.

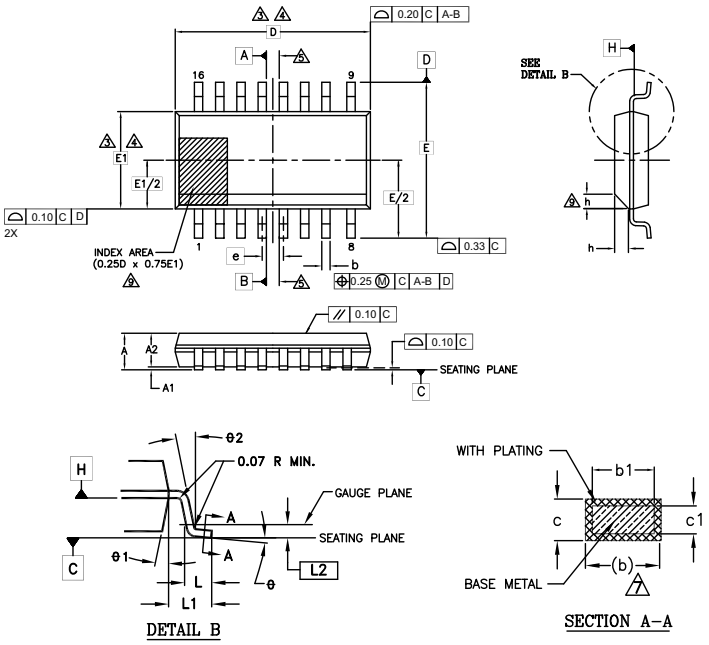
Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 69 Valid combinations - Automotive grade / AEC-Q100

Product	Speed option	Package and temperature	Model number	Packing type	Package marking
S25FL128L	AG	MFA, MFB, MFM	00	0, 1, 3	(Base) + A + (temp) + F + (model number)
		MFA, MFB, MFM	01		
		NFA, NFB, NFM			
		BHA, BHB, BHM	02, 03	0, 3	(Base) + A + (temp) + H + (model number)
		NFA, NFB, NFM	04	0,3	(Base) + A + (temp) + F + (model number)
	DP	MFA, MFB, MFM	00	0, 1, 3	(Base) + D + (temp) + F + (model number)
		MFA, MFB, MFM	01		
		NFA, NFB, NFM			
		BHA, BHB, BHM	02, 03	0, 3	(Base) + D + (temp) + H + (model number)
		NFA, NFB, NFM	04	0,3	(Base) + D + (temp) + F + (model number)
S25FL256L	AG	MFA, MFB, MFM	00	0, 1, 3	(Base) + A + (temp) + F + (model number)
		NFA, NFB, NFM	01		
		BHA, BHB, BHM	02, 03	0, 3	(Base) + A + (temp) + H + (model number)
	DP	MFA, MFB, MFM	00	0, 1, 3	(Base) + D + (temp) + F + (model number)
		NFA, NFB, NFM	01		
		BHA, BHB, BHM	02, 03	0, 3	(Base) + D + (temp) + H + (model number)

14 Package diagrams



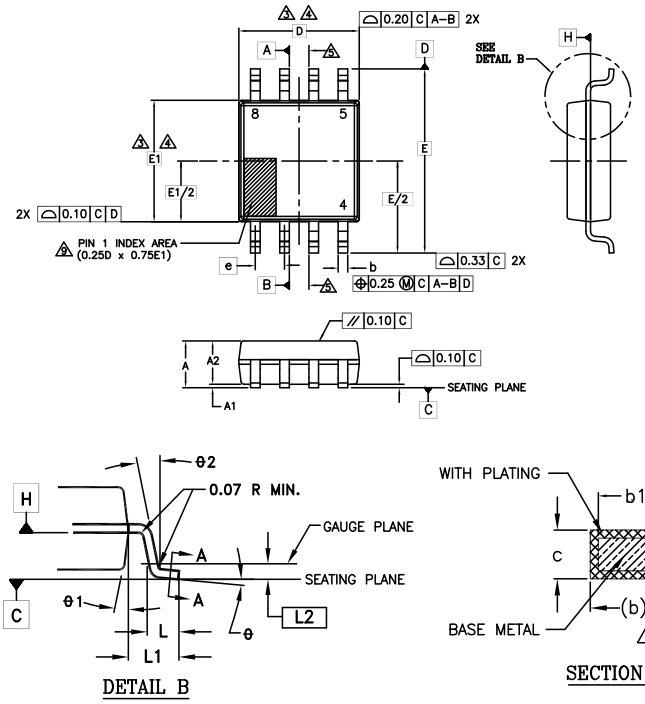
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	2.35	-	2.65
A1	0.10	-	0.30
A2	2.05	-	2.55
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.20	-	0.33
c1	0.20	-	0.30
D	10.30 BSC		
E	10.30 BSC		
E1	7.50 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.40 REF		
L2	0.25 BSC		
N	16		
h	0.25	-	0.75
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUSIVE OF ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

002-15547 *A

Figure 150 16-lead SOIC (10.30 × 7.50 × 2.65 mm) package outline (PG-DSO-16), 002-15547



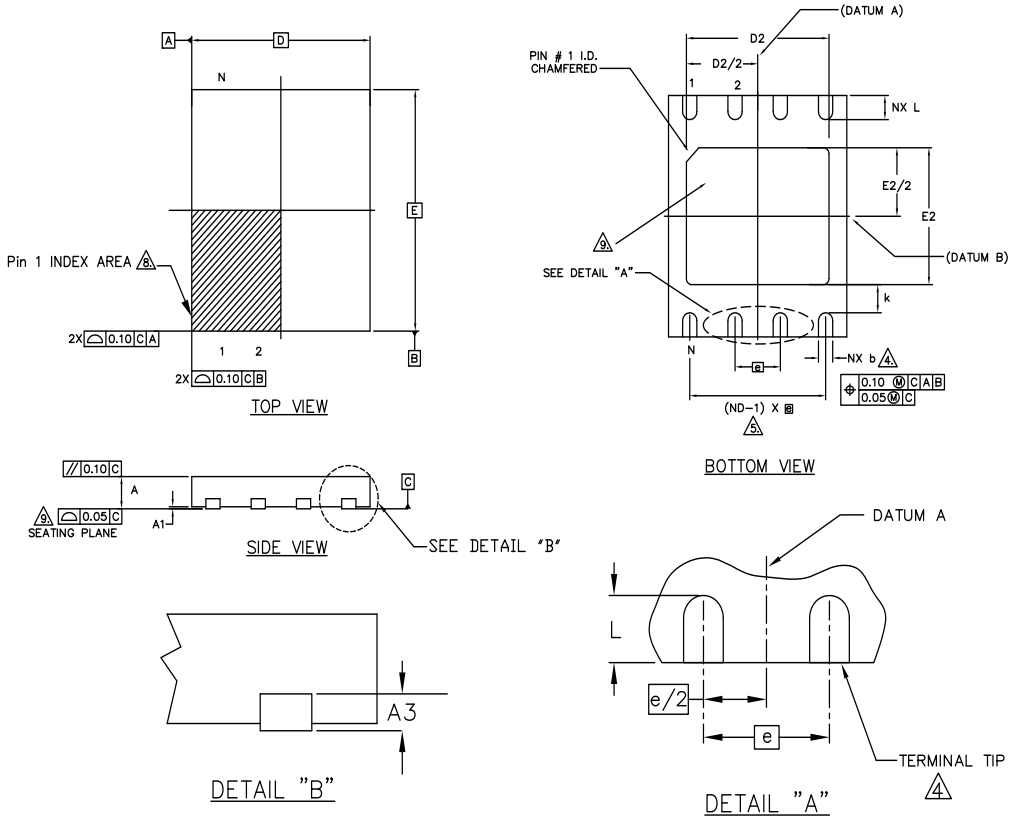
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	1.75	-	2.16
A1	0.05	-	0.25
A2	1.70	-	1.90
b	0.36	-	0.48
b1	0.33	-	0.46
c	0.19	-	0.24
c1	0.15	-	0.20
D	5.28 BSC		
E	8.00 BSC		
E1	5.28 BSC		
e	1.27 BSC		
L	0.51	-	0.76
L1	1.36 REF		
L2	0.25 BSC		
N	8		
θ	0°	-	8°
θ 1	5°	-	15°
θ 2	0-8° REF		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUSIVE OF ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

002-15548 **

Figure 151 8-lead SOIC (5.28 × 5.28 × 2.16 mm) package outline (PG-DSO-8), 002-15548



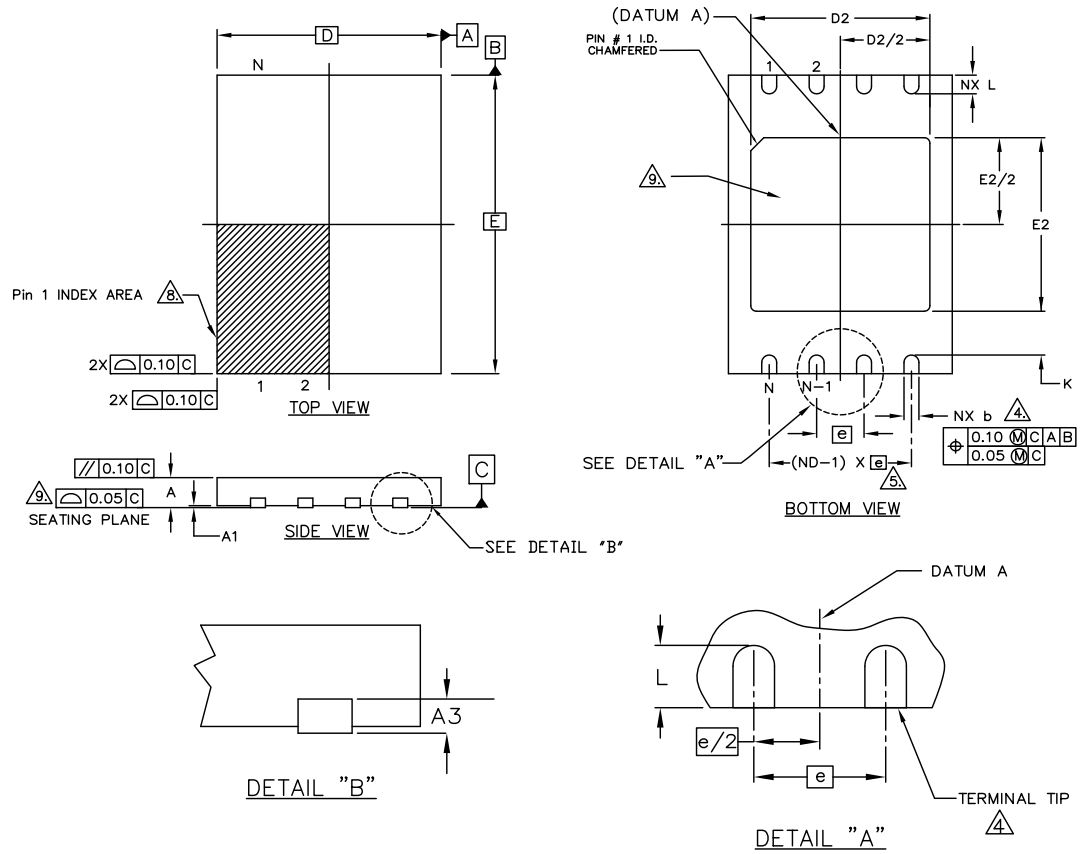
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		1.27 BSC.	
N		8	
ND		4	
L	0.55	0.60	0.65
b	0.35	0.40	0.45
D2	3.90	4.00	4.10
E2	3.30	3.40	3.50
D		5.00 BSC	
E		6.00 BSC	
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
K		0.20 MIN.	

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. A MAXIMUM 0.15mm PULL BACK (L1) MAY BE PRESENT.

002-18755 **

Figure 152 8-lead DFN ((5 × 6 × 0.8 mm) 4.0 × 3.4 mm E-Pad (Sawn)) package outline (PG-WSON-8), 002-18755



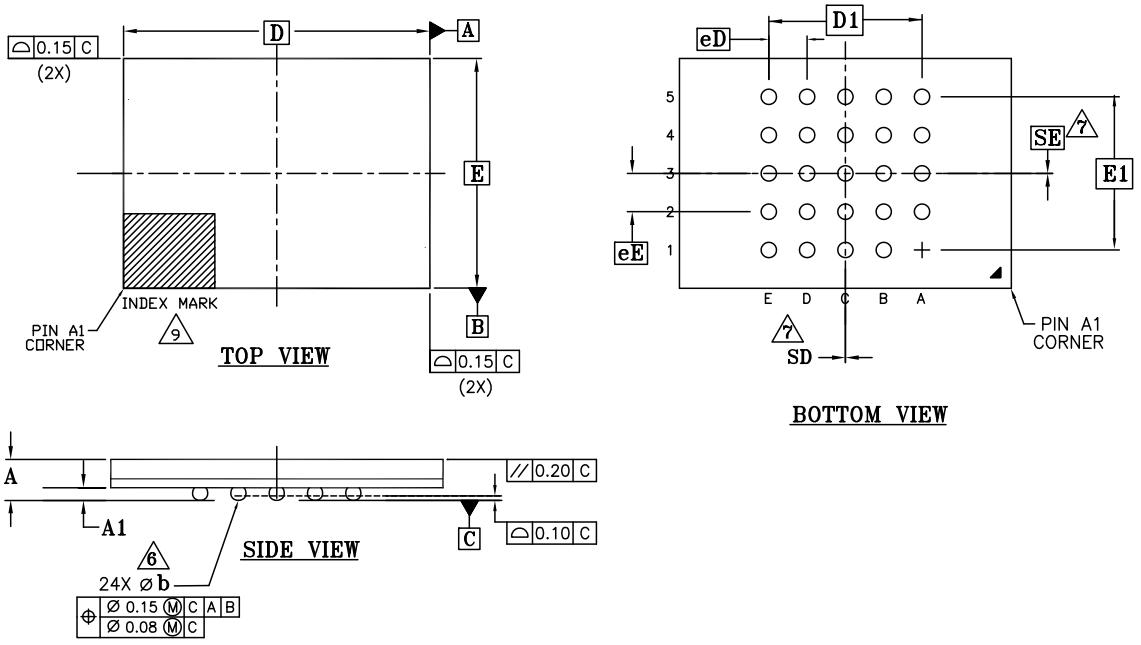
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		1.27 BSC.	
N		8	
ND		4	
L	0.45	0.50	0.55
b	0.35	0.40	0.45
D2	4.70	4.80	4.90
E2	4.55	4.65	4.75
D		6.00 BSC	
E		8.00 BSC	
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
K		0.20 MIN.	

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. A MAXIMUM 0.15mm PULL BACK (L1) MAY BE PRESENT.

002-18827 **

Figure 153 8-lead DFN ((6 × 8 × 0.8 mm) 4.80 × 4.65 mm E-Pad (Sawn)) package outline (PG-WSON-8), 002-18827



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.20	-	-
D		8.00 BSC	
E		6.00 BSC	
D1		4.00 BSC	
E1		4.00 BSC	
MD		5	
ME		5	
N		24	
Ø b	0.35	0.40	0.45
eE		1.00 BSC	
eD		1.00 BSC	
SD		0.00 BSC	
SE		0.00 BSC	

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

△6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

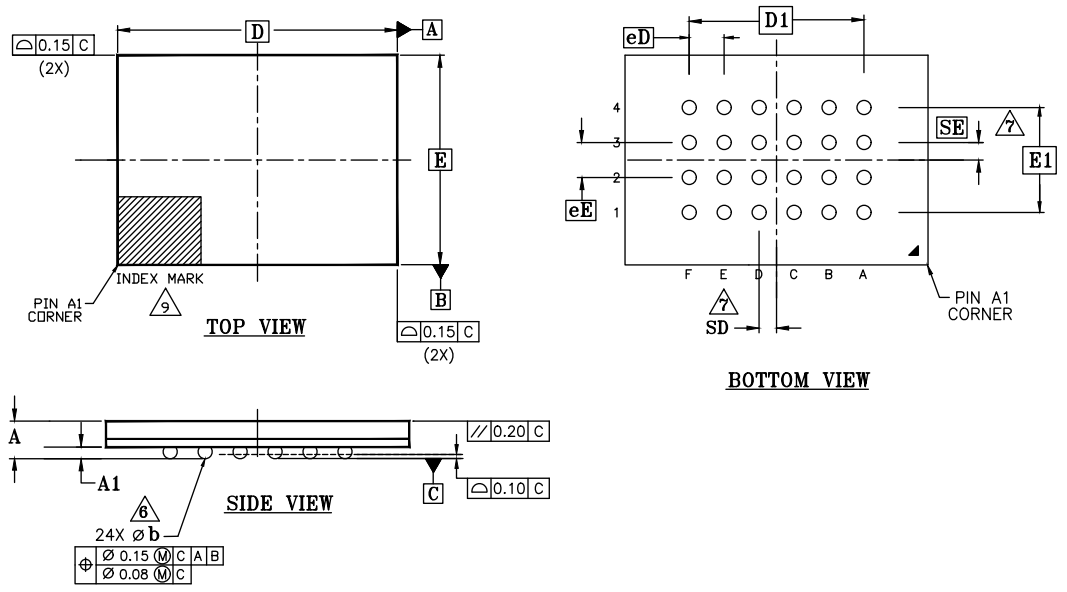
△7 "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

△9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

002-15534 **

Figure 154 24-ball FBGA (8 × 6 × 1.2 mm) package outline (PG-TFBGA-24), 002-15534



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.25	-	-
D	8.00 BSC		
E	6.00 BSC		
D1	5.00 BSC		
E1	3.00 BSC		
MD	6		
ME	4		
N	24		
∅ b	0.35	0.40	0.45
eE	1.00 BSC		
eD	1.00 BSC		
SD	0.50 BSC		
SE	0.50 BSC		

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7 "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

002-15535 *A

Figure 155 24-ball FBGA (8 × 6 × 1.2 mm) package outline (PG-TFBGA-24), 002-15535

Revision history

Document revision	Date	Description of changes
*C	2016-09-26	Changed status from Advance to Final. Updated **Features**: Added Automotive Grade related information. Updated **Data integrity**: Updated **Data retention**: Updated **Table 46**. Updated **Electrical specifications**: Updated **Thermal resistance**: Updated **Table 54**. Updated **Operating ranges**: Updated **Temperature ranges**: Added Automotive Grade related information.
*C (cont.)	2016-09-26	Updated **Ordering information**: Updated **Ordering part number**: Updated details corresponding to “01” under “Model Number (Additional Ordering Options)”. Added Automotive Grade related information. Removed “Valid Combinations”. Added **Valid combinations — Standard**. Added **Valid combinations — Automotive grade / AEC-Q100**. Updated **Package diagrams**: Updated SOIC 16-Lead, 300-mil Body Width (SO3016): Replaced existing spec with 002-15547 **. Updated SOIC 8-Lead, 208 mil Body Width (SOC008): Replaced existing spec with 002-15548 **. Added “WSON 8-Contact 6 x 8 mm Leadless (WNG008)”. Removed “WSON 8-Contact 6 x 8 mm Leadless (WNH008)”: Updated Ball Grid Array 24-ball 6 x 8 mm (FAB024): Replaced existing spec with 002-15534 **. Updated Ball Grid Array 24-ball 6 x 8 mm (FAC024): Replaced existing spec with 002-15535 **.
*D	2017-01-11	Updated Other Resources: Updated Link to Cypress Flash Roadmap: Updated hyperlinks. Updated Link to Software: Updated hyperlinks. Updated Link to Application Notes: Updated hyperlinks. Updated to new template. Completing Sunset Review.

Revision history

Document revision	Date	Description of changes
*E	2017-05-15	Replaced “V_{DD}” with “V_{CC}” in all instances across the document. Updated **Data protection**: Updated **Array protection**: Updated **Legacy block protection**: Added **Table 37**. Updated **Software interface reference**: Updated **JEDEC JESD216B serial flash discoverable parameters**: Updated **JEDEC SFDP basic SPI flash parameter**: Updated **Table 49**. Updated **Timing specifications**: Updated **Embedded algorithm performance tables**: Updated **Table 66**. Updated **Ordering information**: Updated **Ordering part number**: Replaced “Lead (Pb)-free” with “F = Halogen-free, Lead (Pb)-free” in “F” option under “Package Materials”. Updated **Valid combinations — Standard**: Updated **Table 68**. Updated **Valid combinations — Automotive grade / AEC-Q100**: Updated **Table 69**.
*E (cont.)	2017-05-15	Updated **Package diagrams**: Updated SOIC 16-Lead, 300-mil Body Width (SO3016): spec 002-15547 – Changed revision from ** to *A. Updated WSON 8-Contact 5 x 6 mm Leadless (WND008): Replaced existing spec with 002-18755 **. Updated WSON 8-Contact 6 x 8 mm Leadless (WNG008): Replaced existing spec with 002-18827 **. Updated to new template.
*F	2017-08-07	Updated **Features**: Updated description. Updated **Electrical specifications**: Updated **Latchup characteristics**: Updated **Table 53**. Updated **Ordering information**: Updated **Ordering part number**: Removed “(not in production)” under “Density”. Updated **Valid combinations — Standard**: Updated **Table 68**. Updated **Valid combinations — Automotive grade / AEC-Q100**: Updated **Table 69**. Completing Sunset Review.

Revision history

Document revision	Date	Description of changes
*G	2018-04-03	Updated **Signal protocols**: Updated **Command protocol**: Updated **Command sequence examples**: Updated **Figure 22**. Updated **Figure 23**. Updated **Commands**: Updated **Read Memory Array commands**: Updated **DDR Quad I/O Read (EDh, EEh)**: Updated **Figure 74**. Updated **Figure 75**. Updated **Figure 76**. Updated **Software interface reference**: Updated **Device ID address map**: Updated **Field definitions**: Updated **Table 52**. Updated **Electrical specifications**: Updated **DC characteristics**: Updated **Table 58**. Updated **Table 59**. Updated **Table 60**. Updated **Timing specifications**: Updated **DDR AC characteristics**: Removed “DDR Minimum Data Valid Window”. Added **DDR data valid timing using DLP**. Updated to new template.
*H	2018-07-11	Updated **Address space maps**: Updated **Registers**: Updated description. Updated **Timing specifications**: Updated **DDR AC characteristics**: Updated **DDR data valid timing using DLP**: Updated description. Updated **Ordering information**: Updated **Ordering part number**: Changed Low-halogen to Halogen free under “Package Materials”. Added Note 97 and referred the same note in “Package Materials”. Updated Other Resources: Updated Glossary: Updated Definition of MSb and LSb. Completing Sunset Review.
*I	2022-08-05	Updated **Electrical specifications**: Updated **Thermal resistance**: Updated **Table 54**. Updated **DC characteristics**: Updated **Table 59**. Updated **Package diagrams**: spec 002-15535 – Changed revision from ** to *A. Removed “Other resources”. Migrated to Infineon template. Completing Sunset Review.
*J	2022-11-03	Updated **Electrical specifications**: Updated **Thermal resistance**: Updated **Table 54**.

Revision history

Document revision	Date	Description of changes
*K	2023-04-10	Updated **Address space maps**: Updated **Registers**: Updated **Configuration Register 3**: Updated **Configuration Register 3 Non-Volatile (CR3NV)**: Updated **Table 19**. Updated **Table 20**. Updated to new template.
*L	2024-01-11	Updated **Table 68**. Updated **Table 69**.

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