THE DATASHEET OF

S29CL032J0RQFM030

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S29CD032J
S29CD016J
S29CL032J
S29CL016J

32/16 Mbit, 2.6/3.3 V, Dual Boot, Simultaneous Read/Write, Burst Flash

General Description

The Cypress S29CD-J and S29CL-J devices are Floating Gate products fabricated in 110-nm process technology. These burst-mode Flash devices are capable of performing simultaneous read and write operations with zero latency on two separate banks, using separate data and address pins. These products can operate up to 75 MHz (32 Mb) or 66 MHz (16 Mb), and use a single V_{CC} of 2.5V to 2.75V (S29CD-J) or 3.0V to 3.6V (S29CL-J) that make them ideal for today's demanding automotive applications.

Distinctive Characteristics

- Single 2.6V (S29CD-J) or 3.3V (S29CL-J) for read/program/erase
- 110 nm Floating Gate Technology
- Simultaneous Read/Write operation with zero latency
- x32 Data Bus
- Dual Boot Sector Configuration (top and bottom)
- Flexible Sector Architecture
  - CD016J and CL016J: Eight 2k Double word, Thirty 16k Double word, and Eight 2k Double Word sectors
  - CD032J and CL032J: Eight 2k Double word, Sixty-two 16k Double Word, and Eight 2k Double Word sectors
- VersatileI/O™ control (1.65V to 3.6V)
- Programmable Burst Interface
  - Linear for 2, 4, and 8 double word burst with wrap around
- Secured Silicon Sector that can be either factory or customer locked
- 20 year data retention (typical)
- Cycling Endurance: 1 million write cycles per sector (typical)
- Command set compatible with JEDEC (JC42.4) standard
- Supports Common Flash Interface (CFI)
- Extended Temperature range
- Persistent and Password methods of Advanced Sector Protection
- Unlock Bypass program command to reduce programming time
- ACC input pin to reduce factory programming time
- Data Polling bits indicate program and erase operation completion
- Hardware (WP#) protection of two outermost sectors in the large bank
- Ready/Busy (RY/BY#) output indicates data available to system
- Suspend and Resume commands for Program and Erase Operation
- Offered Packages
  - 80-pin PQFP
  - 80-ball Fortified BGA (13 x 11 mm and 11 x 9mm versions)
  - Pb-free package option available
  - Known Good Die

Performance Characteristics

Read Access Times				
Speed Option (MHz)	75 (32 Mb only)	66	56	40
Max Asynch. Access Time, ns (t_{ACC})	54	54	54	54
Max Synch. Burst Access, ns (t_{BACC})	8	8	8	8
Min Initial Clock Delay (clock cycles)	5	5	5	4
Max CE# Access Time, ns (t_{CE})	54	54	54	54
Max OE# Access time, ns (t_{OE})	20	20	20	20

Current Consumption (Max values)	
Continuous Burst Read @ 75 MHz	90 mA
Program	50 mA
Erase	50 mA
Standby Mode	60 µA

Typical Program and Erase Times	
Double Word Programming	18 µs
Sector Erase	1.0 s

Notice for the 32Mb S29CD-J and S29CL-J devices only:
Refer to the application note "*Recommended Mode of Operation for Cypress® 110 nm S29CD032J/S29CL032J Flash Memory*" publication number *S29CD-CL032J_Recommend_AN* for programming best practices.

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1. Ordering Information

The order number (Valid Combination) is formed by the following:

S29CD032J / S29CL032J 0 J F A I 0 0 0

Packing Type
0 = Tray, FBGA: 180 per tray, min. 10 trays per box
Tray, PQFP: 66 per tray, min. 10 trays per box
2 = 7” Tape and Reel, FBGA: 400 per reel
3 = 13” Tape and Reel, FBGA: 1600 per reel
13” Tape and Reel, PQFP: 500 per reel

Boot Sector Option (16th Character)
0 = Top Boot with Simultaneous Operation
1 = Bottom Boot with Simultaneous Operation
2 = Top Boot without Simultaneous Operation
3 = Bottom Boot without Simultaneous Operation

Autoselect ID Option (15th Character)

0 = 7E, 08, 01/00 Autoselect ID	*S29CD016J only*
1 = 7E, 36, 01/00 Autoselect ID	
0 = 7E, 46, 01/00 Autoselect ID	*S29CL016J only*
0 = 7E, 09, 01/00 Autoselect ID	*S29CD032J only*
0 = 7E, 49, 01/00 Autoselect ID	*S29CL032J only*

Temperature Range
I = Industrial (–40 °C to +85 °C)
M = Extended (–40 °C to +125 °C)

Material Set
A = Standard
F = Pb-free Option

Package Type
Q = Plastic Quad Flat Package (PQFP)
F = Fortified Ball Grid Array, 1.0 mm pitch package, 13 × 11 mm package
B = Fortified Ball Grid Array, 1.0 mm pitch package, 11 × 9 mm package

Clock Frequency (11th Character)
J = 40 MHz
M = 56 MHz
P = 66 MHz
R = 75 MHz

Initial Burst Access Delay (10th Character)
0 = 5-1-1-1, 6-1-1-1, and above
1 = 4-1-1-1 (40 MHz only)

Device Number/Description
S29CD032J/S29CD016J (2.5 volt-only), S29CL032J/S29CL016J (3.3 Volt-only)
32 or 16 Mbit (1M or 512k × 32-Bit) CMOS Burst Mode, Dual Boot, Simultaneous Read/Write Flash Memory
Manufactured on 110 nm floating gate technology

1.1 Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

S29CD-J/CL-J Valid Combinations								
Device Number	**Initial Burst Access Delay**	**Clock Frequency**	**Package Type**	**Material Set**	**Temperature Range**	**Autoselect ID Option**	**Boot Sector Option**	**Packing Type**
S29CD016J	0, 1	J	Q	A, F	I, M	0, 1	0, 1, 2, 3	0, 3
			B, F					0, 2, 3
	0	M, P	Q					0, 3
			B, F					0, 2, 3
S29CL016J	0, 1	J	Q			0		0, 3
			B, F					0, 2, 3
	0	M, P	Q					0, 3
			B, F					0, 2, 3
S29CD032J	0, 1	J	Q					0, 3
			B, F					0, 2, 3
	0	M, P	Q					0, 3
			B, F					0, 2, 3
		R	Q				0, 1 (2)	0, 3
							2, 3	
			B, F				0, 1 (2)	0, 2, 3
							2, 3	
S29CL032J	0, 1	J	Q				0, 1, 2, 3	0, 3
			B, F					0, 2, 3
	0	M, P	Q					0, 3
			B, F					0, 2, 3
		R	Q				0, 1 (2)	0, 3
							2, 3	
			B, F				0, 1 (2)	0, 2, 3
							2, 3	

Notes

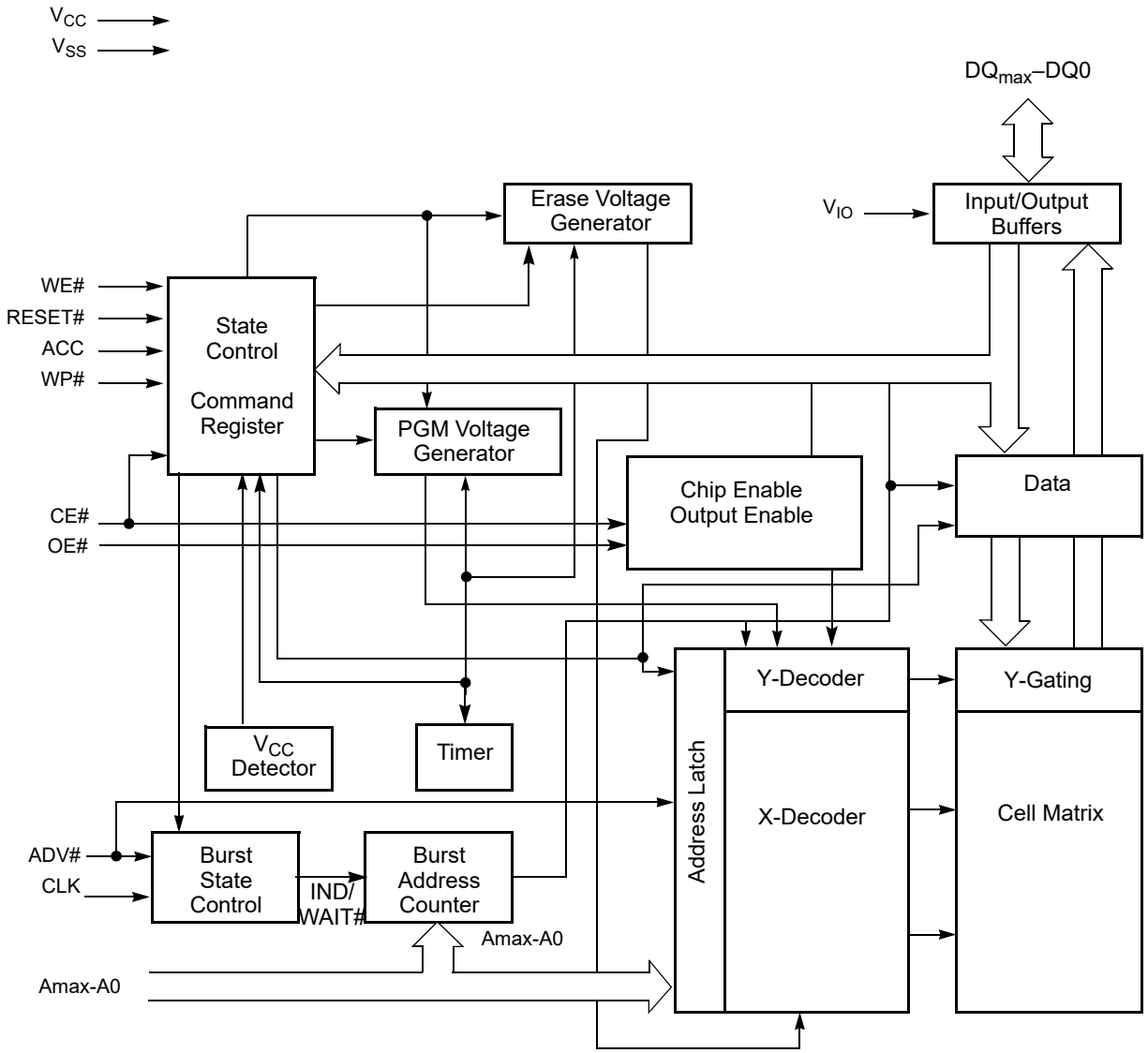
1. The ordering part number that appears on BGA packages omits the leading “S29”.
2. Contact factory for availability.

2. Input/Output Descriptions and Logic Symbols

Table identifies the input and output package connections provided on the device.

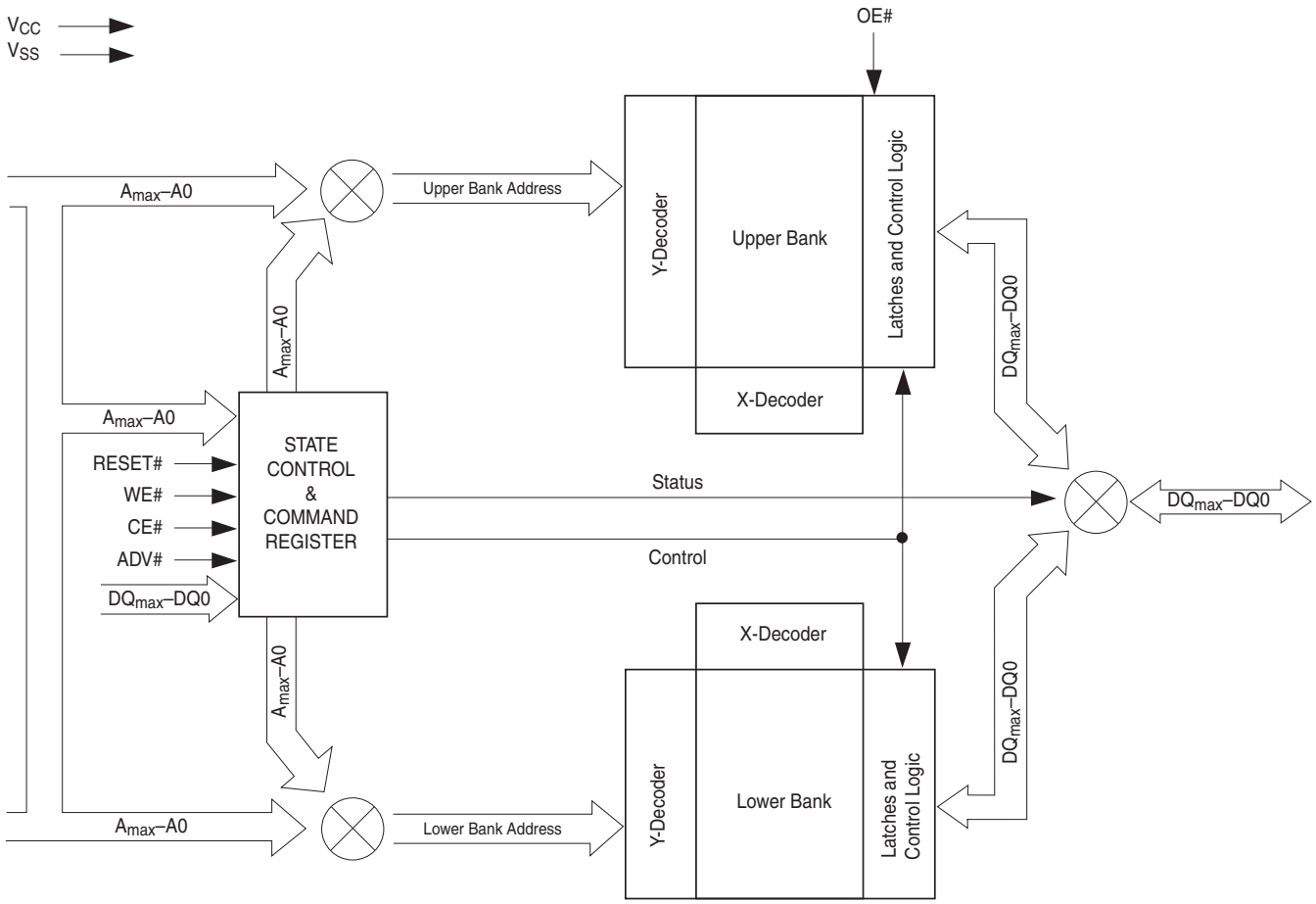
Symbol	Type	Description
A19-A0	Input	Address lines for S29CD-J and S29CL-J (A18-A0 for 16 Mb and A19-A0 for 32 Mb). A9 supports 12V autoselect input.
DQ31-DQ0	I/O	Data input/output
CE#	Input	Chip Enable. This signal is asynchronous relative to CLK for the burst mode.
OE#	Input	Output Enable. This signal is asynchronous relative to CLK for the burst mode.
WE#	Input	Write Enable
V_{CC}	Supply	Device Power Supply. This signal is asynchronous relative to CLK for the burst mode.
V_{IO}	Supply	VersatileI/O™ Input.
V_{SS}	Supply	Ground
NC	No Connect	Not connected internally
RY/BY#	Output	Ready/Busy output and open drain which require a external pull up resistor. When RY/BY# = V_{OH}, the device is ready to accept read operations and commands. When RY/BY# = V_{OL}, the device is either executing an embedded algorithm or the device is executing a hardware reset operation.
CLK	Input	Clock Input that can be tied to the system or microprocessor clock and provides the fundamental timing and internal operating frequency.
ADV#	Input	Load Burst Address input. Indicates that the valid address is present on the address inputs.
IND#	Output	End of burst indicator for finite bursts only. IND is low when the last word in the burst sequence is at the data outputs.
WAIT#	Output	Provides data valid feedback only when the burst length is set to continuous.
WP#	Input	Write Protect Input. At V_{IL}, disables program and erase functions in two outermost sectors of the large bank.
ACC	Input	Acceleration input. At V_{HH}, accelerates erasing and programming. When not used for acceleration, ACC = V_{SS} or V_{CC}.
RESET#	Input	Hardware Reset.

3. Block Diagram



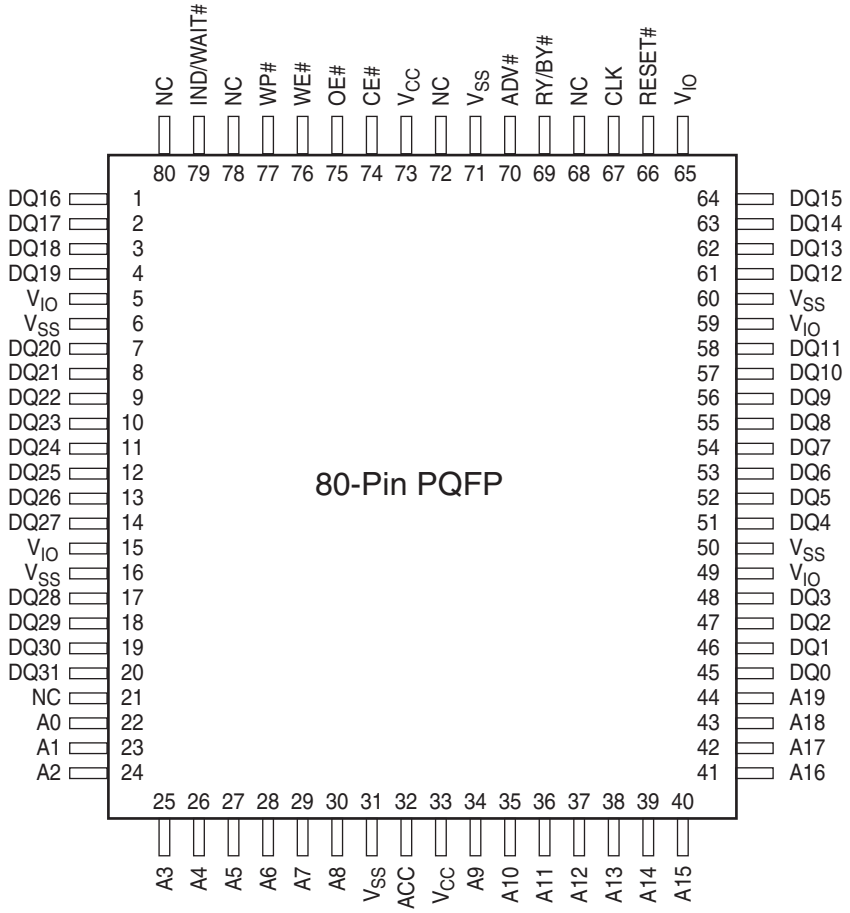
Note
3.Address bus is A19–A0 for 32 Mb device, A18–A0 for 16 Mb device. Data bus is D31–DQ0.

4. Block Diagram of Simultaneous Read/Write Circuit



5. Physical Dimensions/Connection Diagrams

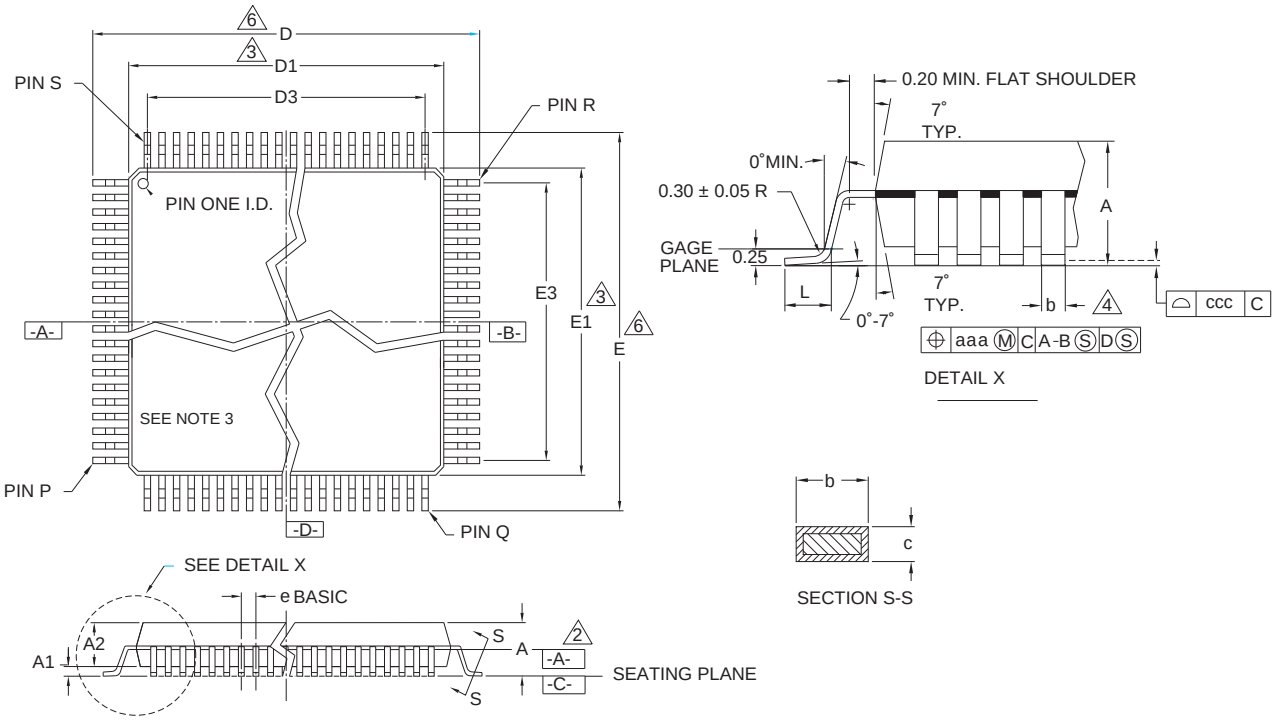
5.1 80-Pin PQFP Connection Diagram



Notes

4. On 16 Mb device, pin 44 (A19) is NC.
5. Pin 69 (RY/BY#) is Open Drain and requires an external pull-up resistor.

5.2 PQR080–80-Lead Plastic Quad Flat Package Physical Dimensions



PACKAGE	PQR 080			NOTES
JEDEC	MO-108(B)CB-1			
SYMBOL	MIN	NOM	MAX	
A	--	--	3.35	
A1	0.25	--	--	
A2	2.70	2.80	2.90	
b	0.30	--	0.45	SEE NOTE 4
c	0.15	--	0.23	
D	17.00	17.20	17.40	
D1	13.90	14.00	14.10	SEE NOTE 3
D3	--	12.0	--	REFERENCE
e	--	0.80	--	BASIC, SEE NOTE 7
E	23.00	23.20	23.40	
E1	19.90	20.00	20.10	SEE NOTE 3
E3	--	18.40	--	REFERENCE
aaa	---	0.20	---	
ccc	0.10			
L	0.73	0.88	1.03	
P	24			
Q	40			
R	64			
S	80			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DATUM PLANE -A- IS LOCATED AT THE MOLD PARTING LINE AND IS COINCIDENT WITH THE BOTTOM OF THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY.
3. DIMENSIONS "D1" AND "E1" DO NOT INCLUD MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS "D1" AND "E1" INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -A-
4. DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION.
5. CONTROLLING DIMENSIONS: MILLIMETER.
6. DIMENSIONS "D" AND "E" ARE MEASURED FROM BOTH INNERMOST AND OUTERMOST POINTS.
7. DEVIATION FROM LEAD-TIP TRUE POSITION SHALL BE WITHIN ±0.0076 mm FOR PITCH > 0.5 mm AND WITHIN ±0.04 FOR PITCH $\leq$ 0.5 mm.
8. LEAD COPLANARITY SHALL BE WITHIN: (REFER TO 06-500)
   1 - 0.10 mm FOR DEVICES WITH LEAD PITCH OF 0.65 - 0.80 mm
   2 - 0.076 mm FOR DEVICES WITH LEAD PITCH OF 0.50 mm.
   COPLANARITY IS MEASURED PER SPECIFICATION 06-500.
9. HALF SPAN (CENTER OF PACKAGE TO LEAD TIP) SHALL BE WITHIN ±0.0085".

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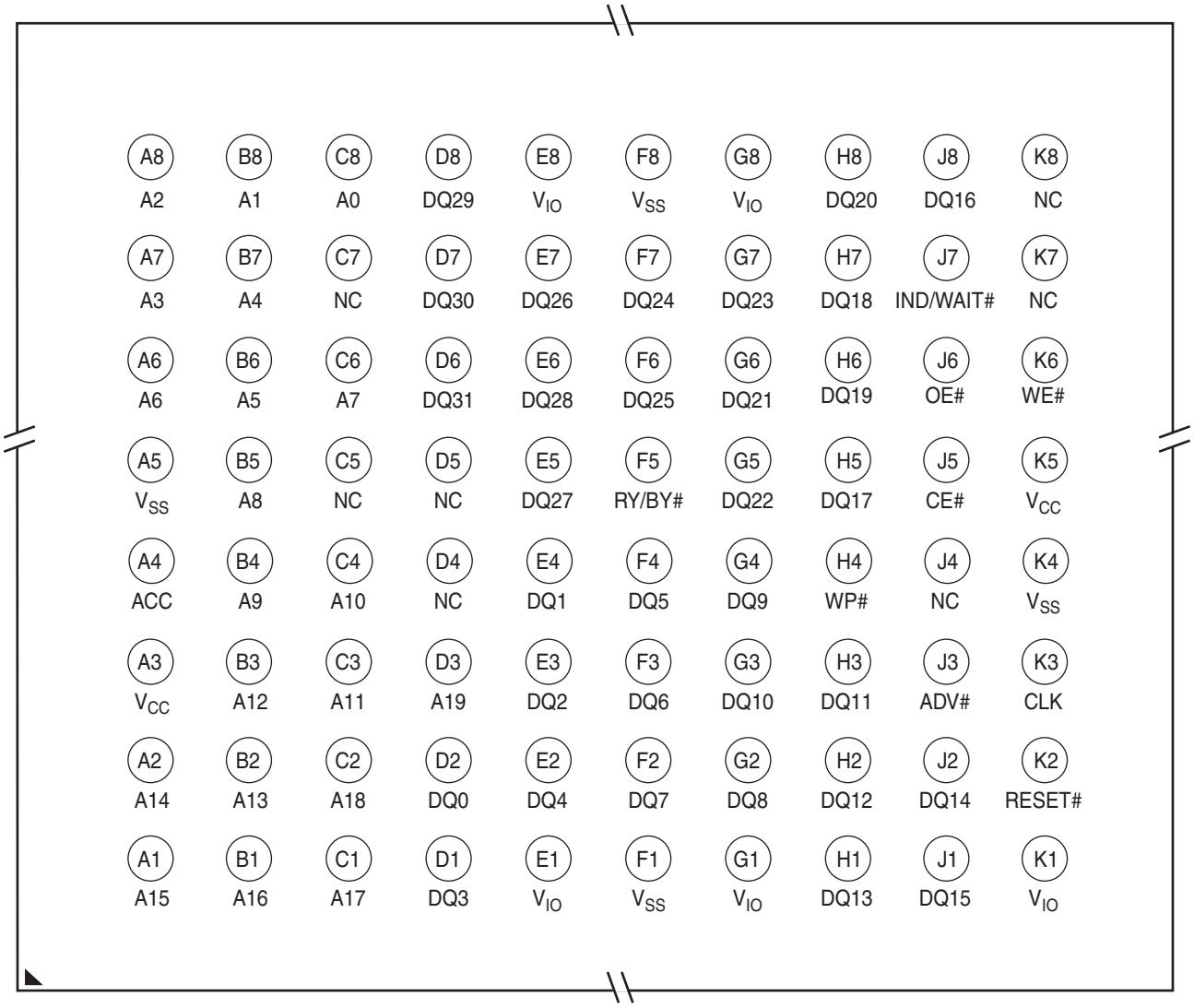
5.3 80-Ball Fortified BGA Connection Diagram



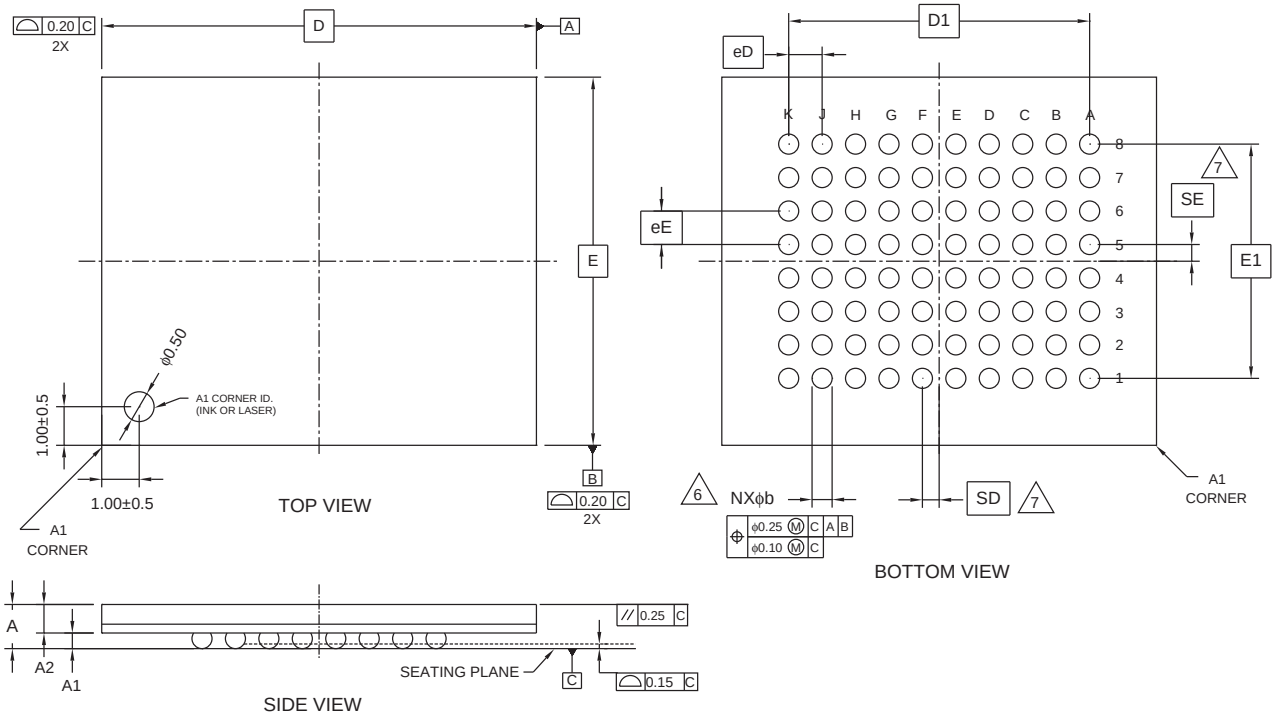
Notes

6. On 16 Mb device, ball D3 (A19) is NC.
7. Ball F5 (RY/BY#) is Open Drain and requires an external pull-up resistor.

5.4 Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (BGA). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

5.5 LAA080–80-ball Fortified Ball Grid Array (13 x 11 mm) Physical Dimensions



PACKAGE	LAA 080			NOTE
JEDEC	N/A			
	13.00 x 11.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	--	--	1.40	PROFILE HEIGHT
A1	0.40	--	--	STANDOFF
A2	0.60	--	--	BODY THICKNESS
D	13.00 BSC.			BODY SIZE
E	11.00 BSC.			BODY SIZE
D1	9.00 BSC.			MATRIX FOOTPRINT
E1	7.00 BSC.			MATRIX FOOTPRINT
MD	10			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
N	80			BALL COUNT
ϕb	0.50	0.60	0.70	BALL DIAMETER
eD	1.00 BSC.			BALL PITCH - D DIRECTION
eE	1.00 BSC.			BALL PITCH - E DIRECTION
SD/SE	0.50 BSC			SOLDER BALL PLACEMENT

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION. N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW , SD OR SE = e/2
8. N/A
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

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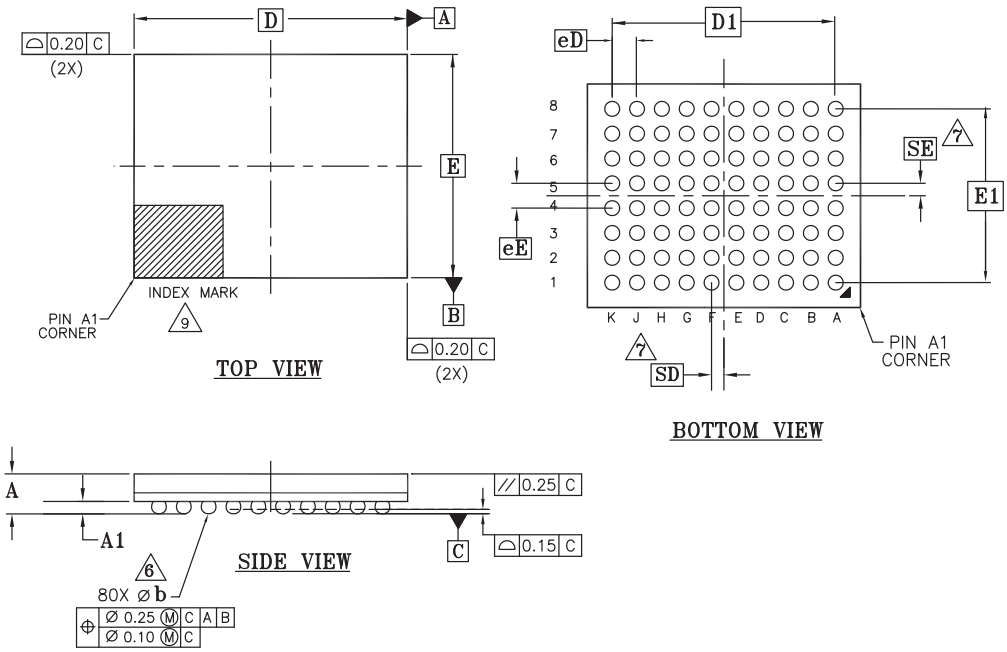
5.6 LAD080–80-ball Fortified Ball Grid Array (11 x 9 mm) Physical Dimensions



PACKAGE	LAD 080			
JEDEC	N/A			
D X E	11.00 mm x 9.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.40	PROFILE
A1	0.35	0.45	0.55	BALL HEIGHT
D	11.00 BSC			BODY SIZE
E	9.00 BSC			BODY SIZE
D1	9.00 BSC			MATRIX FOOTPRINT
E1	7.00 BSC			MATRIX FOOTPRINT
MD	10			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
N	80			BALL COUNT
øb	0.55	0.65	0.75	BALL DIAMETER
eE	1.00 BSC			BALL PITCH
eD	1.00 BSC			BALL PITCH
SD / SE	0.50 BSC			SOLDER BALL PLACEMENT
	N/A			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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6. Product Overview

The S29CD-J and S29CL-J families consist of 32 Mb and 16 Mb, 2.6 volt-only (CD-J) or 3.3 volt-only (CL-J), simultaneous read/write, dual boot burst mode Flash devices optimized for today's automotive designs.

These devices are organized in 1,048,576 double words (32 Mb) or 524,288 double words (16 Mb) and are capable of linear burst read (2, 4, or 8 double words) with wraparound. (Note that 1 double word = 32 bits.) These products also offer single word programming with program/erase suspend and resume functionality. Additional features include:

- Advanced Sector Protection methods for protecting sectors as required.
- 256 bytes of Secured Silicon area for storing customer or factory secured information. The Secured Silicon Sector is One-Time Programmable.
- Electronic marking.

6.1 Memory Map

The S29CD-J and S29CL-J devices consist of two banks organized as shown in Table 1, Table 2, Table 3 and Table 4.

Table 1. S29CD016J/CL016J (Top Boot) Sector and Memory Address Map

	Sector	Sector Group	x32 Address Range (A18:A0)	Sector Size (KDwords)		Sector	Sector Group	x32 Address Range (A18:A0)	Sector Size (KDwords)
Bank 0 (Note 9)	SA0 (Note 8)	SG0	00000h–007FFh	2	Bank 1 (Note 9)	SA15	SG10	20000h–23FFFh	16
	SA1	SG1	00800h–00FFFh	2		SA16		24000h–27FFFh	16
	SA2	SG2	01000h–017FFh	2		SA17		28000h–2BFFFh	16
	SA3	SG3	01800h–01FFFh	2		SA18		2C000h–2FFFFh	16
	SA4	SG4	02000h–027FFh	2		SA19	SG11	30000h–33FFFh	16
	SA5	SG5	02800h–02FFFh	2		SA20		34000h–37FFFh	16
	SA6	SG6	03000h–037FFh	2		SA21		38000h–3BFFFh	16
	SA7	SG7	03800h–03FFFh	2		SA22		3C000h–3FFFFh	16
	SA8	SG8	04000h–07FFFh	16		SA23	SG12	40000h–43FFFh	16
	SA9		08000h–0BFFFh	16		SA24		44000h–47FFFh	16
	SA10		0C000h–0FFFFh	16		SA25		48000h–4BFFFh	16
	SA11	SG9	10000h–13FFFh	16		SA26		4C000h–4FFFFh	16
	SA12		14000h–17FFFh	16		SA27	SG13	50000h–53FFFh	16
	SA13		18000h–1BFFFh	16		SA28		54000h–57FFFh	16
	SA14		1C000h–1FFFFh	16		SA29		58000h–5BFFFh	16
						SA30		5C000h–5FFFFh	16
						SA31	SG14	60000h–63FFFh	16
						SA32		64000h–67FFFh	16
						SA33		68000h–6BFFFh	16
						SA34		6C000h–6FFFFh	16
						SA35	SG15	70000h–73FFFh	16
						SA36		74000h–77FFFh	16
						SA37		78000h–7BFFFh	16
						SA38	SG16	7C000h–7C7FFh	2
						SA39	SG17	7C800h–7CFFFh	2
						SA40	SG18	7D000h–7D7FFh	2
						SA41	SG19	7D800h–7DFFFh	2
						SA42	SG20	7E000h–7E7FFh	2
						SA43	SG21	7E800h–7EFFFh	2
						SA44 (Note 10)	SG22	7F000h–7F7FFh	2
						SA45 (Note 10)	SG23	7F800h–7FFFFh	2

Notes

8. Secured Silicon Sector overlays this sector when enabled.
9. The bank address is determined by A18 and A17. BA = 00 for Bank 0 and BA = 01, 10, or 11 for Bank 1.
10. This sector has the additional WP# pin sector protection feature.

Table 2. S29CD016J/CL016J (Bottom Boot) Sector and Memory Address Map

Sector		Sector Group	x32 Address Range (A18:A0)	Sector Size (KDwords)		Sector	Sector Group	x32 Address Range (A18:A0)	Sector Size (KDwords)
Bank 0 (Note 12)	SA0 (Note 11)	SG0	00000h–007FFh	2	Bank 1 (Note 12)	SA31	SG14	60000h–63FFFh	16
	SA1 (Note 11)	SG1	00800h–00FFFh	2		SA32		64000h–67FFFh	16
	SA2	SG2	01000h–017FFh	2		SA33		68000h–6BFFFh	16
	SA3	SG3	01800h–01FFFh	2		SA34		6C000h–6FFFFh	16
	SA4	SG4	02000h–027FFh	2		SA35	SG15	70000h–73FFFh	16
	SA5	SG5	02800h–02FFFh	2		SA36		74000h–77FFFh	16
	SA6	SG6	03000h–037FFh	2		SA37		78000h–7BFFFh	16
	SA7	SG7	03800h–03FFFh	2		SA38	SG16	7C000h–7C7FFh	2
	SA8	SG8	04000h–07FFFh	16		SA39	SG17	7C800h–7CFFFh	2
	SA9		08000h–0BFFFh	16		SA40	SG18	7D000h–7D7FFh	2
	SA10		0C000h–0FFFFh	16		SA41	SG19	7D800h–7DFFFh	2
	SA11	SG9	10000h–13FFFh	16		SA42	SG20	7E000h–7E7FFh	2
	SA12		14000h–17FFFh	16		SA43	SG21	7E800h–7EFFFh	2
	SA13		18000h–1BFFFh	16		SA44	SG22	7F000h–7F7FFh	2
	SA14		1C000h–1FFFFh	16		SA45 (Note 13)	SG23	7F800h–7FFFFh	2
	SA15	SG10	20000h–23FFFh	16					
	SA16		24000h–27FFFh	16					
	SA17		28000h–2BFFFh	16					
	SA18		2C000h–2FFFFh	16					
	SA19	SG11	30000h–33FFFh	16					
	SA20		34000h–37FFFh	16					
	SA21		38000h–3BFFFh	16					
	SA22		3C000h–3FFFFh	16					
	SA23	SG12	40000h–43FFFh	16					
	SA24		44000h–47FFFh	16					
	SA25		48000h–4BFFFh	16					
	SA26		4C000h–4FFFFh	16					
	SA27	SG13	50000h–53FFFh	16					
	SA28		54000h–57FFFh	16					
	SA29		58000h–5BFFFh	16					
	SA30		5C000h–5FFFFh	16					

Notes

11. This sector has the additional WP# pin sector protection feature.
12. The bank address is determined by A18 and A17. BA = 00, 01, or 10 for Bank 0 and BA = 11 for Bank 1.
13. Secured Silicon Sector overlays this sector when enabled.

Table 3. S29CD032J/CL032J (Top Boot) Sector and Memory Address Map

Sector	Sector Group	x32 Address Range (A19:A0)	Sector Size (KDwords)		Sector	Sector Group	x32 Address Range (A19:A0)	Sector Size (KDwords)
Bank 0 (Note 15)					**Bank 1 continued (Note 15)**			
SA0 (Note 14)	SG0	00000h–007FFh	2		SA39	SG16	80000h–83FFFh	16
SA1	SG1	00800h–00FFFh	2		SA40		84000h–87FFFh	16
SA2	SG2	01000h–017FFh	2		SA41		88000h–8BFFFh	16
SA3	SG3	01800h–01FFFh	2		SA42		8C000h–8FFFFh	16
SA4	SG4	02000h–027FFh	2		SA43	SG17	90000h–93FFFh	16
SA5	SG5	02800h–02FFFh	2		SA44		94000h–97FFFh	16
SA6	SG6	03000h–037FFh	2		SA45		98000h–9BFFFh	16
SA7	SG7	03800h–03FFFh	2		SA46		9C000h–9FFFFh	16
SA8	SG8	04000h–07FFFh	16		SA47	SG18	A0000h–A3FFFh	16
SA9		08000h–0BFFFh	16		SA48		A4000h–A7FFFh	16
SA10		0C000h–0FFFFh	16		SA49		A8000h–ABFFFh	16
SA11	SG9	10000h–13FFFh	16		SA50		AC000h–AFFFFh	16
SA12		14000h–17FFFh	16		SA51	SG19	B0000h–B3FFFh	16
SA13		18000h–1BFFFh	16		SA52		B4000h–B7FFFh	16
SA14		1C000h–1FFFFh	16		SA53		B8000h–BBFFFh	16
SA15	SG10	20000h–23FFFh	16		SA54		BC000h–BFFFFh	16
SA16		24000h–27FFFh	16		SA55	SG20	C0000h–C3FFFh	16
SA17		28000h–2BFFFh	16		SA56		C4000h–C7FFFh	16
SA18		2C000h–2FFFFh	16		SA57		C8000h–CBFFFh	16
SA19	SG11	30000h–33FFFh	16		SA58		CC000h–CFFFFh	16
SA20		34000h–37FFFh	16		SA59	SG21	D0000h–D3FFFh	16
SA21		38000h–3BFFFh	16		SA60		D4000h–D7FFFh	16
SA22		3C000h–3FFFFh	16		SA61		D8000h–DBFFFh	16
Bank 1 (Note 15)					SA62		DC000h–DFFFFh	16
SA23	SG12	40000h–43FFFh	16		SA63	SG22	E0000h–E3FFFh	16
SA24		44000h–47FFFh	16		SA64		E4000h–E7FFFh	16
SA25		48000h–4BFFFh	16		SA65		E8000h–EBFFFh	16
SA26		4C000h–4FFFFh	16		SA66		EC000h–EFFFFh	16
SA27	SG13	50000h–53FFFh	16		SA67	SG23	F0000h–F3FFFh	16
SA28		54000h–57FFFh	16		SA68		F4000h–F7FFFh	16
SA29		58000h–5BFFFh	16		SA69		F8000h–FBFFFh	16
SA30		5C000h–5FFFFh	16		SA70	SG24	FC000h–FC7FFh	2
SA31	SG14	60000h–63FFFh	16		SA71	SG25	FC800h–FCFFFh	2
SA32		64000h–67FFFh	16		SA72	SG26	FD000h–FD7FFh	2
SA33		68000h–6BFFFh	16		SA73	SG27	FD800h–FDFFFh	2
SA34		6C000h–6FFFFh	16		SA74	SG28	FE000h–FE7FFh	2

Table 3. S29CD032J/CL032J (Top Boot) Sector and Memory Address Map (Continued)

Sector	Sector Group	x32 Address Range (A19:A0)	Sector Size (KDwords)		Sector	Sector Group	x32 Address Range (A19:A0)	Sector Size (KDwords)
Bank 0 (Note 15)					**Bank 1 continued (Note 15)**			
SA35	SG15	70000h–73FFFh	16		SA75	SG29	FE800h–FEFFFh	2
SA36		74000h–77FFFh	16		SA76 (Note 16)	SG30	FF000h–FF7FFh	2
SA37		78000h–7BFFFh	16		SA77 (Note 16)	SG31	FF800h–FFFFFh	2
SA38		7C000h–7FFFFh	16					

Notes

14. Secured Silicon Sector overlays this sector when enabled.
15. The bank address is determined by A19 and A18. BA = 00 for Bank 0 and BA = 01, 10, or 11 for Bank 1.
16. This sector has the additional WP# pin sector protection feature.

Table 4. S29CD032J/CL032J (Bottom Boot) Sector and Memory Address Map

Sector	Sector Group	x32 Address Range (A19:A0)	Sector Size (KDwords)		Sector	Sector Group	x32 Address Range (A19:A0)	Sector Size (KDwords)
Bank 0 (Note 18)					**Bank 0 continued (Note 18)**			
SA0 (Note 19)	SG0	00000h–007FFh	2		SA39	SG16	80000h–83FFFh	16
SA1 (Note 19)	SG1	00800h–00FFFh	2		SA40		84000h–87FFFh	16
SA2	SG2	01000h–017FFh	2		SA41		88000h–8BFFFh	16
SA3	SG3	01800h–01FFFh	2		SA42		8C000h–8FFFFh	16
SA4	SG4	02000h–027FFh	2		SA43	SG17	90000h–93FFFh	16
SA5	SG5	02800h–02FFFh	2		SA44		94000h–97FFFh	16
SA6	SG6	03000h–037FFh	2		SA45		98000h–9BFFFh	16
SA7	SG7	03800h–03FFFh	2		SA46		9C000h–9FFFFh	16
SA8	SG8	04000h–07FFFh	16		SA47	SG18	A0000h–A3FFFh	16
SA9		08000h–0BFFFh	16		SA48		A4000h–A7FFFh	16
SA10		0C000h–0FFFFh	16		SA49		A8000h–ABFFFh	16
SA11	SG9	10000h–13FFFh	16		SA50		AC000h–AFFFFh	16
SA12		14000h–17FFFh	16		SA51	SG19	B0000h–B3FFFh	16
SA13		18000h–1BFFFh	16		SA52		B4000h–B7FFFh	16
SA14		1C000h–1FFFFh	16		SA53		B8000h–BBFFFh	16
SA15	SG10	20000h–23FFFh	16		SA54		BC000h–BFFFFh	16
SA16		24000h–27FFFh	16		**Bank 1 (Note 18)**			
SA17		28000h–2BFFFh	16		SA55	SG20	C0000h–C3FFFh	16
SA18		2C000h–2FFFFh	16		SA56		C4000h–C7FFFh	16
SA19	SG11	30000h–33FFFh	16		SA57		C8000h–CBFFFh	16
SA20		34000h–37FFFh	16		SA58		CC000h–CFFFFh	16
SA21		38000h–3BFFFh	16		SA59	SG21	D0000h–D3FFFh	16
SA22		3C000h–3FFFFh	16		SA60		D4000h–D7FFFh	16
SA23	SG12	40000h–43FFFh	16		SA61		D8000h–DBFFFh	16
SA24		44000h–47FFFh	16		SA62		DC000h–DFFFFh	16
SA25		48000h–4BFFFh	16		SA63	SG22	E0000h–E3FFFh	16
SA26		4C000h–4FFFFh	16		SA64		E4000h–E7FFFh	16
SA27	SG13	50000h–53FFFh	16		SA65		E8000h–EBFFFh	16
SA28		54000h–57FFFh	16		SA66		EC000h–EFFFFh	16
SA29		58000h–5BFFFh	16		SA67	SG23	F0000h–F3FFFh	16
SA30		5C000h–5FFFFh	16		SA68		F4000h–F7FFFh	16
SA31	SG14	60000h–63FFFh	16		SA69		F8000h–FBFFFh	16
SA32		64000h–67FFFh	16		SA70	SG24	FC000h–FC7FFh	2
SA33		68000h–6BFFFh	16		SA71	SG25	FC800h–FCFFFh	2
SA34		6C000h–6FFFFh	16		SA72	SG26	FD000h–FD7FFh	2
SA35	SG15	70000h–73FFFh	16		SA73	SG27	FD800h–FDFFFh	2
SA36		74000h–77FFFh	16		SA74	SG28	FE000h–FE7FFh	2
SA37		78000h–7BFFFh	16		SA75	SG29	FE800h–FEFFFh	2
SA38		7C000h–7FFFFh	16		SA76	SG30	FF000h–FF7FFh	2
					SA77 (Note 17)	SG31	FF800h–FFFFFh	2

Notes

17. This sector has the additional WP# pin sector protection feature.
18. The bank address is determined by A19 and A18. BA = 00, 01, or 10 for Bank 0 and BA = 11 for Bank 1.
19. The Secured Silicon Sector overlays this sector when enabled.

7. Device Operations

This section describes the read, program, erase, simultaneous read/write operations, and reset features of the Flash devices.

Operations are initiated by writing specific commands or a sequence with specific address and data patterns into the command register (see Table 5). The command register itself does not occupy any addressable memory location; rather, it is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as input to the internal state machine; the state machine outputs dictate the function of the device. Writing incorrect address and data values or writing them in an improper sequence may place the device in an unknown state, in which case the system must write the reset command in order to return the device to the reading array data mode.

7.1 Device Operation Table

The device must be set up appropriately for each operation. Table 5 describes the required state of each control pin for any particular operation.

Table 5. Device Bus Operation

Operation	CE#	OE#	WE#	RESET#	CLK	ADV#	Addresses	Data (DQ0–DQ31)
Read	L	L	H	H	X	X	A_{IN}	D_{OUT}
Asynchronous Write	L	H	L	H	X	X	A_{IN}	D_{IN}
Synchronous Write	L	H	L	H	↑	↑	A_{IN}	D_{IN}
Standby (CE#)	H	X	X	H	H	X	X	High-Z
Output Disable	L	H	H	H	X	X	High-Z	High-Z
Reset	X	X	X	L	X	X	X	High-Z
PPB Protection Status (Note 2)	L	L	H	H	X	X	Sector Address, A9 = V_{ID}, A7 – A0 = 02h	00000001h, (protected) A6 = H 00000000h (unprotect) A6 = L
Burst Read Operations								
Load Starting Burst Address	L	X	H	H	↑	↓	A_{IN}	X
Advance Burst to next address with appropriate Data presented on the Data bus	L	L	H	H	↑	H	X	Burst Data Out
Terminate Current Burst Read Cycle	H	X	H	H	↑	X	X	High-Z
Terminate Current Burst Read Cycle with RESET#	X	X	H	L	X	X	X	High-Z
Terminate Current Burst Read Cycle; Start New Burst Read Cycle	L	H	H	H	↑	↓	A_{IN}	X

Legend

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, X = Don't care.

Notes

20. WP# controls the two outermost sectors of the top boot block or the two outermost sectors of the bottom boot block.
21. DQ0 reflects the sector PPB (or sector group PPB) and DQ1 reflects the DYB.

7.2 Asynchronous Read

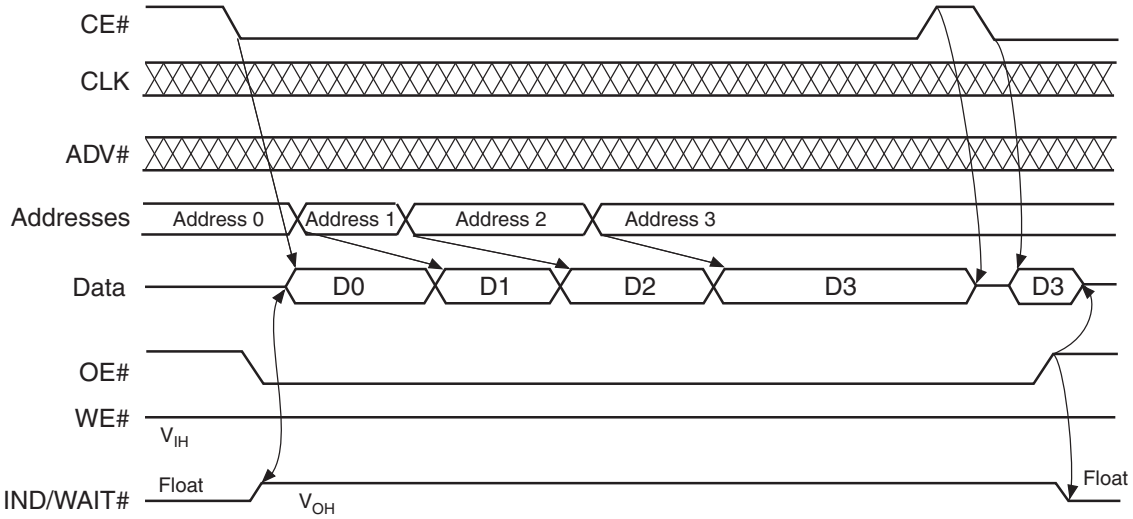
All memories require access time to output array data. In an asynchronous read operation, data is read from one memory location at a time. Addresses are presented to the device in random order, and the propagation delay through the device causes the data on its outputs to arrive asynchronously with the address on its inputs.

The internal state machine is set for asynchronously reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

The device has two control functions which must be satisfied in order to obtain data at the outputs. CE# is the power control and should be used for device selection (CE# must be set to V_{IL} to read data). OE# is the output control and should be used to gate data to the output pins if the device is selected (OE# must be set to V_{IL} in order to read data). WE# should remain at V_{IH} (when reading data).

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the output pins. The output enable access time (t_{OE}) is the delay from the falling edge of OE# to valid data at the output pins (assuming the addresses have been stable for at least a period of t_{ACC}-t_{OE} and CE# has been asserted for at least t_{CE}-t_{OE} time). Figure 1 shows the timing diagram of an asynchronous read operation.

Figure 1. Asynchronous Read Operation



Note
22.Operation is shown for the 32-bit data bus. For the 16-bit data bus, A-1 is required.

Refer to Asynchronous Operations on page 52 for timing specifications and to Figure 19 Conventional Read Operations Timings on page 53 for another timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

7.3 Hardware Reset (RESET#)

The RESET# pin is an active low signal that is used to reset the device under any circumstances. A logic “0” on this input forces the device out of any mode that is currently executing back to the reset state. RESET# may be tied to the system reset circuitry. A system reset would thus also reset the device. To avoid a potential bus contention during a system reset, the device is isolated from the DQ data bus by tristating the data outputs for the duration of the RESET pulse. All data outputs are “don’t care” during the reset operation.

If RESET# is asserted during a program or erase operation, the RY/BY# output remains low until the reset operation is internally complete. The RY/BY# pin can be used to determine when the reset operation is complete. Since the device offers simultaneous read/write operation, the host system may read a bank after a period of t_{READY2}, if the bank was in the read/reset mode at the time RESET# was asserted. If one of the banks was in the middle of either a program or erase operation when RESET# was asserted, the user must wait a period of t_{READY} before accessing that bank.

Asserting RESET# during a program or erase operation leaves erroneous data stored in the address locations being operated on at the time of device reset. These locations need updating after the reset operation is complete. See Hardware Reset (RESET#) on page 56 for timing specifications.

Asserting RESET# active during V_{CC} and V_{IO} power-up is required to guarantee proper device initialization until V_{CC} and V_{IO} have reached their steady state voltages. See V_{CC} and V_{IO} Power-up on page 52.

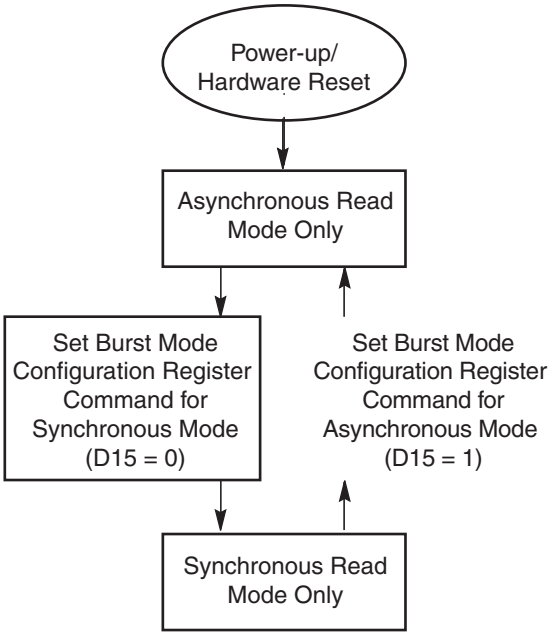
7.4 Synchronous (Burst) Read Mode and Configuration Register

When a series of adjacent addresses need to be read from the device, the synchronous (or burst read) mode can be used to significantly reduce the overall time needed for the device to output array data. After an initial access time required for the data from the first address location, subsequent data is output synchronized to a clock input provided by the system.

The device offers a linear method of burst read operation which is discussed in 2-, 4-, 8- Double Word Linear Burst Operation on page 22.

Since the device defaults to asynchronous read mode after power-up or a hardware reset, the configuration register must be set in order to enable the burst read mode. Other Configuration Register settings include the number of wait states to insert before the initial word (t_{IACC}) of each burst access and when RDY indicates that data is ready to be read. Prior to entering the burst mode, the system first determines the configuration register settings (and read the current register settings if desired via the Read Configuration Register command sequence), then write the configuration register command sequence. See Configuration Register on page 24, and Table 34 on page 67 for further details. Once the configuration register is written to enable burst mode operation, all subsequent reads from the array are returned using the burst mode protocols.

Figure 2. Synchronous/Asynchronous State Diagram



The device outputs the initial word subject to the following operational conditions:

- t_{IACC} specification: The time from the rising edge of the first clock cycle after addresses are latched to valid data on the device outputs.
- Configuration register setting CR13-CR10: The total number of clock cycles (wait states) that occur before valid data appears on the device outputs. The effect is that t_{IACC} is lengthened.

Like the main memory access, the Secured Silicon Sector memory is accessed with the same burst or asynchronous timing as defined in the Configuration Register. However, the user must recognize burst operations past the 256 byte Secured Silicon boundary returns invalid data.

Burst read operations occur only to the main flash memory arrays. The Configuration Register and protection bits are treated as single cycle reads, even when burst mode is enabled. Read operations to these locations results in the data remaining valid while OE# is at V_{IL}, regardless of the number of CLK cycles applied to the device.

7.4.1 2-, 4-, 8- Double Word Linear Burst Operation

In a linear burst read operation, a fixed number of words (2, 4, or 8 double words) are read from consecutive addresses that are determined by the group within which the starting address falls. Note that 1 double word = 32 bits. See Table 6 for all valid burst output sequences.

The IND/WAIT# signal, or End of Burst Indicator signal, transitions active (V_{IL}) during the last transfer of data in a linear burst read before a wrap around. This transition indicates that the system should initiate another ADV# to start the next burst access. If the system continues to clock the device, the next access wraps around to the starting address of the previous burst access. The IND/WAIT# signal is floating when not active.

Table 6. 32-Bit Linear and Burst Data Order

Data Transfer Sequence	Output Data Sequence (Initial Access Address)
Two Linear Data Transfers	0-1 (A0 = 0) 1-0 (A0 = 1)
Four Linear Data Transfers	0-1-2-3 (A1-A0 = 00) 1-2-3-0 (A1-A0 = 01) 2-3-0-1 (A1-A0 = 10) 3-0-1-2 (A1-A0 = 11)
Eight Linear Data Transfers	0-1-2-3-4-5-6-7 (A2-A0 = 000) 1-2-3-4-5-6-7-0 (A2-A0 = 001) 2-3-4-5-6-7-0-1 (A2-A0 = 010) 3-4-5-6-7-0-1-2 (A2-A0 = 011) 4-5-6-7-0-1-2-3 (A2-A0 = 100) 5-6-7-0-1-2-3-4 (A2-A0 = 101) 6-7-0-1-2-3-4-5 (A2-A0 = 110) 7-0-1-2-3-4-5-6 (A2-A0 = 111)

Notes

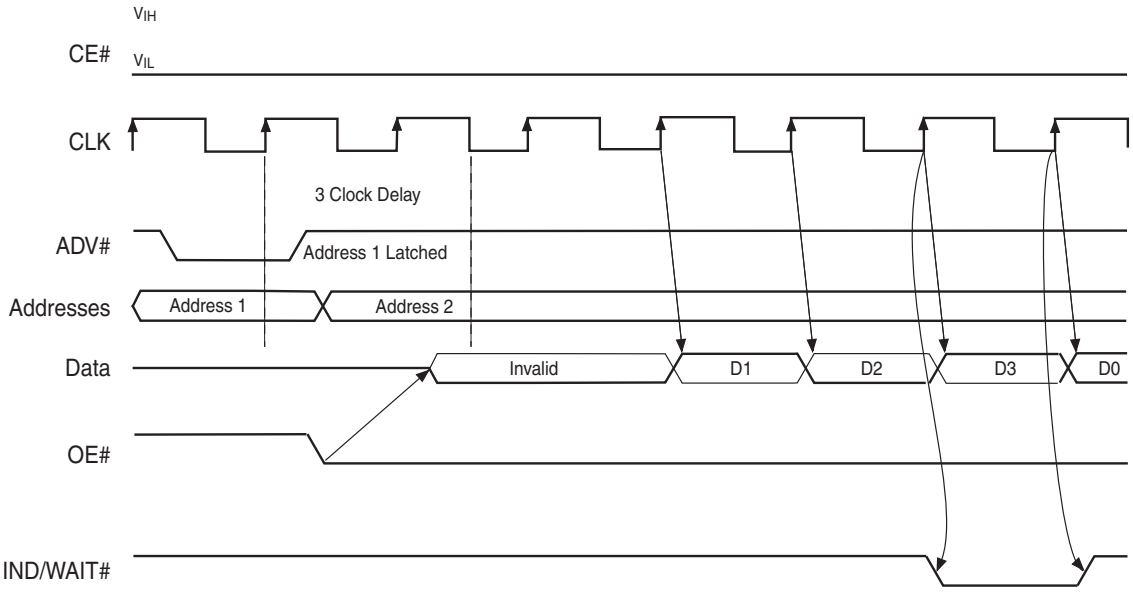
23. The default configuration in the Control Register for Bit 6 is “1,” indicating that the device delivers data on the rising edge of the CLK signal.
24. The device is capable of holding data for one CLK cycle.
25. If RESET# is asserted low during a burst access, the burst access is immediately terminated and the device defaults back to asynchronous read mode. When this happens, the DQ data bus signal floats and the Configuration Register contents are reset to their default conditions.
26. CE# must meet the required burst read setup times for burst cycle initiation. If CE# is taken to V_{IH} at any time during the burst linear or burst cycle, the device immediately exits the burst sequence and floats the DQ bus signal.
27. Restarting a burst cycle is accomplished by taking CE# and ADV# to V_{IL}.
28. A burst access is initiated and the address is latched on the first rising CLK edge when ADV# is active or upon a rising ADV# edge, whichever occurs first. If the ADV# signal is taken to VIL prior to the end of a linear burst sequence, the previous address is discarded and subsequent burst transfers are invalid. A new burst is initiated when ADV# transitions back to V_{IH} before a clock edge.
29. The OE# (Output Enable) pin is used to enable the linear burst data on the DQ data bus pin. De-asserting the OE# pin to V_{IH} during a burst operation floats the data bus, but the device continues to operate internally as if the burst sequence continues until the linear burst is complete. The OE# pin does not halt the burst sequence, The DQ bus remains in the float state until OE# is taken to V_{IL}.
30. Halting the burst sequence is accomplished by either taking CE# to V_{IH} or re-issuing a new ADV# pulse.

The IND/WAIT# signal is controlled by the OE# signal. If OE# is at V_{IH}, the IND/WAIT# signal floats and is not driven. If OE# is at V_{IL}, the IND/ WAIT# signal is driven at V_{IH} until it transitions to V_{IL}, indicating the end of the burst sequence. Table 7 lists the valid combinations of the Configuration Register bits that impact the IND/WAIT# timing. See Figure 3 for the IND/WAIT# timing diagram.

Table 7. Valid Configuration Register Bit Definition for IND/WAIT#

CR9 (DOC)	CR8 (WC)	CR6 (CC)	Definition
0	0	1	IND/WAIT# = V_{IL} for 1-CLK cycle, Active on last transfer, Driven on rising CLK edge
0	1	1	IND/WAIT# = V_{IL} for 1-CLK cycle, Active on second to last transfer, Driven on rising CLK edge

Figure 3. End of Burst Indicator (IND/WAIT#) Timing for Linear 4 Double Word Burst Operation



Note
31.Operation is shown for the 32-bit data bus. Figure shown with 3-CLK initial access delay configuration, linear address, 4-doubleword burst, output on rising CLK edge, data hold for 1-CLK, IND/WAIT# asserted on the last transfer before wrap-around.

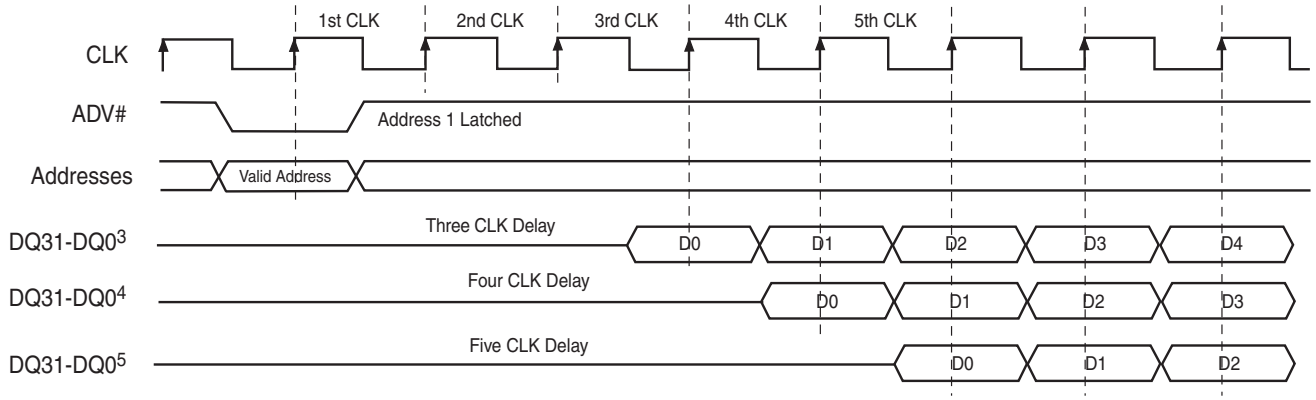
7.4.2 Initial Burst Access Delay

Initial Burst Access Delay is defined as the number of clock cycles that must elapse from the first valid clock edge after ADV# assertion (or the rising edge of ADV#) until the first valid CLK edge when the data is valid. Burst access is initiated and the address is latched on the first rising CLK edge when ADV# is active or upon a rising ADV# edge, whichever comes first. The Initial Burst Access Delay is determined in the Configuration Register (CR13-CR10). Refer to Table 9 for the initial access delay configurations under CR13-CR10. See Figure 4 for the Initial Burst Delay Control timing diagram. Note that the Initial Access Delay for a burst access has no effect on asynchronous read operations.

Table 8. Burst Initial Access Delay

CR13	CR12	CR11	CR10	Initial Burst Access (CLK cycles)
0	0	0	1	3
0	0	1	0	4
0	0	1	1	5
0	1	0	0	6
0	1	0	1	7
0	1	1	0	8
0	1	1	1	9

Figure 4. Initial Burst Delay Control



Notes

32. Burst access starts with a rising CLK edge and when ADV# is active.
33. Configurations register 6 is always set to 1 (CR6 = 1). Burst starts and data outputs on the rising CLK edge.
34. CR [13-10] = 1 or three clock cycles.
35. CR [13-10] = 2 or four clock cycles.
36. CR [13-10] = 3 or five clock cycles.

7.4.3 Configuration Register

The configuration register sets various operational parameters associated with burst mode. Upon power-up or hardware reset, the device defaults to the asynchronous read mode and the configuration register settings are in their default state. (See Table 10 for the default Configuration Register settings.) The host system determines the proper settings for the entire configuration register, and then execute the Set Configuration Register command sequence before attempting burst operations. The configuration register is not reset after deasserting CE#.

The Configuration Register does not occupy any addressable memory location, but rather, is accessed by the Configuration Register commands. The Configuration Register is readable at any time, however, writing the Configuration Register is restricted to times when the Embedded Algorithm™ is not active. If the user attempts to write the Configuration Register while the Embedded Algorithm is active, the write operation is ignored and the contents of the Configuration Register remain unchanged.

The Configuration Register is a 16 bit data field which is accessed by DQ15–DQ0. During a read operation, DQ31–DQ16 returns all zeroes. Also, the Configuration Register reads operate the same as the Autoselect command reads. When the command is issued, the bank address is latched along with the command. Read operations to the bank that was specified during the Configuration Register read command return Configuration Register contents. Read operations to the other bank return flash memory data. Either bank address is permitted when writing the Configuration Register read command.

The configuration register can be read with a four-cycle command sequence. See Command Definitions on page 67 for sequence details.

Table 9 describes the Configuration Register settings.

Table 9. Configuration Register

Configuration Register	
CR15 = Read Mode (RM) 0 = Synchronous Burst Reads Enabled 1 = Asynchronous Reads Enabled (Default)	
CR14 = Reserved for Future Enhancements These bits are reserved for future use. Set these bits to *0*.	
CR13–CR10 = Initial Burst Access Delay Configuration (IAD3-IAD0)	
0000 = 2 CLK cycle initial burst access delay 0001 = 3 CLK cycle initial burst access delay 0010 = 4 CLK cycle initial burst access delay 0011 = 5 CLK cycle initial burst access delay	0100 = 6 CLK cycle initial burst access delay 0101 = 7 CLK cycle initial burst access delay 0110 = 8 CLK cycle initial burst access delay 0111 = 9 CLK cycle initial burst access delay—Default
CR9 = Data Output Configuration (DOC) 0 = Hold Data for 1-CLK cycle—Default 1 = Reserved	
CR8 = IND/WAIT# Configuration (WC) 0 = IND/WAIT# Asserted During Delay—Default 1 = IND/WAIT# Asserted One Data Cycle Before Delay	
CR7 = Burst Sequence (BS) 0 = Reserved 1 = Linear Burst Order—Default	
CR6 = Clock Configuration (CC) 0 = Reserved 1 = Burst Starts and Data Output on Rising Clock Edge—Default	
CR5–CR3 = Reserved For Future Enhancements (R) These bits are reserved for future use. Set these bits to *0*.	
CR2–CR0 = Burst Length (BL2–BL0) 000 = Reserved, burst accesses disabled (asynchronous reads only) 001 = 64 bit (8-byte) Burst Data Transfer - x32 Linear 010 = 128 bit (16-byte) Burst Data Transfer - x32 Linear 011 = 256 bit (32-byte) Burst Data Transfer - x32 Linear (device default) 100 = Reserved, burst accesses disabled (asynchronous reads only) 101 = Reserved, burst accesses disabled (asynchronous reads only) 110 = Reserved, burst accesses disabled (asynchronous reads only)	

Table 10. Configuration Register After Device Reset

CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
RM	**Reserve**	**IAD3**	**IAD2**	**IAD1**	**IAD0**	**DOC**	**Reserve**
1	0	0	1	1	1	0	0
CR7	**CR6**	**CR5**	**CR4**	**CR3**	**CR2**	**CR1**	**CR0**
BS	**CC**	**Reserve**	**Reserve**	**Reserve**	**BL2**	**BL1**	**BL0**
1	1	0	0	0	1	0	0

7.5 Autoselect

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Ad-dress pins A6, A1, and A0 must be as shown in Table 11. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Table 11 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command. This method does not require VID. See Command Definitions on page 67 for details on using the autoselect mode. Autoselect mode can be used in either synchronous (Burst) mode or asynchronous (Non Burst) mode.

The system must write the reset command to exit the autoselect mode and return to reading the array data. See Table 11 for command sequence details.

Table 11. S29CD-J and S29CL-J Flash Family Autoselect Codes (High Voltage Method)

Description		CE#	OE#	WE#	A19 to A11	A10	A9	A8	A7	A6	A5 to A4	A3	A2	A1	A0	DQ7 to DQ0
Manufacturer ID: Cypress		L	L	H	X	X	V_{ID}	X	X	L	X	X	X	L	L	0001h
Autoselect Device Code	Read Cycle 1	L	L	H	X	X	V_{ID}	X	L	L	X	L	L	L	H	007Eh
	Read Cycle 2	L	L	H	X	X	V_{ID}	X	L	L	L	H	H	H	L	08h or 36h for CD016J 46h for CL016J 09h for CD032J 49h for CL032J
	Read Cycle 3	L	L	H	X	X	V_{ID}	X	L	L	L	H	H	H	H	0000h Top Boot Option
																0001h Bottom Boot Option
PPB Protection Status		L	L	H	SA	X	V_{ID}	X	L	L	L	L	L	H	L	0000h (unprotected)
																0001h (protected)

Legend
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Note
37.The autoselect codes can also be accessed in-system via command sequences. See Table 35.

7.6 VersatileI/O (V_{IO}) Control

The VersatileI/O (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{IO} pin. The output voltage generated on the device is determined based on the V_{IO} level. For the 2.6 V (CD-J), a V_{IO} of 1.65 V–3.6 V (CD032J has a V_{IO} of 1.65 V to 2.75 V) allows the device to interface with I/Os lower than 2.5 V. For a 3.3 V V_{CC} (CL-J), a V_{IO} of 1.65 V–3.60 V allows the device to interface with I/Os lower than 3.0 V.

7.7 Program/Erase Operations

These devices are capable of several modes of programming and or erase operations which are described in detail in the following sections. However, prior to any programming and or erase operation, devices must be set up appropriately as outlined in the configuration register (see Table 9 on page 25). During a synchronous write operation, to write a command or command sequence (including programming data to the device and erasing sectors of memory), the system must drive ADV# and CE# to V_{IL}, and OE# to V_{IH} when providing an address to the device, and drive WE# and CE# to V_{IL}, and OE# to V_{IH} when writing commands or programming data.

7.7.1 Programming

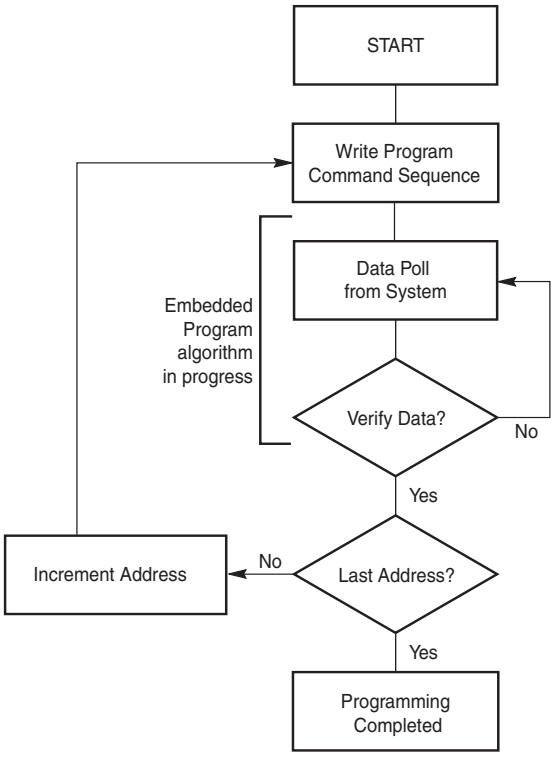
Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program setup command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Command Definitions on page 67 shows the address and data requirements for the program command sequence.

Note the following:

- When the Embedded Program algorithm is complete, the device returns to the read mode and address are no longer latched. An address change is required to begin reading valid array data.
- The system can determine the status of the program operation by using DQ7, DQ6 or RY/BY#. Refer to Write Operation Status on page 32 for information on these status bits.
- A “0” cannot be programmed back to a “1.” Attempting to do so may halt the operation and set DQ5 to 1, or cause the Data# Polling algorithm to indicate the operation was successful. A succeeding read shows that the data is still “0.” Only erase operations can convert a “0” to a “1.”
- Any commands written to the device during the Embedded Program Algorithm are ignored except the Program Suspend command.
- A hardware reset immediately terminates the program operation; the program command sequence should be re-initiated once the device has returned to the read mode, to ensure data integrity.
- For the 32Mb S29CD-J and S29CL-J devices only:

  Refer to the application note “*Recommended Mode of Operation for Cypress® 110 nm S29CD032J/S29CL032J Flash Memory*” publication number *S29CD-CL032J_Recommend_AN* for programming best practices.

Figure 5. Program Operation



Note
38.See Table 30 and Table 35 for program command sequence.

7.7.2 Sector Erase

The sector erase function erases one or more sectors in the memory array. (See Table 34. Memory Array Command Definitions (x32 Mode) on page 67 and Figure 6 Erase Operation on page 29.) The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all-zero data pattern prior to electrical erase. After a successful sector erase, all locations within the erased sector contain FFFFh. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of no less than 80 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 80 µs. Any sector erase address and command following the exceeded time-out (80 µs) may or may not be accepted. A time-out of 80 µs from the rising edge of the last WE# (or CE#) initiates the execution of the Sector Erase command(s). If another falling edge of the WE# (or CE#) occurs within the 80 µs time-out window, the timer is reset. Any command other than Erase Suspend during the time-out period will be interpreted as an additional sector to erase. The device does not decode the data bus, but latches the address. (See *S29CD016J Sector Erase Time-Out Functionality Application Note* for further information.). The system can monitor DQ3 to determine if the sector erase timer has timed out (See DQ3: Sector Erase Timer on page 35.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data; addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7 or DQ6/DQ2 in the erasing bank. Refer to Write Operation Status on page 32 for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the sector erase command sequence should be re-initiated once that bank has returned to reading array data, in order to ensure data integrity.

Figure 6 on page 29 illustrates the algorithm for the erase operation. Refer to Program/Erase Operations on page 27 for parameters and timing diagrams.

7.7.3 Chip Erase

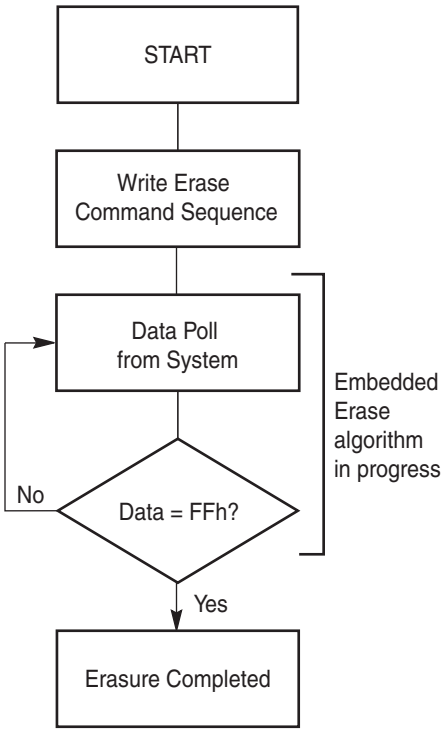
Chip erase is a six-bus cycle operation as indicated by Command Definitions on page 67. The Chip Erase command is used to erase the entire flash memory contents of the chip by issuing a single command. However, chip erase does not erase protected sectors.

This command invokes the Embedded Erase algorithm, which does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all-zero data pattern prior to electrical erase. After a successful chip erase, all locations of the chip contain FFFFh. The system is not required to provide any controls or timings during these operations. Command Definitions on page 67 in the appendix shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6 or the RY/BY#. Refer to Write Operation Status on page 32 for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 6. Erase Operation



Notes

39. See Command Definitions on page 67 for erase command sequence.
40. See DQ3: Sector Erase Timer on page 35 for more information.

7.7.4 Erase Suspend / Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. When the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the minimum 80-µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation.

When the Erase Suspend command is written after the 80-µs time-out period has expired and during the sector erase operation, the device takes 20 µs maximum to suspend the erase operation.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector that is not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Note that when the device is in the Erase Suspend mode, the Reset command is not required for read operations and is ignored.

Further nesting of erase operation is not permitted. Reading at any address within erase suspended sectors produces status information on DQ7-DQ0. The system can use DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to Table 12 on page 33 for information on these status bits.

A read operation from the erase-suspended bank returns polling data during the first 8 µs after the erase suspend command is issued; read operations thereafter return array data. Read operations from the other bank return array data with no latency.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend read mode. The system can determine the status of the program operation using the DQ7, DQ6, and/or RY/BY# status bits, just as in the standard program operation.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

The following are the allowable operations when Erase Suspend is issued under certain conditions:

For the Busy Sectors, the host system may

- Read status
- Write the Erase Resume command

For the Non Busy Sectors, the system may

- Read data
- Program data or write the Suspend/Resume Erase command

7.7.5 Program Suspend/Program Resume Commands

The Program Suspend command allows the system to interrupt an embedded programming operation so that data can read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the programming operation and updates the status bits.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. If a read is needed from the Secured Silicon Sector area, then user must use the proper command sequences to enter and exit this region. The Sector Erase and Program Resume Command is ignored if the Secured Silicon sector is enabled.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7, DQ6, and/or RY/BY# status bits, just as in the standard program operation. See Write Operation Status on page 32 for more information.

The system must write the Program Resume command in order to exit the Program Suspend mode, and continue the programming operation. Further writes of the Program Resume command are ignored. Another Program Suspend command can be written after the device has resumed programming.

The following are the allowable operations when Program Suspend is issued under certain conditions:

- For the Busy Sectors, the host system may write the Program Resume command
- For the Non Busy Sectors, the system may read data

7.7.6 Accelerated Program Operations

Accelerated programming is enabled through the ACC function. This method is faster than the standard program command sequences.

The device offers accelerated program operations through the ACC pin. When the system asserts V_{HH} (12V) on the ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence to do accelerated programming. The device uses the higher voltage on the ACC pin to accelerate the operation. Any sector that is being protected with the WP# pin is still protected during accelerated program. Removing V_{HH} from the ACC input, upon completion of the embedded program operation, returns the device to normal operation.

Notes

- In this mode, the write protection function is bypassed unless the PPB Lock Bit = 1.
- The ACC pin must not be at V_{HH} for operations other than accelerated programming or device damage may result.
- The ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.
- The Accelerated Program command is not permitted if the Secured Silicon sector is enabled.

7.7.7 Unlock Bypass

The device features an Unlock Bypass mode to facilitate faster programming, erasing (Chip Erase), as well as CFI commands. Once the device enters the Unlock Bypass mode, only two write cycles are required to program or erase data, instead of the normal four cycles for program or 6 cycles for erase. This results in faster total programming/erasing time.

Command Definitions on page 67 shows the requirements for the unlock bypass command sequences.

During the unlock bypass mode only the Read, Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence, which returns the device to read mode.

Notes

1. The Unlock Bypass Command is ignored if the Secured Silicon sector is enabled.
2. Unlike the standard program or erase commands, there is no Unlock Bypass Program/Erase Suspend or Program/Erase Resume command.

7.7.8 Simultaneous Read/Write

The simultaneous read/write feature allows the host system to read data from one bank of memory while programming or erasing in another bank of memory.

The Simultaneous Read/Write feature can be used to perform the following:

- Programming in one bank, while reading in the other bank
- Erasing in one bank, while reading in the other bank
- Programming a PPB, while reading data from the large bank or status from the small bank
- Erasing a PPB, while reading data from the large bank or status from the small bank
- Any of the above situations while in the Secured Silicon Sector Mode

The Simultaneous R/W feature can not be performed during the following modes:

- CFI Mode
- Password Program operation
- Password Verify operation

As an alternative to using the Simultaneous Read/Write feature, the user may also suspend an erase or program operation to read in another location within the same bank (except for the sector being erased).

Restrictions

The Simultaneous Read/Write function is tested by executing an embedded operation in the small (busy) bank while performing other operations in the big (non-busy) bank. However, the opposite case is neither tested nor valid. That is, it is not tested by executing an embedded operation in the big (busy) bank while performing other operations in the small (non-busy) bank.

7.8 Write Operation Status

The device provides several bits to determine the status of a program or erase operation. The following subsections describe the function of DQ7, DQ6, DQ2, DQ5, DQ3, and RY/BY#.

7.8.1 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence. Note that Data# Polling returns invalid data for the address being programmed or erased.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7.

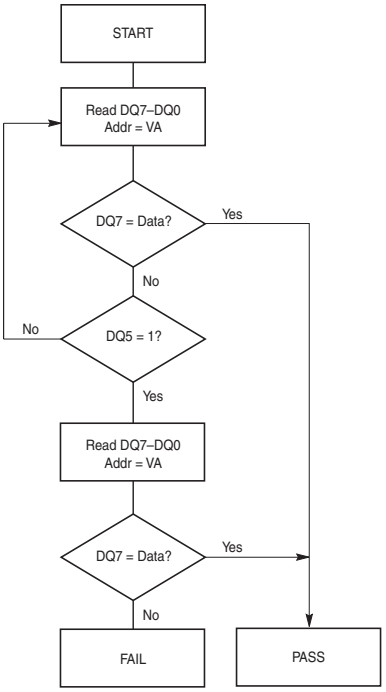
If a program address falls within a protected sector, Data# polling on DQ7 is active for approximately 1 µs, then that bank returns to the read mode without programming the sector. If an erase address falls within a protected sector, Toggle BIT (DQ6) is active for 150 s, then the device returns to the read mode without erasing the sector. Please note that Data# polling (DQ7) may give misleading status when an attempt is made to program or erase a protected sector.

During the Embedded Erase Algorithm, Data# polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

In asynchronous mode, just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ6-DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ6-DQ0 may be still invalid. Valid data on DQ7-D00 appears on successive read cycles.

See the following for more information: Table 13. Write Operation Status on page 36 shows the outputs for Data# Polling on DQ7. Figure 7 Data# Polling Algorithm on page 32 shows the Data# Polling timing diagram.

Figure 7. Data# Polling Algorithm



Notes

41. VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.
42. DQ7 should be rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.

7.8.2 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode.

Toggle Bit I may be read at any address in the same bank, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, two immediate consecutive read cycles to any address cause DQ6 to toggle. When the operation is complete, DQ6 stops toggling. For asynchronous mode, either OE# or CE# can be used to control the read cycles. For synchronous mode, the rising edge of ADV# is used or the rising edge of clock while ADV# is Low.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program Algorithm is complete. See Figure 29 Toggle Bit Timings (During Embedded Algorithms) on page 60 for additional information.

7.8.3 DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. DQ2 toggles when the system performs two consecutive reads at addresses within those sectors that have been selected for erasure. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 12 to compare outputs for DQ2 and DQ6. See DQ6: Toggle Bit I on page 33 for additional information.

7.8.4 Reading Toggle Bits DQ6/DQ2

Whenever the system initially begins reading toggle bit status, it must perform two consecutive reads of DQ7-DQ0 in a row in order to determine whether a toggle bit is toggling. Typically, the system notes and stores the value of the toggle bit after the first read. After the second read, the system compares the new value of the toggle bit with the first. If the toggle bit is not toggling, the device completes the program or erases operation. The system can read array data on DQ7-DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also notes whether the value of DQ5 is high (see the section on DQ5). If it is, the system then determines again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erases operation. If it is still toggling, the device had not completed the operation successfully, and the system writes the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, the system may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation. Refer to Figure 8 for more on the Toggle Bit Algorithm.

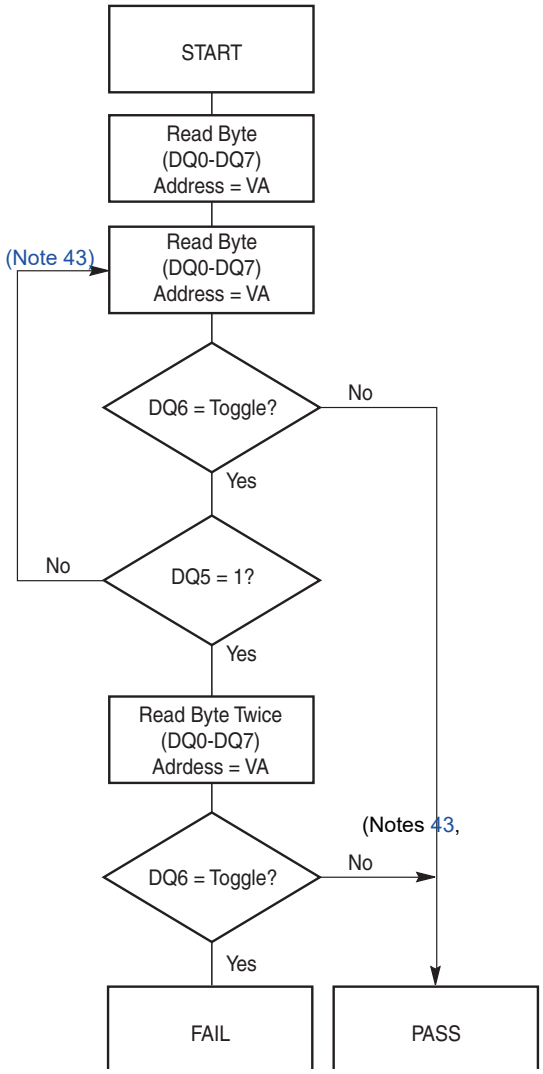
Table 12. DQ6 and DQ2 Indications

If device is	and the system reads	then DQ6	and DQ2
programming,	at any address,	toggles,	does not toggle.
actively erasing,	at an address within a sector selected for erasure,	toggles,	also toggles.
	at an address within sectors not selected for erasure,	toggles,	does not toggle.

Table 12. DQ6 and DQ2 Indications

If device is	and the system reads	then DQ6	and DQ2
erase suspended,	at an address within sectors selected for erasure,	does not toggle,	toggles.
	at an address within sectors not selected for erasure,	returns array data,	returns array data. The system can read from any sector not selected for erasure.
programming in erase suspend,	at any address,	toggles,	is not applicable.

Figure 8. Toggle Bit Algorithm



Notes

43. Read toggle bit with two immediately consecutive reads to determine whether or not it is toggling.
44. Recheck toggle bit because it may stop toggling as DQ5 changes to 1.

7.8.5 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a 1. This is a failure condition that indicates the program or erase cycle was not successfully completed.

The DQ5 failure condition may appear if the system tries to program a 1 to a location that is previously programmed to 0. Only an erase operation can change a 0 back to a 1. Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a 1.

Under both these conditions, the system issues the reset command to return the device to reading array data.

7.8.6 DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a “0” to a “1.” If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See Sector Erase on page 28 for more details.

After the sector erase command is written, the system reads the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, then reads DQ3. If DQ3 is “1,” the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0,” the device accepts additional sector erase commands.

To ensure the command has been accepted, the system software check the status of DQ3 prior to and following each sub-sequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 13 shows the status of DQ3 relative to the other status bits.

7.8.7 RY/BY#: Ready/Busy#

The device provides a RY/BY# open drain output pin as a way to indicate to the host system that the Embedded Algorithms are either in progress or have been completed. If the output of RY/BY# is low, the device is busy with either a program, erase, or reset operation. If the output is floating, the device is ready to accept any read/write or erase operation. When the RY/BY# pin is low, the device will not accept any additional program or erase commands with the exception of the Erase suspend command. If the device has entered Erase Suspend mode, the RY/BY# output is floating. For programming, the RY/BY# is valid (RY/BY# = 0) after the rising edge of the fourth WE# pulse in the four write pulse sequence. For chip erase, the RY/BY# is valid after the rising edge of the sixth WE# pulse in the six write pulse sequence. For sector erase, the RY/BY# is also valid after the rising edge of the sixth WE# pulse.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a 0 (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is floating), the reset operation is completed in a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Since the RY/BY# pin is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}. An external pull-up resistor is required to take RY/BY# to a V_{IH} level since the output is an open drain.

Table 13 shows the outputs for RY/BY#, DQ7, DQ6, DQ5, DQ3 and DQ2. Figure 19, Figure 23, Figure 25, and Figure 26 show RY/BY# for read, reset, program, and erase operations, respectively.

Table 13. Write Operation Status

Operation		DQ7 (Note 46)	DQ6	DQ5 (Note 45)	DQ3	DQ2 (Note 46)	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program	DQ7#	Toggle	0	N/A	N/A	0

Notes

45. DQ5 switches to 1 when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See DQ5: Exceeded Timing Limits on page 35 for more information.
46. DQ7 and DQ2 require a valid address when reading status information. See DQ7: Data# Polling on page 32 and DQ2: Toggle Bit II on page 33 for further details.

7.9 Reset Command

Writing the reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the cycles in an erase command sequence before erasing begins. This resets the device to the read mode. However, once erasure begins, the device ignores the reset commands until the operation is complete.

The reset command may be written between the cycles in a program command sequence before programming begins. This resets the device to the read mode. If the program command sequence is written while the device is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. However, once programming begins, the device ignores the reset commands until the operation is complete.

The reset command may be written between the cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to exit the autoselect mode and return to the read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode or erase-suspend-read-mode if the device was in Erase Suspend. When the reset command is written, before the embedded operation starts, the device requires t_{RR} before it returns to the read or erase-suspend-read mode.

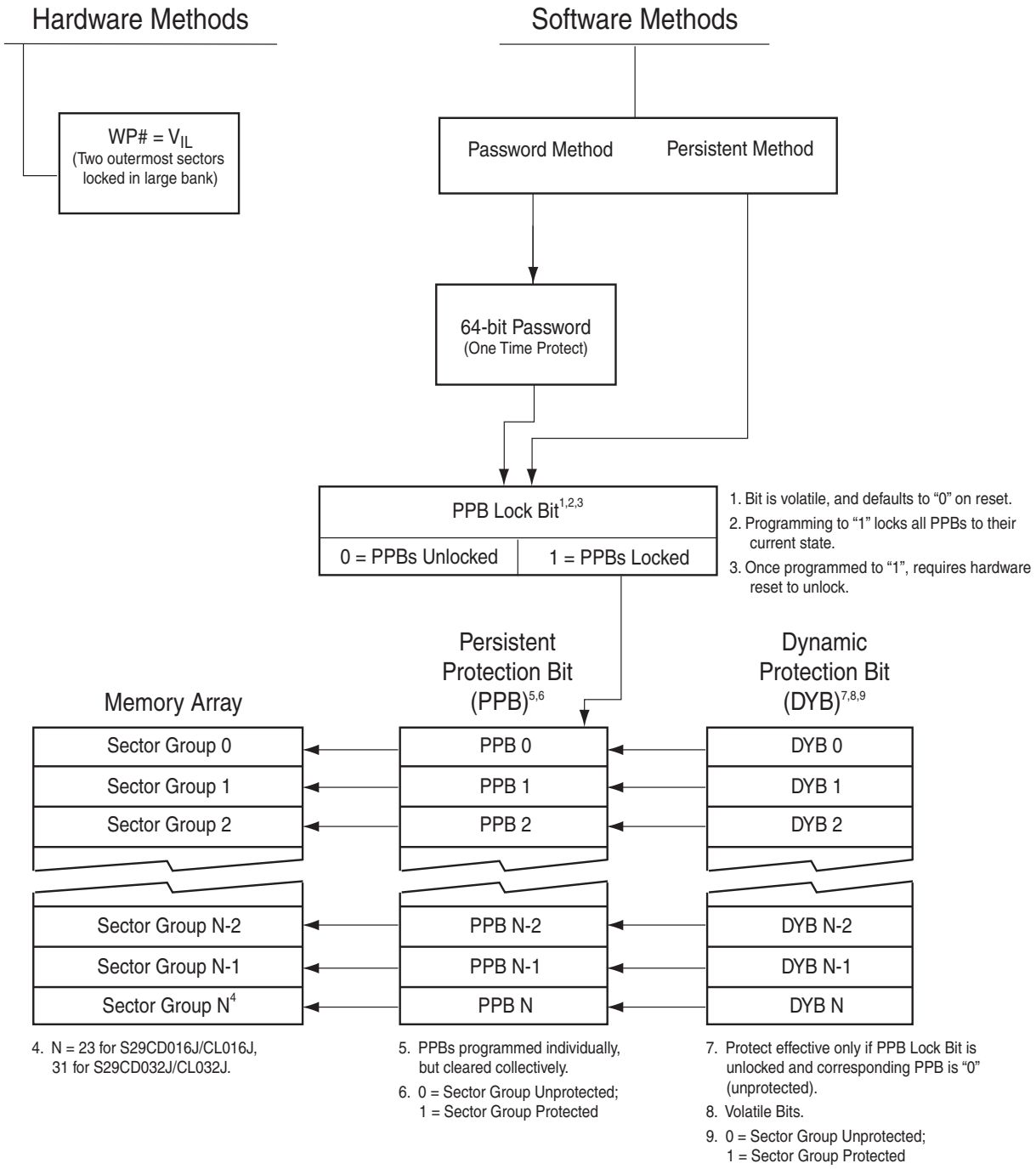
Table 14. Reset Command Timing

Parameter	Description	Max.	Unit
t_{RR}	Reset Command to Read Mode or Erase-Suspend-Read Mode	250	ns

8. Advanced Sector Protection/Unprotection

The Advanced Sector Protection/Unprotection feature disables or enables programming or erase operations in any or all sectors and can be implemented through software and/or hardware methods, which are independent of each other. This section describes the various methods of protecting data stored in the memory array. An overview of these methods in shown in Figure 9.

Figure 9. Advanced Sector Protection/Unprotection



8.1 Advanced Sector Protection Overview

As shipped from the factory, all devices default to the persistent mode when power is applied, and all sector groups are unprotected. The device programmer or host system must then choose which sector group protection method to use. Programming (setting to “0”) any one of the following two one-time programmable, non-volatile bits locks the device permanently in that mode:

- Persistent Protection Mode Lock Bit
- Password Protection Mode Lock Bit

After selecting a sector group protection method, each sector group can operate in any of the following three states:

1. Persistently Locked. A sector group is protected and cannot be changed.
2. Dynamically locked. The selected sector groups are protected and can be altered via software commands.
3. Unlocked. The sector groups are unprotected and can be erased and/or programmed.

These states are controlled by the bit types described in sections Persistent Protection Bits on page 39 to Hardware Data Protection Methods on page 43.

Notes

1. If the password mode is chosen, the password must be programmed before setting the corresponding lock register bit. The user must be sure that the password is correct when the Password Mode Locking Bit is set, as there is no means to verify the password afterwards.
2. If both lock bits are selected to be programmed (to zeros) at the same time, the operation aborts.
3. Once the Password Mode Lock Bit is programmed, the Persistent Mode Lock Bit is permanently disabled, and no changes to the protection scheme are allowed. Similarly, if the Persistent Mode Lock Bit is programmed, the Password Mode is permanently disabled.
4. It is important that the mode is explicitly selected when the device is first programmed, rather than relying on the default mode alone. This is so that it is impossible for a system program or virus to later set the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.
5. If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1 µs before the device returns to read mode without modifying the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50 µs, after which the device returns to read mode without having erased the protected sector.
6. For the command sequence required for programming the lock register bits, refer to Command Definitions on page 67.

8.2 Persistent Protection Bits

The Persistent Protection Bits are unique and nonvolatile. A single Persistent Protection Bit is assigned to a maximum for four sectors (see the sector address tables for specific sector protection groupings). All eight-Kbyte boot-block sectors have individual sector Persistent Protection Bits (PPBs) for greater flexibility.

Notes

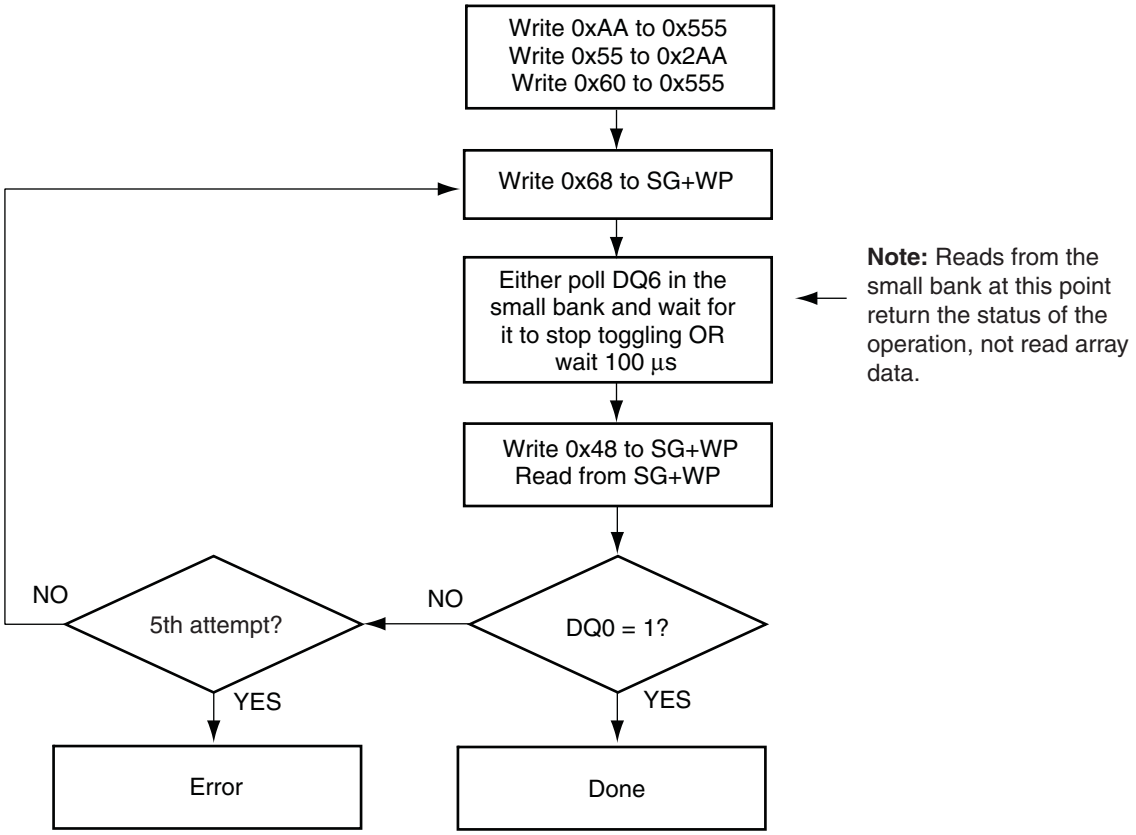
1. Each PPB is individually programmed and all are erased in parallel. There are no means for individually erasing a specific PPB and no specific sector address is required for this operation.
2. If a PPB requires erasure, all of the sector PPBs must first be programmed prior to PPB erasing. It is the responsibility of the user to perform the preprogramming operation. Otherwise, an already erased sector PPB has the potential of being over-erased. There is no hardware mechanism to prevent sector PPB over-erasure.
3. If the PPB Lock Bit is set, the PPB Program or erase command does not execute and times-out without programming or erasing the PPB.

8.2.1 Programming PPB

The PPB Program Command is used to program, or set, a given PPB. The first three cycles in the PPB Program Command are standard unlock cycles. The fourth cycle in the PPB Program Command executes the pulse which programs the specified PPB. The user must wait either 100 µs or until DQ6 stops toggling before executing the fifth cycle, which is the read verify portion of the PPB Program Command. The sixth cycle outputs the status of the PPB Program operation.

In the event that the program PPB operation was not successful, the user can loop directly to the fourth cycle of the PPB Program Command to perform the program pulse and read verification again. After four unsuccessful loops through the program pulse and read verification cycles the PPB programming operation should be considered a failure.

Figure 10. PPB Program Operation



8.2.2 Erasing PPB

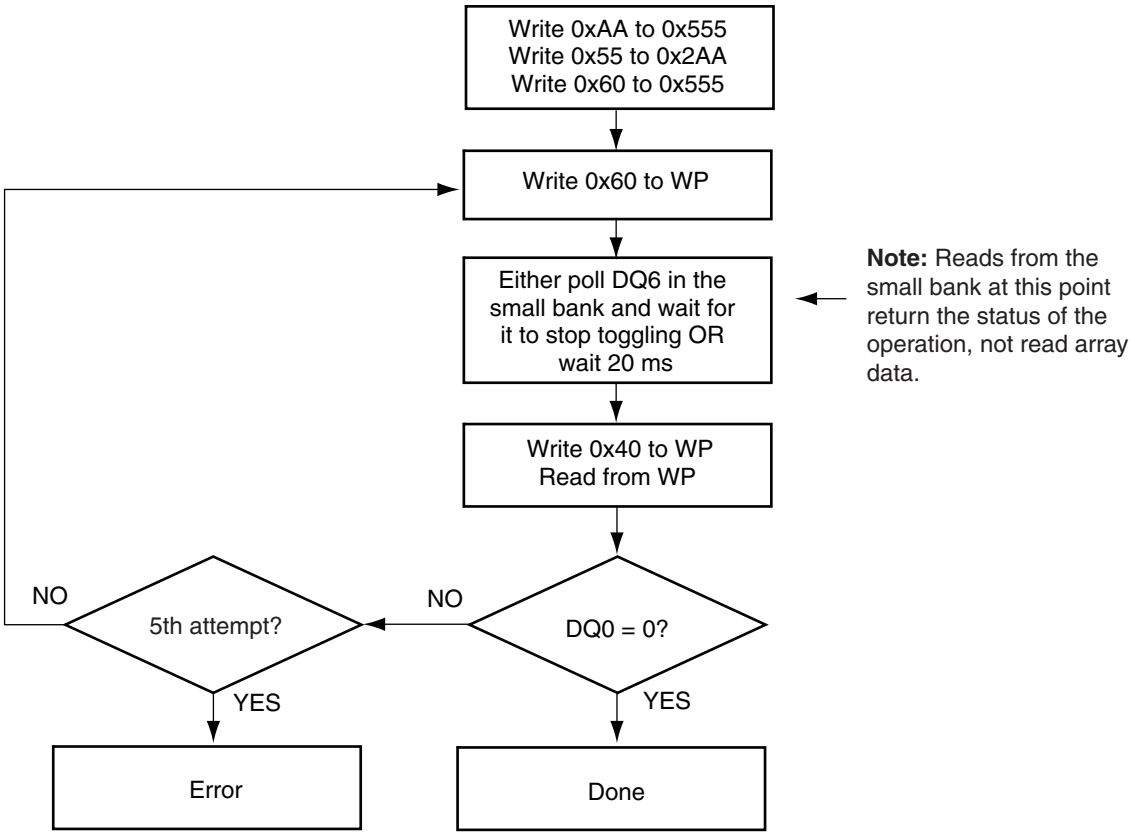
The All PPB Erase command is used to erase all the PPBs in bulk. There are no means for individually erasing a specific PPB. The first three cycles of the PPB Erase command are standard unlock cycles. The fourth cycle executes the erase pulse to all the PPBs. The user must wait either 20 ms or until DQ6 stops toggling before executing the fifth cycle, which is the read verify portion of the PPB Erase Command. The sixth cycle outputs the status of the PPB Erase operation.

In the event that the erase PPB operation was not successful, the user can loop directly to the fourth cycle of the All PPB Erase Command to perform the erase pulse and read verification again. After four unsuccessful loops through the erase pulse and read verification cycles, the PPB erasing operation should be considered a failure.

Note

- All PPB must be preprogrammed prior to issuing the All PPB Erase Command.

Figure 11. PPB Erase Operation



8.3 Persistent Protection Bit Lock Bit

The Persistent Protection Bit Lock Bit is a global volatile bit for all sectors. When set to “1”, it locks all PPBs; when set to “0”, it allows the PPBs to be changed. There is only one PPB Lock Bit per device.

Notes

1. No software command sequence unlocks this bit unless the device is in the password protection mode; only a hardware reset or a power-up clears this bit.
2. The PPB Lock Bit must be set only after all PPBs are configured to the desired settings.

8.4 Dynamic Protection Bits

A Dynamic Protection Bit (DYB) is volatile and unique for each sector group and can be individually modified. DYBs only control the protection scheme for unprotected sector groups that have their PPBs set to “0”. By issuing the DYB Set or Clear command sequences, the DYBS are set or cleared, thus placing each sector group in the protected or unprotected state respectively. This feature allows software to easily protect sector groups against inadvertent changes, yet does not prevent the easy removal of protection when changes are needed.

Notes

1. The DYBs can be set or cleared as often as needed with the DYB Write Command.
2. When the parts are first shipped, the PPBs are cleared, the DYBs are cleared, and PPB Lock is defaulted to power up in the cleared state – meaning the PPBs are changeable. The DYB are also always cleared after a power-up or reset.
3. It is possible to have sector groups that are persistently locked with sector groups that are left in the dynamic state.
4. The DYB Set or Clear commands for the dynamic sector groups signify the protected or unprotected state of the sector groups respectively. However, if there is a need to change the status of the persistently locked sector groups, a few more steps are required. First, the PPB Lock Bit must be cleared by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB Lock Bit once again locks the PPBs, and the device operates normally again.

Table 15. Sector Protection Schemes

DYB	PPB	PPB Lock	Sector State
0	0	0	Unprotected—PPB and DYB are changeable
0	0	1	Unprotected—PPB not changeable, DYB is changeable
0	1	0	Protected—PPB and DYB are changeable
1	0	0	
1	1	0	
0	1	1	Protected—PPB not changeable, DYB is changeable
1	0	1	
1	1	1	

8.5 Password Protection Method

The Password Protection Method allows an even higher level of security than the Persistent Sector Protection Mode by requiring a 64-bit password for unlocking the device PPB Lock Bit. In addition to this password requirement, after power-up and reset, the PPB Lock Bit is set “1” in order to maintain the password mode of operation. Successful execution of the Password Unlock command by entering the entire password clears the PPB Lock Bit, allowing for sector PPBs modifications.

Notes

1. There is no special addressing order required for programming the password. Once the password is written and verified, the Password Mode Locking Bit must be set in order to prevent access.
2. The Password Program Command is only capable of programming “0”s. Programming a “1” after a cell is programmed as a “0” results in a time-out with the cell as a “0”. (This is an OTP area).
3. The password is all “1”s when shipped from the factory.
4. When the password is undergoing programming, Simultaneous Read/Write operation is disabled. Read operations to any memory location returns the programming status. Once programming is complete, the user must issue a Read/Reset command to return the device to normal operation.
5. All 64-bit password combinations are valid as a password.
6. There is no means to read, program or erase the password is after it is set.
7. The Password Mode Lock Bit, once set, prevents reading the 64-bit password on the data bus and further password programming.
8. The Password Mode Lock Bit is not erasable.
9. The exact password must be entered in order for the unlocking function to occur.
10. There is a built-in 2-µs delay for each password check. This delay is intended to stop any efforts to run a program that tries all possible combinations in order to crack the password.

8.6 Hardware Data Protection Methods

The device offers several methods of data protection by which intended or accidental erasure of any sectors can be prevented via hardware means. The following subsections describe these methods.

8.6.1 WP# Method

The Write Protect feature provides a hardware method of protecting the two outermost sectors of the large bank.

If the system asserts V_{IL} on the WP# pin, the device disables program and erase functions in the two “outermost” boot sectors (8-Kbyte sectors) in the large bank. If the system asserts V_{IH} on the WP# pin, the device reverts to whether the boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected.

Note that the WP# pin must not be left floating or unconnected as inconsistent behavior of the device may result.

The WP# pin must be held stable during a command sequence execution

8.6.2 Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down.

The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

8.6.3 Write Pulse “Glitch Protection”

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

8.6.4 Power-Up Write Inhibit

If WE# = CE# = RESET# = V_{IL} and OE# = V_{IH} during power-up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

8.6.5 V_{CC} and V_{IO} Power-up And Power-down Sequencing

The device imposes no restrictions on V_{CC} and V_{IO} power-up or power-down sequencing. Asserting RESET# to V_{IL} is required during the entire V_{CC} and V_{IO} power sequence until the respective supplies reach the operating voltages. Once V_{CC} and V_{IO} attain the operating voltages, deassertion of RESET# to V_{IH} is permitted. Refer to timing in V_{CC} and V_{IO} Power-up on page 52.

8.6.6 Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH}, or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero (V_{IL}) while OE# is a logical one (V_{IH}).

9. Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector provides an extra Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Sector is a 256-byte flash memory area that is either programmable at the customer, or by Cypress at the request of the customer. See Table 16 for the Secured Silicon Sector address ranges.

All Secured Silicon reads outside of the 256-byte address range return invalid data.

Table 16. Secured Silicon Sector Addresses

Ordering Option	Sector Size (Bytes)	Address Range
Top Boot	256	00000h-0003Fh (16 Mb and 32 Mb)
Bottom Boot	256	FFFC0h–FFFFFh (32 Mb) 7FFC0h–7FFFFh (16 Mb)

The device allows Simultaneous Read/Write operation while the Secured Silicon Sector is enabled. However, several restrictions are associated with Simultaneous Read/Write operation and device operation when the Secured Silicon Sector is enabled:

1. The Secured Silicon Sector is not available for reading while the Password Unlock, any PPB program/erase operation, or Password programming are in progress. Reading to any location in the small bank will return the status of these operations until these operations have completed execution.
2. Programming the DYB associated with the overlaid boot-block sector results in the DYB NOT being updated. This occurs only when the Secured Silicon sector is not enabled.
3. Reading the DYB associated with the overlaid boot-block sector when the PPB Lock/DYB Verify command is issued, causes the read command to return invalid data. This function occurs only when the Secured Silicon Sector is not enabled.
4. All commands are available for execution when the Secured Silicon Sector is enabled, except the following:
   a. Any Unlock Bypass command
   b. CFI
   c. Accelerated Program
   d. Program and Sector Erase Suspend
   e. Program and Sector Erase Resume

Issuing the above commands while the Secured Silicon Sector is enabled results in the command being ignored.

5. It is valid to execute the Sector Erase command on any sector other than the Secured Silicon Sector when the Secured Silicon Sector is enabled. However, it is not possible to erase the Secured Silicon Sector using the Sector Erase Command, as it is a one-time programmable (OTP) area that can not be erased.
6. Executing the Chip Erase command is permitted when the Secured Silicon Sector is enabled. The Chip Erase command erases all sectors in the memory array, except for sector 0 in top-boot block configuration, or sector 45 in bottom-boot block configuration. The Secured Silicon Sector is a one-time programmable memory area that cannot be erased.
7. Executing the Secured Silicon Sector Entry command during program or erase suspend mode is allowed. The Sector Erase/Program Resume command is disabled when the Secured Silicon sector is enabled; the user cannot resume programming of the memory array until the Exit Secured Silicon Sector command is written.
8. Address range 00040h–007FFh for the top bootblock, and FF00h–FFF7Fh return invalid data when addressed with the Secured Silicon sector enabled.
9. The Secured Silicon Sector Entry command is allowed when the device is in either program or erase suspend modes. If the Secured Silicon sector is enabled, the program or erase suspend command is ignored. This prevents resuming either programming or erasure on the Secured Silicon sector if the overlayed sector was undergoing programming or erasure. The host system must ensure that the device resume any suspended program or erase operation after exiting the Secured Silicon sector.

9.1 Secured Silicon Sector Protection Bit

The Secured Silicon Sector can be shipped unprotected, allowing customers to utilize that sector in any manner they choose.

Please note the following:

- The Secured Silicon Sector can be read any number of times, but can be programmed and locked only once. The Secured Silicon Sector Protection Bit must be used with caution as once locked, there is no procedure available for unlocking the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.
- Once the Secured Silicon Sector is locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return the device to the memory array.

9.2 Secured Silicon Sector Entry and Exit Commands

The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. See the Table 34. Memory Array Command Definitions (x32 Mode) on page 67 and Table 35. Sector Protection Command Definitions (x32 Mode) on page 68 for address and data requirements for both command sequences.

The Secured Silicon Sector Entry Command allows the following commands to be executed

- Read Secured Silicon areas
- Program Secured Silicon Sector (only once)

After the system has written the Enter Secured Silicon Sector command sequence, it can read the Secured Silicon Sector by using the addresses listed in Table 16 on page 44. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device.

10. Electronic Marking

Electronic marking has been programmed into the device, prior to shipment from Cypress, to ensure traceability of individual products. The electronic marking is stored and locked within a one-time programmable region. Detailed information on Electronic Marking will be provided in a data sheet supplement.

11. Power Conservation Modes

11.1 Standby Mode

When the system is not reading or writing to the device, it can place the device in standby mode. In this mode, current consumption is greatly reduced, and outputs are placed in a high impedance state, independent of OE# input. The device enters CMOS standby mode when the CE# and RESET# inputs are both held at V_{CC} ± 10%. The device requires standard access time (t_{CE}) for read access before it is ready to read data. If the device is deselected during erasure or programming, the device draws active current until the operation is completed. I_{CC5} in Table 19 on page 49 represents the standby current specification.

Caution

Entering standby mode via the RESET# pin also resets the device to read mode and floats the data I/O pins. Furthermore, entering I_{CC7} during a program or erase operation leaves erroneous data in the address locations being operated on at the time of the RESET# pulse. These locations require updating after the device resumes standard operations. See Hardware RESET# Input Operation on page 46 for further discussion of the RESET# pin and its functions.

11.2 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The automatic sleep mode is independent of the CE#, WE# and OE# control signals. While in sleep mode, output data is latched and always available to the system.

While in asynchronous mode, the device automatically enables this mode when addresses remain stable for t_{ACC} + 60 ns. Standard address access timings provide new data when addresses are changed. While in synchronous mode, the device automatically enables this mode when either the first active CLK level is greater than t_{ACC} or the CLK runs slower than 5 MHz. A new burst operation is required to provide new data. I_{CC8} in DC Characteristic, CMOS Compatible on page 49 represents the automatic sleep mode current specification.

11.3 Hardware RESET# Input Operation

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low, the device immediately terminates any operation in progress, tristates all outputs, resets the configuration register, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. Any operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, in order to ensure data integrity.

When RESET# is held at V_{SS} ±0.2 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS} ±0.2 V, the standby current is greater.

RESET# may be tied to the system reset circuitry, thus a system reset would also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains low until the reset operation is internally complete. This action requires between 1 µs and 7 µs for either Chip Erase or Sector Erase. The RY/BY# pin can be used to determine whether the reset operation is complete. Otherwise, allow for the maximum reset time of 11 µs.

If RESET# is asserted when a program or erase operation is not executing (RY/BY# = 1), the reset operation completes within 500 ns. The Simultaneous Read/Write feature of this device allows the user to read a bank after 500 ns if the bank is in the read/reset mode at the time RESET# is asserted. If one of the banks is in the middle of either a program or erase operation when RESET# is asserted, the user must wait 11 µs before accessing that bank.

Asserting RESET# active during V_{CC} and V_{IO} power up is required to guarantee proper device initialization until V_{CC} and V_{IO} have reached steady state voltages.

11.4 Output Disable (OE#)

When the OE# input is at V_{IH}, output from the device is disabled. The outputs are placed in the high impedance state.

12. Electrical Specifications

12.1 Absolute Maximum Ratings

Table 17. Absolute Maximum Ratings

Parameter		Rating
Storage Temperature, Plastic Packages		–65 °C to +150 °C
Ambient Temperature with Power Applied		–65 °C to +145 °C
V_{CC}, V_{IO} (Note 47) for 2.6 V devices (S29CD-J)		–0.5V to +3.6V
V_{CC}, V_{IO} (Note 47) for 3.3 V devices (S29CL-J)		–0.5V to +3.6V
ACC, A9, and RESET# (Note 48)		–0.5V to +13.0V
Address, Data, Control Signals (Note 47)	(with the exception of CLK)	–0.5V to +3.6V (CL016J)
		–0.5V to +2.75V (CD016J)
	All other pins (Note 47)	–0.5V to +3.6V (CL032J)
		–0.5V to +2.75V (CD032J)
Output Short Circuit Current (Note 49)		200 mA

Notes

47. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input at I/O pins may overshoot V_{SS} to –2.0V for periods of up to 20 ns. See Figure 13. Maximum DC voltage on output and I/O pins is 3.6V. During voltage transitions output pins may overshoot to V_{CC} + 2.0V for periods up to 20 ns. See Figure 13.
48. Minimum DC input voltage on pins ACC, A9, and RESET# is -0.5V. During voltage transitions, A9 and RESET# may overshoot V_{SS} to –2.0V for periods of up to 20 ns. See Figure 12. Maximum DC input voltage on pin A9 is +13.0V which may overshoot to 14.0V for periods up to 20 ns.
49. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
50. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 12. Maximum Negative Overshoot Waveform

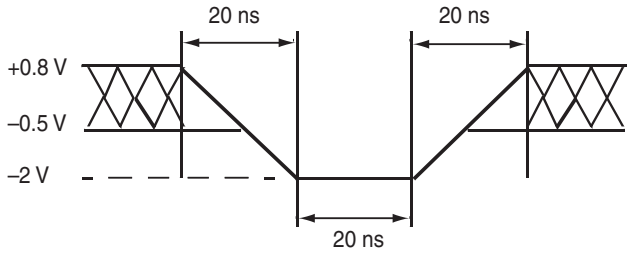
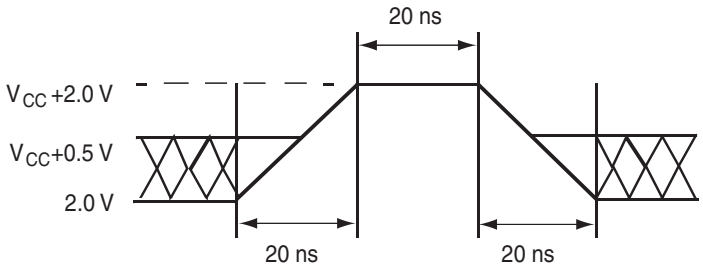


Figure 13. Maximum Positive Overshoot Waveform



13. Operating Ranges

Table 18. Operating Ranges

Parameter		Range
Ambient Temperature (T_A)	Industrial Devices	–40°C to +85°C
	Extended Devices	–40°C to +125°C
V_{CC} Supply Voltages	V_{CC} for 2.6V regulated voltage range (S29CD-J devices)	2.50V to 2.75V
	V_{CC} for 3.3V regulated voltage range (S29CL-J devices)	3.00V to 3.60V
V_{IO} Supply Voltages	V_{IO} (S29CD-J devices)	1.65V to 2.75V
	V_{IO} (S29CL-J devices)	1.65V to 3.6V

Note
51.Operating ranges define those limits between which the functionality of the device is guaranteed.

14. DC Characteristics

Table 19. DC Characteristic, CMOS Compatible

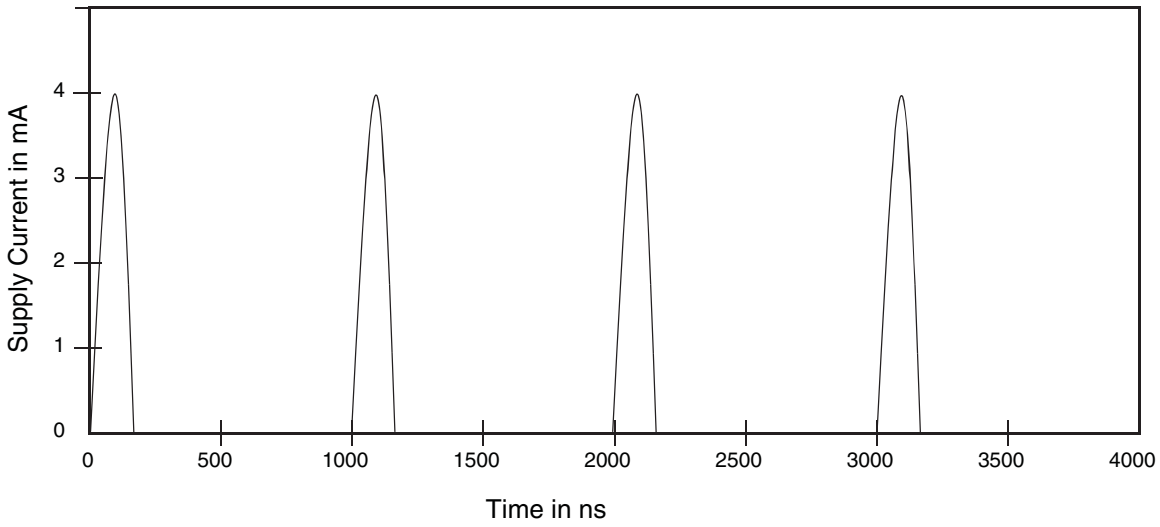
Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{IO}, $V_{IO} = V_{IO\ max}$				±1.0	µA
I_{LIWP}	WP# Input Load Current	$V_{IN} = V_{SS}$ to V_{IO}, $V_{IO} = V_{IO\ max}$				–25	µA
I_{LIT}	A9, ACC Input Load Current	$V_{CC} = V_{CCmax}$; A9 = 12.5V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CCB}	V_{CC} Active Burst Read Current (52)	CE# = V_{IL}, OE# = V_{IL}, 8 Double Word	S29CD-J		45	55	mA
			S29CL-J		65	90	mA
I_{CC1}	V_{CC} Active Asynchronous Read Current (52)	CE# = V_{IL}, OE# = V_{IL}	1 MHz			10	mA
I_{CC3}	V_{CC} Active Program Current (53, 54, 55)	CE# = V_{IL}, OE# = V_{IH}, ACC = V_{IH}			40	50	mA
I_{CC4}	V_{CC} Active Erase Current (53, 54, 55)	CE# = V_{IL}, OE# = V_{IH}, ACC = V_{IH}			20	50	mA
I_{CC5}	V_{CC} Standby Current (CMOS)	V_{CC}= $V_{CC\ max}$, CE# = V_{CC} ± 0.3V				60	µA
I_{CC6}	V_{CC} Active Current (Read While Write) (54)	CE# = V_{IL}, OE# = V_{IL}			30	90	mA
I_{CC7}	V_{CC} Reset Current	RESET# = V_{IL}				60	µA
I_{CC8}	Automatic Sleep Mode Current	$V_{IH} = V_{CC}$ ± 0.3 V, $V_{IL} = V_{SS}$ ± 0.3V				60	µA
I_{ACC}	V_{ACC} Acceleration Current	ACC = V_{HH}				20	mA
V_{IL}	Input Low Voltage			–0.5		0.3 x V_{IO}	V
V_{IH}	Input High Voltage			0.7 x V_{IO}		V_{CC}	V
V_{ILCLK}	CLK Input Low Voltage			–0.2		0.3 x V_{IO}	V
V_{IHCLK}	CLK Input High Voltage (CD-J)			0.7 x V_{CC}		2.75	V
V_{IHCLK}	CLK Input High Voltage (CL-J)			0.7 x V_{CC}		3.6	V
V_{ID}	Voltage for Autoselect	V_{CC} = 2.5V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min}$				0.45	V
I_{OLRB}	RY/BY#, Output Low Current	V_{OL} = 0.4V		8			mA
V_{HH}	Accelerated (ACC pin) High Voltage	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min}$		0.85 x V_{CC}			V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{IO} –0.1			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (54)			1.6		2.0	V

Notes

52. The I_{CC} current listed includes both the DC operating current and the frequency dependent component.
53. I_{CC} active while Embedded Erase or Embedded Program is in progress.
54. Not 100% tested.
55. Maximum I_{CC} specifications are tested with $V_{CC} = V_{CCmax}$.

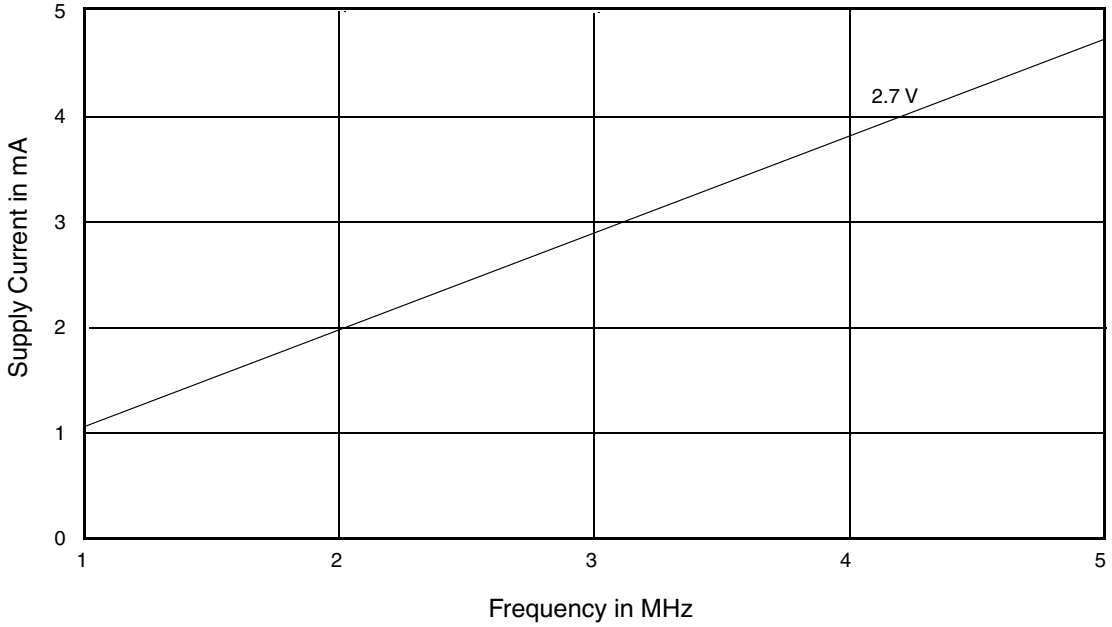
14.1 Zero Power Flash

Figure 14. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



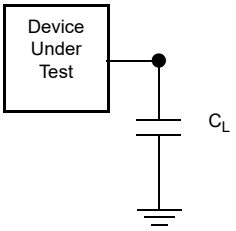
Note
56.Addresses are switching at 1 MHz.

Figure 15. Typical I_{CC1} vs. Frequency



15. Test Conditions

Figure 16. Test Setup



16. Test Specifications

Table 20. Test Specifications

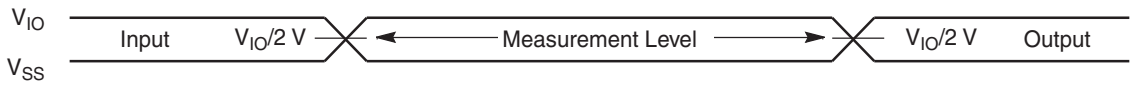
Test Condition	All Options	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0V – V_{IO}	V
Input timing measurement reference levels	$V_{IO}/2$	V
Output timing measurement reference levels	$V_{IO}/2$	V

Table 21. Key to Switching Waveforms

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High-Z)

16.1 Switching Waveforms

Figure 17. Input Waveforms and Measurement Levels



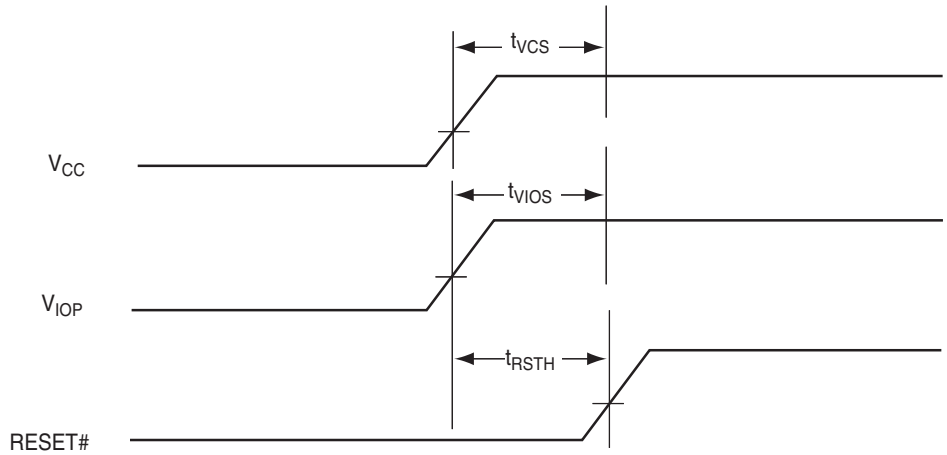
17. AC Characteristics

17.1 V_{CC} and V_{IO} Power-up

Table 22. V_{CC} and V_{IO} Power-up

Parameter	Description	Test Setup	Speed	Unit
t_{VCS}	V_{CC} Setup Time	Min	50	µs
t_{VIOS}	V_{IO} Setup Time	Min	50	µs
t_{RSTH}	RESET# Low Hold Time	Min	50	µs

Figure 18. V_{CC} and V_{IO} Power-up Diagram



17.2 Asynchronous Operations

Table 23. Asynchronous Read Operations

Parameter		Description		Test Setup		Speed Options				Unit
JEDEC	Std.					75 MHz 0R	66 MHz 0P	56 MHz 0M	40 MHz 0J/1J	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	54				ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL} OE# = V_{IL}	Max	54				ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	54				ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	20				ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z (Note 57)			Max	10				ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z (Note 57)			Min	2				ns
					Max	10				ns
	t_{OEH}	Output Enable Hold Time (Note 57)	Read		Min	0				ns
			Toggle and Data# Polling		Min	10				ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 57)			Min	2				ns

Notes
57. Not 100% tested.
58. See Figure 16 and Table 20 for test specifications.
59. TOE during Read Array.

Figure 19. Conventional Read Operations Timings

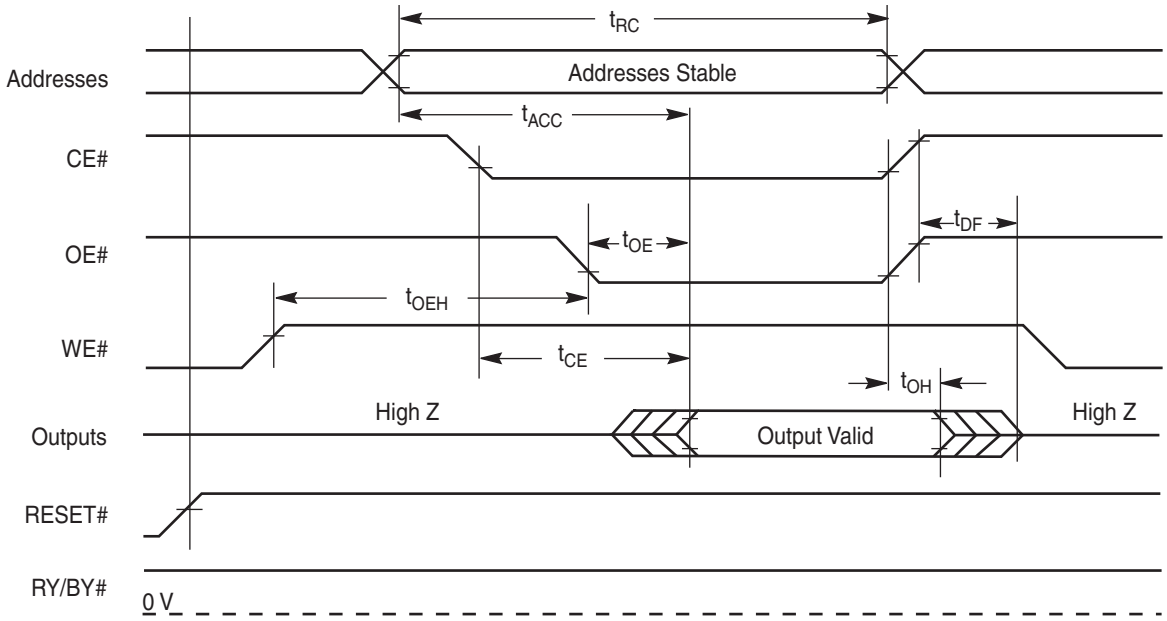
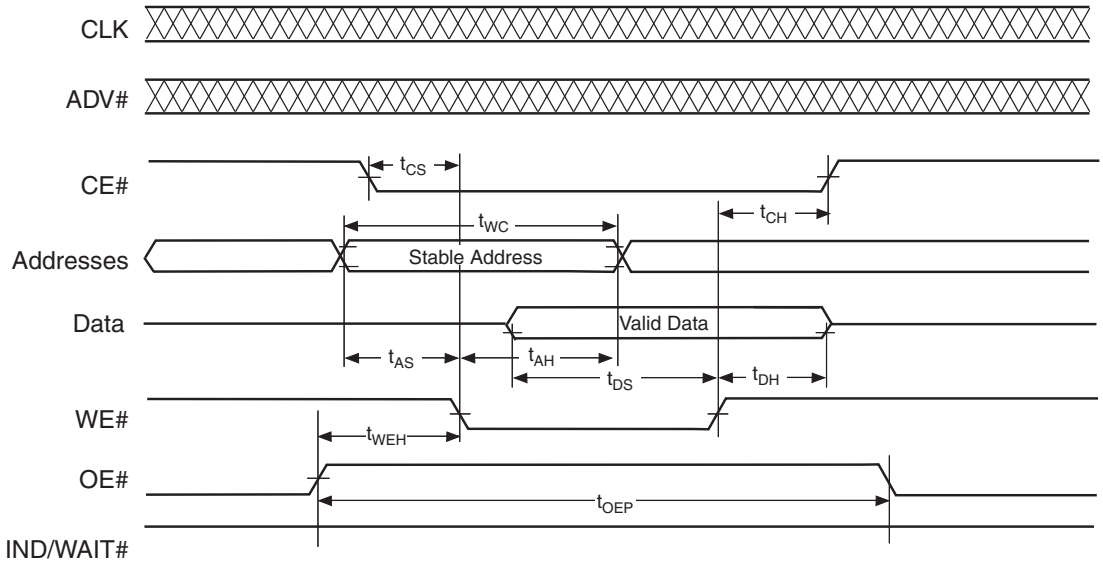


Figure 20. Asynchronous Command Write Timing



Notes

60. All commands have the same number of cycles in both asynchronous and synchronous modes, including the READ/RESET command. Only a single array access occurs after the F0h command is entered. All subsequent accesses are burst mode when the burst mode option is enabled in the Configuration Register.
61. Refer to Table 26 for write timing parameters.

17.3 Synchronous Operations

Table 24. Burst Mode for 32 Mb and 16 Mb

Parameter		Description			Speed Options				Unit
JEDEC	Std.				75 MHz, 0R	66 MHz, 0P	56 MHz, 0M	40 MHz, 0J/1J	
	t_{BACC}	Burst Access Time Valid Clock to Output Delay		Max	8	8	8	8	ns
	t_{ADVCS}	ADV# Setup Time to Rising Edge of CLK		Min	6				ns
	t_{ADVCH}	ADV# Hold Time from Rising Edge of CLK		Min	1.5				ns
	t_{ADVP}	ADV# Pulse Width		Min	7.5	8.5	9.5	10.5	ns
	t_{BDH}	Valid Data Hold from CLK (Note 63)	16 Mb	Min	2	2	3	3	ns
			32 Mb	Min	0	0	0	0	ns
	t_{INDS}	CLK to Valid IND/WAIT# (Note 63)		Max	8				ns
	t_{INDH}	IND/WAIT# Hold from CLK (Note 63)		Min	2	2	3	3	ns
	t_{IACC}	CLK to Valid Data Out, Initial Burst Access		Max	48	54	54	54	ns
	t_{CLK}	CLK Period		Min	13.3	15.15	17.85	25	ns
				Max	60				
	t_{CR}	CLK Rise Time (Note 63)		Max	3				ns
	t_{CF}	CLK Fall Time (Note 63)		Max	3				ns
	t_{CLKH}	CLK High Time (Note 64)		Min	6.65	6.8	8.0	11.25	ns
	t_{CLKL}	CLK Low Time (Note 64)		Min	6.65	6.8	8.0	11.25	ns
	t_{OE}	Output Enable to Output Valid		Max	20				ns
t_{DF}	t_{OEZ}	Output Enable to Output High-Z (Note 63)		Min	2	2	3	3	ns
				Max	7.5	10	15	17	
t_{EHQZ}	t_{CEZ}	Chip Enable to Output High-Z (Note 63)		Max	7.5	10	15	17	ns
	t_{CES}	CE# Setup Time to Clock		Min	4	4	5	6	ns
	t_{AAVS}	ADV# Falling Edge to Address Valid (Note 62)		Max	6.5				ns
	t_{AAVH}	Address Hold Time from Rising Edge of ADV#		Min	1				CLK cycle
	t_{RSTZ}	RESET# Low to Output High-Z (Note 63)		Max	7.5	10	15	17	ns
	t_{WADVH1}	ADV# Falling Edge to WE# Falling Edge		Min	0				ns
	t_{WADVH2}	ADV# Rising Edge to WE# Rising Edge		Min	10				ns
	t_{WADVS}	WE# Rising Edge Setup to ADV# Falling Edge		Min	11.75				ns

Notes

62. Using the max t_{AAVS} and min t_{ADVCS} specs together will result in incorrect data output.
63. Not 100% tested
64. Recommended 50% Duty Cycle

Figure 21. Burst Mode Read (x32 Mode)

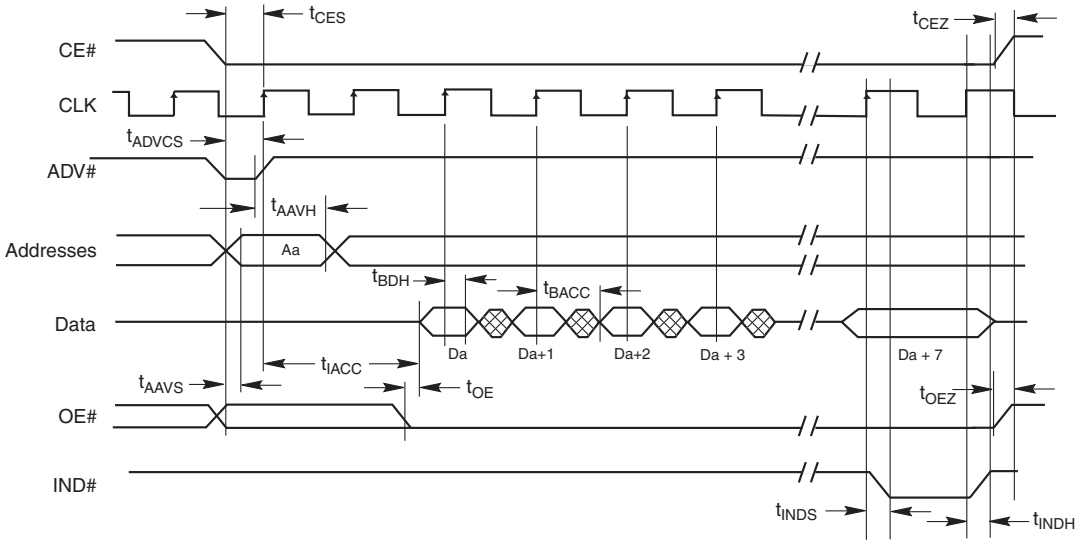
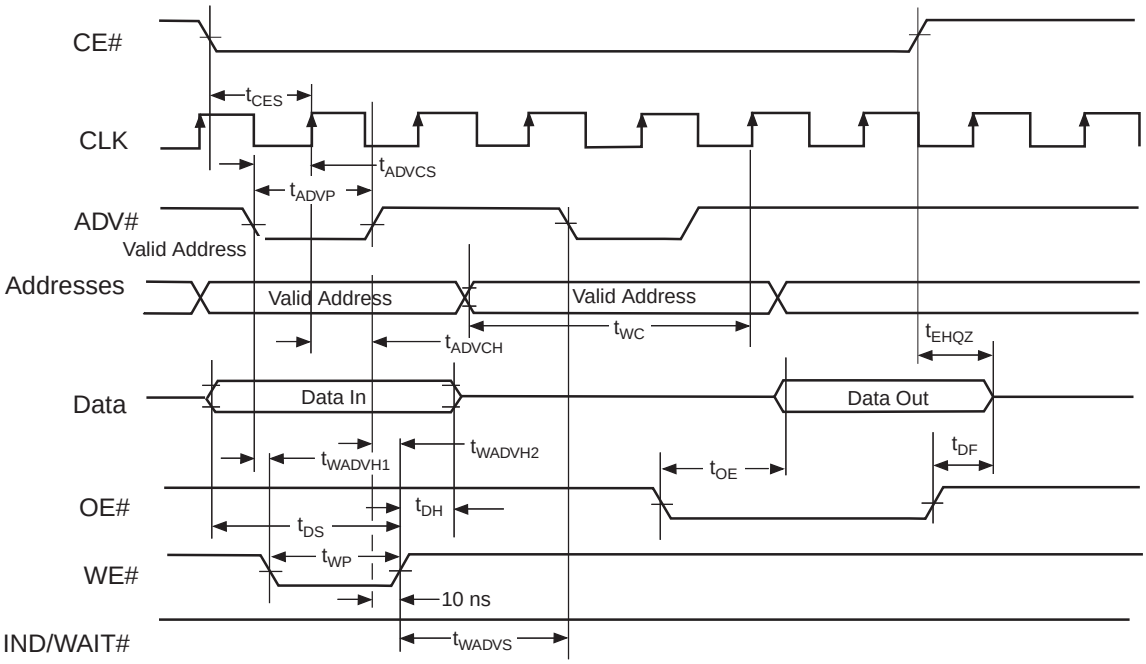


Figure 22. Synchronous Command Write/Read Timing



Note

65. All commands have the same number of cycles in both asynchronous and synchronous modes, including the READ/RESET command. Only a single array access occurs after the F0h command is entered. All subsequent accesses are burst mode when the burst mode option is enabled in the Configuration Register.

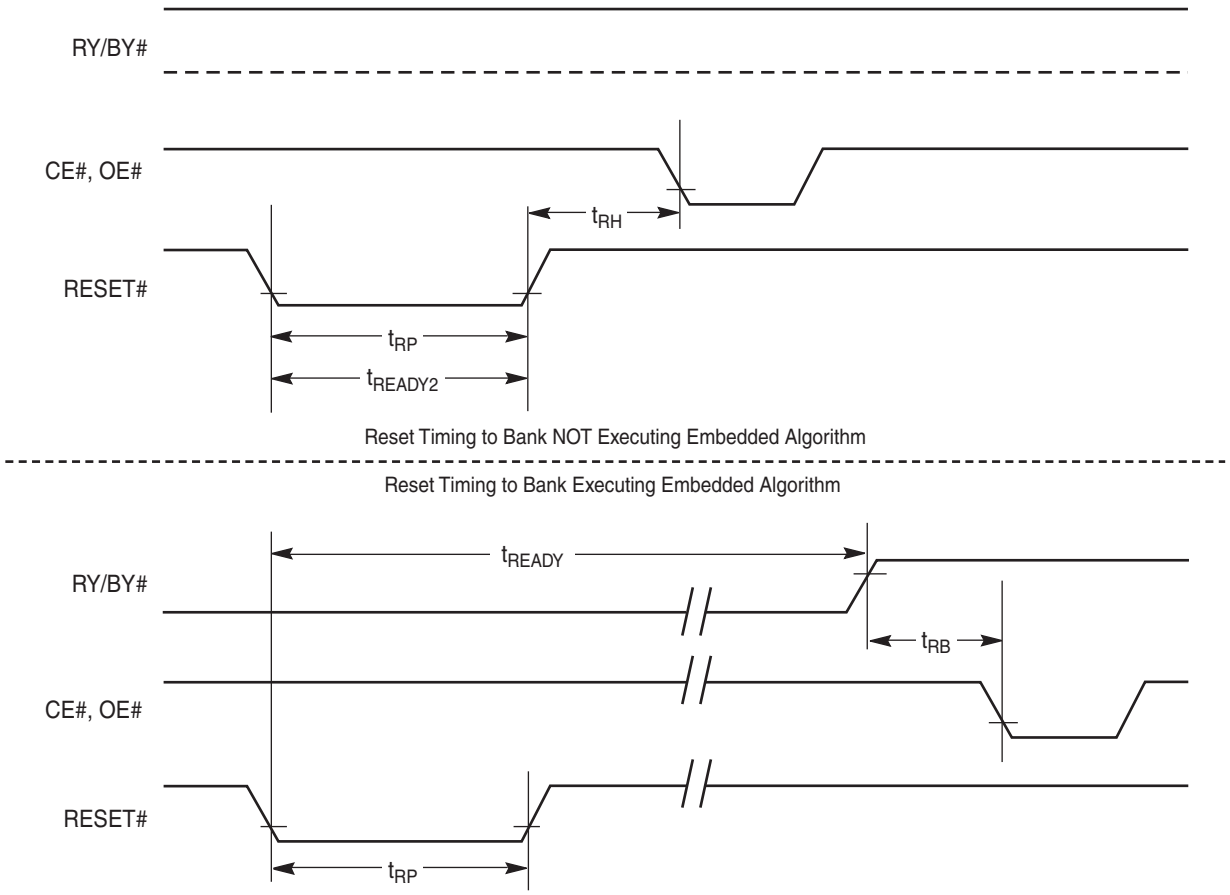
17.4 Hardware Reset (RESET#)

Table 25. Hardware Reset (RESET#)

Parameter		Description	Test Setup	All Speed Options	Unit
JEDEC	Std.				
	t_{READY}	RESET# Pin Low (During embedded Algorithms) to Read or Write (See Note)	Max	11	µs
	t_{READY2}	RESET# Pin Low (Not during embedded Algorithms) to Read or Write (See Note)	Min	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	RESET# High time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY # Recovery Time	Min	0	ns
	t_{READY3}	RESET # Active for Bank NOT Executing Algorithm	Min	500	ns

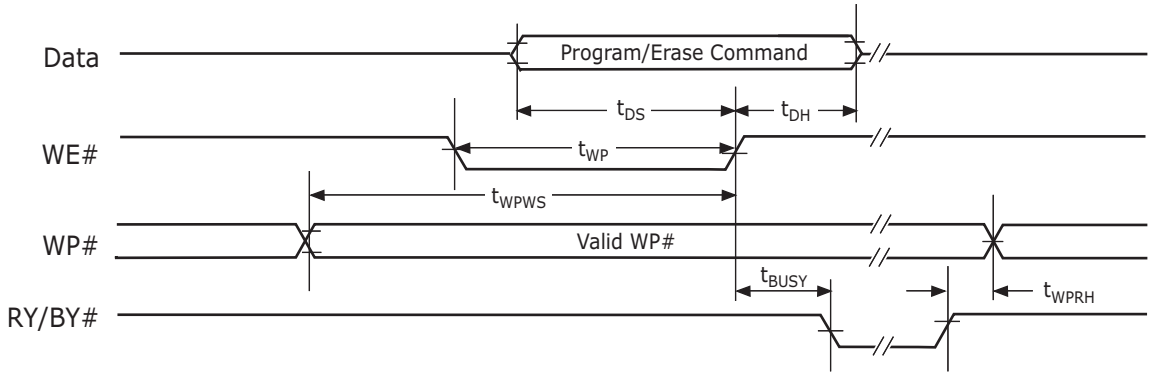
Note
66. Not 100% tested.

Figure 23. RESET# Timings



17.5 Write Protect (WP#)

Figure 24. WP# Timing



17.6 Erase/Program Operations

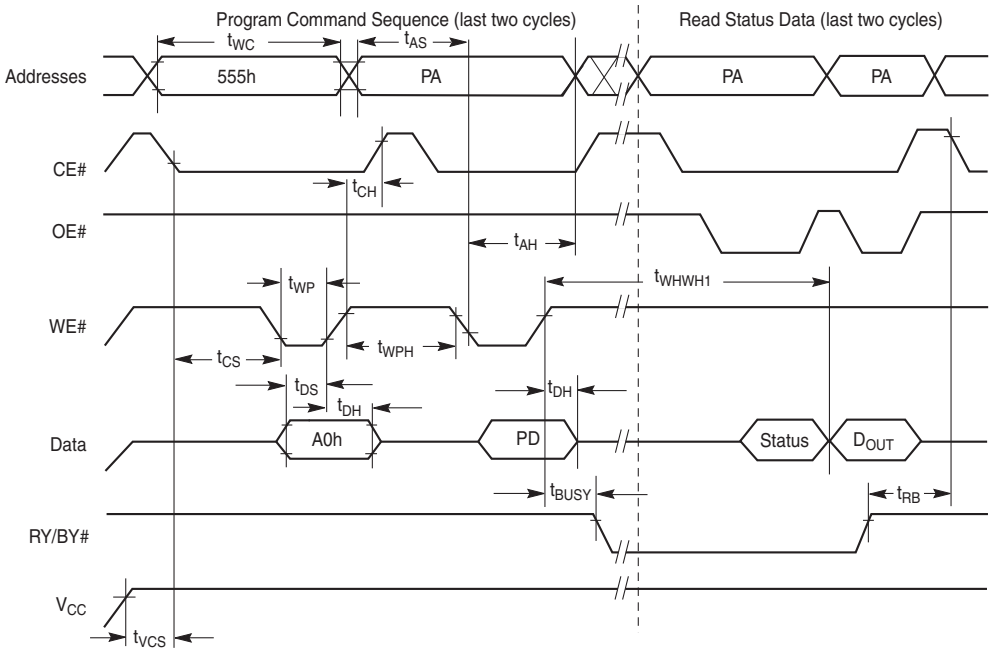
Table 26. Erase/Program Operations

Parameter		Description		All Speed Options	Unit
JEDEC	Std.				
t_{AVAX}	t_{WC}	Write Cycle Time (Note 67)	Min	60	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	ns
t_{WLAX}	t_{AH}	Address Hold Time from WE# Falling Edge	Min	11.75	ns
t_{DVWH}	t_{DS}	Data Setup to WE# Rising Edge	Min	18	ns
t_{WHDX}	t_{DH}	Data Hold from WE# Rising Edge	Min	2	ns
t_{GHWL}	t_{WEH}	Read Recovery Time Before Write (OE# High to WE# Low, WE# Hold Time) (Note 67)	Min	0	ns
	t_{OEP}	OE# Pulse Width (Note 67)	Min	16	ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0	ns
t_{WLWH}	t_{WP}	WE# Width	Min	25	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	30	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 68), Double-Word	Typ	9	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 68)	Typ	0.5	sec.
	t_{VCS}	V_{CC} Setup Time (Note 67)	Min	50	µs
	t_{RB}	Recovery Time from RY/BY# (Note 67)	Min	0	ns
	t_{BUSY}	RY/BY# Delay After WE# Rising Edge (Note 67)	Max	90	ns
	t_{WPWS}	WP# Setup to WE# Rising Edge with Command (Note 67)	Min	20	ns
	t_{WPRH}	WP# Hold after RY/BY# Rising Edge (Note 67)	Max	2	ns

Notes

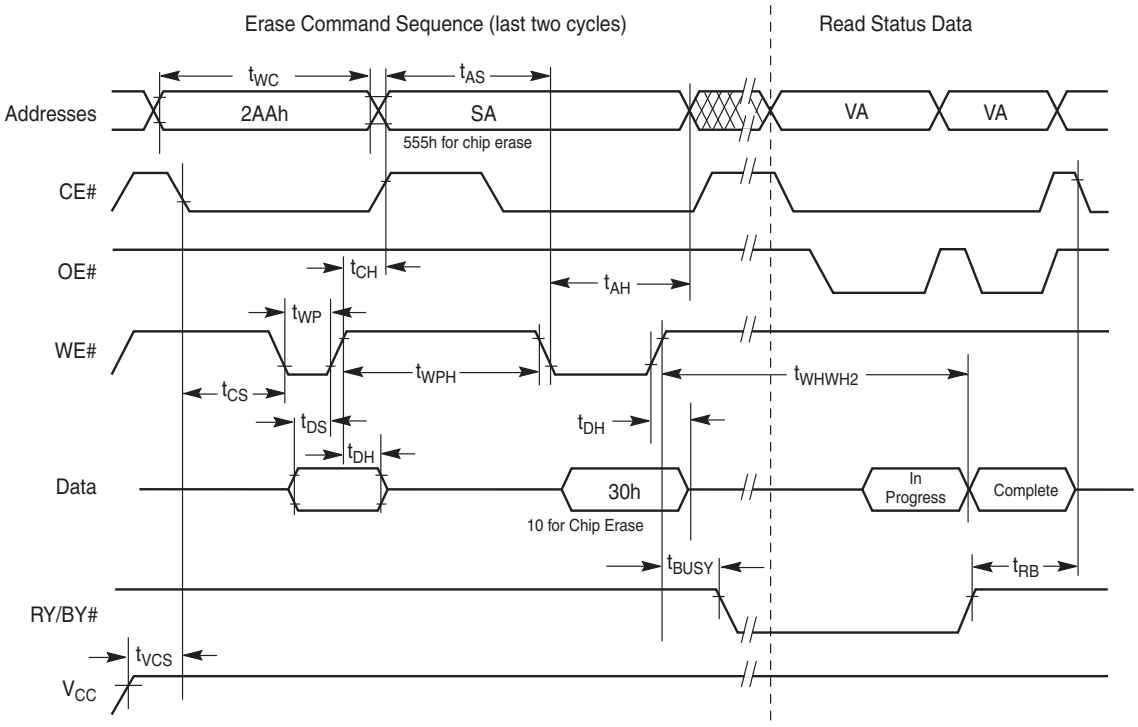
67. Not 100% tested.
68. See Command Definitions on page 67 for more information.
69. Program Erase Parameters are the same, regardless of Synchronous or Asynchronous mode.

Figure 25. Program Operation Timings



Note
70.PA = program address, PD = program data, D_{OUT} is the true data at the program address.

Figure 26. Chip/Sector Erase Operation Timings



Note
71.SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see Write Operation Status on page 32).

Figure 27. Back-to-back Cycle Timings

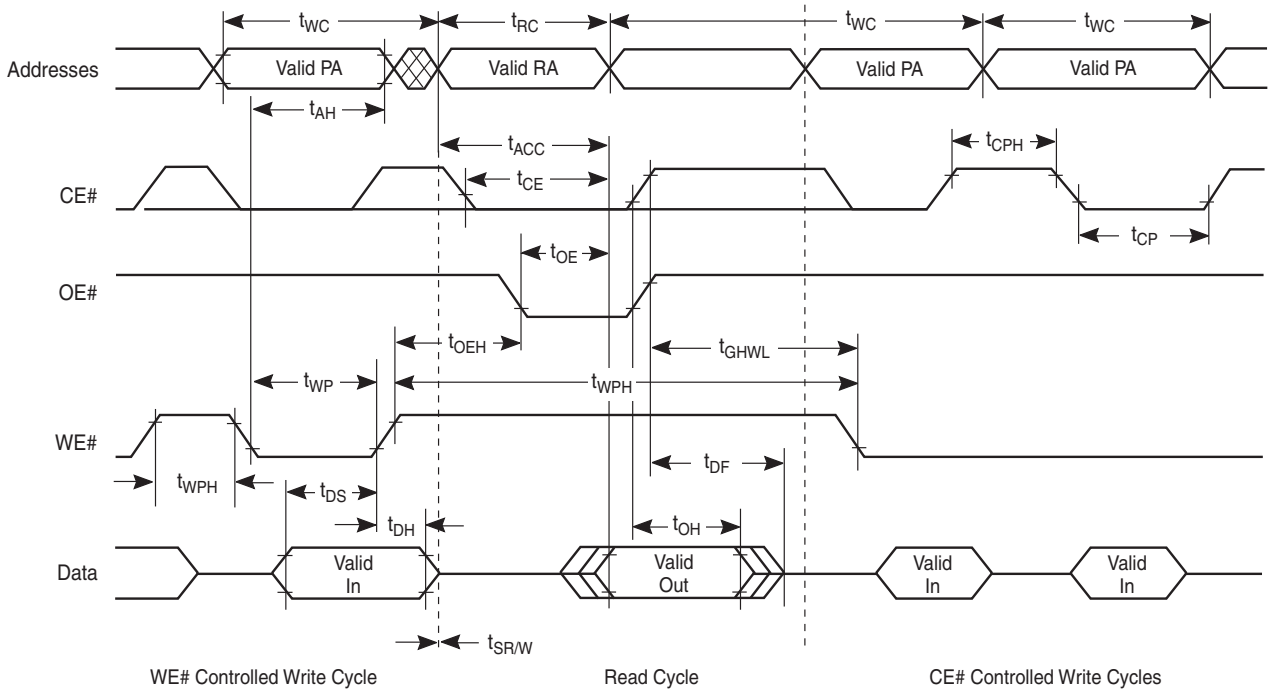
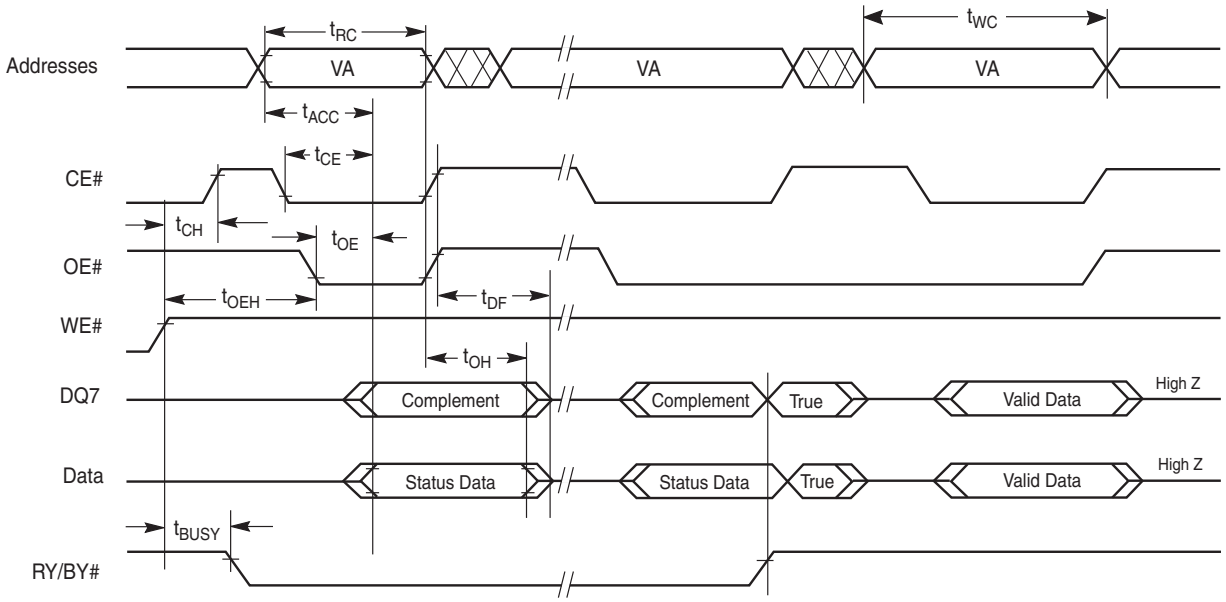
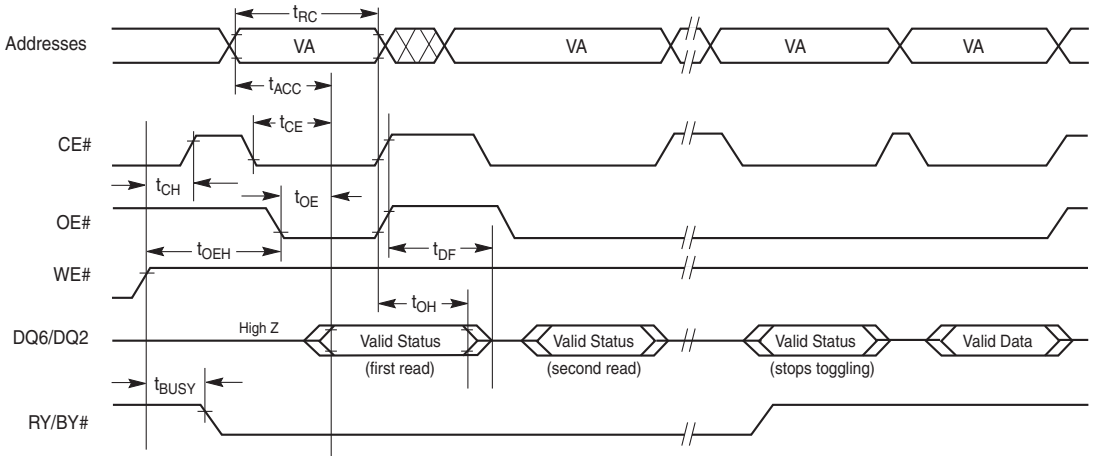


Figure 28. Data# Polling Timings (During Embedded Algorithms)



Note
72.VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

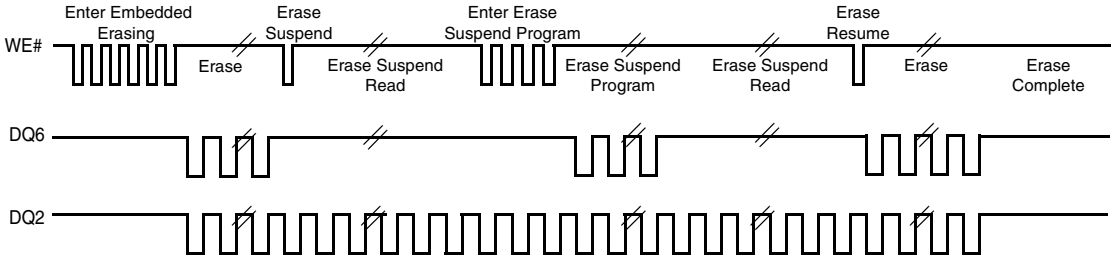
Figure 29. Toggle Bit Timings (During Embedded Algorithms)



Note

73. VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

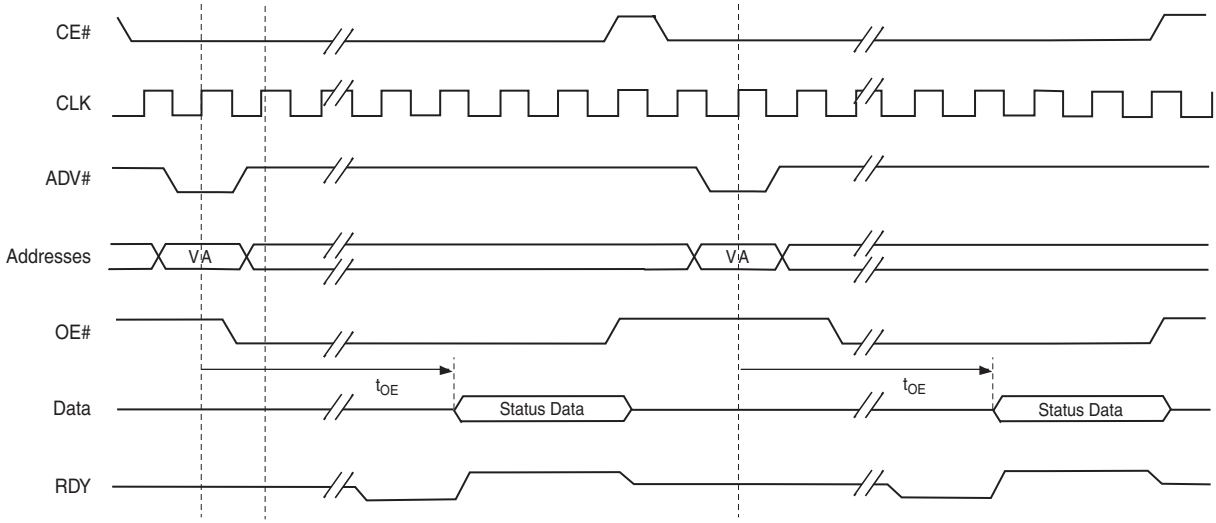
Figure 30. DQ2 vs. DQ6 for Erase/Erase Suspend Operations



Note

74. The system may use CE# or OE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.

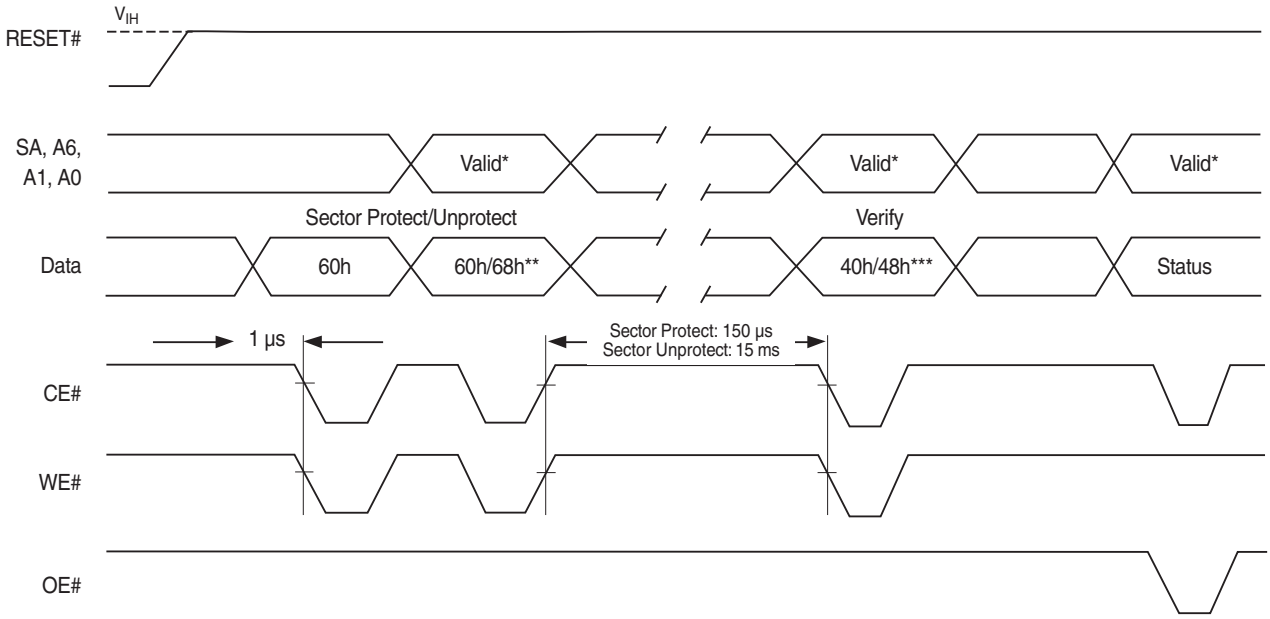
Figure 31. Synchronous Data Polling Timing/Toggle Bit Timings



Notes

75. The timings are similar to synchronous read timings and asynchronous data polling Timings/Toggle bit Timing.
76. VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.
77. RDY is active with data (A18 = 0 in the Configuration Register). When A18 = 1 in the Configuration Register, RDY is active one clock cycle before data.
78. Data polling requires burst access time delay.

Figure 32. Sector Protect/Unprotect Timing Diagram



Notes

79.* Valid address for sector protect: A[7:0] = 3Ah. Valid address for sector unprotect: A[7:0] = 3Ah.
** Command for sector protect is 68h. Command for sector unprotect is 60h.
*** Command for sector protect verify is 48h. Command for sector unprotect verify is 40h.

17.7 Alternate CE# Controlled Erase/Program Operations

Table 27. Alternate CE# Controlled Erase/Program Operations

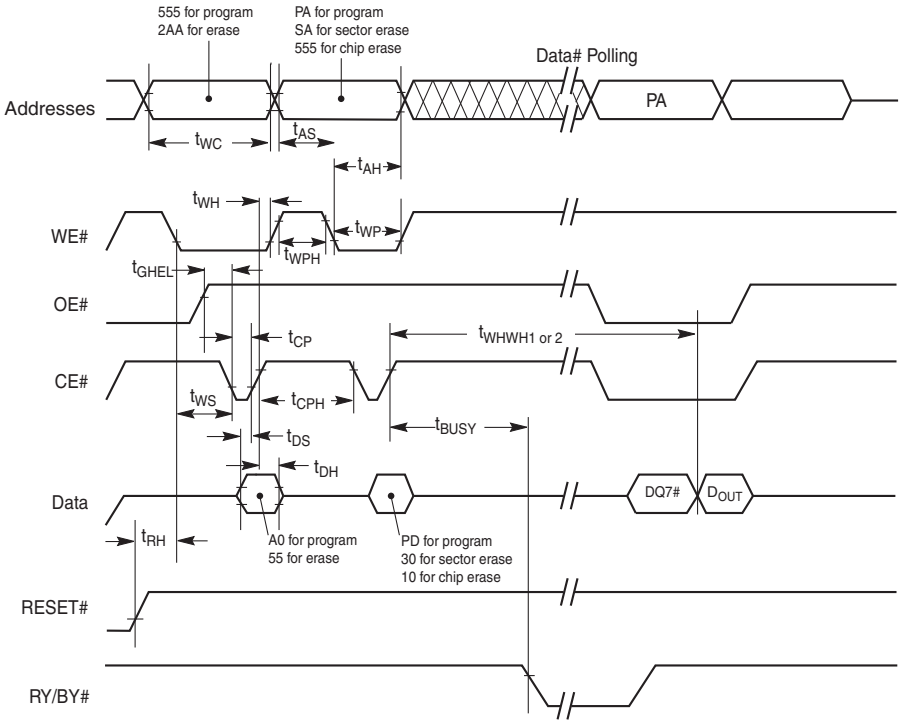
Parameter		Description			All Speed Options	Unit
JEDEC	Std.					
t_{AVAV}	t_{WC}	Write Cycle Time (Note 80)		Min	65	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	35	ns
t_{EHDX}	t_{DH}	Data Hold Time	16 Mb	Min	2	ns
			32 Mb	Min	5	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0	ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0	ns
	t_{WP}	WE# Width		Min	25	ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	20	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 81)	Double-Word	Typ	9	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 81)		Typ	0.5	sec
	t_{WCKS}	WE# Rising Edge Setup to CLK Rising Edge		Min	5	ns

Notes

80. Not 100% tested.

81. See Command Definitions on page 67 for more information.

Figure 33. Alternate CE# Controlled Write Operation Timings



Notes

82. PA = program address, PD = program data, DQ7# = complement of the data written to the device, D_{OUT} = data written to the device.

83. Figure indicates the last two bus cycles of the command sequence.

17.8 Erase and Programming Performance

Table 28. Erase and Programming Performance

Parameter	Typ (Note 84)	Max (Note 85)	Unit	Comments
Sector Erase Time	0.5	5	s	Excludes 00h programming prior to erasure (Note 87)
Chip Erase Time	16 Mb = 23 32 Mb = 46	16 Mb = 230 32 Mb = 460	s	
Double Word Program Time	8	130	µs	Excludes system level overhead (Note 88)
Accelerated Double Word Program Time	8	130	µs	
Accelerated Chip Program Time	16 Mb = 5 32 Mb = 10	16 Mb = 50 32 Mb = 100	s	
Chip Program Time, x32 (Note 86)	16 Mb = 12 32 Mb = 24	16 Mb = 120 32 Mb = 240	s	

Notes

84. Typical program and erase times assume the following conditions: 25°C, 2.5V V_{CC}, 100K cycles. Additionally, programming typicals assume checkerboard pattern.
85. Under worst case conditions of 145°C, V_{CC} = 2.5V, 1M cycles.
86. The typical chip programming time is considerably less than the maximum chip programming time listed.
87. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
88. System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 34 and Table 35 for further information on command definitions.
89. PPBs have a program/erase cycle endurance of 100 cycles.
90. Guaranteed cycles per sector is 100K minimum.

17.9 PQFP and Fortified BGA Pin Capacitance

Table 29. PQFP and Fortified BGA Pin Capacitance

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes

91. Sampled, not 100% tested.
92. Test conditions T_A = 25°C, f = 1.0 MHz.

18. Appendix 1

18.1 Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 30-Table 32. In order to terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table 30-Table 32. The system must write the reset command to return the device to the autoselect mode.

For further information, please refer to the CFI Specification and CFI Publication 100. Contact a Cypress representative for copies of these documents.

Table 30. CFI Query Identification String

Addresses	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string *QRY*
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 31. CFI System Interface String

Addresses	Data	Description
1Bh	(see description)	V_{CC} Min. (write/erase) DQ7–DQ4: volts, DQ3–DQ0: 100 millivolt 0025h = S29CD-J devices 0030h = S29CL-J devices
1Ch	(see description)	V_{CC} Max. (write/erase) DQ7–DQ4: volts, DQ3–DQ0: 100 millivolt 0027h = S29CD-J devices 0036h = S29CL-J devices
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0004h	Typical timeout per single word/doubleword program 2^N µs
20h	0000h	Typical timeout for Min. size buffer program 2^N µs (00h = not supported)
21h	0009h	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0005h	Max. timeout for word/doubleword program 2^N times typical
24h	0000h	Max. timeout for buffer write 2^N times typical
25h	0007h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 32. Device Geometry Definition

Addresses	Data	Description
27h	(see description)	Device Size = 2^N byte 0015h = 16 Mb device 0016h = 32 Mb device
28h 29h	0003h 0000h	Flash Device Interface description (for complete description, please refer to CFI publication 100) 0000 = x8-only asynchronous interface 0001 = x16-only asynchronous interface 0002 = supports x8 and x16 via BYTE# with asynchronous interface 0003 = x 32-only asynchronous interface 0005 = supports x16 and x32 via WORD# with asynchronous interface
2Ah 2Bh	0000h 0000h	Max. number of byte in multi-byte program = 2^N (00h = not supported)
2Ch	0003h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	(See description) 0000h 0000h 0001h	Erase Block Region 2 Information (refer to the CFI specification or CFI publication 100) Address 31h data: 001Dh = 16 Mb device 003Dh = 32 Mb device
35h 36h 37h 38h	0007h 0000h 0020h 0000h	Erase Block Region 3 Information (refer to the CFI specification or CFI publication 100)
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to the CFI specification or CFI publication 100)

Table 33. CFI Primary Vendor-Specific Extended Query

Addresses	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string *PRI*
43h	0031h	Major version number, ASCII (reflects modifications to the silicon)
44h	0033h	Minor version number, ASCII (reflects modifications to the CFI table)
45h	000Ch	Address Sensitive Unlock (DQ1, DQ0) 00 = Required, 01 = Not Required Silicon Revision Number (DQ5–DQ2) 0000 = CS49 0001 = CS59 0010 = CS99 0011 = CS69 0100 = CS119
46h	0002h	Erase Suspend (1 byte) 00 = Not Supported 01 = To Read Only 02 = To Read and Write
47h	0001h	Sector Protect (1 byte) 00 = Not Supported, X = Number of sectors in per group
48h	0000h	Temporary Sector Unprotect 00h = Not Supported, 01h = Supported

Table 33. CFI Primary Vendor-Specific Extended Query (Continued)

Addresses	Data	Description
49h	0006h	Sector Protect/Unprotect scheme (1 byte) 01 =29F040 mode, 02 = 29F016 mode 03 = 29F400 mode, 04 = 29LV800 mode 05 = 29BDS640 mode (Software Command Locking) 06 = BDD160 mode (New Sector Protect) 07 = 29LV800 + PDL128 (New Sector Protect) mode
4Ah	0037h	Simultaneous Read/Write (1 byte) 00h = Not Supported, X = Number of sectors in all banks except Bank 1
4Bh	0001h	Burst Mode Type 00h = Not Supported, 01h = Supported
4Ch	0000h	Page Mode Type 00h = Not Supported, 01h = 4 Word Page, 02h = 8 Word Page
4Dh	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported (DQ7-DQ4: volt in hex, DQ3-DQ0: 100 mV in BCD)
4Eh	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, (DQ7-DQ4: volt in hex, DQ3-DQ0: 100 mV in BCD)
4Fh	0001h	Top/Bottom Boot Sector Flag (1 byte) 00h = Uniform device, no WP# control, 01h = 8 x 8 Kb sectors at top and bottom with WP# control 02h = Bottom boot device 03h = Top boot device 04h = Uniform, Bottom WP# Protect 05h = Uniform, Top WP# Protect If the number of erase block regions = 1, then ignore this field
50h	0001h	Program Suspend 00 = Not Supported 01 = Supported
51h	0000h	Write Buffer Size $2^{(N+1)}$ word(s)
57h	0002h	Bank Organization (1 byte) 00 = If data at 4Ah is zero XX = Number of banks
58h	0017h	Bank 1 Region Information (1 byte) XX = Number of Sectors in Bank 1
59h	0037h	Bank 2 Region Information (1 byte) XX = Number of Sectors in Bank 2
5Ah	0000h	Bank 3 Region Information (1 byte) XX = Number of Sectors in Bank 3
5Bh	0000h	Bank 4 Region Information (1 byte) XX = Number of Sectors in Bank 4

19. Appendix 2

19.1 Command Definitions

Table 34. Memory Array Command Definitions (x32 Mode)

Command (Notes)		Cycles	Bus Cycles (Notes 93–96)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (97)		1	RA	RD										
Reset (98)		1	XXX	F0										
Autoselect (99)	Manufacturer ID	4	555	AA	2AA	55	555	90	BA+X00	01				
	Device ID (100)	6	555	AA	2AA	55	555	90	BA+X01	7E	BA+X0E	09	BA+X0F	00/01
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Program/Erase Suspend (101)		1	BA	B0										
Program/Erase Resume (102)		1	BA	30										
CFI Query (103, 104)		1	55	98										
Accelerated Program (105)		2	XX	A0	PA	PD								
Configuration Register Verify (104)		3	555	AA	2AA	55	BA+555	C6	BA+XX	RD				
Configuration Register Write (106)		4	555	AA	2AA	55	555	D0	XX	WD				
Unlock Bypass Entry (107)		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (107)		2	XX	A0	PA	PD								
Unlock Bypass Erase (107)		2	XX	80	XX	10								
Unlock Bypass CFI (103, 107)		1	XX	98										
Unlock Bypass Reset (107)		2	XX	90	XX	00								

Legend

BA = Bank Address. The set of addresses that comprise a bank. The system may write any address within a bank to identify that bank for a command.

PA = Program Address (Amax–A0). Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Program Data (DQmax–DQ0) written to location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

RA = Read Address (Amax–A0).

RD = Read Data. Data DQmax–DQ0 at address location RA.

SA = Sector Address. The set of addresses that comprise a sector. The system may write any address within a sector to identify that sector for a command.

WD = Write Data. See “Configuration Register” definition for specific write data. Data latched on rising edge of WE#.

X = Don’t care

Notes

93. See Table 5 for description of bus operations.
94. All values are in hexadecimal.
95. Shaded cells in table denote read cycles. All other cycles are write operations.
96. During unlock cycles, (lower address bits are 555 or 2AAh as shown in table) address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don’t cares.
97. No unlock or command cycles required when bank is reading array data.
98. The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 goes high (while the bank is providing status information).
99. The fourth cycle of the autoselect command sequence is a read cycle. The system must provide the bank address to obtain the manufacturer ID or device ID information. See Autoselect on page 26 for more information.
100. The device ID must be read across the fourth, fifth, and sixth cycles. 00h in the sixth cycle indicates ordering option 00, 01h indicates ordering option 01.
101. The system may read and program in non-erasing sectors when in the Program/Erase Suspend mode. The Program/Erase Suspend command is valid only during a sector erase operation, and requires the bank address.
102. The Program/Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.
103. Command is valid when device is ready to read array data.
104. Asynchronous read operations.
105. ACC must be at V_{ID} during the entire operation of this command.
106. Command is ignored during any Embedded Program, Embedded Erase, or Suspend operation.
107. The Unlock Bypass Entry command is required prior to any Unlock Bypass operation. The Unlock Bypass Reset command is required to return to the read mode.

Table 35. Sector Protection Command Definitions (x32 Mode)

Command (Notes)	Cycles	Bus Cycles (Notes 108–111)											
		First		Second		Third		Fourth		Fifth		Sixth	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	XXX	F0										
Secured Silicon Sector Entry	3	555	AA	2AA	55	555	88						
Secured Silicon Sector Exit	4	555	AA	2AA	55	555	90	XX	00				
Secured Silicon Protection Bit Program (112, 113)	6	555	AA	2AA	55	555	60	OW	68	OW	48	OW	RD(0)
Secured Silicon Protection Bit Status	6	555	AA	2AA	55	555	60	OW	RD(0)				
Password Program (112, 114, 115)	4	555	AA	2AA	55	555	38	PWA[0-1]	PWD[0-1]				
Password Verify	4	555	AA	2AA	55	555	C8	PWA[0-1]	PWD[0-1]				
Password Unlock (114, 115)	5	555	AA	2AA	55	555	28	PWA[0-1]	PWD[0-1]				
PPB Program (112, 113)	6	555	AA	2AA	55	555	60	SG+WP	68	SG+WP	48	SG+WP	RD(0)
All PPB Erase (112, 116, 117)	6	555	AA	2AA	55	555	60	WP	60	WP	40	WP	RD(0)
PPB Status (118, 119)	4	555	AA	2AA	55	BA+555	90	SA+X02	00/01				
PPB Lock Bit Set	3	555	AA	2AA	55	555	78						
PPB Lock Bit Status	4	555	AA	2AA	55	BA+555	58	SA	RD(1)				
DYB Write (114)	4	555	AA	2AA	55	555	48	SA	X1				
DYB Erase (114)	4	555	AA	2AA	55	555	48	SA	X0				
DYB Status (119)	4	555	AA	2AA	55	BA+555	58	SA	RD(0)				
PPMLB Program (112, 113)	6	555	AA	2AA	55	555	60	PL	68	PL	48	PL	RD(0)
PPMLB Status (112)	6	555	AA	2AA	55	555	60	PL	RD(0)				
SPMLB Program (112, 113)	6	555	AA	2AA	55	555	60	SL	68	SL	48	SL	RD(0)
SPMLB Status (112)	6	555	AA	2AA	55	555	60	SL	RD(0)				

Legend

DYB = Dynamic Protection Bit
OW = Address (A5–A0) is (011X10).
PPB = Persistent Protection Bit
PWA = Password Address. A0 selects between the low and high 32-bit portions of the 64-bit Password
PWD = Password Data. Must be written over two cycles.
PL = Password Protection Mode Lock Address (A5–A0) is (001X10)
RD(0) = Read Data DQ0 protection indicator bit. If protected, DQ0= 1, if unprotected, DQ0 = 0.
RD(1) = Read Data DQ1 protection indicator bit. If protected, DQ1 = 1, if unprotected, DQ1 = 0.
SA = Sector Address. The set of addresses that comprise a sector. The system may write any address within a sector to identify that sector for a command.
SG = Sector Group Address
BA = Bank Address. The set of addresses that comprise a bank. The system may write any address within a bank to identify that bank for a command.
SL = Persistent Protection Mode Lock Address (A5–A0) is (010X10)
WP = PPB Address (A5–A0) is (111010)
X = Don’t care
PPMLB = Password Protection Mode Locking Bit
SPMLB = Persistent Protection Mode Locking Bit

Notes

108. See Table 5 for description of bus operations.
109. All values are in hexadecimal.
110. Shaded cells in table denote read cycles. All other cycles are write operations.
111. During unlock cycles, (lower address bits are 555 or 2AAh as shown in table) address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don’t cares.
112. The reset command returns the device to reading the array.
113. The fourth cycle programs the addressed locking bit. The fifth and sixth cycles are used to validate whether the bit has been fully programmed. If DQ0 (in the sixth cycle) reads 0, the program command must be issued and verified again.
114. Data is latched on the rising edge of WE#.
115. The entire four bus-cycle sequence must be entered for each portion of the password.
116. The fourth cycle erases all PPBs. The fifth and sixth cycles are used to validate whether the bits have been fully erased. If DQ0 (in the sixth cycle) reads 1, the erase command must be issued and verified again.
117. Before issuing the erase command, all PPBs should be programmed in order to prevent over-erasure of PPBs.
118. In the fourth cycle, 00h indicates PPB set; 01h indicates PPB not set.
119. The status of additional PPBs and DYBs may be read (following the fourth cycle) without reissuing the entire command sequence.

20. Revision History

Document Title: S29CD032J, S29CD016J, S29CL032J, S29CL016J, 32/16 Mbit, 2.6/3.3 V, Dual Boot, Simultaneous Read/ Write, Burst Flash Document Number: 002-00948				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	RYSU	03/01/2005	**Spansion Publication Number:** S29CD-J_CL-J_00 A0:Initial release
			04/15/2005	A1:Ordering Information and Valid Combinations tables Updated to include lead Pb-free options.
			01/20/2006	**Ordering Information** Added “Contact factory” for 75 MHz. Modified Ordering Options for Characters 15 and 16 to reflect autoselect ID and top/bottom boot. Changed “N” for Extended Temperature Range to “M”. **Input/Output Descriptions** Removed Logic Symbol Diagrams. **Additional Resources** Added section. **Memory Address Map** Changed “Bank 2” to “Bank 1”. **Simultaneous Read/Write Operation** Removed Ordering Options Table (Tables 3 and 4). Advanced Sector Protection/Unprotection Added Advanced Sector Protection/Unprotection figure. Added figures for PPB Erase and Program Algorithm. **Electronic Marking** Added in Electronic Marking section. **Absolute Maximum Ratings** Modified VCC Ratings to reflect 2.6 V and 3.6 V devices. Modified VCC Ratings to reflect 16 Mb and 32 Mb devices. **AC Characteristics** Added Note “tOE during Read Array”. **Asynchronous Read Operation** Changed values of tAVAV, tAVQV, tELQV, tGLQV in table. **Conventional Read Operation Timings** Moved tDF line to 90% on the high-Z output in figure. **Burst Mode Read for 32 Mb and 16 Mb** Added tAAVS and tAAVH timing parameters to table. Changed tCH to tCLKH. Changed tCL to tCLKL. Removed the following timing parameters: • tDS (Data Setup to WE# Rising Edge) • tDH (Data Hold from WE# Rising Edge) • tAS (Address Setup to Falling Edge of WE#) • tAH (Address Hold from Falling Edge of WE#) • tCS (CE# Setup Time) • tCH (CE# Hold Time) • tACS (Address Setup Time to CLK) • tACH (Address Hold Time from ADV# Rising Edge of CLK while ADV# is Low) Burst Mode Read (x32 Mode) Added the following timing parameters: • tAAVS • tDVCH • tINDS • tINDH

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	RYSU	01/20/2006	**Asynchronous Command Write Timing** In figure, changed tOEH to tWEH; changed tWPH to tOEP. Synchronous Command Write/Read Timing Removed tWADVH and tWCKS from figure. **WP# Timing** In figure, changed tCH to tBUSY Erase/Program Operations In table, added Note 3: Program/Erase parameters are the same regardless of synchronous or asynchronous mode. Added tOEP (OE# High Pulse) Alternative CE# Controlled Erase/Program Operations Removed tOES from table. Added tWADVS and tWCKS **Appendix 2: Command Definitions** Removed “or when device is in autoselect mode” from Note 14.
			06/12/2006	**Global** Changed document status to Preliminary. **Distinctive Characteristics** Changed cycling endurance from typical to guaranteed. **Performance Characteristics** Updated Max Asynch. Access Time, Max CE# Access Time, and Max OE# Access time in table. **Ordering Information** Updated additional ordering options in designator breakout table. Updated valid combination tables. Input/Output Descriptions and Logic Symbols Changed RY/BY# description. Physical Dimensions/Connection Diagrams Changed note on connection diagrams. **Additional Resources** Updated contact information. **Hardware Reset (RESET#)** Added section. Autoselect Updated third and fourth paragraphs in section. Updated Autoselect Codes table. Erase Suspend / Erase Resume Commands Modified second paragraph. Replaced allowable operations table with bulleted list. Program Suspend / Program Resume Commands Replaced allowable operations table with bulleted list. **Reset Command** Added section. Secured Silicon Sector Flash Memory Region Modified Secured Silicon Sector Addresses table. **Absolute Maximum Ratings** Modified VCC and VIO ratings. Modified Note 1. **Operating Ranges** Modified specification titles and descriptions (no specification value changes). DC Characteristics, CMOS Compatible table Modified ICCB specification. Deleted Note 5. Added Note 3 references to table. Burst Mode Read for 32 Mb and 16 Mb table Modified tADVCS, tCLKH, tCLKL, tAAVS specifications. Added tRSTZ, tWADVH1, and tWADVH2 specifications. Added Notes 2 and 3, and note references to table. Synchronous Command Write/Read Timing figure Added tWADVH1 and tWADVH2 to figure. Deleted tACS and tACH from figure. **Hardware Reset (RESET#)** Added table to section. **Erase/Program Operations table** Added note references. Deleted tOEP specification. **Erase and Programming Performance** Changed Double Word Program Time specification.
			06/12/2006	Common Flash Memory Interface (CFI) CFI System Interface String table: Changed description and data for addresses 1Bh and 1Ch. Device Geometry Definition table: Changed description and data for address 27h.

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	RYSU	09/27/2006	**Global** Data sheet format reorganized. **Distinctive Characteristics** Changed cycling endurance specification to typical. **Performance Characteristics** Changed tBACC specifications for 66 MHz, 56 MHz, 40 MHz speed options. **Ordering Information** Added quantities to packing type descriptions, restructured table for easier reference. S29CD-J and S29CL-J Flash Family Autoselect Codes (High Voltage Method) In table, modified description of read cycle 3 DQ7–DQ0. DQ6 and DQ2 Indications In table, corrected third column heading Section 8.9, Reset Command Added table. Section 13.1, Absolute Maximum Ratings Deleted OE# from section. Table 18.3, Burst Mode Read for 32 Mb and 16 Mb In table, changed tADVCS, tBDH specifications. Modified description for tIACC. Deleted minimum specifications for tAAVH. **Burst Mode Read (x32 Mode)** In figure, modified period for tIACC in drawing.
			03/07/2007	**Distinctive Characteristics** Corrected number of 16K sectors in 16 Mb devices. Modified read access times table. Ordering Information Changed boot sector option part number designators. Changed valid combinations. Modified 10th character option descriptions. **Block Diagram** Deleted WORD# input. 2-, 4-, 8- Double Word Linear Burst Operation In 32- Bit Linear and Burst Data Order table, deleted reference to WORD# input. **Sector Erase** Modified second paragraph; added reference to application note. Advanced Sector Protection/ Unprotection Modified Advanced Sector Protection/Unprotection figure and notes. In some subsections, changed “sector” to “sector group”. **DC Characteristics** Changed ICCB test conditions and ICC1 maximum specification. **Test Specifications** Changed CL. Asynchronous Operations *Asynchronous Command Write Timing figure:* Added note. *Asynchronous Read Operations table:* Changed tRC, tACC, tCE for 75 MHz device. Synchronous Operations *Burst Mode Read for 32 Mb and 16 Mb table:* Changed tINDS, tCLKL, tAAVH, and tWADVH1 specifications. *Burst Mode Read figure:* Modified period lengths for several specifications. **Erase/Program Operations** Added tWEH and tOEP specifications to table. **Latchup Characteristics** Deleted section. **Common Flash Memory Interface (CFI)** *CFI System Interface String table:* Modified description of address 1Bh. *CFI Primary Vendor-Specific Extended Query table:* Modified data at address 45h.

Document Title: S29CD032J, S29CD016J, S29CL032J, S29CL016J, 32/16 Mbit, 2.6/3.3 V, Dual Boot, Simultaneous Read/ Write, Burst Flash Document Number: 002-00948				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	RYSU	03/30/2009	Global Removed “Preliminary” Changed all instances of VCCQ to VIO **Distinctive Characteristics** Removed “or without” (wrap around) from Programmable Burst Interface bullet **Performance Characteristics** Added notice to refer to programming best practices application note for 32 Mb devices. Ordering Information Added S29CL032J to valid OPN diagram. Corrected valid combinations table. Input/Output Descriptions and Logic Symbols Subscript CC for VCC, IO for VIO, SS for VSS in table. Changed type for VIO to “Supply” Changed type for VSS to “Supply” Block Diagram Removed DQmax-DQ0 label from inputs to Burst Address Counter and Address Latch. Removed Amax-A0 label from I/O Buffers. Table: S29CD016J/CL016J (Top Boot) Sector and Memory Address Map Changed Note 2 to refer to Bank 0 and 1 instead of Bank 1 and 2. Table: 32-Bit Linear and Burst Data Order Removed “x16” Removed “A0:A-1” from Output Data Sequence column for Four Linear Data Transfers. Removed “A1:A-1” from Output Data Sequence column for Eight Linear Data Transfers. **Programming** Added notice to refer to programming best practices application note for 32 Mb devices. Table: DC Characteristic, CMOS Compatible Changed Max ICCB for S29CL-J to 90 mA. Table: Burst Mode for 32 Mb and 16 Mb Corrected values for tBDH with separate values for 16Mb and 32Mb. Added tWADVS parameter to table. Figure: Synchronous Command Write/ Read Timing Added timing definition for tWADVS. Table: Erase/Program Operations Appended “from WE# Rising Edge” to tAH description. Changed tAH Min to 11.75 ns. **Figure: Program Operation Timings** Updated timing diagram to reflect new tAH value. Figure: Chip/Sector Erase Operation Timings Updated timing diagram to reflect new tAH value.
			03/30/2009	Table: Alternate CE# Controlled Erase/Program Operations Removed tWADVS parameter. Product Overview Removed “or without”. Table: Device Bus Operation Changed “X” to “H” under CLK column for CE# row. Accelerated Program and Erase Operations Removed all mention of accelerated erase. **Unlock Bypass** Removed mention of unlock bypass sector erase. **Simultaneous Read/Write** Added in warning to indicate restrictions on Simultaneous Read/Write conditions. VCC and VIO Power-up And Powerdown Sequencing Added reference to timing section. **Standby Mode** Changed Vcc ± 0.2V to Vcc ± 10%. **Figure: Test Setup** Removed Note “Diodes are IN3064 or equivalent”. Table: Alternate CE# Controlled Erase/Program Operations Corrected values for tDH with separate values for 16 Mb and 32 Mb. Table: Memory Array Command Definitions (x32 Mode) Cleaned up Notes.

Document Title: S29CD032J, S29CD016J, S29CL032J, S29CL016J, 32/16 Mbit, 2.6/3.3 V, Dual Boot, Simultaneous Read/ Write, Burst Flash Document Number: 002-00948				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	RYSU	10/30/2009	**Absolute Maximum Ratings** Corrected *Address, Data, Control Signals* identifiers to correctly distinguish different ratings between CL016L, CL032J, CD016J, and CD032J. **DC Characteristics** Added line item to distinguish VIHCLK value differences between CL-J and CD-J. Synchronous Operation Corrected Figure “Burst Mode Read (x32 Mode)” to reflect max linear burst length of 8 double words instead of 32. **Hardware Reset (RESET#)** Corrected Table “Burst Initial Access Delay”: changed tREADY2, tRP, and tREADY3 set up to Min instead of Max. Corrected Figure “RESET# Timings” to add tREADY2 to timing diagram for bank not executing embedded algorithm.
			05/25/2011	Physical Dimensions/Connection Diagrams On the 80-ball Fortified BGA Connection Diagram, corrected the K1 pin name from VCCQ to VIO.
			03/15/2012	**Global** Added LAD080 Fortified BGA package option and drawing. **Additional Resources** Updated relevant application note links. **Revision History** Corrected heading for May 25, 2011 edits from revision B4 to B5.
			10/11/2012	Valid Combinations Updated Valid Combinations table to add clarity and make explicit which offerings require a customer to “contact factory for availability”. Asynchronous Operations In Figure 18.3, “Asynchronous Command Write Timing”, corrected the tWC measurement to be of the Stable Address period, not the Valid Data period. Erase/Program Operations In Table 18.5, “Erase/Program Operations”, corrected JEDEC symbol tAVAV to tAVAX. In Table 18.5, merged redundant rows tGHWL and tWEH. In Figures 18.8 “Program Operation Timings” and 18.9 “Chip/Sector Erase Operation Timings”, corrected tAH measurement to be from the falling edge of WE#.
*A	5048814	RYSU	12/16/2015	Updated to Cypress template
*B	5741593	AESATMP7	05/18/2017	Updated Cypress Logo and Copyright.
*C	5875054	NFB	11/08/2017	Updated template. Removed “Preliminary” document status. Removed Section 6. Additional Resources.

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