



THE DATASHEET OF SN74HC251DG4

SNx4HC251 Data Selectors/Multiplexers With 3-State Outputs

1 Features

- 3-state version of 'HC151
- Wide operating voltage range of 2 V to 6 V
- High-current 3-state outputs interface directly with system bus or can drive up to 15 LSTTL loads
- Low power consumption, 80- μ A max I_{CC}
- Typical $t_{pd} = 9$ ns
- ± 6 -mA output drive at 5 V
- Low input current of 1 μ A max
- Perform parallel-to-serial conversion
- Complementary outputs provide true and inverted data

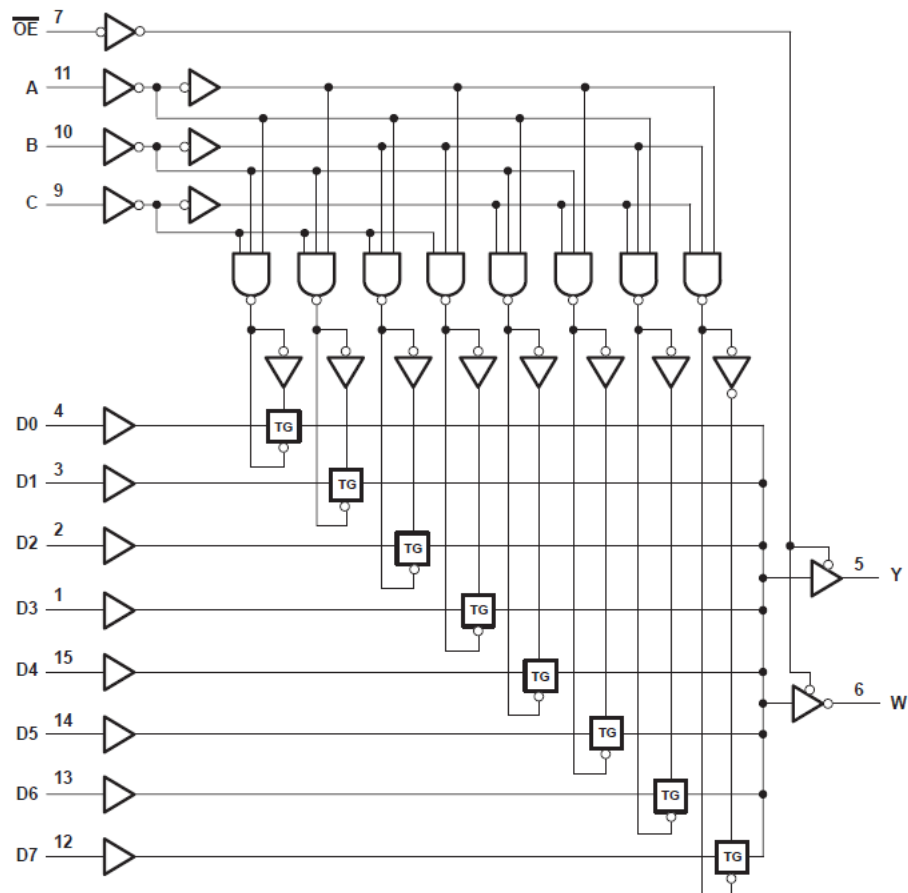
2 Description

The SNx4HC251 is a data selector/multiplexer containing full binary decoding to select 1-of-8 data sources and features strobe-controlled complementary 3-state outputs.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
SN74HC251D	SOIC (16)	9.90 mm $\times$ 3.90 mm
SN74HC251DB	SSOP (16)	6.20 mm $\times$ 5.30 mm
SN74HC251N	PDIP (16)	19.31 mm $\times$ 6.35 mm
SN74HC251NS	SO (16)	6.20 mm $\times$ 5.30 mm
SN74HC251PW	TSSOP (16)	5.00 mm $\times$ 4.40 mm
SN54HC251J	CDIP (16)	24.38 mm $\times$ 6.92 mm
SNJ54HC251FK	LCCC (20)	8.89 mm $\times$ 8.45 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

Functional Block Diagram



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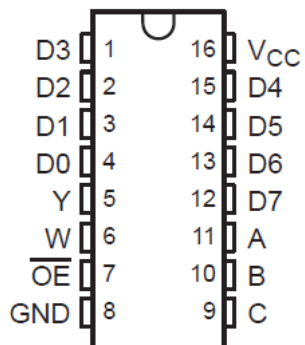
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3 Revision History

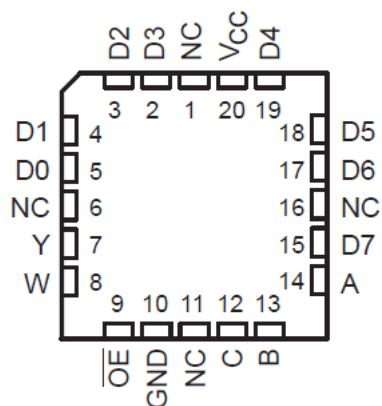
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (September 2003) to Revision F (February 2022)	Page
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....	1

4 Pin Configuration and Functions



J, D, DB, N, NS, or PW Package
16-Pin CDIP, SOIC, SSOP, PDIP, SO, or TSSOP
Top View



NC - No internal connection

FK Package
20-Pin LCCC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		−0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	V _I < 0 or V _I > V _{CC}		±20	mA
I _{OK}	Output clamp current ⁽²⁾	V _O < 0 or V _O > V _{CC}		±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±35	mA
	Continuous current through V _{CC} or GND			±70	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		−65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

			SN54HC251			SN74HC251			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5			1.5			V
		V _{CC} = 4.5 V	3.15			3.15			
		V _{CC} = 6 V	4.2			4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V			0.5			0.5	V
		V _{CC} = 4.5 V			1.35			1.35	
		V _{CC} = 6 V			1.8			1.8	
V _I	Input voltage		0		V _{CC}	0		V _{CC}	V
V _O	Output voltage		0		V _{CC}	0		V _{CC}	V
Δt/Δv	Input transition rise/fall time	V _{CC} = 2 V			1000			1000	ns
		V _{CC} = 4.5 V			500			500	
		V _{CC} = 6 V			400			400	
T _A	Operating free-air temperature		−55		125	−40		85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	73	82	67	64	108	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	V _{CC} (V)	T _A = 25°C			SN54HC251		SN74HC251		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -20 µA	2	1.9	1.998		1.9		1.9		V
		4.5	4.4	4.499		4.4		4.4		
		6	5.9	5.999		5.9		5.9		
	I _{OH} = -6 mA	4.5	3.98	4.3		3.7		3.84		
	I _{OH} = -7.8 mA	6	5.48	5.8		5.2		5.34		
V _{OL}	I _{OL} = 20 µA	2		0.002	0.1		0.1		0.1	V
		4.5		0.001	0.1		0.1		0.1	
		6		0.001	0.1		0.1		0.1	
	I _{OL} = 6 mA	4.5		0.17	0.26		0.4		0.33	
	I _{OL} = 7.8 mA	6		0.15	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0	6		±0.1	±100		±1000		±1000	nA
I _{OZ}	V _O = V _{CC} or 0	6		±0.01	±0.5		±10		±5	µA
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6			8		160		80	µA
C _i		2 to 6		3	10		10		10	pF

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

5.5 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} (V)	T _A = 25°C			SN54HC251		SN74HC251		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A, B, or C	W or Y	2		58	205		300		256	ns
			4.5		21	41		60		51	
			6		19	35		51		44	
	Any D	W or Y	2		44	195		283		244	
			4.5		17	39		57		49	
			6		15	33		48		41	
t _{en}	$\overline{OE}$	W or Y	2		30	145		210		181	ns
			4.5		10	29		42		36	
			6		9	25		36		31	
t _{dis}	$\overline{OE}$	W or Y	2		25	195		283		244	ns
			4.5		15	39		57		49	
			6		14	33		48		41	
t _t		W or Y	2		20	75		110		95	ns
			4.5		8	15		22		19	
			6		6	13		19		16	

5.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} (V)	$T_A = 25^\circ\text{C}$			SN54HC251		SN74HC251		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	W or Y	2		72	300		450		375	ns
			4.5		25	60		90		75	
			6		22	52		77		65	
	Any D	W or Y	2		59	300		450		375	
			4.5		21	60		90		75	
			6		18	52		77		65	
t_{en}	$\overline{OE}$	W or Y	2		50	230		340		285	ns
			4.5		17	46		68		57	
			6		15	40		58		50	
t_t		W or Y	2		45	210		315		265	ns
			4.5		17	42		63		53	
			6		13	36		53		45	

5.7 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	70	pF

6 Parameter Measurement Information

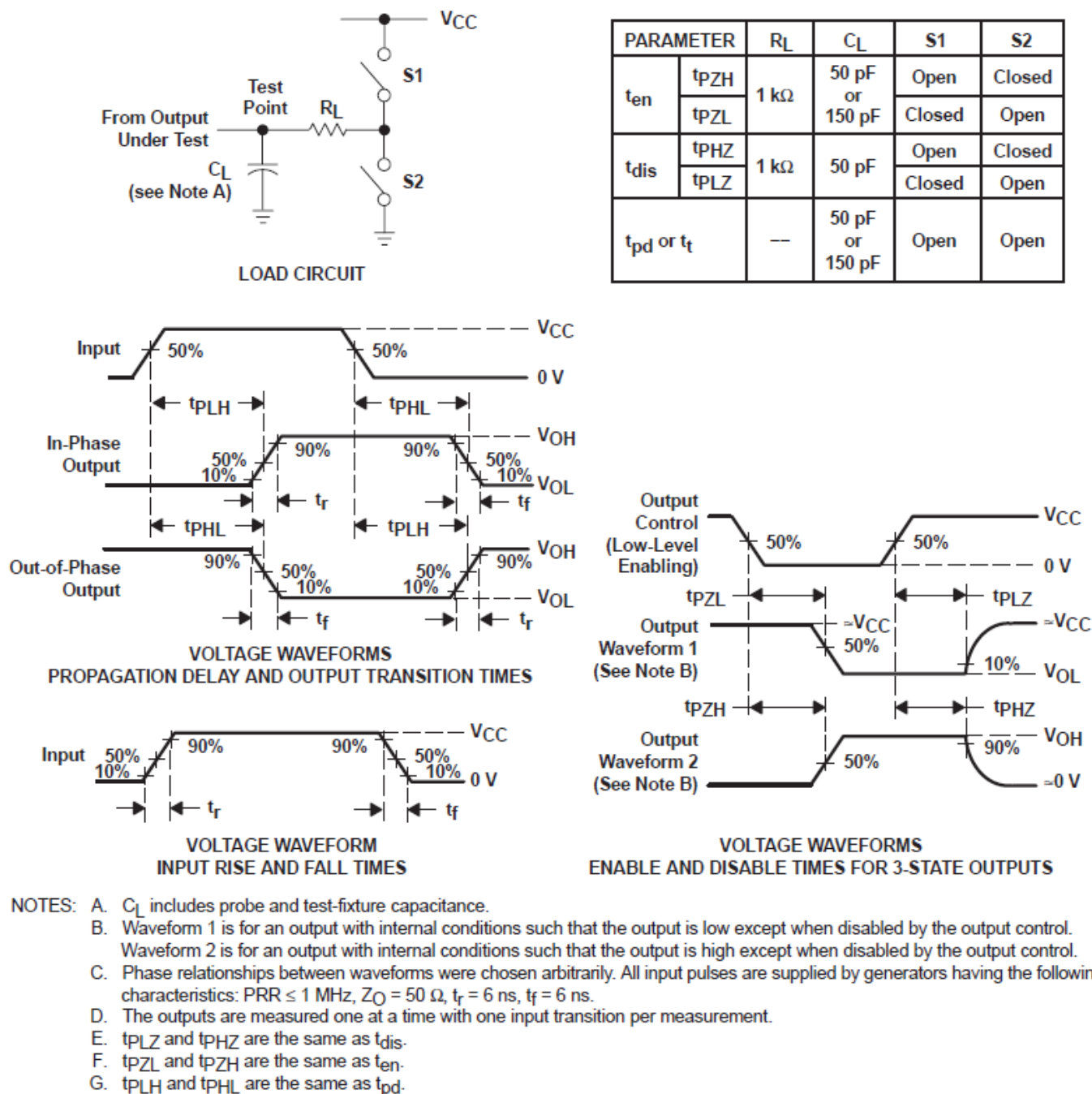


Figure 6-1. Load Circuit and Voltage Waveforms

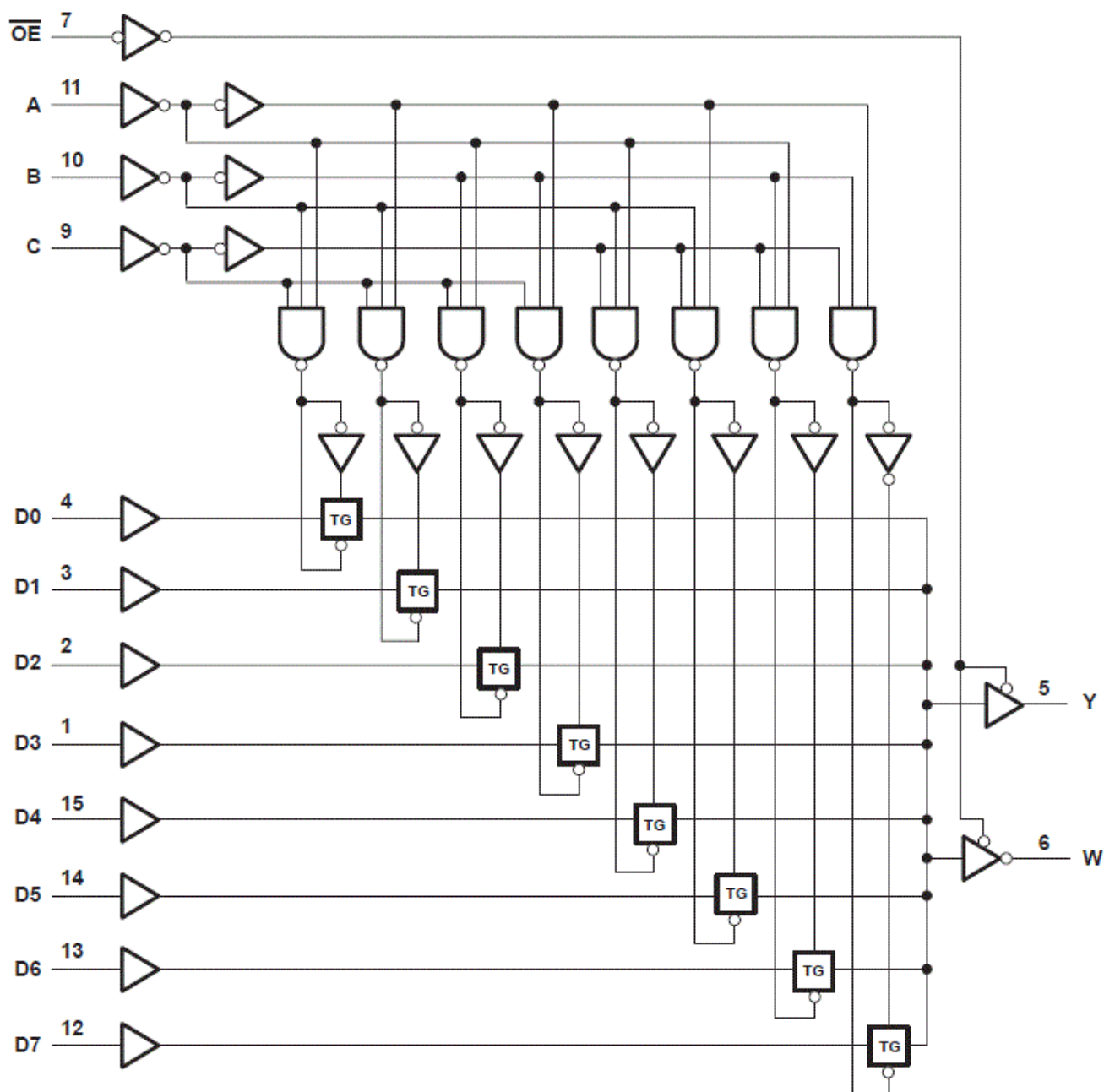
7 Detailed Description

7.1 Overview

These data selectors/multiplexers contain full binary decoding to select 1-of-8 data sources and feature strobe-controlled complementary 3-state outputs.

The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (in the high-impedance state), the low impedance of the single enabled output drives the bus line to a high or low logic level. Both outputs are controlled by the output-enable ($\overline{OE}$) input. The outputs are disabled when $\overline{OE}$ is high.

7.2 Functional Block Diagram



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

7.3 Device Functional Modes

Table 7-1. Function Table⁽¹⁾

INPUTS				OUTPUTS	
SELECT			$\overline{OE}$	Y	W
C	B	A			
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

(1) D0, D1 . . . D7 = the level of the respective D input.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
85125012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	85125012A SNJ54HC 251FK	Samples
8512501EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8512501EA SNJ54HC251J	Samples
SN54HC251J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC251J	Samples
SN74HC251DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC251	Samples
SN74HC251DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HC251	Samples
SN74HC251N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC251N	Samples
SN74HC251NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC251	Samples
SN74HC251PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HC251	Samples
SNJ54HC251FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	85125012A SNJ54HC 251FK	Samples
SNJ54HC251J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8512501EA SNJ54HC251J	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- ⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- ⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- ⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- ⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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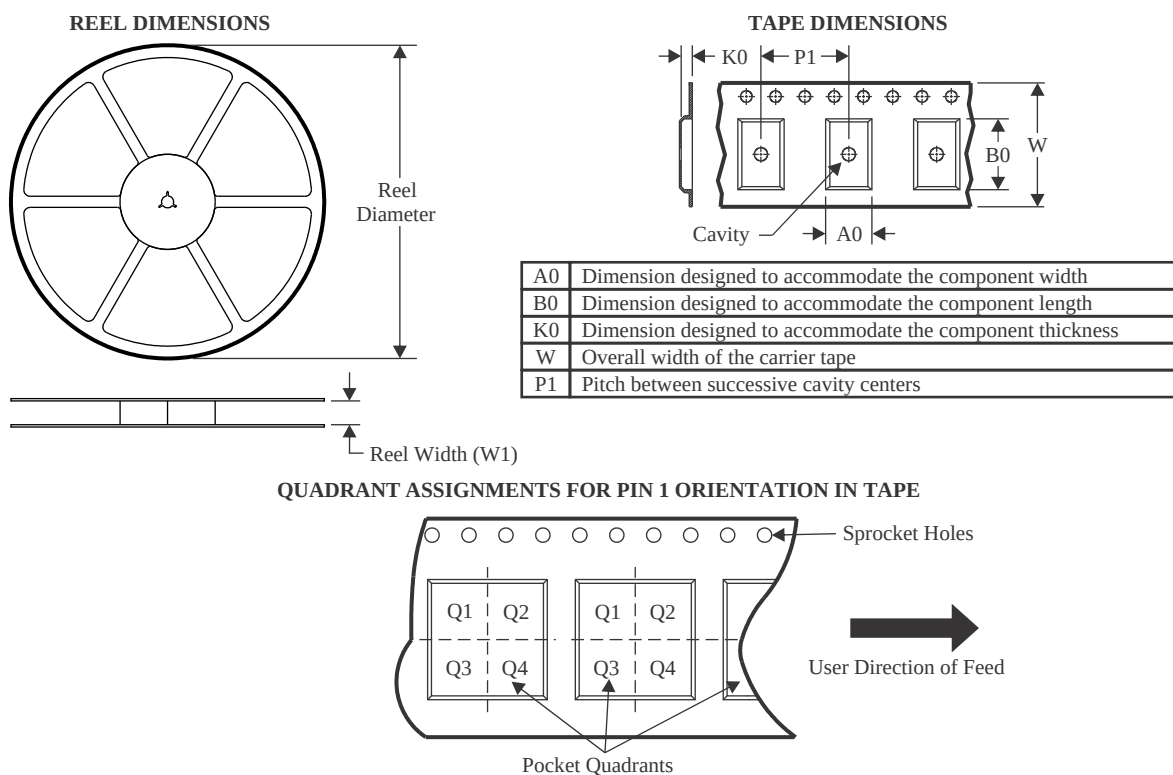
OTHER QUALIFIED VERSIONS OF SN54HC251, SN74HC251 :

- Catalog : [SN74HC251](#)
- Military : [SN54HC251](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

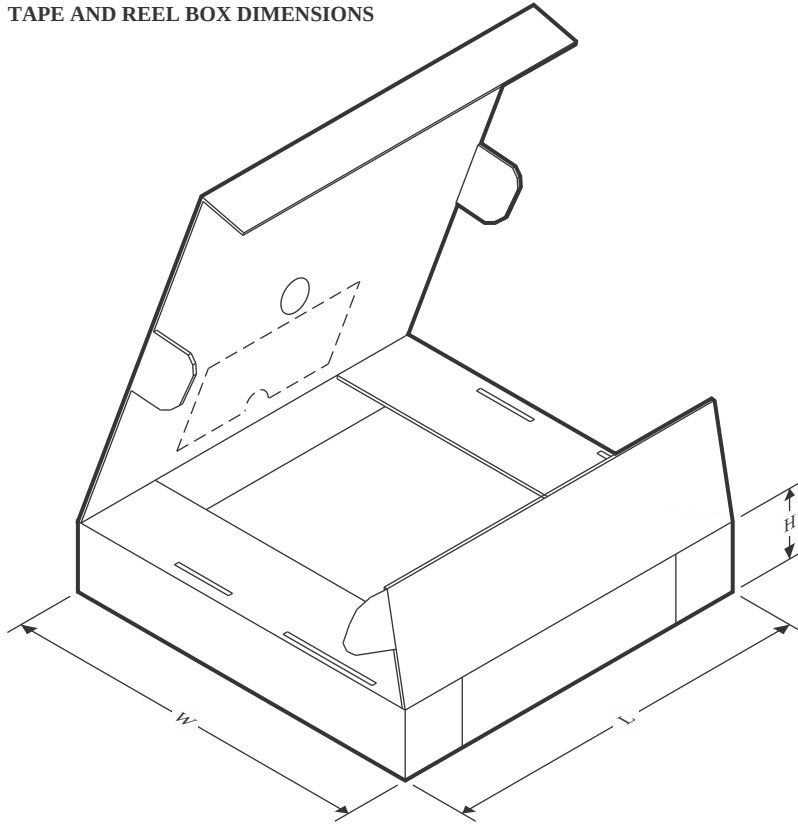
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC251DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HC251DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC251NSR	SO	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74HC251NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC251PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC251PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

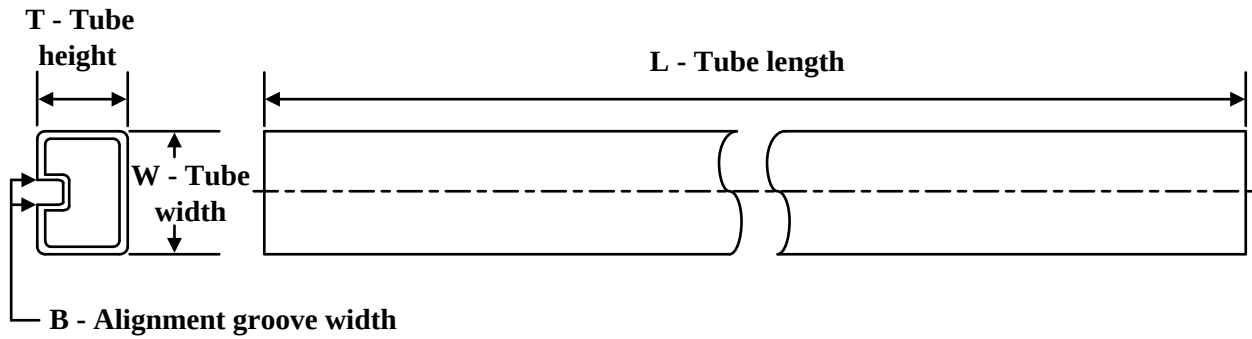
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC251DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74HC251DR	SOIC	D	16	2500	356.0	356.0	35.0
SN74HC251NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74HC251NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74HC251PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HC251PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE

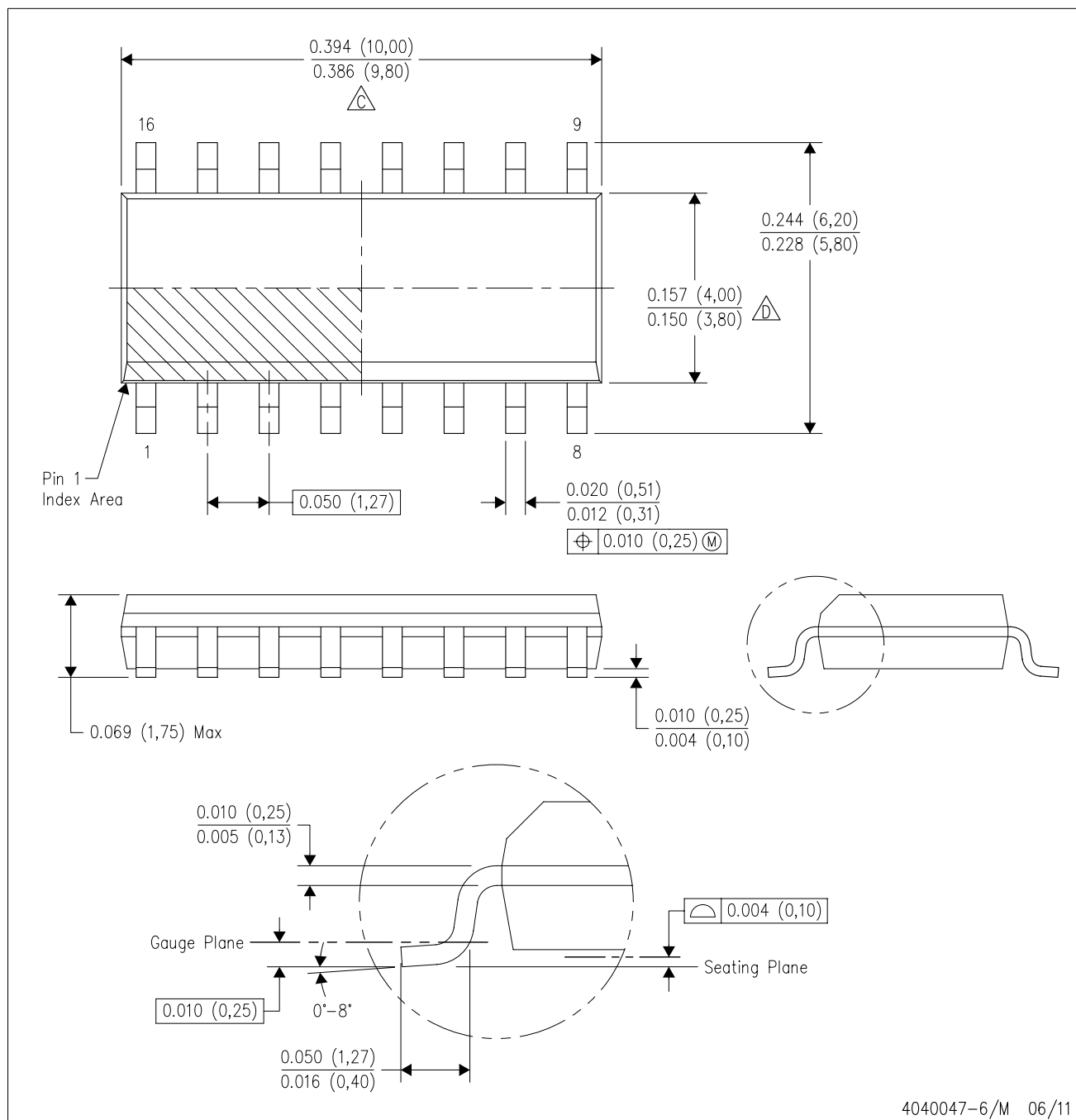


*All dimensions are nominal

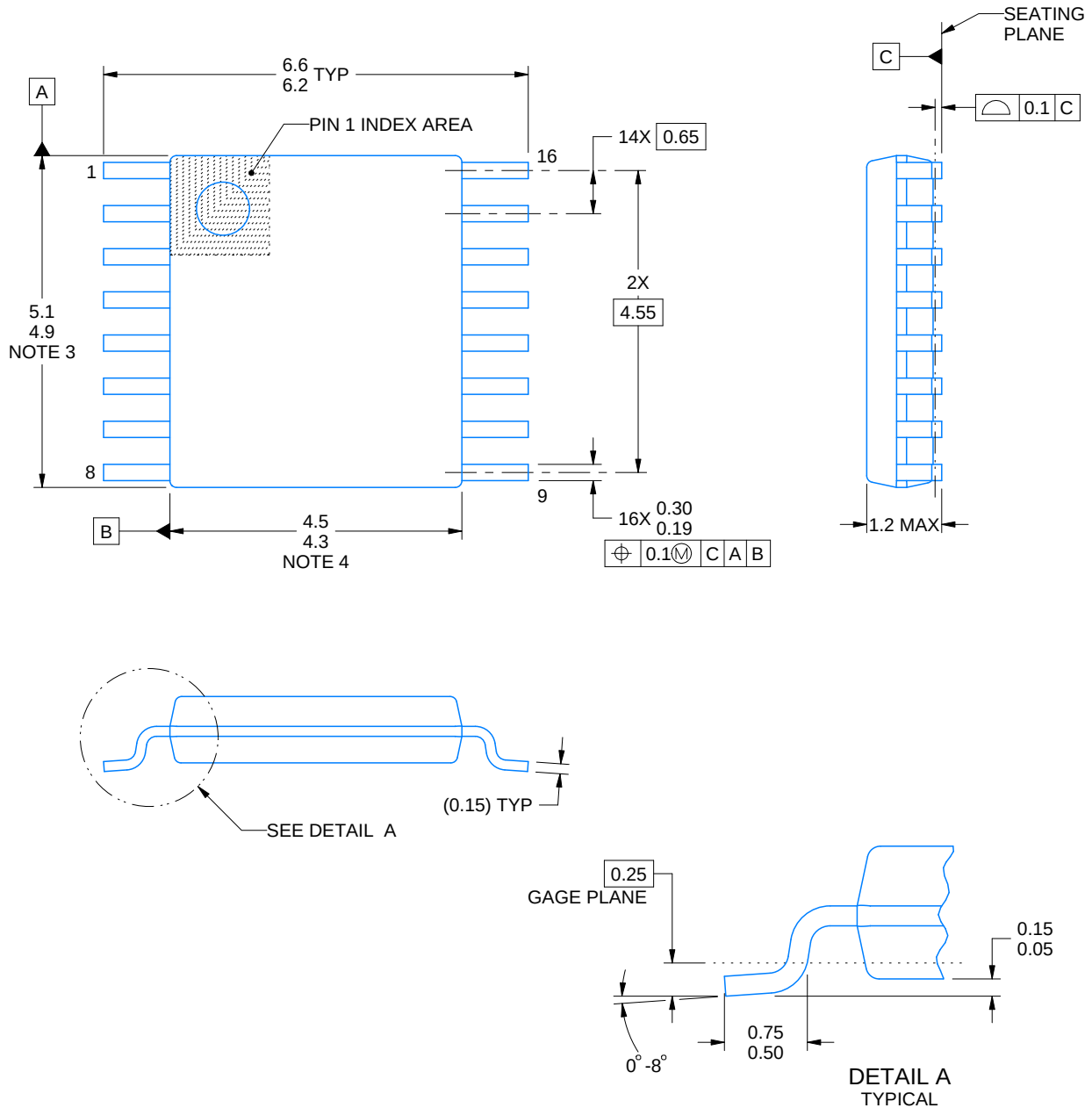
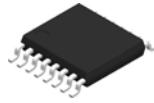
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
85125012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74HC251N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC251N	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC251FK	FK	LCCC	20	55	506.98	12.06	2030	NA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



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NOTES:

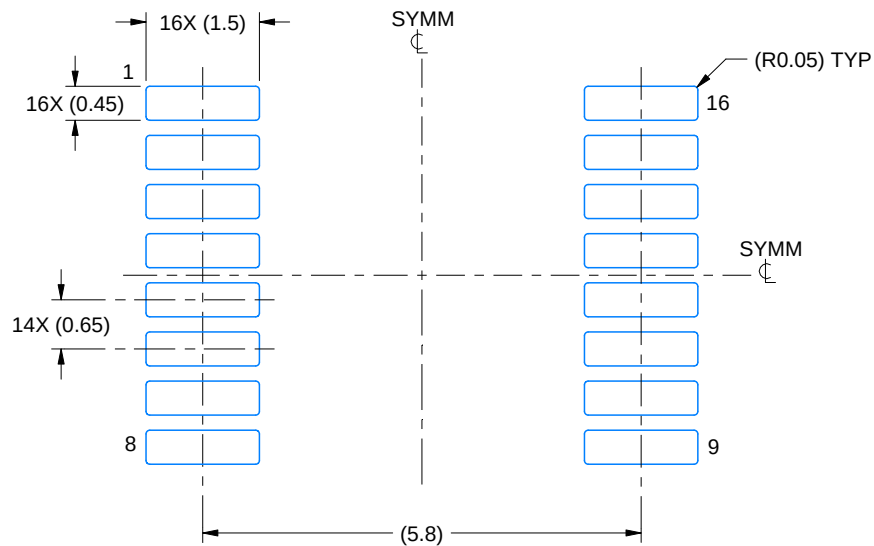
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

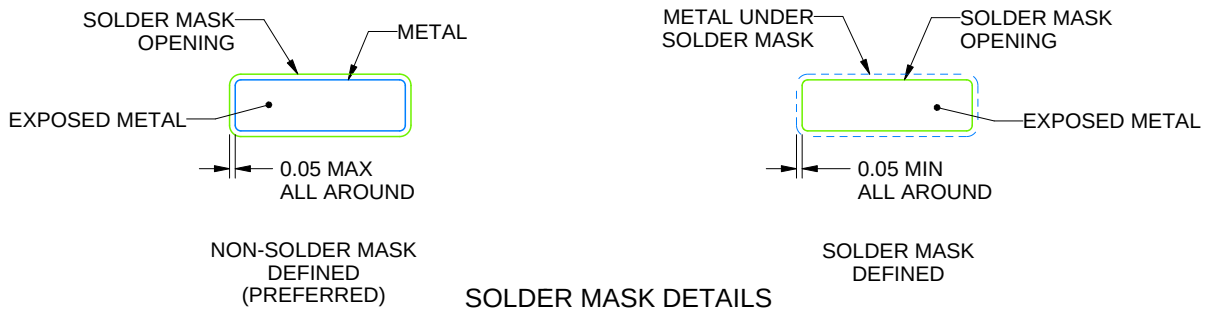
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

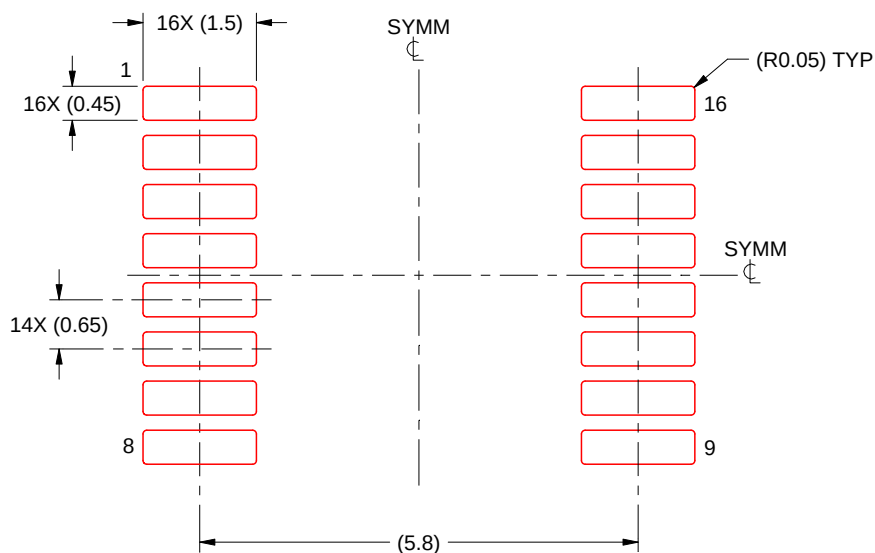
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

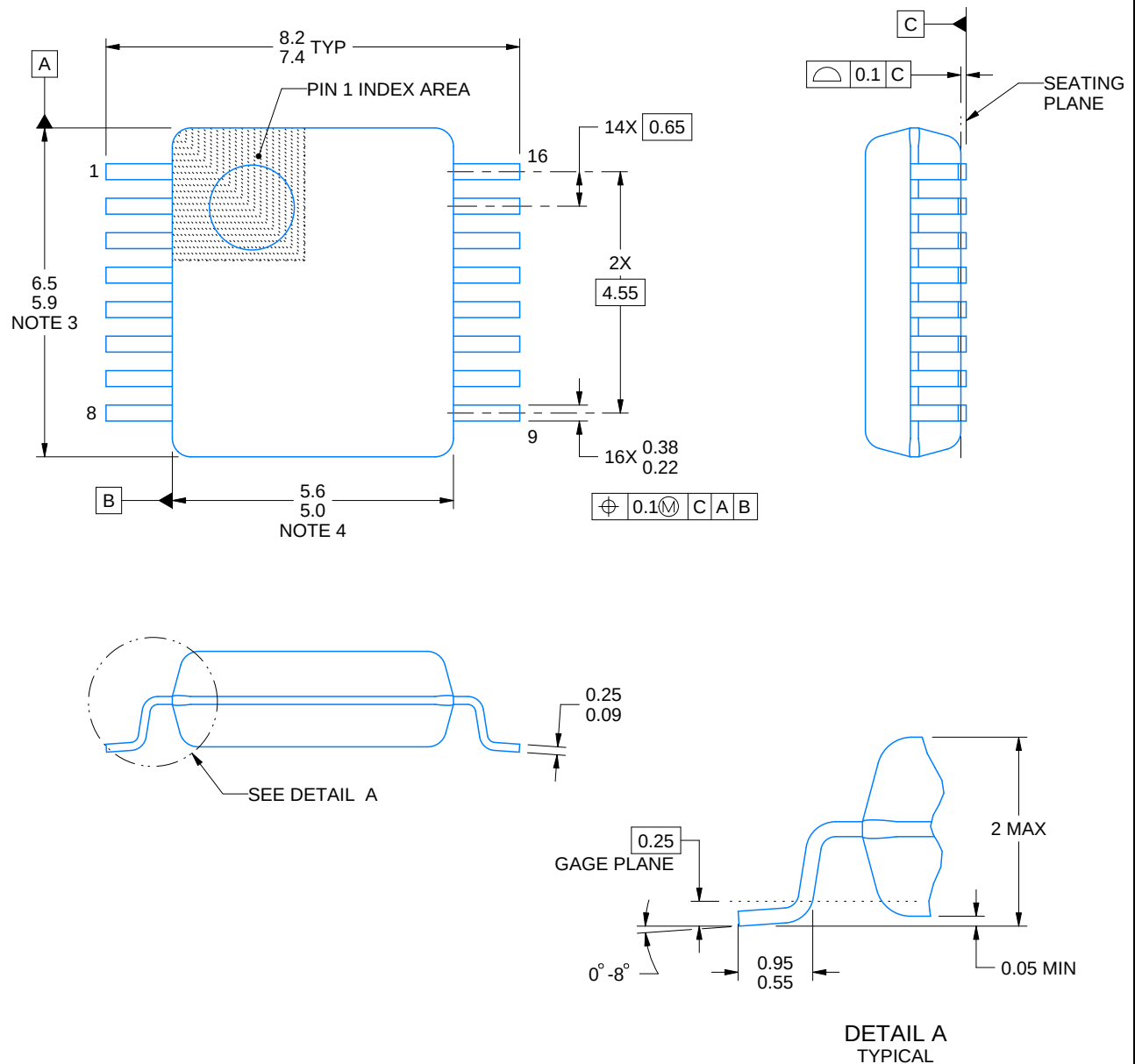


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220763/A 05/2022

NOTES:

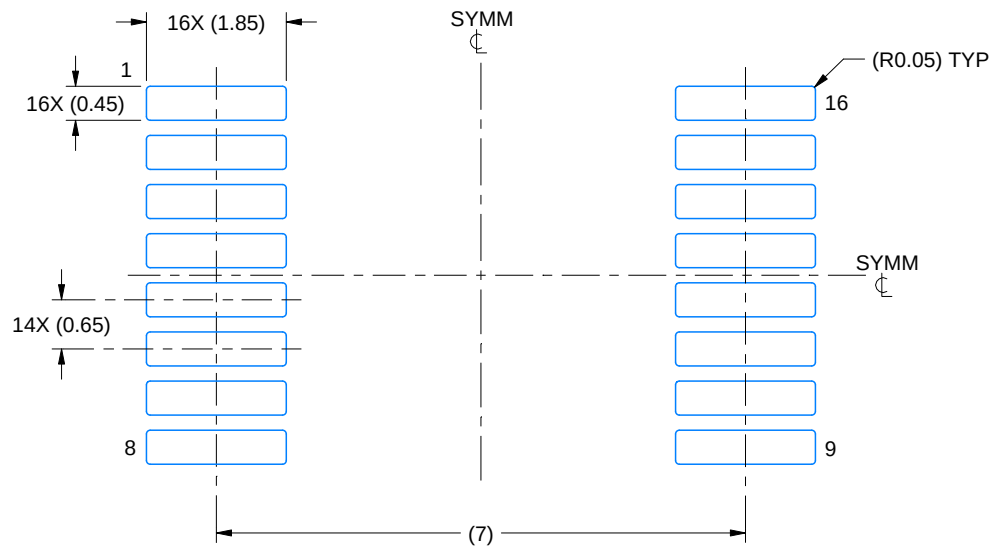
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

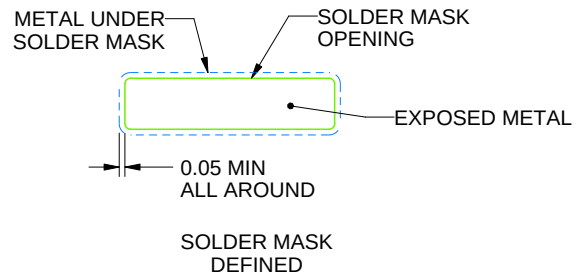
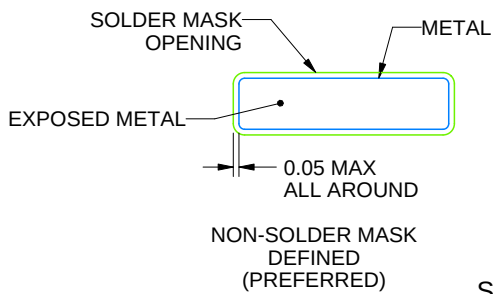
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

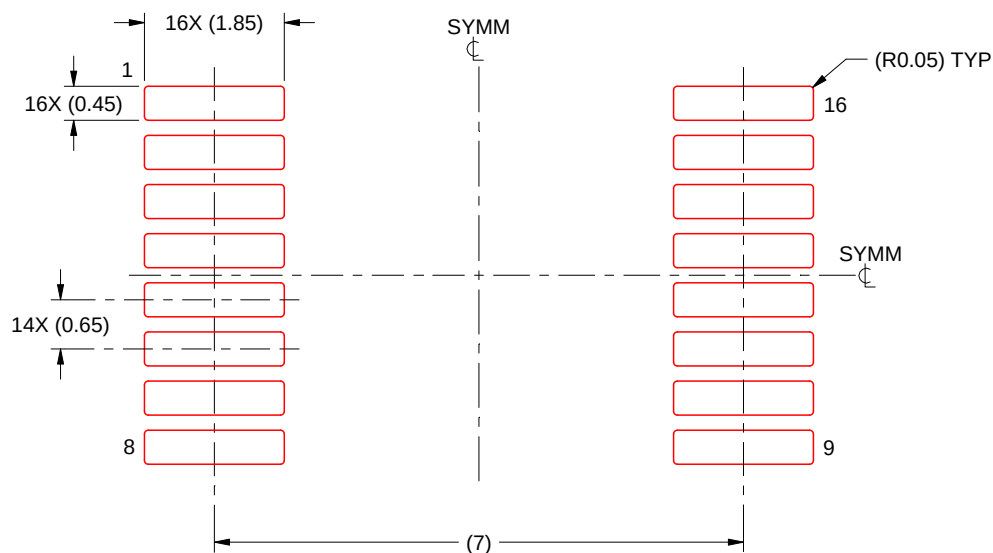
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

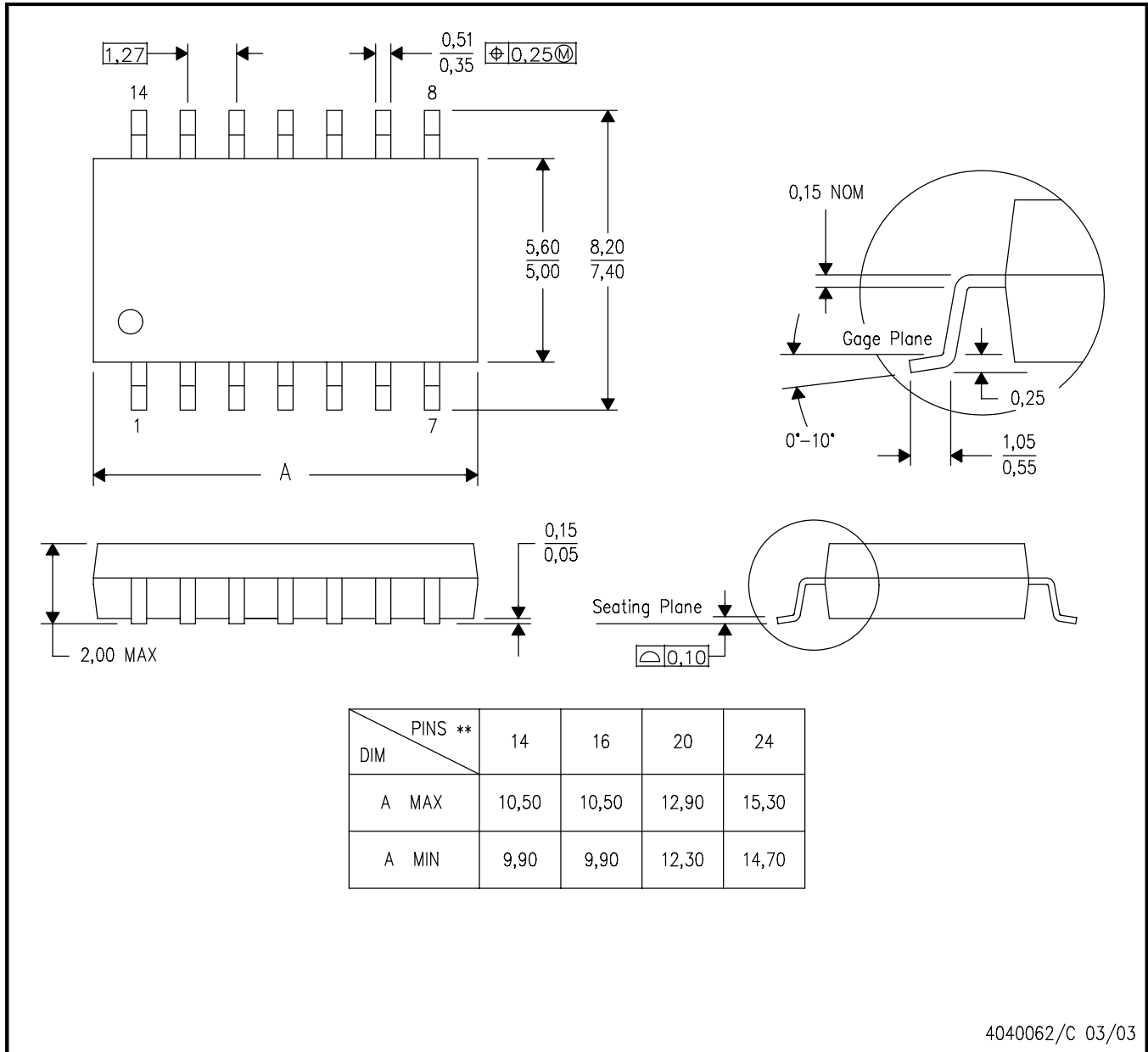
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

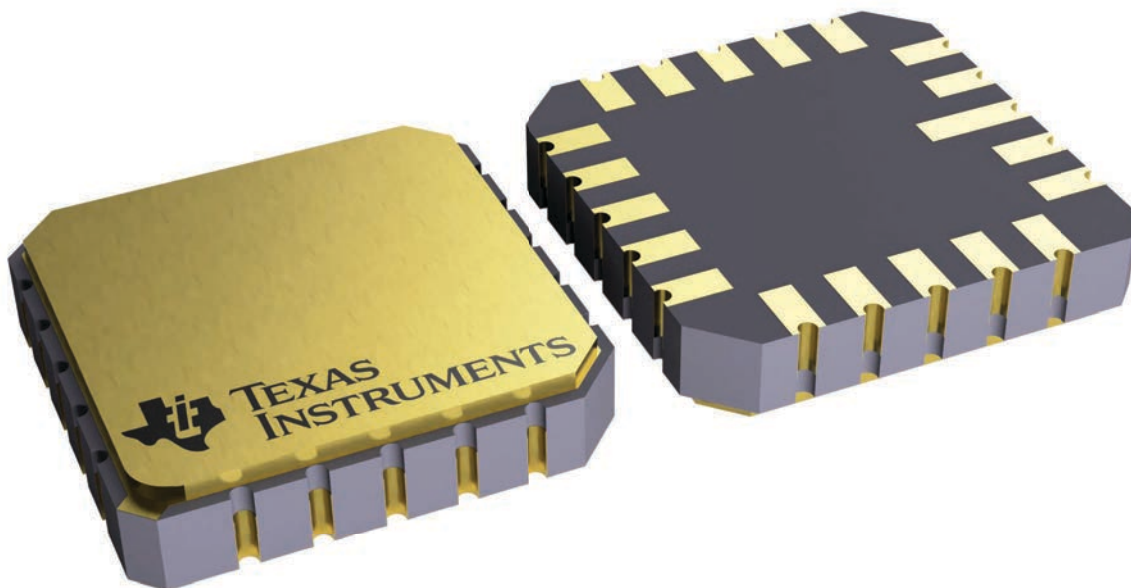
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

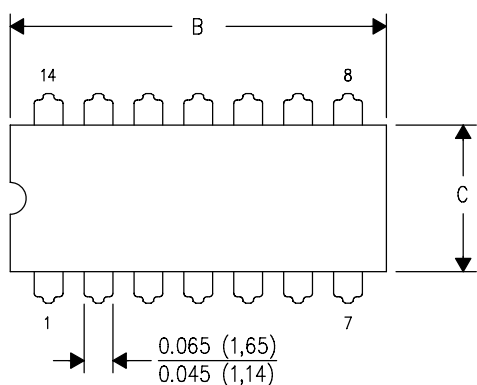


4229370VA\

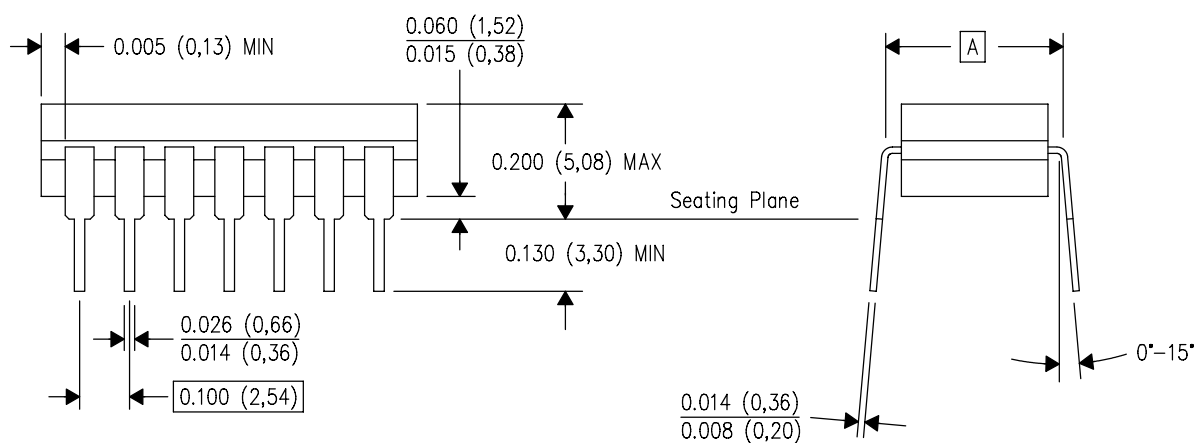
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



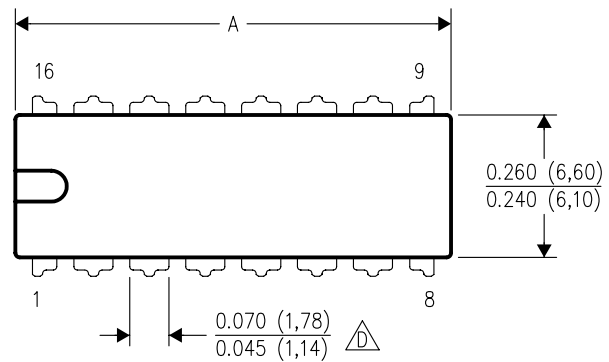
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

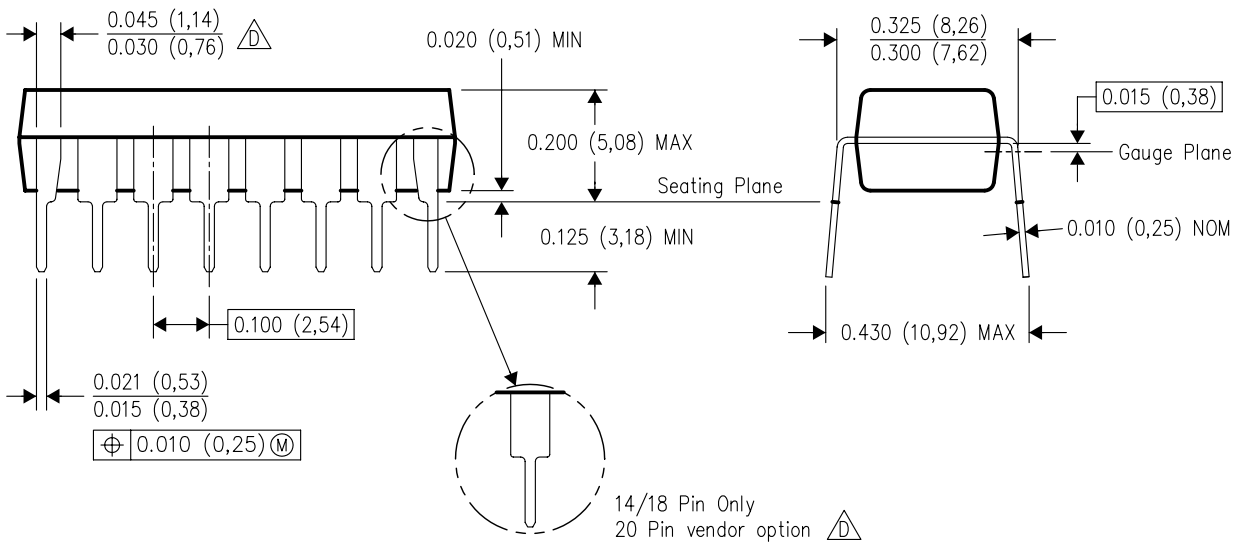
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

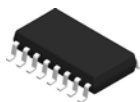


PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

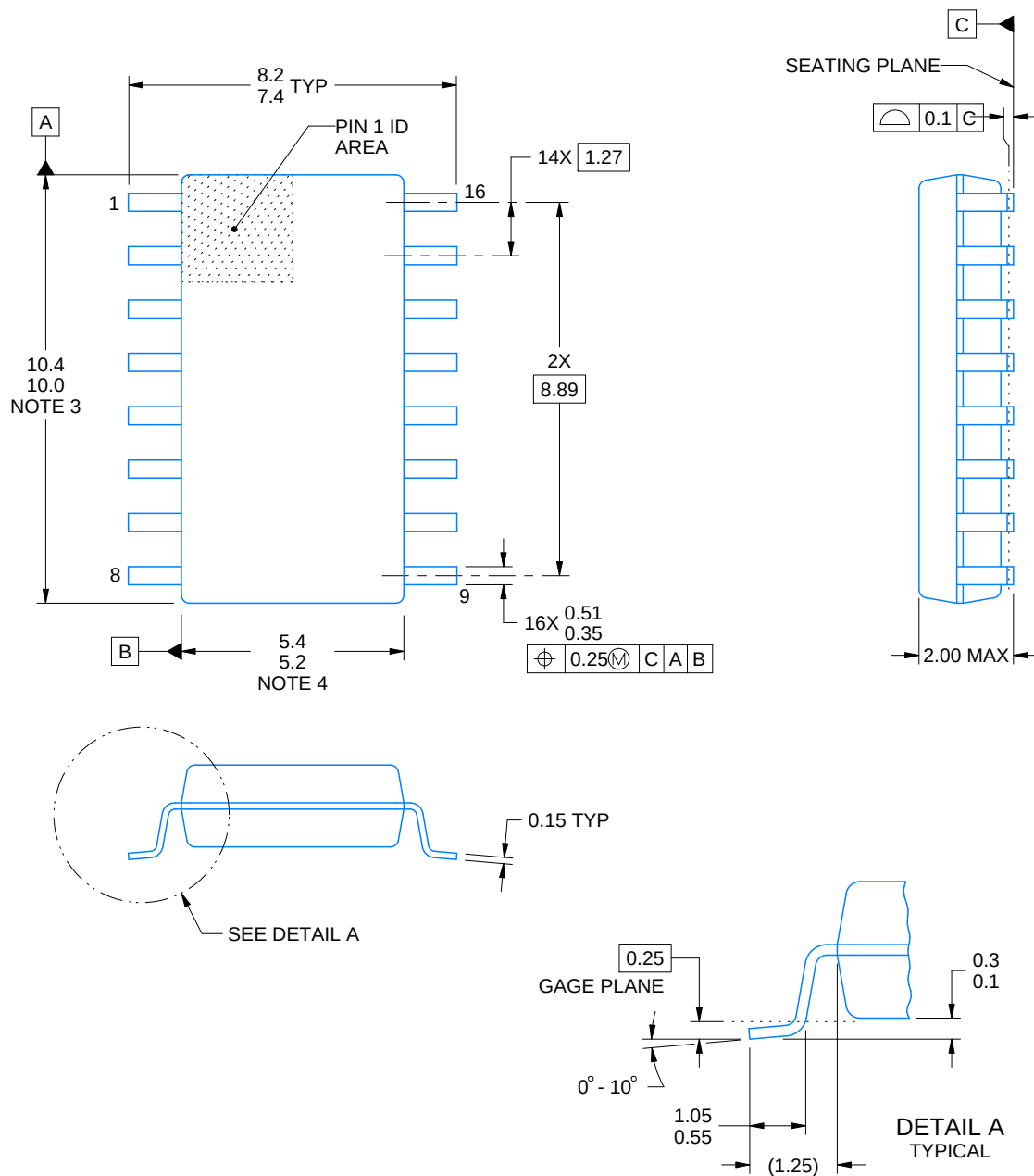


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

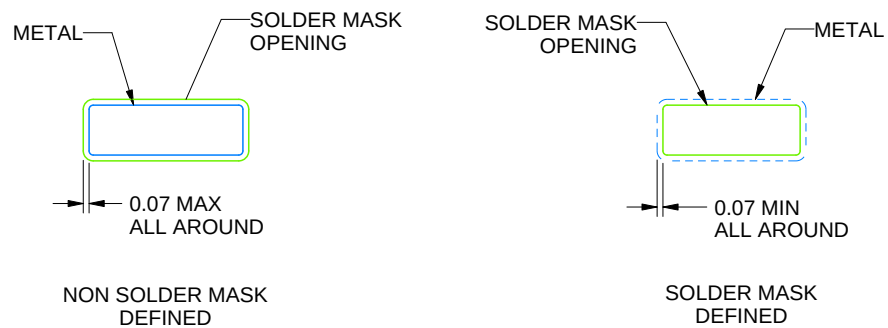
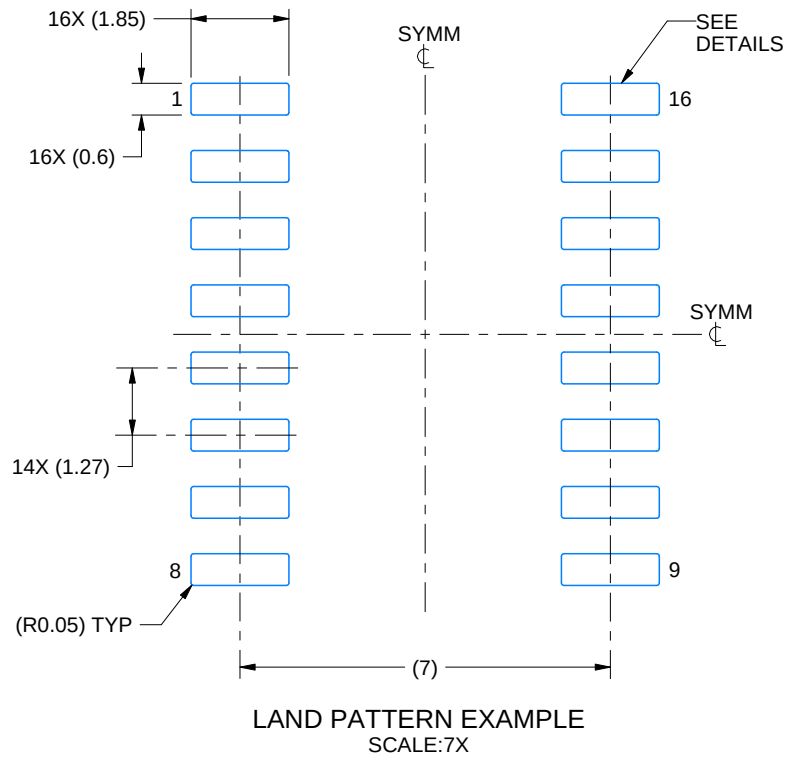
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

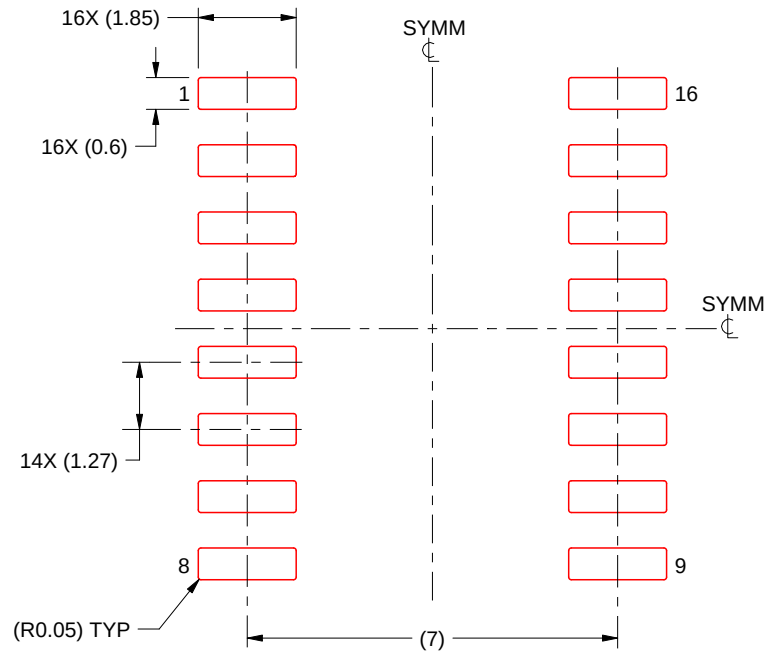
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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