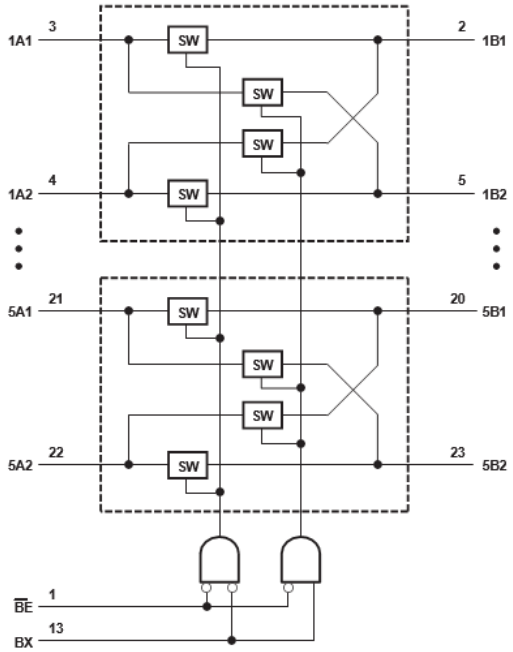
THE DATASHEET OF

SN74CBT3383CPWR

SN74CBT3383C 10-Bit FET Bus-Exchange Switch 5-V Bus Switch With −2-V Undershoot Protection

1 Features

- Undershoot protection for off-isolation on A and B ports up to −2 V
- Bidirectional data flow, with near-zero propagation delay
- Low on-state resistance (r_{on}) characteristics (r_{on} = 3 Ω typical)
- Low input output capacitance minimizes loading and signal distortion (Cio (OFF) = 8 pF typical)
- Data and control inputs provide undershoot clamp diodes
- Low power consumption (ICC = 3 µA maximum)
- V_{CC} operating range from 4 V to 5.5 V data I/Os support 0 to 5-V signaling levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, and 5-V)
- Control inputs can be driven by TTL or 5-V/3.3-V CMOS outputs
- Ioff supports partial-power-down mode operation
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance tested per JESD 22− 2000-V Human-Body Model (A114-B, Class II)− 1000-V Charged-Device Model (C101)
- Supports both digital and analog applications: PCI interface, memory interleaving, bus isolation, low-distortion signal gating



Logic Diagram (Positive Logic)

2 Applications

- Enterprise servers
- Ethernet switches
- Routers
- Servers
- Industrial PCs

3 Description

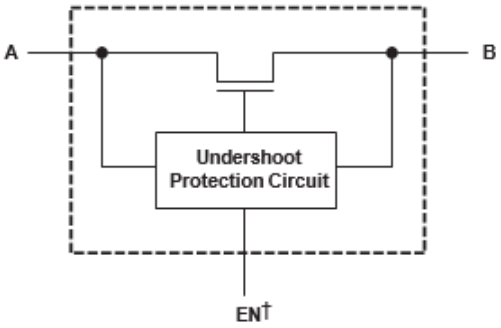
The SN74CBT3383C is a high-speed TTL-compatible FET bus-exchange switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3383C provides protection for undershoot up to −2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3383C is organized as a 10-bit bus switch, or as a 5-bit bus-exchange switch with a single output-enable ($\overline{BE}$) input that provides data exchanging between four signal ports. The select (BX) input controls the data path of the bus-exchange switch. When $\overline{BE}$ is low, the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{BE}$ is high, a high-impedance state exists between the A and B ports.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN74CBT3383C	DBQ (SSOP, 24)	8.65 mm × 3.90 mm
	DW (SOIC, 24)	15.40 mm × 7.50 mm
	PW (TSSOP, 24)	7.80 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic, Each FET Switch (SW)

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2004) to Revision A (December 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added the *Applications*, *Pin Configuration and Functions*, *ESD Ratings*, *Thermal Information*, *Detailed Description*, *Application and Implementation*, *Power Supply Recommendation*, and *Layout* sections	1
• Removed the *DGV* and *DB* package information from the data sheet due to (RLOI)	1
• Updated the *Design Requirements* section	11

5 Description (continued)

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{BE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

6 Pin Configuration and Functions

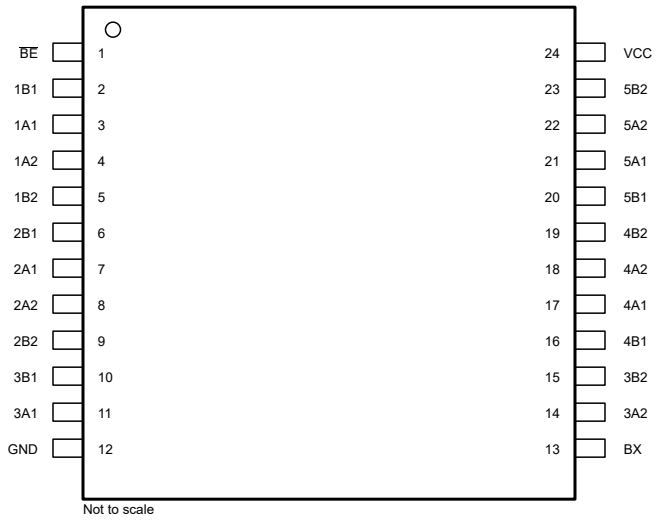


Figure 6-1. DBQ, DW, or PW Package, 24-Pin SSOP, SOIC, and TSSOP (Top View)

Table 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
$\overline{BE}$	1	I	Active-low input enable pin
1B1	2	I/O	I/O pin, can be input or output
1A1	3	I/O	I/O pin, can be input or output
1A2	4	I/O	I/O pin, can be input or output
1B2	5	I/O	I/O pin, can be input or output
2B1	6	I/O	I/O pin, can be input or output
2A1	7	I/O	I/O pin, can be input or output
2A2	8	I/O	I/O pin, can be input or output
2B2	9	I/O	I/O pin, can be input or output
3B1	10	I/O	I/O pin, can be input or output
3A1	11	I/O	I/O pin, can be input or output
GND	12	G	Ground
BX	13	I	Select pin. This controls the data path of the bus exchange. When BX is low xA1 = xB1 and xA2 port = xB2. When BX is high xA1 = xB2 and xA2 = xB1
3A2	14	I/O	I/O pin, can be input or output
3B2	15	I/O	I/O pin, can be input or output
4B1	16	I/O	I/O pin, can be input or output
4A1	17	I/O	I/O pin, can be input or output
4A2	18	I/O	I/O pin, can be input or output
4B2	19	I/O	I/O pin, can be input or output
5B1	20	I/O	I/O pin, can be input or output
5A1	21	I/O	I/O pin, can be input or output
5A2	22	I/O	I/O pin, can be input or output
5B2	23	I/O	I/O pin, can be input or output
V_{CC}	24	P	Power pin

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3) (4) (5) (6)

		MIN	MAX	UNIT
Supply voltage range, V_{CC}		−0.5	7	V
Control input voltage range, V_{IN} (see notes 1 and 2)		−0.5	7	V
Switch I/O voltage range, $V_{I/O}$ (see notes 1, 2, and 3)		−0.5	7	V
Control input clamp current, I_{IK} (V_{IN} < 0)		−50		mA
I/O port clamp current, $I_{I/OK}$($V_{I/O}$ < 0)		−50		mA
ON-state switch current, $I_{I/O}$(see note 4)		128		mA
Continuous current through V_{CC} or GND terminals		100		mA
Package thermal impedance, θ_{JA} (see note 5):				
	DBQ package	61		°C /W
	DW package	46		°C /W
	PW package	88		°C /W
T_{stg}	Storage temperature	−65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal GND.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4	5.5	V
V_{IH}	High-level control input voltage	2	5.5	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	5.5	V
T_A	Operating free-air temperature	−40	85	°C

(1) All unused control input of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

7.4 Thermal Information

THERMAL METRIC[1]		SN74CBT3383			UNIT
		DBQ (SSOP)	DW (SOIC)	PW (TSSOP)	
		24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.0	46.0	88.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.1	19.9	26.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	—	19.33	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS			MIN	TYP[2]	MAX	UNIT
V_{IK}	Control inputs	V_{CC}= 4.5 V,	I_{IN}= −18 mA				−1.8	V
V_{IKU}	Data inputs	V_{CC}= 5 V,	0 mA > I_I≥ −50 mA, V_{IN}= V_{CC} or GND,	Switch OFF			−2	V
I_{IN}	Control inputs	V_{CC}= 5.5 V,	V_{IN}= V_{CC} or GND				±1	mA
IOZ‡[3]		V_{CC}= 5.5 V,	V_O= 0 to 5.5 V, V_I= 0,	Switch OFF, VIN= VCC or GND			±10	mA
I_{off}		V_{CC}= 0,	V_O= 0 to 5.5 V,	VI= 0			10	mA
I_{CC}		V_{CC}= 5.5 V,	$I_{I/O}$= 0, V_{IN}= V_{CC} or GND,	Switch ON or OFF			3	mA
ΔI_{CC} [4]	Control inputs	V_{CC}= 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	V_{IN}= 3 V or 0				3.5		pF
C_{io}(OFF)		$V_{I/O}$= 3 V or 0,	Switch OFF,	V_{IN}= V_{CC} or GND		8		pF
C_{io}(ON)		$V_{I/O}$= 3 V or 0,	Switch ON,	V_{IN}= V_{CC} or GND		18.5		pF
r_{on} [5]		V_{CC}= 4 V, TYP at V_{CC}= 4 V	V_I= 2.4 V,	I_O= −15 mA		8	12	Ω
		V_{CC}= 4.5 V	VI= 0	I_O= 64 mA		3	6	
				I_O= 30 mA		3	6	
			V_I= 2.4 V,	I_O= −15 mA		5	10	

(1) V_{IN} and I_{IN} erfer to control inptus. V_I, V_O, I_I, and I_O refer to data pins.
(2) All the typical values are at V_{CC} = 5 V (unless otherwise noted), T_A=25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. The lower of the voltages of the two (A or B) terminals determines the ON-state resistance.

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC= 4 V		VCC= 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd} (1)	A or B	B or A		0.24		0.15	ns
$t_{pd(s)}$	BX	A or B		5.8	1	5.3	ns
t_{en}	$\overline{BE}$	A or B		6.3	1	5.8	ns
t_{dis}	$\overline{BE}$	A or B		6	1	6	ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

7.7 Undershoot Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{OUTU}	V_{CC} = 5.5 V,	Switch OFF,	V_{IN} = V_{CC} or GND	2	V_{OH}− 0.3		V

(1) All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25 °C.

8 Parameter Measurement Information

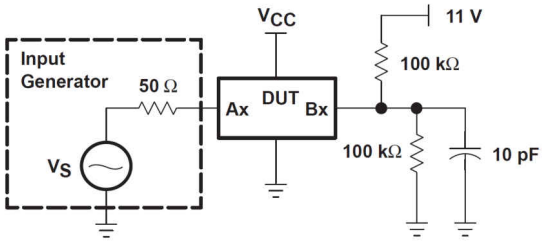


Figure 8-1. Device Test Setup

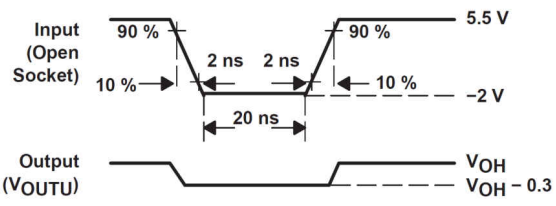
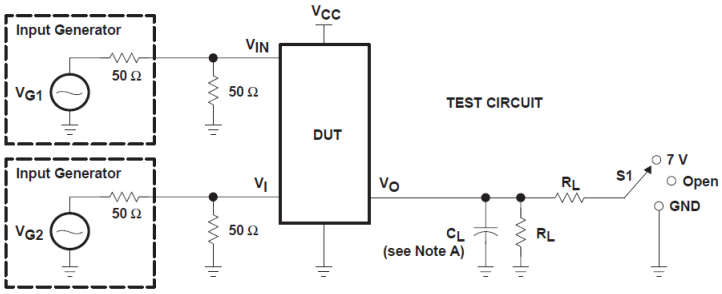
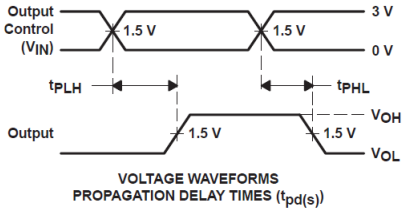
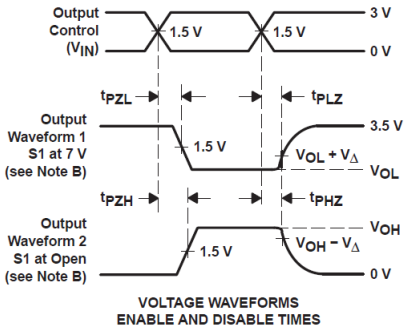


Figure 8-2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	50 pF 50 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V_{CC} V_{CC}	50 pF 50 pF	0.3 V 0.3 V





A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as one or more t_{pds}. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 8-3. Test Circuit and Voltage Waveforms

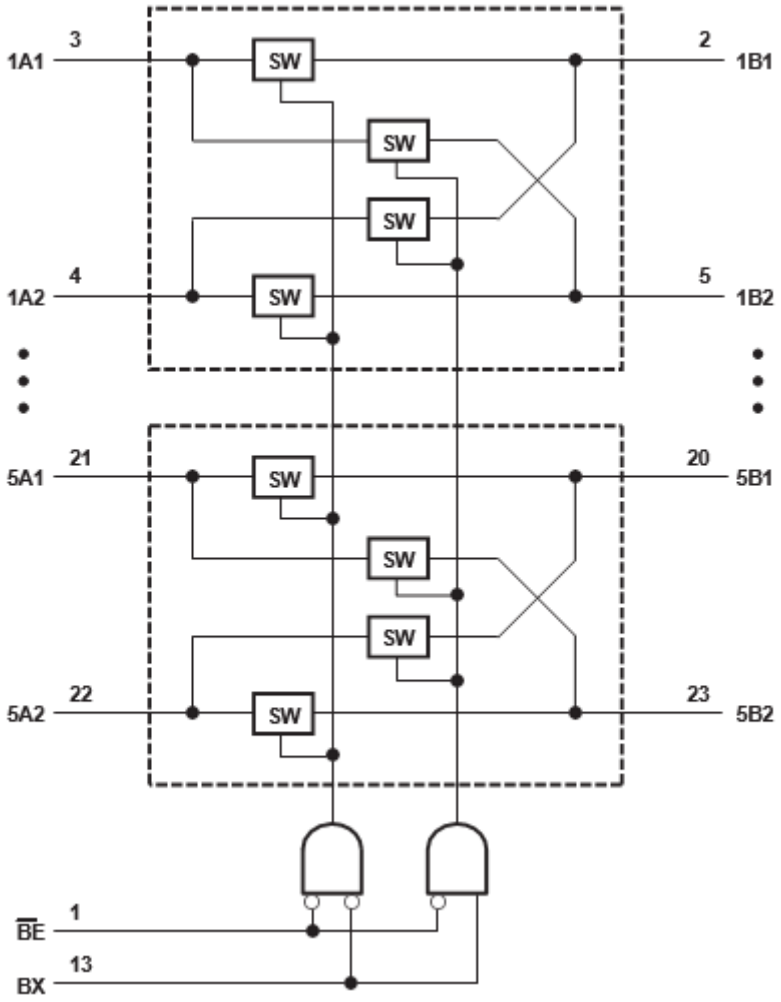
9 Detailed Description

9.1 Overview

The SN74CBT3383C provides ten high-speed CMOS TTL-compatible bus switches. The low ON-resistance of the SN74CBT3383C allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The Bus Enable ($\overline{BE}$) signal turns the switches on. The Bus Exchange (BX) signal provides nibble swap of the 1A and 1B pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a 5-wide, 2-to-1 multiplexer, to create low delay barrel shifters, and so forth.

Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3383C provides protection for undershoot up to −2 V by sensing and undershoot event and ensuring that the switch remains in the proper OFF state.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Bidirectional Data Flow With Near-Zero Propagation Delay

The SN74CBT3383C features a low propagation delay or t_{pd} that works great for multiple rail information transfer (for example, from 1A1 to 1B1 and 1A2 to 1B2). However, the SN74CBT3383C also features BUS exchange functionality, which allows for bidirectional data transfers from the inputs and outputs connected on the B side. By enabling the BX pin, the outputs are now crossed or exchanged. Data can now flow from 1A1 to 1B2 and 1A2 to 1B1 with little to no propagation delay. This can be used to enable byte swapping of buses within a system or to create a 5-wide, 2-to-1 multiplexer.

9.4 Device Functional Modes

Table 9-1. Function Table
(Each 5-Bit Bus-Exchange)

INPUTS		INPUTS/OUTPUTS		FUNCTION
$\overline{BE}$	BX	1A1 – 5A1	1A2 – 5A2	
L	L	1B1 – 5B1	1B2 – 5B2	A1 port = B1 port, A2 port = B2 port
L	H	1B2 – 5B2	1B1 – 5B1	A1 port = B2 port, A2 port = B1 port
H	X	Z	Z	Disconnect

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The SN74CBT3383C can be used to multiplex up to 5 channels simultaneously in a 2:1 configuration. Figure 10-1 shows a 2-bit bus being multiplexed between two devices. The $\overline{BE}$ and BX pins are used to control the chip from the bus controller. This is a very generic example, and could apply to many situations. If an application requires only one bit control or exchange, then remember to tie the unused bit to high or low. By using another bus controller, exchange can be enabled across A1 and A2 to B1 and B2, allowing for greater system communication.

10.2 Typical Application

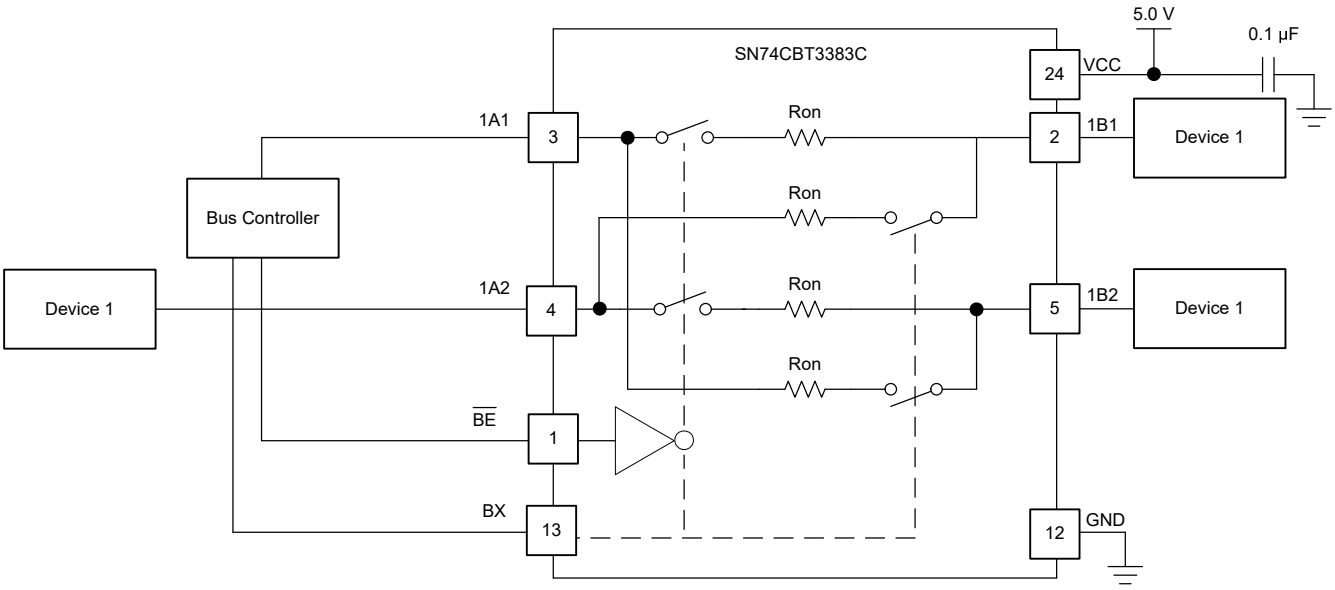


Figure 10-1. 1:2 Multiplexer or Bus and Selector Using 1 Bus Controller

10.2.1 Design Requirements

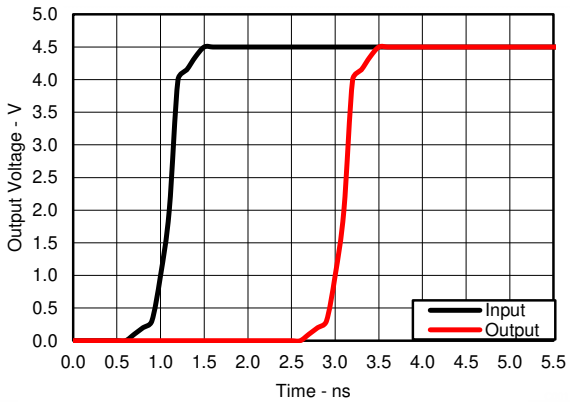
1. Recommended input conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* section.
2. Recommended output conditions:
   - Load currents must not exceed 128 mA per channel.
3. Frequency selection criteria:
   - Added trace resistance and capacitance can reduce maximum frequency capability; use layout practices as directed in the *Layout* section.

10.2.2 Detailed Design Procedure

The 2-bit bus is connected directly to 1A1 and 1A2 on the SN74CBT3383C, which essentially combines in the bus controller to form a single input or split bus bits. When $\overline{BE}$ is low and BX is low, the selected bus uses 1A1 and 1B1 as inputs and outputs. This means that Device 1 is connected to the bus controller and Device 2 is connected to Device 3 when $\overline{BE}$ is low and BX is low. While keeping $\overline{BE}$ low and BX high, communication is enabled from the bus controller to Device 2 and from Device 1 to Device 3. This setup is especially useful when two controllers or devices need to share the same data from Device 1 and Device 2 and the bus addresses are limited or hard coded.

The 0.1-µF capacitor on V_{CC} is a decoupling capacitor and should be placed as close to the device as possible.

10.2.3 Application Curve



V_{CC} = 4.5 V

Figure 10-2. Propagation Delay (t_{pd}) Simulation Results

11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions* table. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

12 Layout

12.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of the trace width. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 12-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

12.2 Layout Example

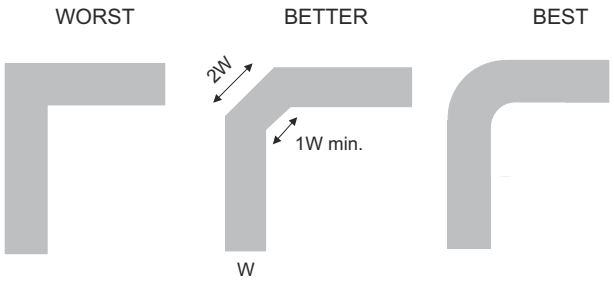


Figure 12-1. Trace Example

13 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBT3383CDBQR	ACTIVE	SSOP	DBQ	24	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CBT3383C	Samples
SN74CBT3383CDW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3383C	Samples
SN74CBT3383CDWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3383C	Samples
SN74CBT3383CPWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU383C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

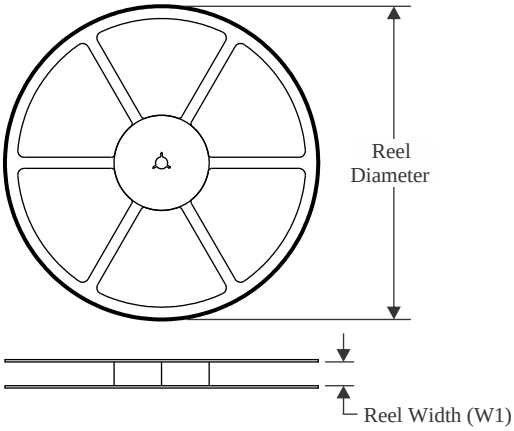
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

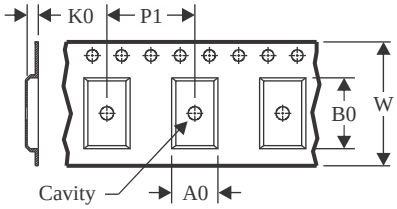
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

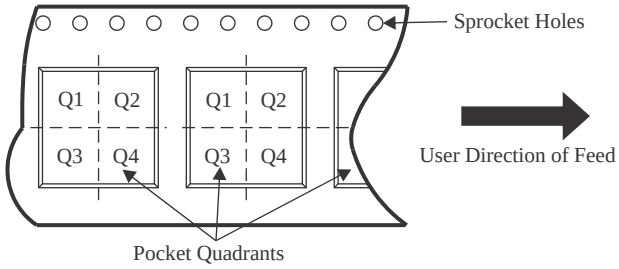


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

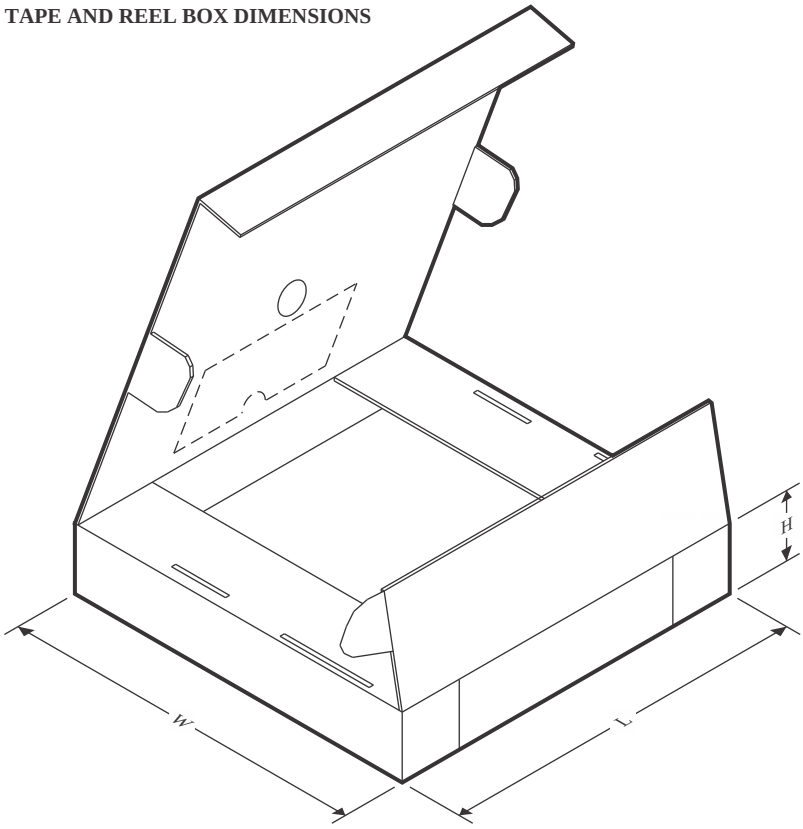
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT3383CDBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CBT3383CDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74CBT3383CPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

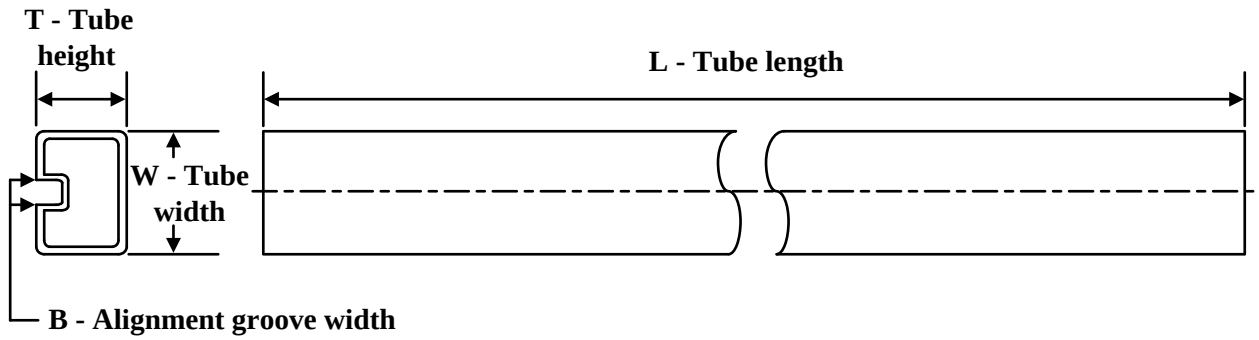
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT3383CDBQR	SSOP	DBQ	24	2500	356.0	356.0	35.0
SN74CBT3383CDWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74CBT3383CPWR	TSSOP	PW	24	2000	367.0	367.0	38.0

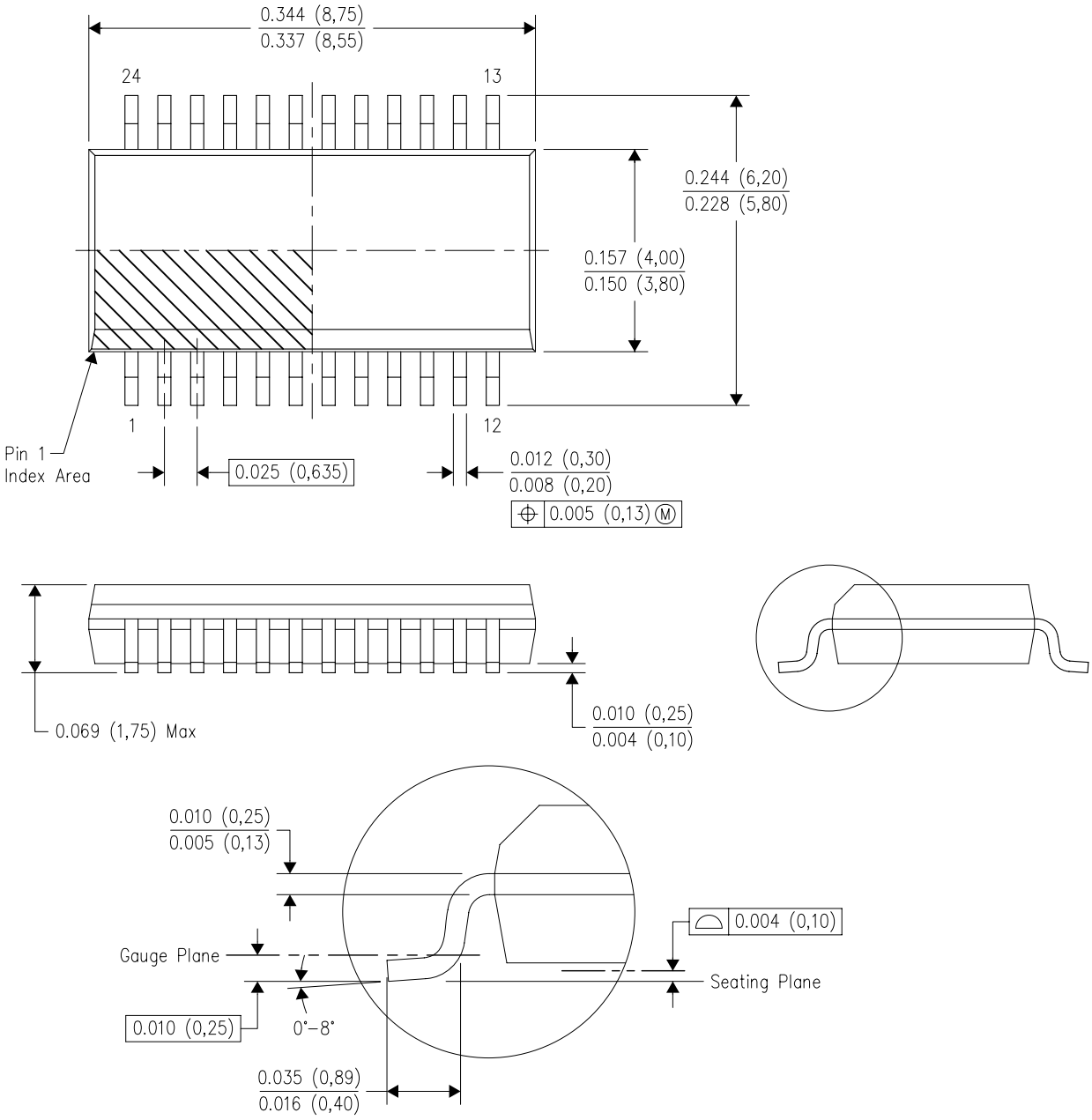
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CBT3383CDW	DW	SOIC	24	25	506.98	12.7	4826	6.6

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



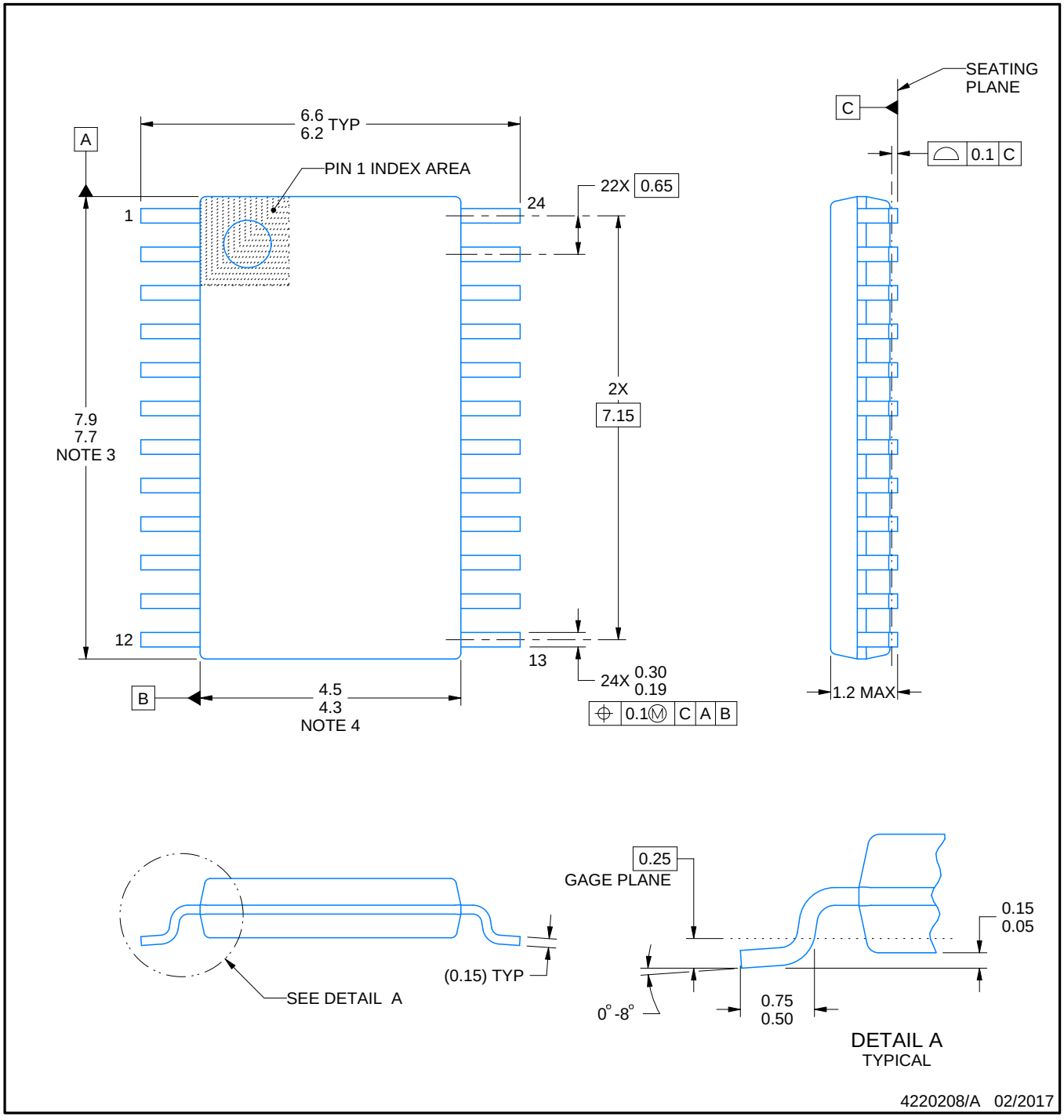
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

PACKAGE OUTLINE

PW0024A

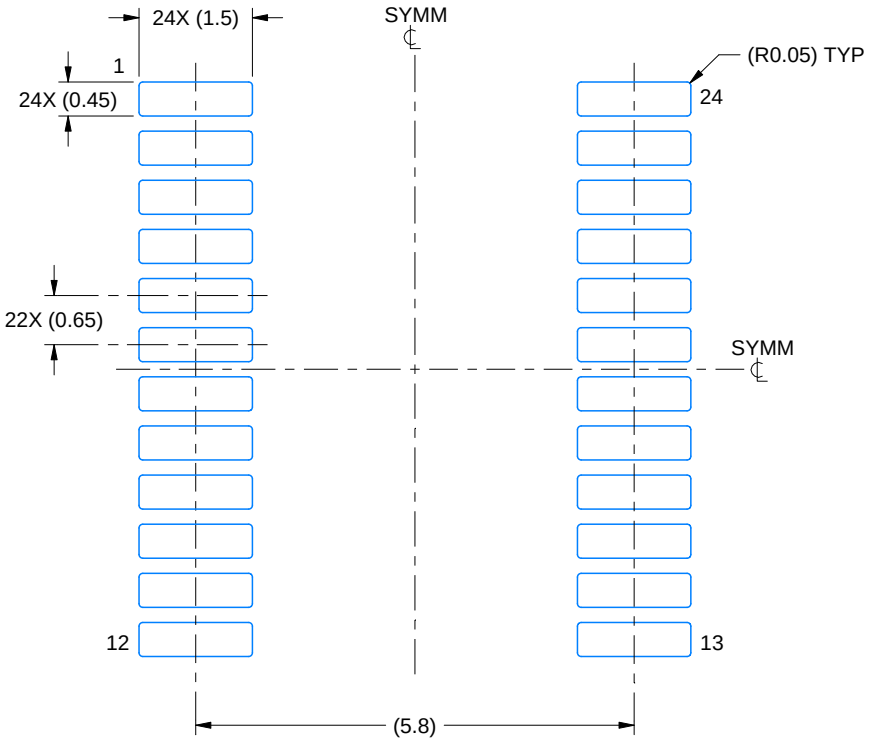
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

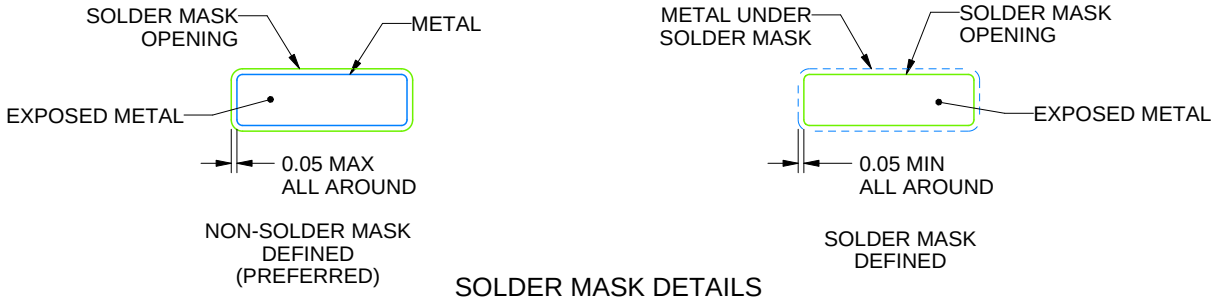


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

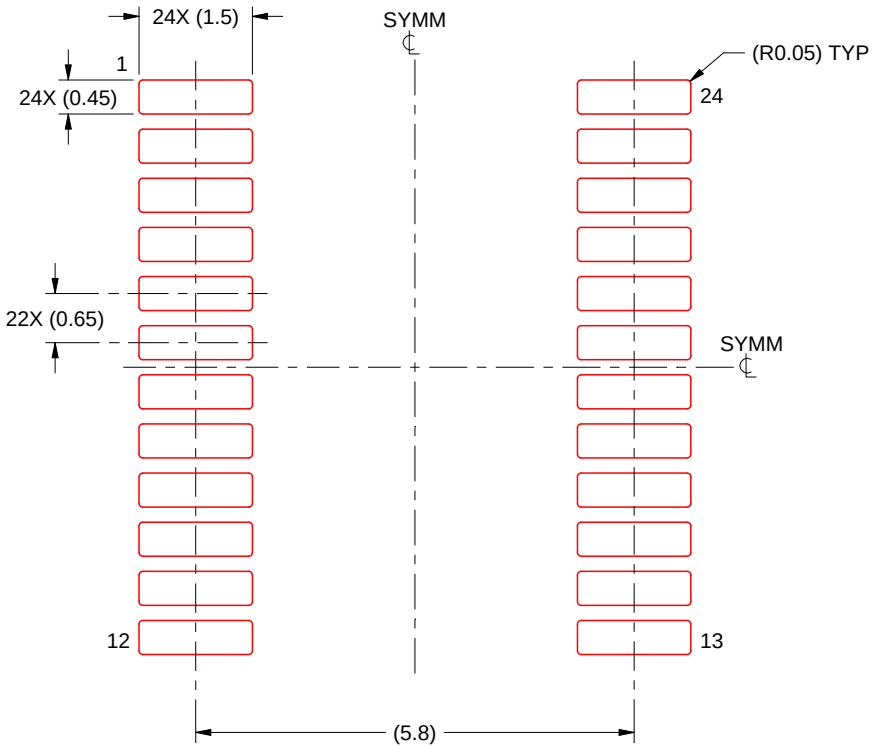


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



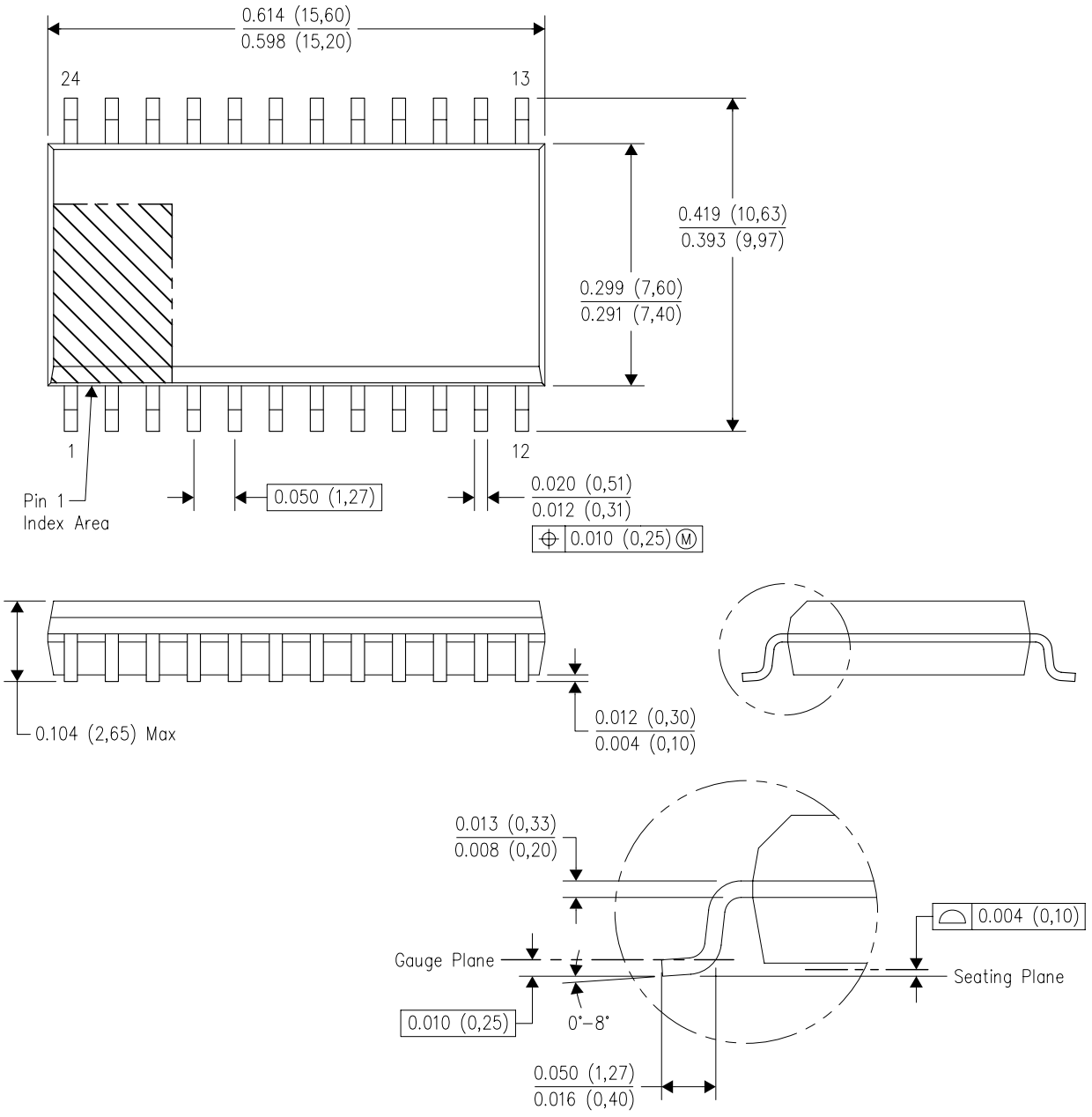
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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