



THE DATASHEET OF SN74CBT16244CDL

SN54CBT16244, SN74CBT16244 16-BIT FET BUS SWITCHES

SCDS031I – MAY 1996 – REVISED OCTOBER 2000

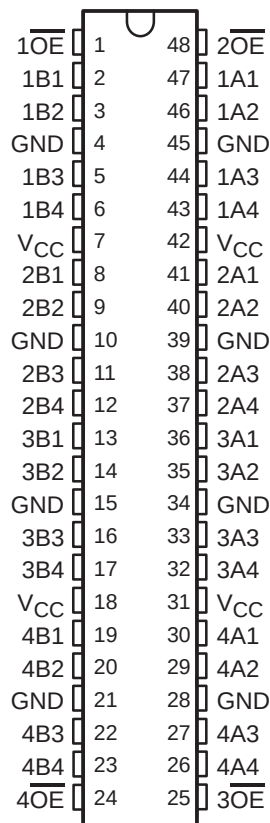
- Members of Texas Instruments' Widebus™ Family
- Standard '16244-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

description

The 'CBT16244 devices provide 16 bits of high-speed TTL-compatible bus switching in a standard '16244 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

These devices are organized as four 4-bit low-impedance switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on, and data can flow from port A to port B, or vice versa. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

SN54CBT16244 . . . WD PACKAGE
SN74CBT16244 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74CBT16244DL	CBT16244
		Tape and reel	SN74CBT16244DLR	
	TSSOP – DGG	Tape and reel	SN74CBT16244DGGR	CBT16244
	TVSOP – DGV	Tape and reel	SN74CBT16244DGVR	CY244
–55°C to 125°C	CFP – WD	Tube	SNJ54CBT16244WD	SNJ54CBT16244WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 4-bit bus switch)

INPUT $\overline{OE}$	OUTPUTS A, B
L	A port = B port
H	Disconnect



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The figure displays four circuit diagrams for the 74VHC04 hex inverters, arranged in a 2x2 grid. Each diagram shows the internal transistor structure and the connection of the input, output, and enable pins.

- Top Left Diagram:** Shows the internal structure of the first inverter. The input pin 1A1 (pin 47) is connected to the base of the input transistor. The output pin 1B1 (pin 2) is connected to the collector of the output transistor. The enable pin 1OE (pin 1) is connected to the base of the input transistor. The input transistor is a PNP type, and the output transistor is an NPN type. The input and output transistors are connected in a common-emitter configuration.
- Top Right Diagram:** Shows the internal structure of the second inverter. The input pin 2A1 (pin 41) is connected to the base of the input transistor. The output pin 2B1 (pin 8) is connected to the collector of the output transistor. The enable pin 2OE (pin 48) is connected to the base of the input transistor. The input transistor is a PNP type, and the output transistor is an NPN type. The input and output transistors are connected in a common-emitter configuration.
- Bottom Left Diagram:** Shows the internal structure of the third inverter. The input pin 3A1 (pin 36) is connected to the base of the input transistor. The output pin 3B1 (pin 13) is connected to the collector of the output transistor. The enable pin 3OE (pin 25) is connected to the base of the input transistor. The input transistor is a PNP type, and the output transistor is an NPN type. The input and output transistors are connected in a common-emitter configuration.
- Bottom Right Diagram:** Shows the internal structure of the fourth inverter. The input pin 4A1 (pin 30) is connected to the base of the input transistor. The output pin 4B1 (pin 19) is connected to the collector of the output transistor. The enable pin 4OE (pin 24) is connected to the base of the input transistor. The input transistor is a PNP type, and the output transistor is an NPN type. The input and output transistors are connected in a common-emitter configuration.

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
Storage temperature range, T_{Stg}	−65°C to 150°C

NOTES:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

		SN54CBT16244		SN74CBT16244		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4	5.5	4	5.5	V
V _{IH}	High-level control input voltage	2		2		V
V _{IL}	Low-level control input voltage		0.8		0.8	V
T _A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54CBT16244			SN74CBT16244			UNIT
		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
I_I	$V_{CC} = 0$ $V_I = 5.5\text{ V}$			10			10	μA
	$V_{CC} = 5.5\text{ V}$ $V_I = 5.5\text{ V or GND}$			± 1			± 1	
I_{CC}	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$ $I_O = 0$,			3.2			3	μA
$\Delta I_{CC}^\ddagger$	Control inputs $V_{CC} = 5.5\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$ One input at 3.4 V ,			2.5			2.5	mA
C_i	Control inputs $V_I = 3\text{ V or 0}$			2.5			2.5	pF
$C_{io}(\text{OFF})$	$V_O = 3\text{ V or 0}$, $\overline{OE} = V_{CC}$			4.5			4.5	pF
$r_{on}^\S$	$V_{CC} = 4\text{ V}$, $V_I = 2.4\text{ V}$, $I_I = 15\text{ mA}$			20			20	Ω
	$V_{CC} = 4.5\text{ V}$, $V_I = 0$, $I_I = 64\text{ mA}$			5 10			5 7	
	$V_{CC} = 4.5\text{ V}$, $V_I = 0$, $I_I = 30\text{ mA}$			5 10			5 7	
	$V_{CC} = 4.5\text{ V}$, $V_I = 2.4\text{ V}$, $I_I = 15\text{ mA}$			8 14			8 12	

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBT16244				SN74CBT16244				UNIT
			V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd} [¶]	A or B	B or A			0.8*		0.35		0.25	ns	
t _{en}	$\overline{OE}$	A or B		10.3	1	9.2		5.5	1	5.1	ns
t _{dis}	$\overline{OE}$	A or B		9.7	1	8.2		5.2	1	5.4	ns

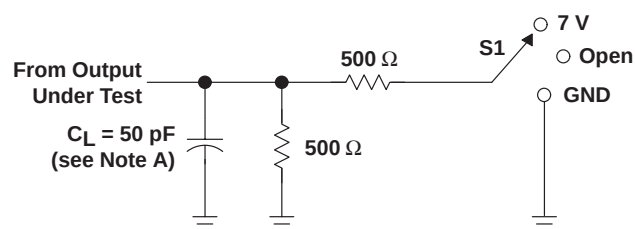
* On products compliant to MIL-PRF-38535, this parameter is not production tested.

^{||} The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

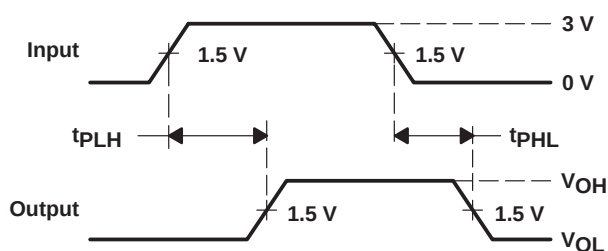
SN54CBT16244, SN74CBT16244 16-BIT FET BUS SWITCHES

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PARAMETER MEASUREMENT INFORMATION

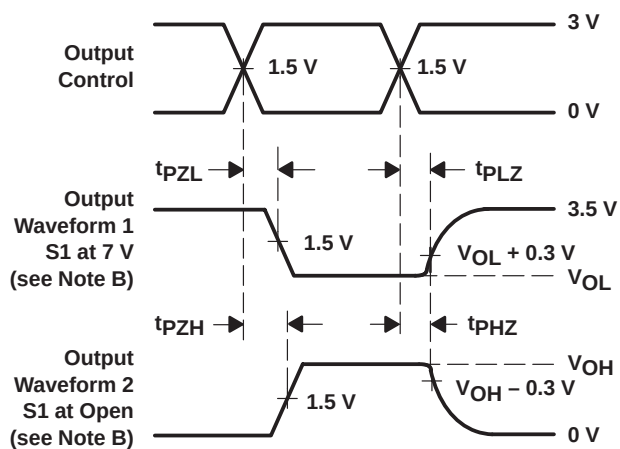


LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBT16244DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16244	Samples
SN74CBT16244DL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16244	Samples
SN74CBT16244DLR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16244	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

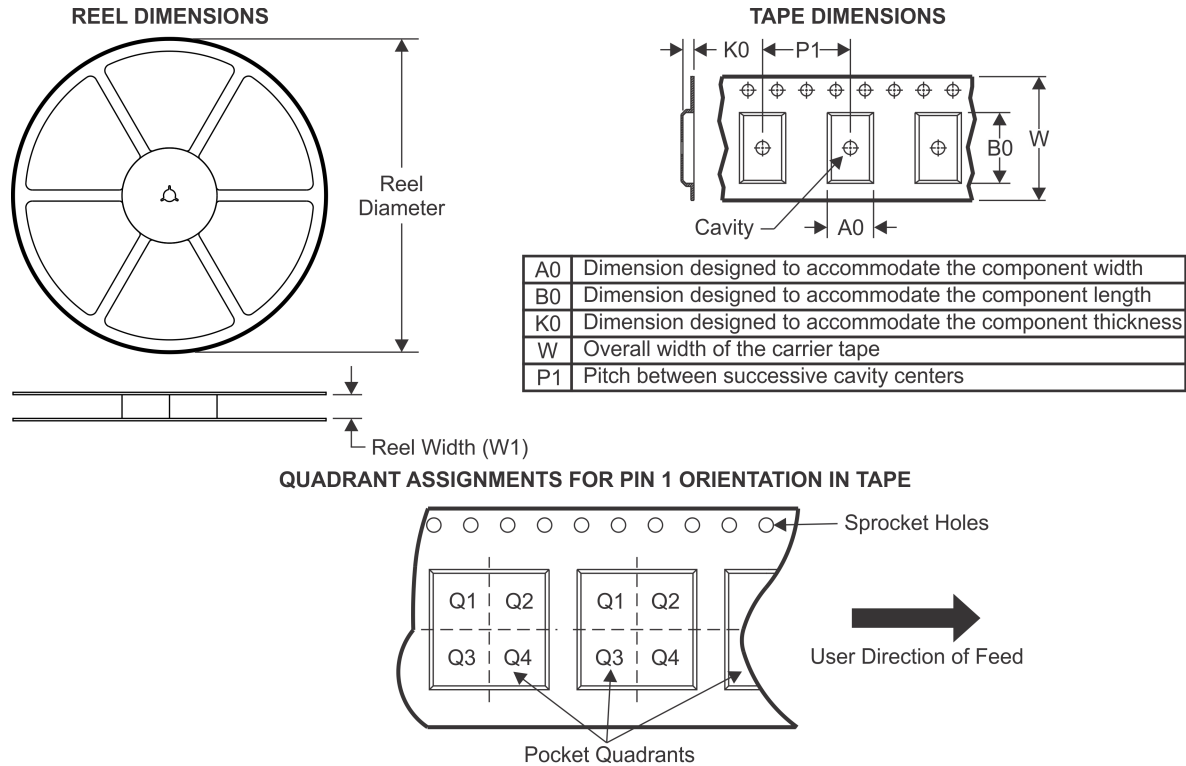
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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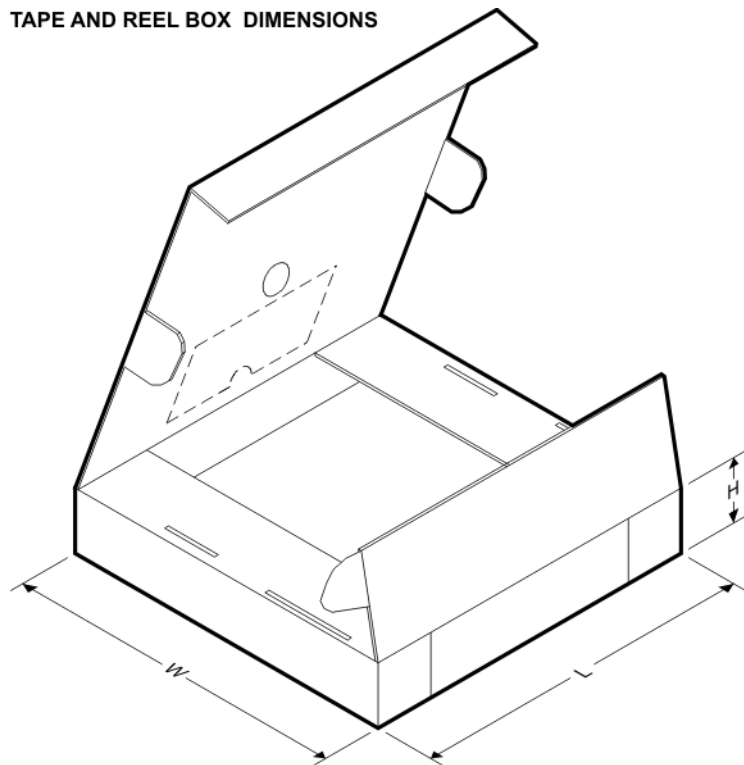
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16244DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74CBT16244DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

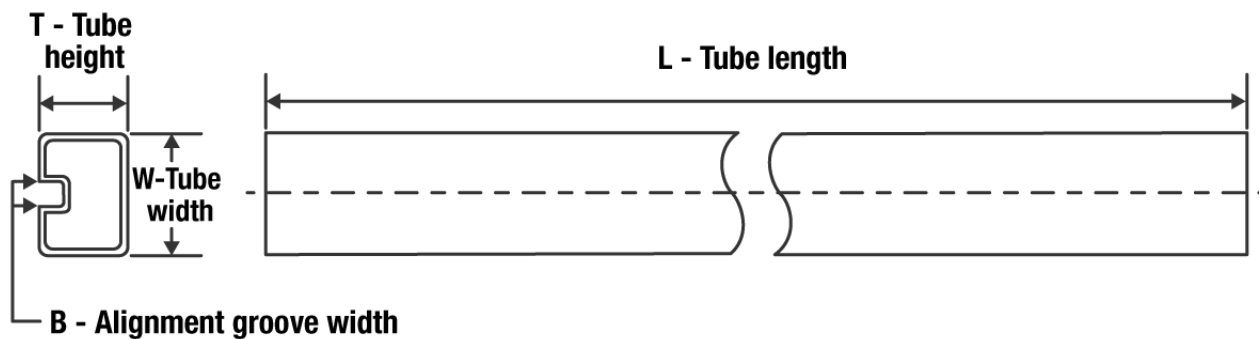
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT16244DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74CBT16244DLR	SSOP	DL	48	1000	367.0	367.0	55.0

TUBE

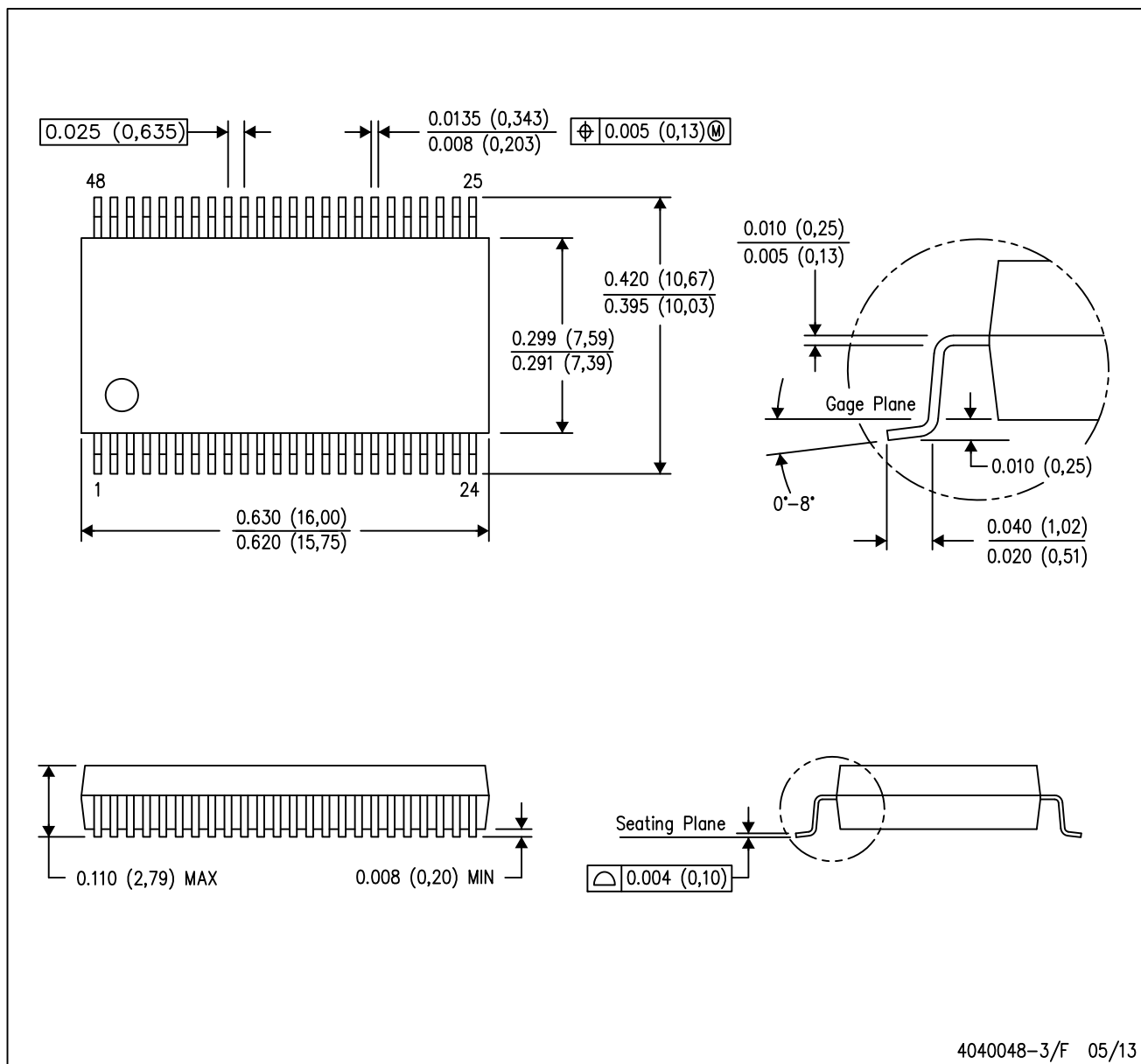


*All dimensions are nominal

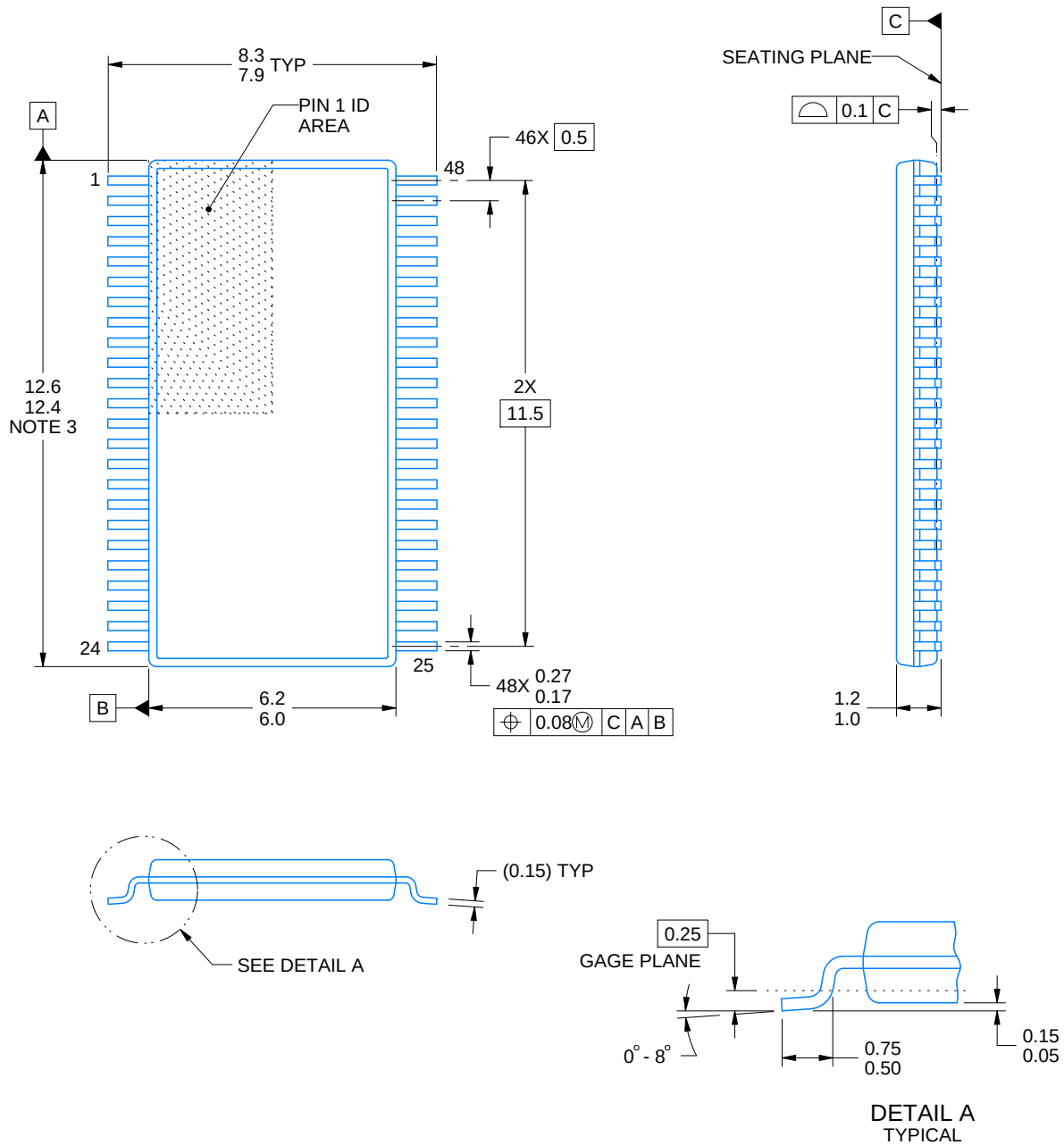
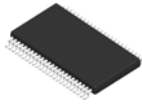
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CBT16244DL	DL	SSOP	48	25	473.7	14.24	5110	7.87

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118



4214859/B 11/2020

NOTES:

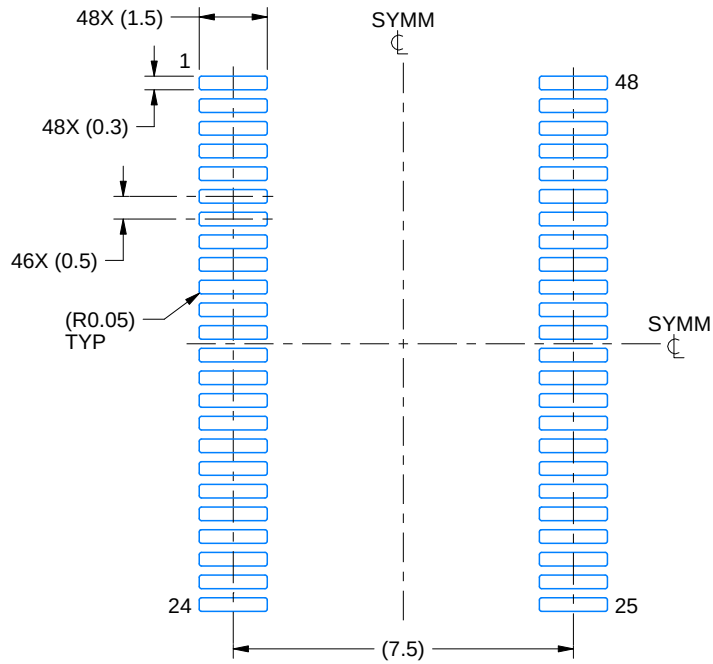
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

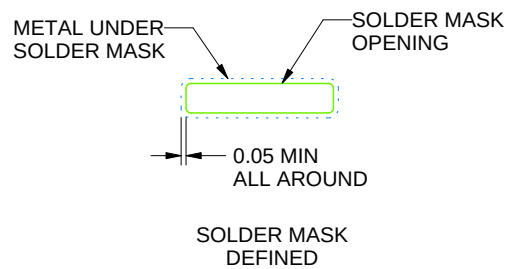
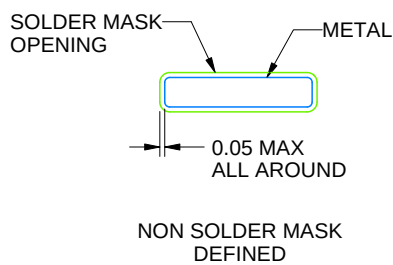
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

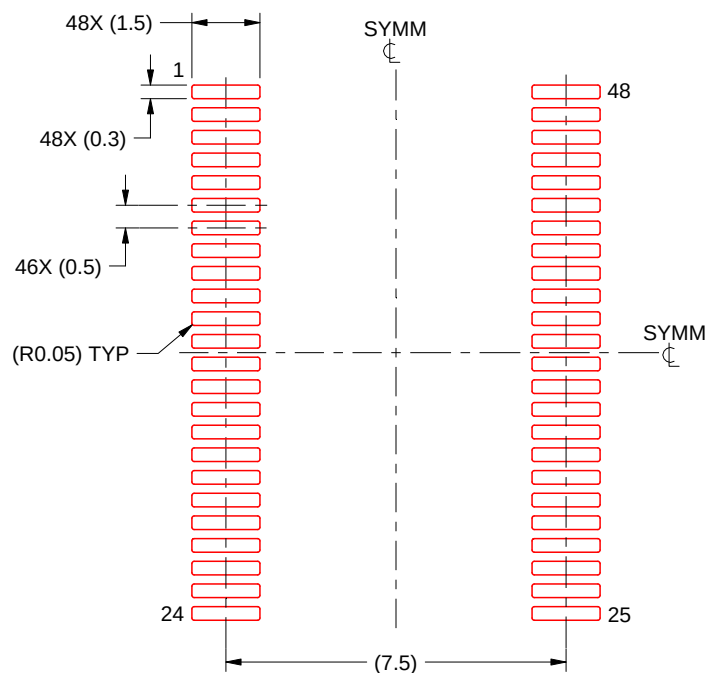
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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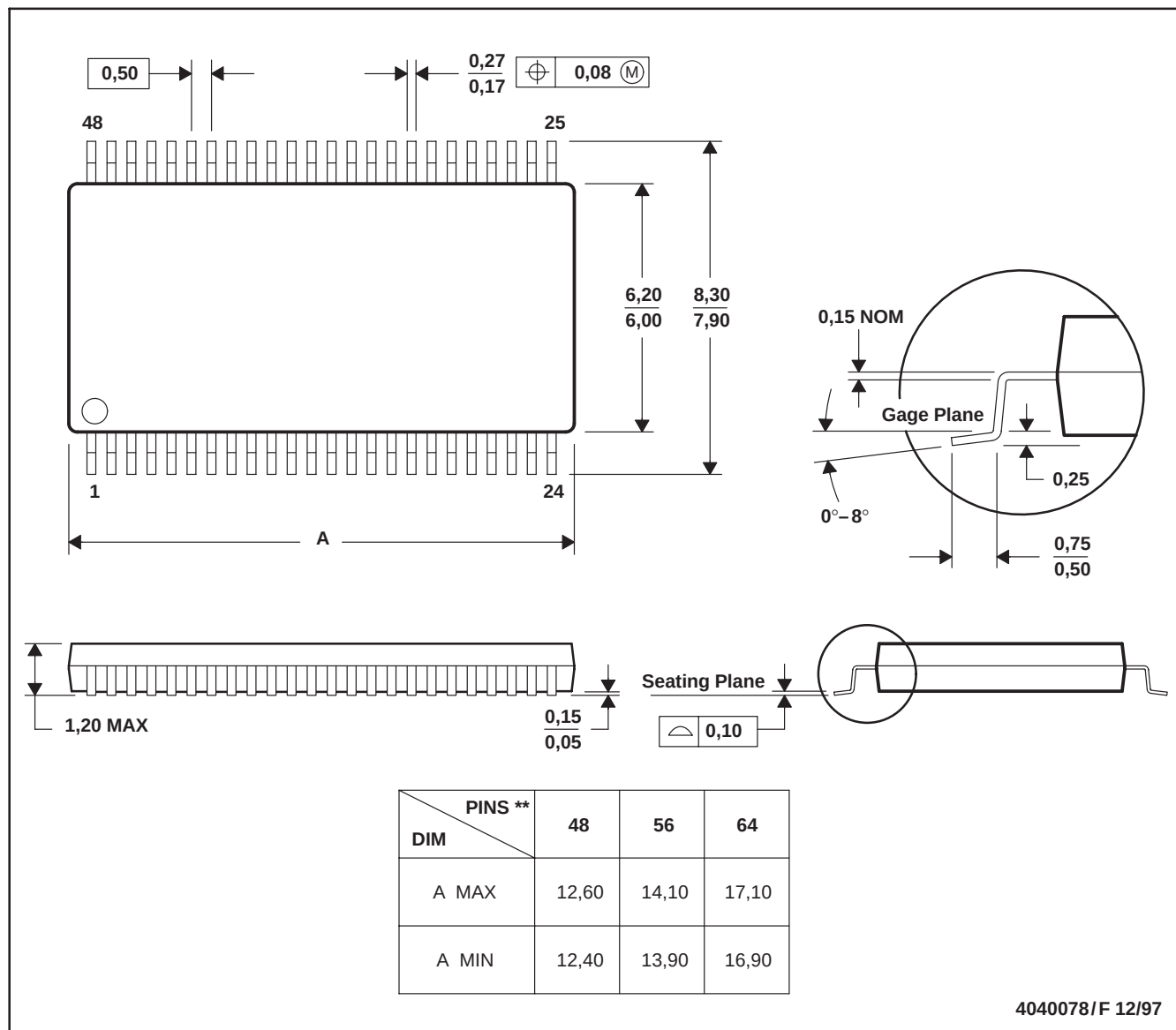
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
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 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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