



**THE DATASHEET OF
SN74CB3T3383PW**



SN74CB3T3383

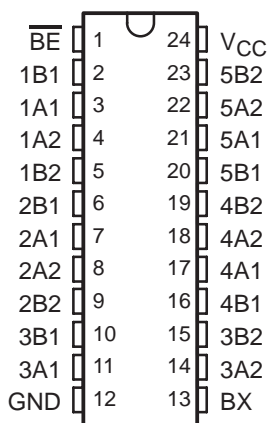
10-BIT FET BUS-EXCHANGE SWITCH

2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V-TOLERANT LEVEL SHIFTER

SCDS158A – OCTOBER 2003 – REVISED DECEMBER 2004

- Output Voltage Translation Tracks V_{CC}
- Supports Mixed-Mode Signal Operation On All Data I/O Ports
 - 5-V Input Down To 3.3-V Output Level Shift With 3.3-V V_{CC}
 - 5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V V_{CC}
- 5-V-Tolerant I/Os With Device Powered Up or Powered Down
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance (r_{ON}) Characteristics ($r_{ON} = 5 \Omega$ Typical)
- Low Input/Output Capacitance Minimizes Loading ($C_{iO(OFF)} = 8 \text{ pF}$ Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ($I_{CC} = 20 \mu\text{A}$ Max)
- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Digital Applications: Level Translation, Memory Interleaving, Bus Isolation
- Ideal for Low-Power Portable Equipment

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

| T_A | PACKAGE† | ORDERABLE PART NUMBER | TOP-SIDE MARKING | |
|---------------|-------------------|-----------------------|------------------|----------|
| –40°C to 85°C | SOIC – DW | Tube | SN74CB3T3383DW | |
| | | Tape and reel | SN74CB3T3383DWR | |
| | SSOP (QSOP) – DBQ | Tape and reel | SN74CB3T3383DBQR | CB3T3383 |
| | | Tube | SN74CB3T3383PW | KS383 |
| | TSSOP – PW | Tape and reel | SN74CB3T3383PWR | |
| TVSOP – DGV | Tape and reel | SN74CB3T3383DGVR | KS383 | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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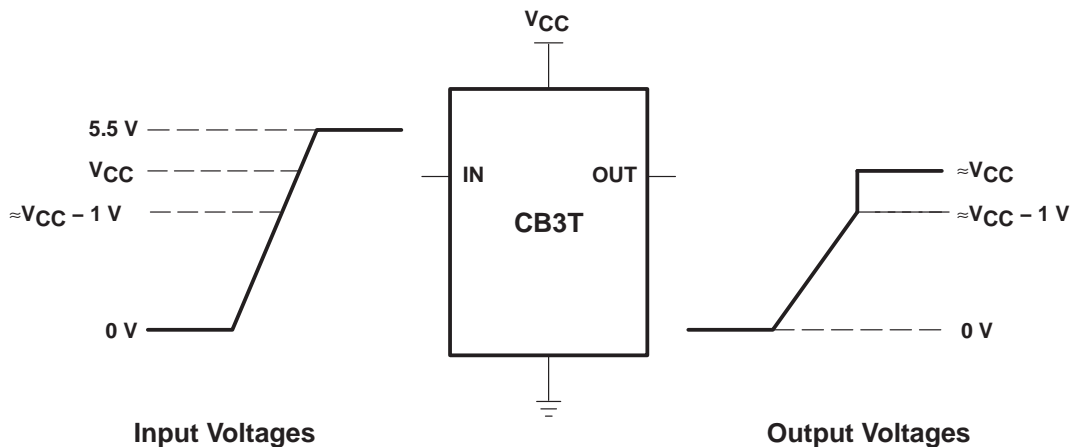
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2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V-TOLERANT LEVEL SHIFTER

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description/ordering information (continued)

The SN74CB3T3383 is a high-speed TTL-compatible FET bus-exchange switch with low ON-state resistance (r_{ON}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC} . The SN74CB3T3383 supports systems using 5-V TTL, 3.3-V LVTTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).



NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to $V_{CC} - 1\text{ V}$, and less than or equal to 5.5 V, then the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage Translation Characteristics

The SN74CB3T3383 is organized as a 10-bit bus switch or as a 5-bit bus-exchange with enable (\overline{BE}) input. When used as a 5-bit bus-exchange, the device provides data exchanging between four signal ports. When \overline{BE} is low, the bus-exchange switch is ON, and the select input (BX) controls the data path. When \overline{BE} is high, the bus-exchange switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{BE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

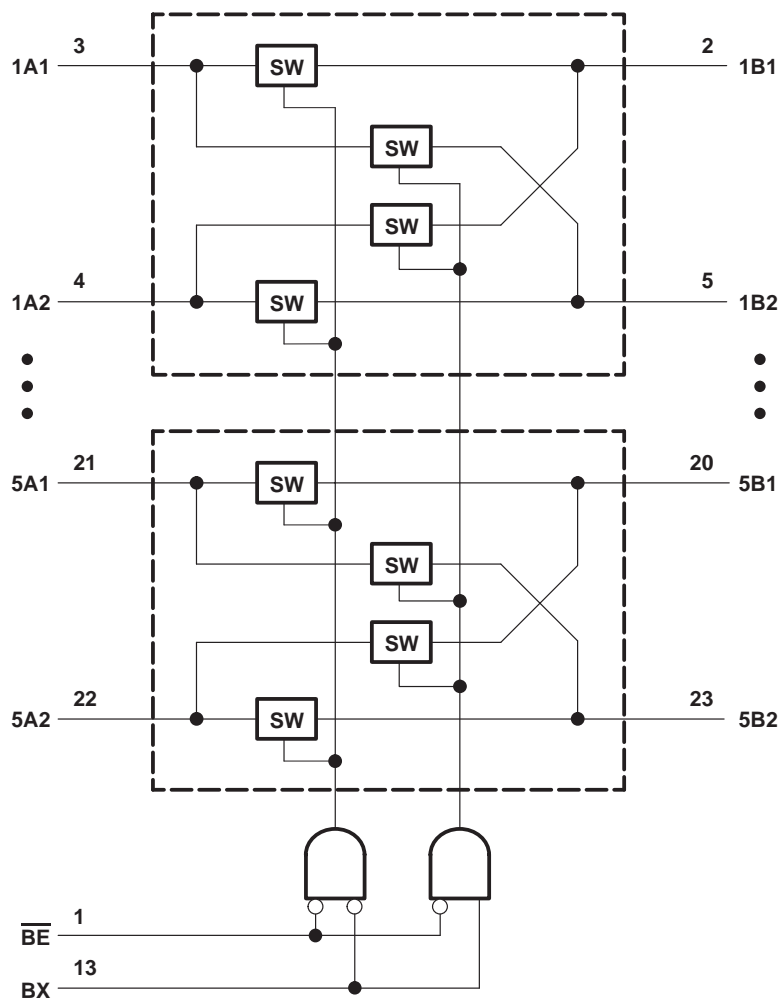
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FUNCTION TABLE
(each 5-bit switch)

| INPUTS | | INPUTS/OUTPUTS | | FUNCTION |
|-----------------|----|----------------|----|--|
| \overline{BE} | BX | A1 | A2 | |
| L | L | B1 | B2 | A1 port = B1 port A2 port = B2 port |
| L | H | B2 | B1 | A1 port = B2 port A2 port = B1 port |
| H | X | Z | Z | Disconnect |

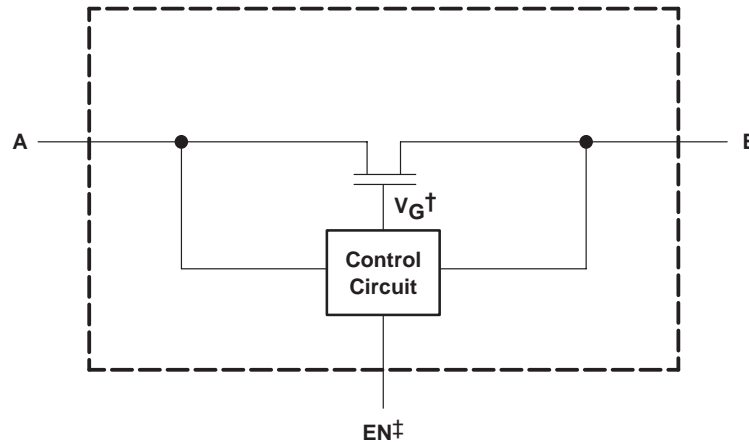
logic diagram (positive logic)



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simplified schematic, each FET switch (SW)



† Gate Voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > V_{CC} + V_T$.
‡ EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

| | | |
|---|-------|----------------|
| Supply voltage range, V_{CC} (see Note 1) | | -0.5 V to 7 V |
| Control input voltage range, V_{IN} (see Notes 1 and 2) | | -0.5 V to 7 V |
| Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) | | -0.5 V to 7 V |
| Control input clamp current, I_{IK} ($V_{IN} < 0$) | | -50 mA |
| I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$) | | -50 mA |
| ON-state switch current, $I_{I/O}$ (see Note 4) | | ± 128 mA |
| Continuous current through V_{CC} or GND terminals | | ± 100 mA |
| Package thermal impedance, θ_{JA} (see Note 5): | | |
| DBQ package | | 61°C/W |
| DGV package | | 86°C/W |
| DW package | | 46°C/W |
| PW package | | 88°C/W |
| Storage temperature range, T_{stg} | | -65°C to 150°C |

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground unless otherwise specified.
 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
 4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
 5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

| | | MIN | MAX | UNIT | |
|-----------|----------------------------------|---------------------------|-----|------|---|
| V_{CC} | Supply voltage | 2.3 | 3.6 | V | |
| V_{IH} | High-level control input voltage | $V_{CC} = 2.3$ V to 2.7 V | 1.7 | 5.5 | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | 2 | 5.5 | |
| V_{IL} | Low-level control input voltage | $V_{CC} = 2.3$ V to 2.7 V | 0 | 0.7 | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | 0 | 0.8 | |
| $V_{I/O}$ | Data input/output voltage | 0 | 5.5 | V | |
| T_A | Operating free-air temperature | -40 | 85 | °C | |

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT | |
|----------------------|----------------|--|---|------|------|------|---|
| V _{IK} | | V _{CC} = 3 V, I _I = -18 mA | | | -1.2 | V | |
| V _{OH} | | See Figures 3 and 4 | | | | | |
| I _{IN} ‡ | Control inputs | V _{CC} = 3.6 V, V _{IN} ‡ = 3.6 V to 5.5 V or GND | | | ±10 | μA | |
| I _I | | V _{CC} = 3.6 V, Switch ON, V _{IN} = V _{CC} or GND | V _I = V _{CC} - 0.7 V to 5.5 V | | ±20 | μA | |
| | | | V _I = 0.7 V to V _{CC} - 0.7 V | | -40 | | |
| | | | V _I = 0 to 0.7 V | | ±5 | | |
| I _{OZ} § | | V _{CC} = 3.6 V, V _O = 0 to 5.5 V, V _I = 0, Switch OFF, V _{IN} = V _{CC} or GND | | | ±10 | μA | |
| I _{off} | | V _{CC} = 0, V _O = 0 to 5.5 V, V _I = 0, | | | 10 | μA | |
| I _{CC} | | V _{CC} = 3.6 V, I _{I/O} = 0, Switch ON or OFF, V _{IN} = V _{CC} or GND | V _I = V _{CC} or GND | | 20 | μA | |
| | | | V _I = 5.5 V | | 20 | | |
| ΔI _{CC} ¶ | Control inputs | V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | | | 300 | μA | |
| C _{in} | Control inputs | V _{CC} = 3.3 V, V _{IN} = V _{CC} or GND | | | 4 | pF | |
| C _{io(OFF)} | | V _{CC} = 3.3 V, V _{I/O} = 5.5 V, 3.3 V, or GND, Switch OFF, V _{IN} = V _{CC} or GND | | | 8 | pF | |
| C _{io(ON)} | | V _{CC} = 3.3 V, Switch ON, V _{IN} = V _{CC} or GND | V _{I/O} = 5.5 V or 3.3 V | | 7 | pF | |
| | | | V _{I/O} = GND | | 21 | | |
| r _{on} # | | V _{CC} = 2.3 V, TYP at V _{CC} = 2.5 V, V _I = 0 | I _O = 24 mA | | 5 | Ω | |
| | | | I _O = 16 mA | | 5 | | |
| | | V _{CC} = 3 V, V _I = 0 | I _O = 64 mA | | 5 | | 8 |
| | | | I _O = 32 mA | | 5 | | 8 |

† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

‡ V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | UNIT |
|------------------------------|-----------------|----------------|------------------------------------|------|------------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t _{pd} [†] | A or B | B or A | 0.15 | | 0.25 | | ns |
| t _{pd(s)} | BX | A or B | 1 | 15 | 1 | 10 | |
| t _{en} | \overline{BE} | A or B | 1 | 13.5 | 1 | 9 | ns |
| t _{dis} | \overline{BE} | A or B | 1 | 7 | 1 | 8.5 | ns |

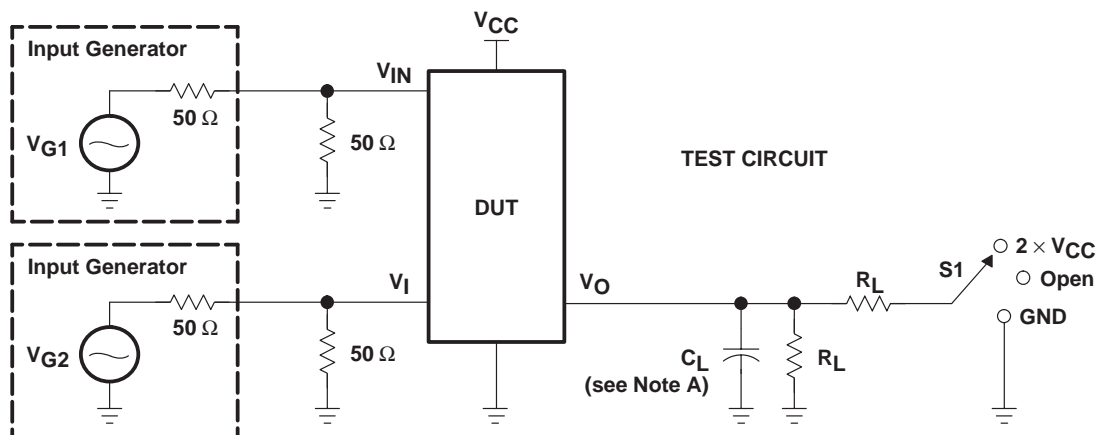
[†] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



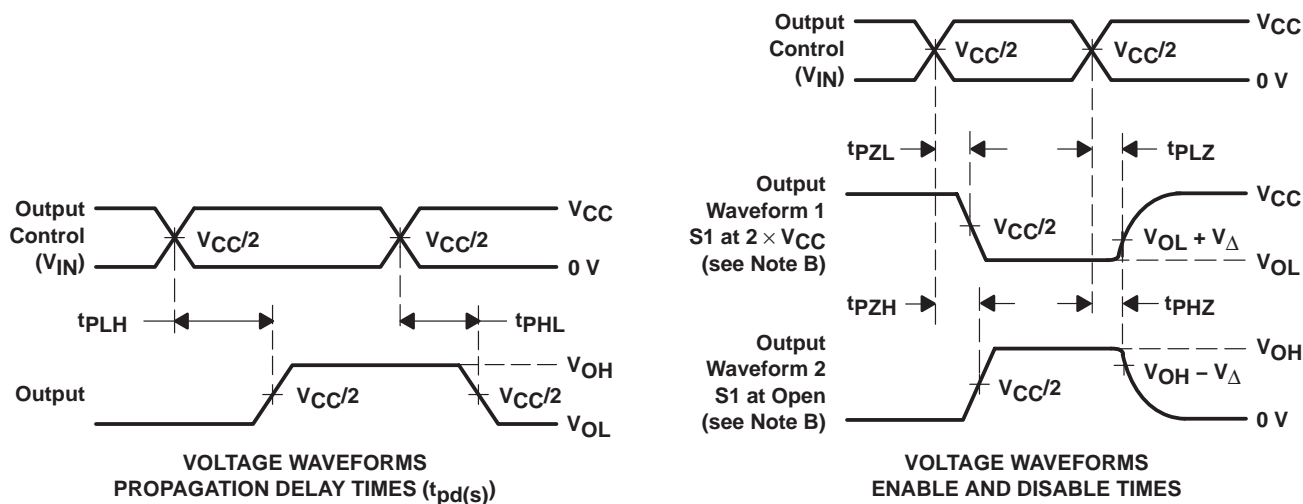
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PARAMETER MEASUREMENT INFORMATION



| TEST | V _{CC} | S1 | R _L | V _I | C _L | V _Δ |
|------------------------------------|-----------------|---------------------|----------------|----------------|----------------|----------------|
| t _{pd} (s) | 2.5 V ± 0.2 V | Open | 500 Ω | 3.6 V or GND | 30 pF | |
| | 3.3 V ± 0.3 V | Open | 500 Ω | 5.5 V or GND | 50 pF | |
| t _{PLZ} /t _{PZL} | 2.5 V ± 0.2 V | 2 × V _{CC} | 500 Ω | GND | 30 pF | 0.15 V |
| | 3.3 V ± 0.3 V | 2 × V _{CC} | 500 Ω | GND | 50 pF | 0.3 V |
| t _{PHZ} /t _{PZH} | 2.5 V ± 0.2 V | Open | 500 Ω | 3.6 V | 30 pF | 0.15 V |
| | 3.3 V ± 0.3 V | Open | 500 Ω | 5.5 V | 50 pF | 0.3 V |



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PZH} are the same as t_{dis}.
 F. t_{PZL} and t_{PZH} are the same as t_{en}.
 G. t_{PLH} and t_{PHL} are the same as t_{pd}(s). The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 H. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

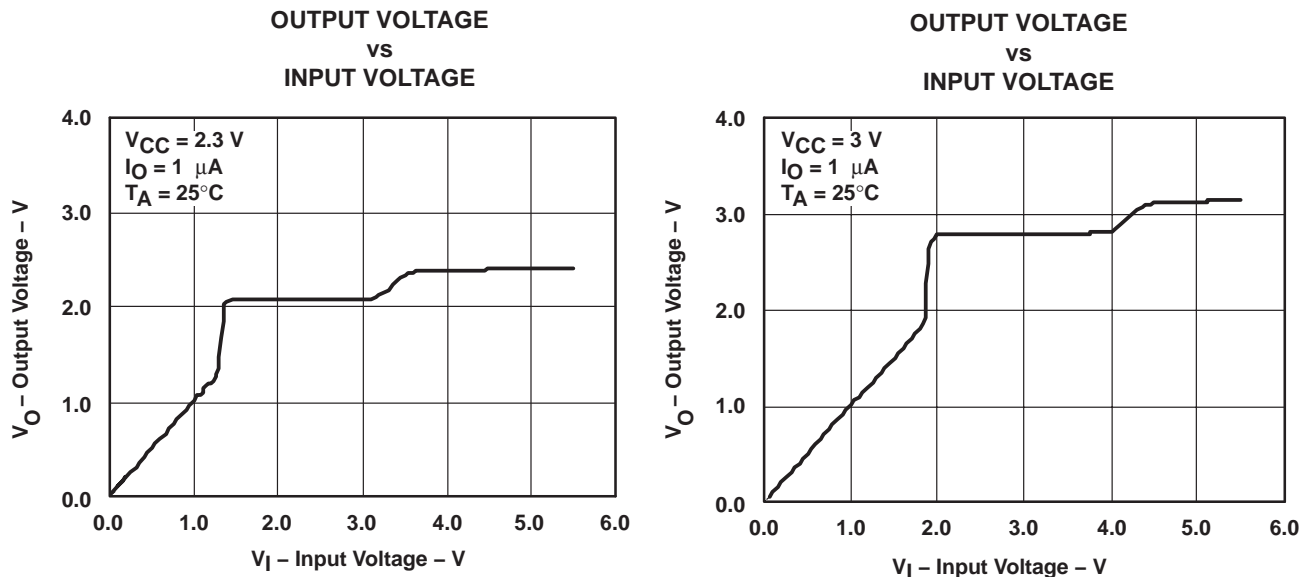


Figure 3. Data Output Voltage vs Data Input Voltage

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TYPICAL CHARACTERISTICS (continued)

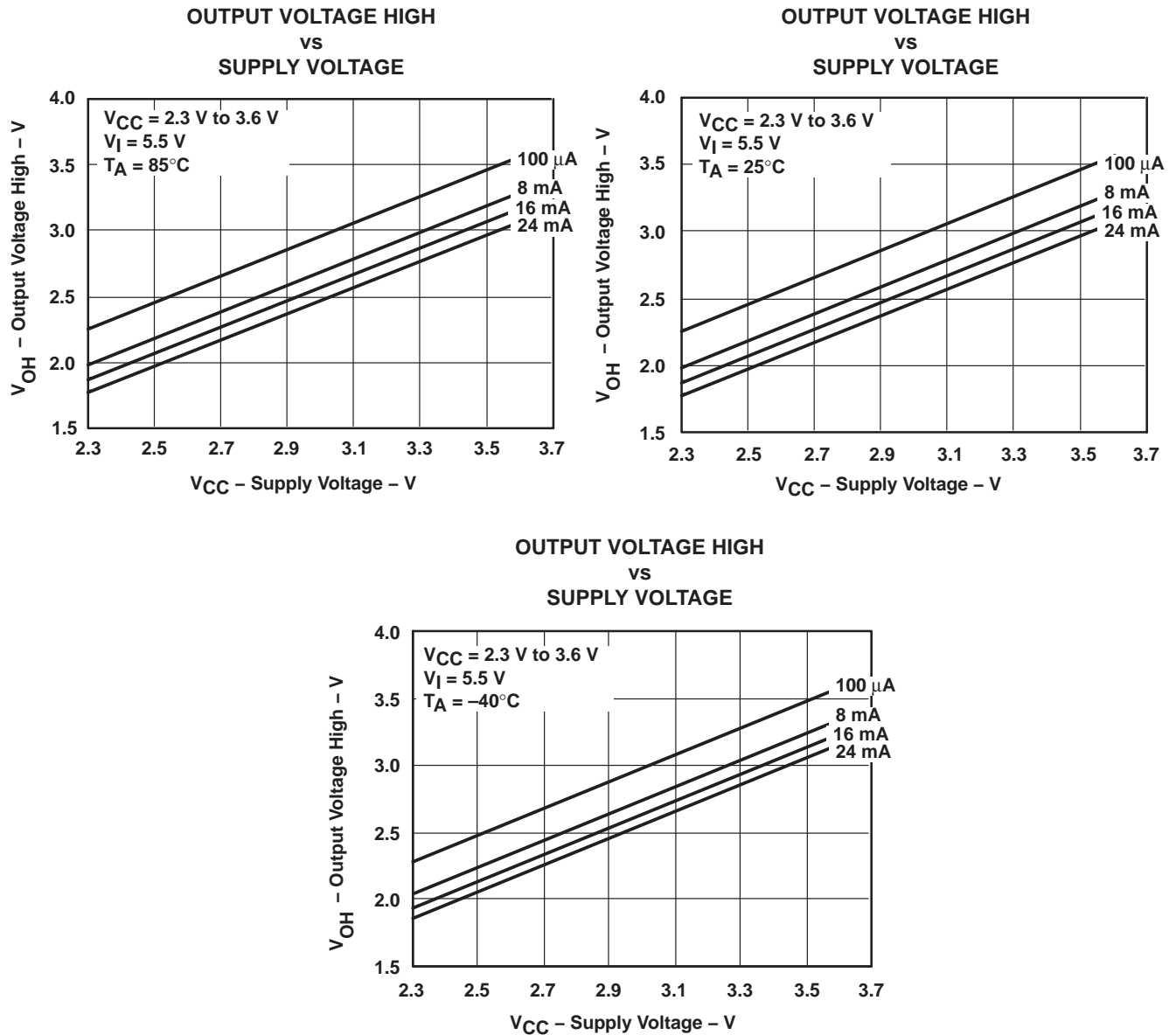


Figure 4. V_{OH} Values

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74CB3T3383DGVR | ACTIVE | TVSOP | DGV | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | KS383 | Samples |
| SN74CB3T3383DWR | ACTIVE | SOIC | DW | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CB3T3383 | Samples |
| SN74CB3T3383PW | ACTIVE | TSSOP | PW | 24 | 60 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | KS383 | Samples |
| SN74CB3T3383PWR | ACTIVE | TSSOP | PW | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | KS383 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

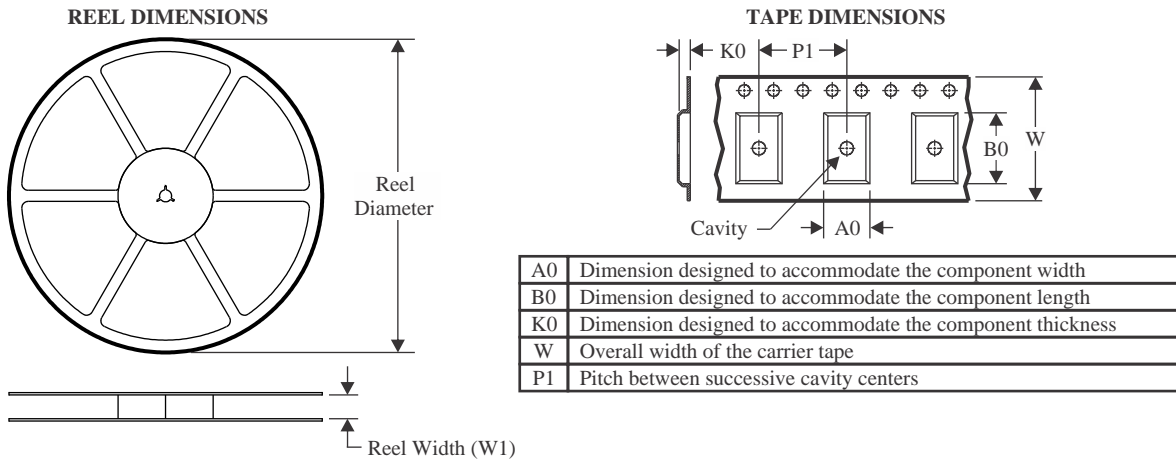
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74CB3T3383DGVR | TVSOP | DGV | 24 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74CB3T3383DWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74CB3T3383PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74CB3T3383DGVR | TVSOP | DGV | 24 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74CB3T3383DWR | SOIC | DW | 24 | 2000 | 350.0 | 350.0 | 43.0 |
| SN74CB3T3383PWR | TSSOP | PW | 24 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74CB3T3383PW | PW | TSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |

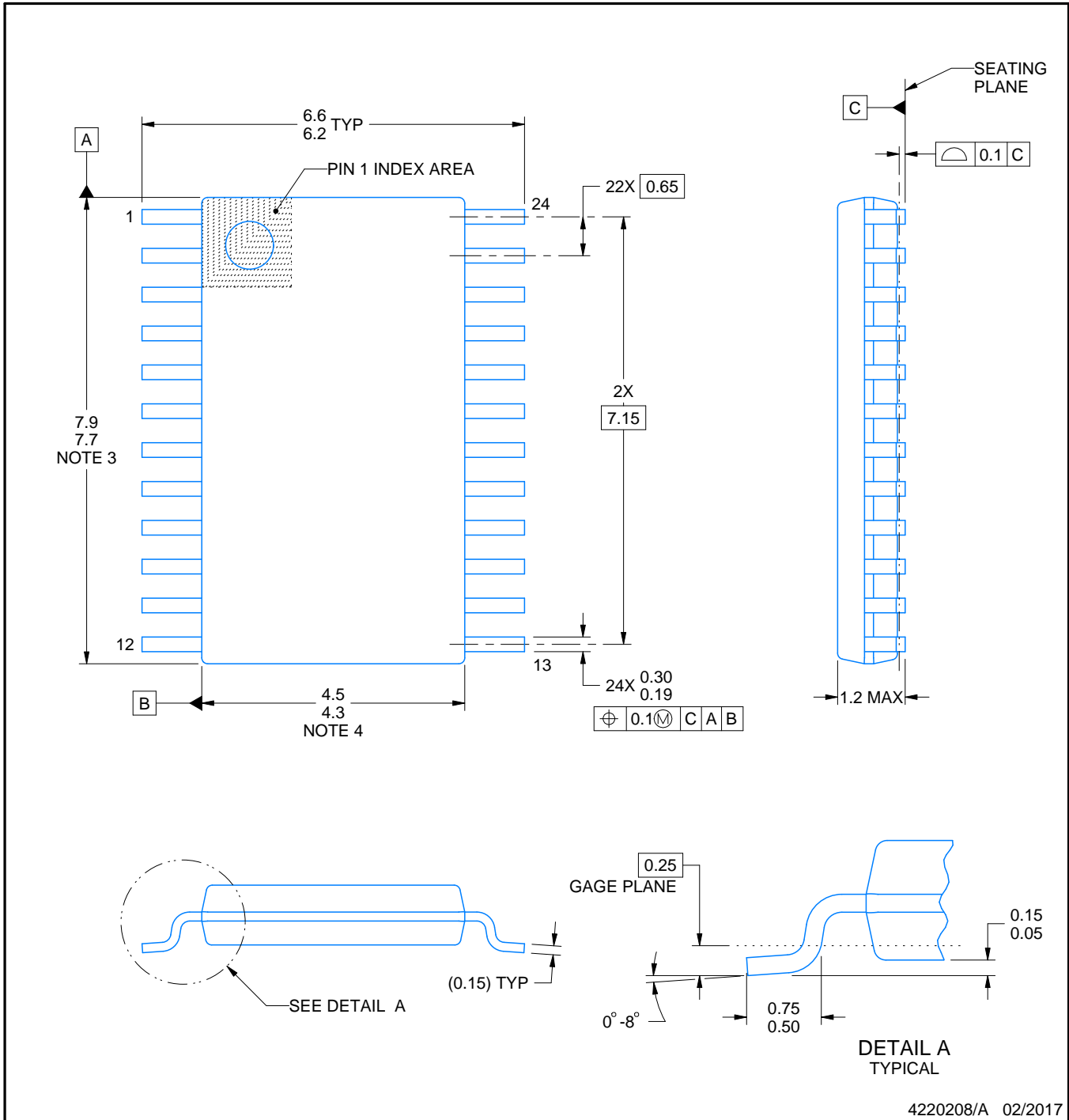
PW0024A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

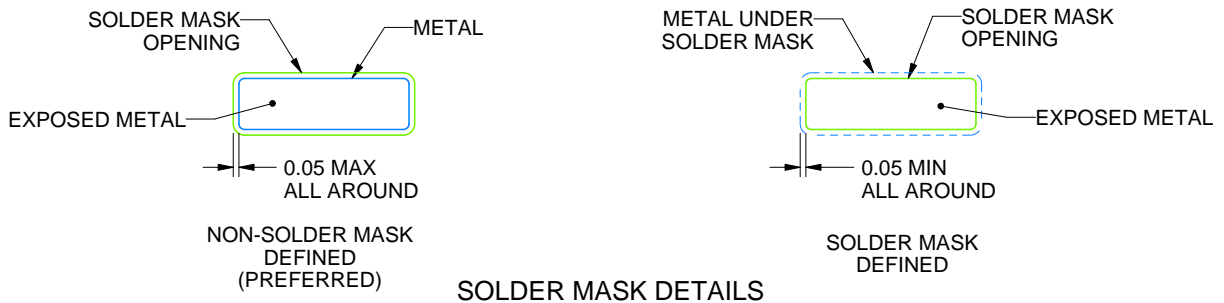
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

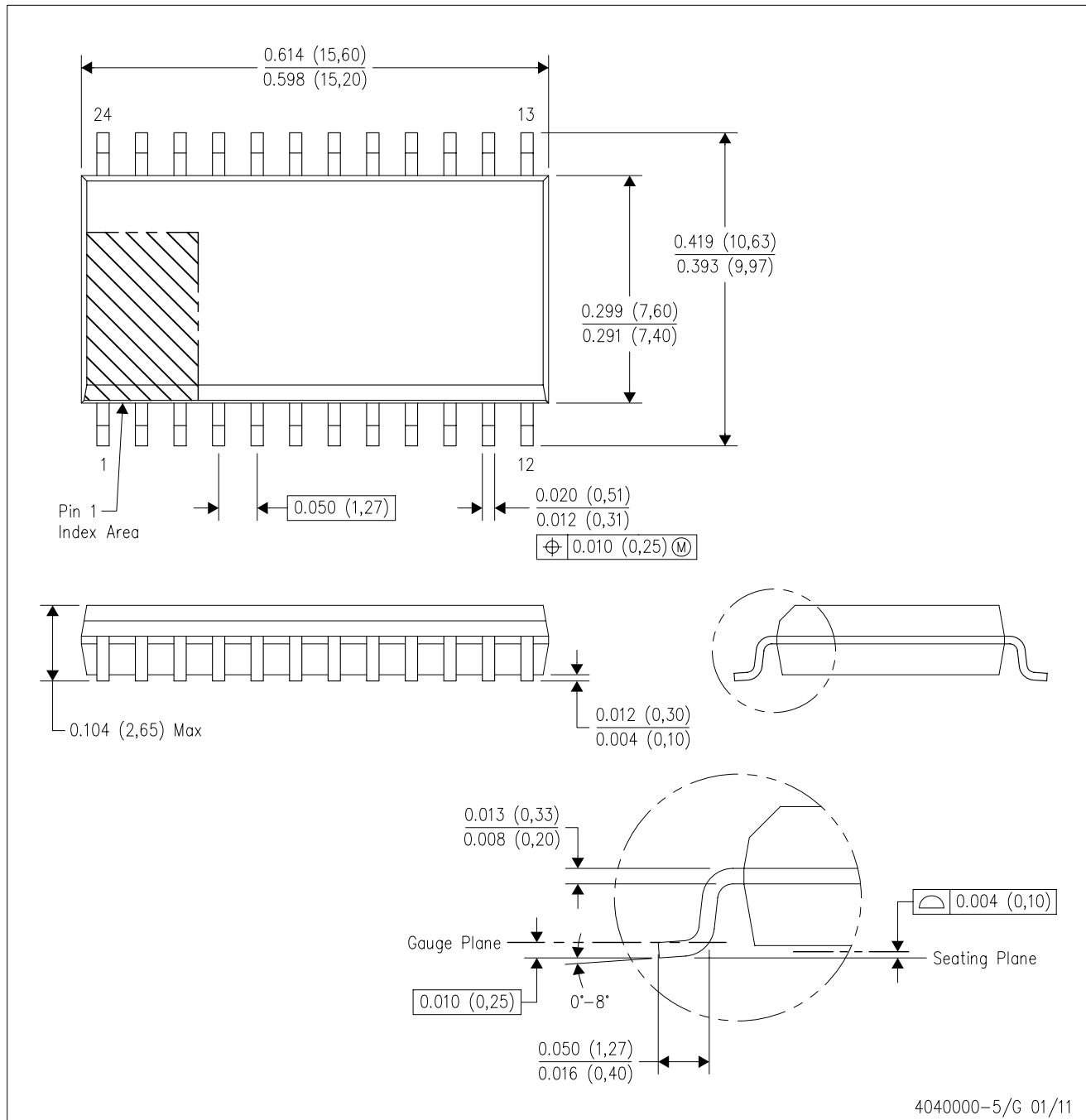


4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

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