

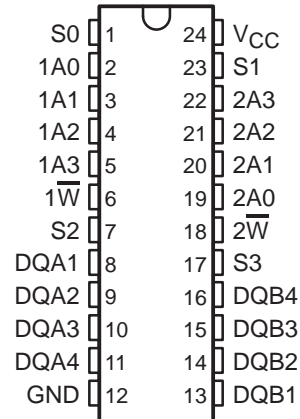


**THE DATASHEET OF  
SN74ALS870DWR**



- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Each Register File Has Individual Write-Enable Controls and Address Lines
- Designed Specifically for Multibus Architecture and Overlapping File Operations
- Prioritized B-Input Port Prevents Write Conflicts During Dual-Input Mode
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

DW OR NT PACKAGE  
(TOP VIEW)



**description**

This device features two 16-word by 4-bit register files. Each register file has individual write-enable ( $1\overline{W}$ ,  $2\overline{W}$ ) controls and address lines. This device has two 4-bit data I/O ports (DQA1–DQA4 and DQB1–DQB4). The data I/O ports can output to bus A and bus B, receive input from bus A and bus B, receive input from bus A and output to bus B, or output to bus A and receive input from bus B. To prevent writing conflicts in the dual-input mode, the B-input port takes priority. Two select (S0 and S1) lines control which port has access to which register. S2 determines whether the A ports are in the input or the output modes and S3 does likewise for the B ports. The address lines (1A0–1A3 or 2A0–2A3) are decoded by an internal 1-of-16 decoder to select which register word is to be accessed. All outputs are 3-state buffer-type outputs designed specifically to drive bus lines directly.

The SN74ALS870 is characterized for operation from 0°C to 70°C.

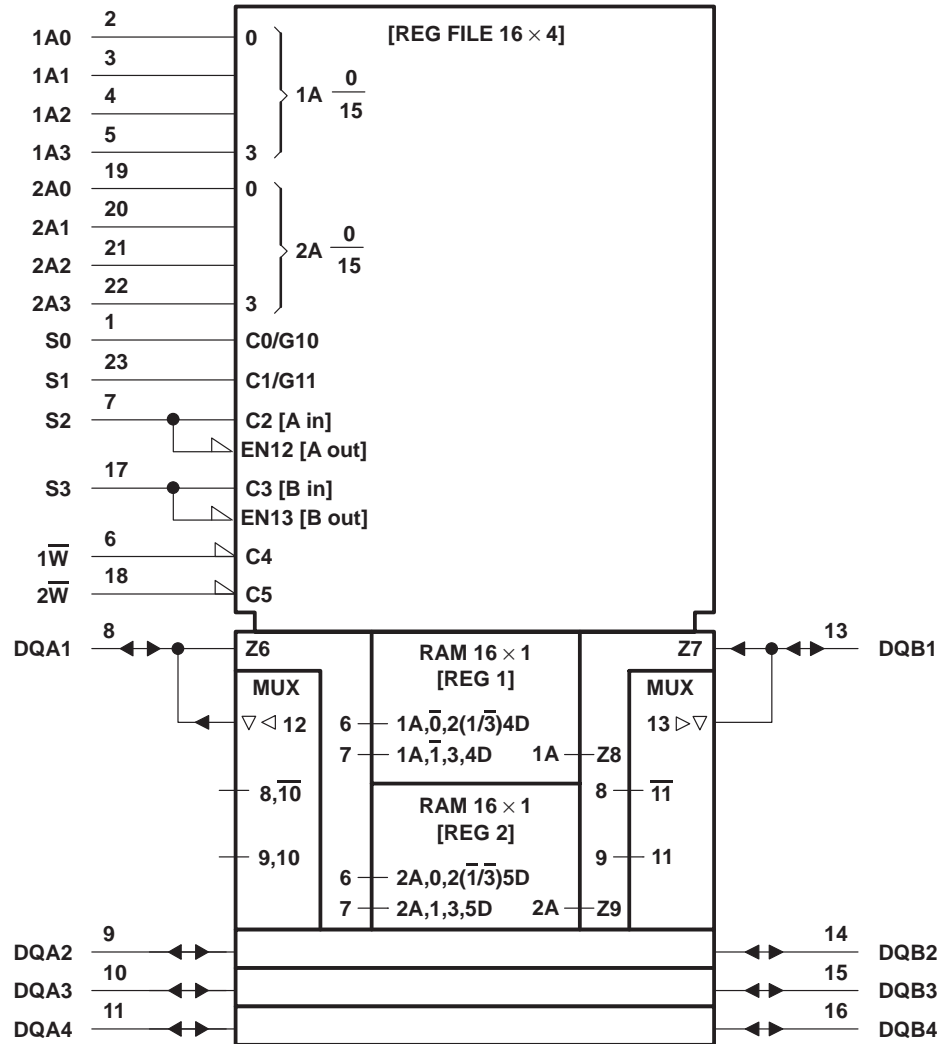
FUNCTION TABLE

FILE SELECT			INPUT/OUTPUT		
S0	S1	FILE SEL	S2	S3	I/O SEL
L	L	1R to A, 1R to B			
H	L	2R to A, 1R to B	L	L	A out, B out
L	H	1R to A, 2R to B			
H	H	2R to A, 2R to B			
L	L	A to 1R, 1R to B			
H	L	A to 2R, 1R to B	H	L	A in, B out
L	H	A to 1R, 2R to B			
H	H	A to 2R, 2R to B			
L	L	1R to A, B to 1R			
H	L	2R to A, B to 1R	L	H	A out, B in
L	H	1R to A, B to 2R			
H	H	2R to A, B to 2R			
L	L	B to 1R			
H	L	A to 2R, B to 1R	H	H	A in, B in
L	H	A to 1R, B to 2R			
H	H	B to 2R			

# SN74ALS870 DUAL 16-BY-4 REGISTER FILES

SDAS139A – DECEMBER 1982 – REVISED JANUARY 1995

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



# SN74ALS870

## DUAL 16-BY-4 REGISTER FILES

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### recommended operating conditions

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>OH</sub>	High-level output current			-2.6	mA
I <sub>OL</sub>	Low-level output current			24	mA
t <sub>w</sub>	Pulse duration, write	12			ns
t <sub>su</sub>	Setup time	Address before write↓	5		ns
		Data before write↑	15		
		Select before write↓	12		
t <sub>h</sub>	Hold time	Address before write↓	0		ns
		Data before write↑	0		
		Select before write↓	12		
T <sub>A</sub>	Operating free-air temperature	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.2	V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -0.4 mA		V <sub>CC</sub> - 2			V
		V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -2.6 mA	2.4	3.2		
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 24 mA		0.35	0.5	V
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 7 V			0.1	mA
	DQA and DQB ports		V <sub>I</sub> = 5.5 V			0.2	
I <sub>IH</sub>	1W and 2W	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			20	μA
	Other control inputs					40	
	DQA and DQB ports‡					50	
I <sub>IL</sub>	Control inputs	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V			-0.2	mA
	DQA and DQB ports‡					-0.2	
I <sub>O</sub> §		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-30		-112	mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V			80	110	mA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.

# SN74ALS870 DUAL 16-BY-4 REGISTER FILES

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## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = MIN to MAX†		UNIT
			MIN	MAX	
t <sub>a(A)</sub>	Any A	Any DQ	3	19	ns
t <sub>a(S)</sub>	S0	Any DQA	3	15	ns
	S1	Any DQB	3	15	
t <sub>dis</sub>	S2	Any DQA	3	14	ns
	S3	Any DQB	3	14	
t <sub>en</sub>	S2	Any DQA	3	17	ns
	S3	Any DQB	3	17	
t <sub>pd</sub>	$\overline{W}$	Any DQ	5	23	ns
	DQA	DQB	5	26	
	DQB	DQA	5	26	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN74ALS870 DUAL 16-BY-4 REGISTER FILES

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74ALS870DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS870DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS870DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS870DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS870DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS870DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS870NSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS870NSRE4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS870NSRG4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS870NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS870NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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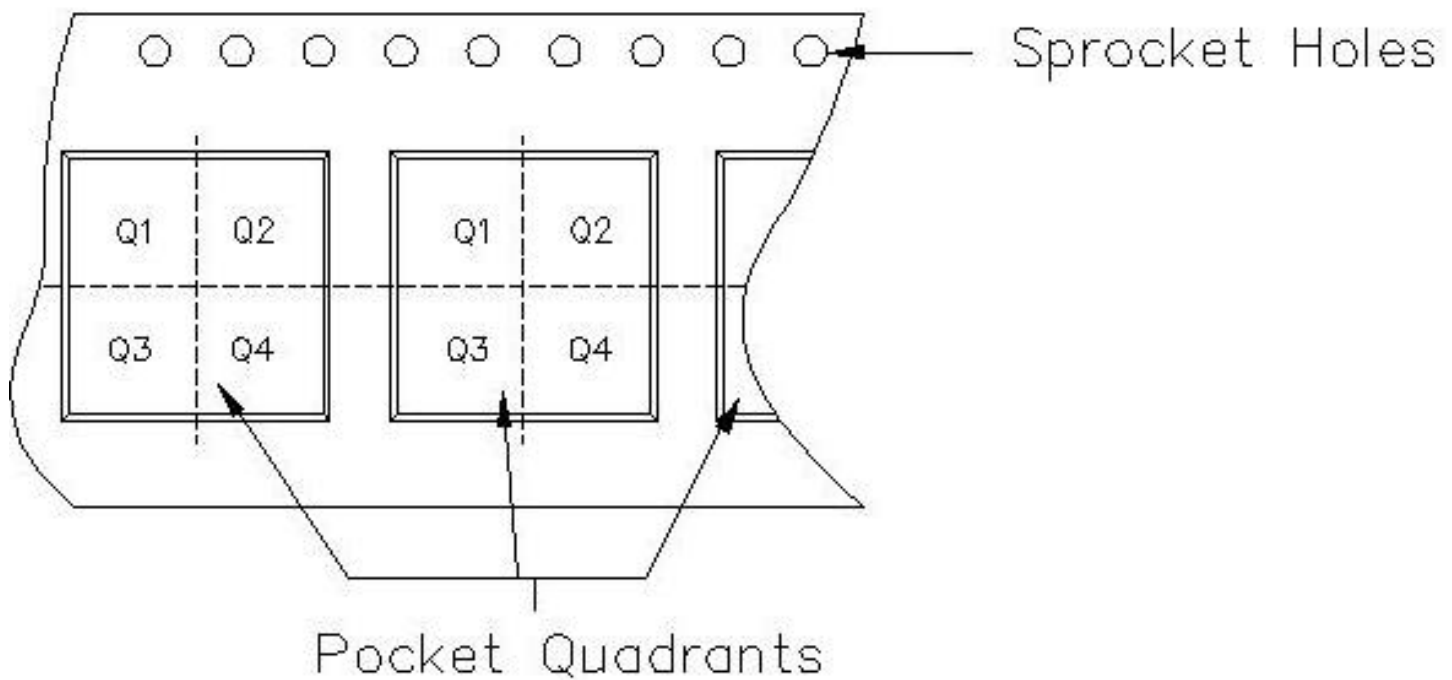
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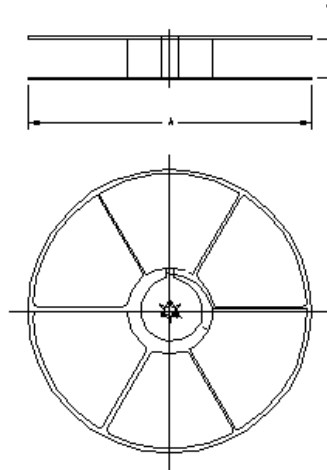
Carrier tape design is defined largely by the component length, width, and thickness.

$A_o$ = Dimension designed to accommodate the component width.
$B_o$ = Dimension designed to accommodate the component length.
$K_o$ = Dimension designed to accommodate the component thickness.
$W$ = Overall width of the carrier tape.
$P$ = Pitch between successive cavity centers.



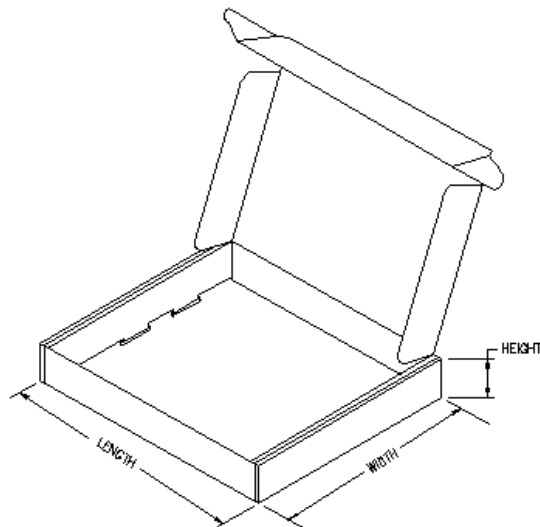
**TAPE AND REEL INFORMATION**

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS870DWR	DW	24	TAI	330	24	10.75	15.7	2.7	12	24	Q1
SN74ALS870NSR	NS	24	MLA	330	24	8.2	15.4	2.5	12	24	Q1



**TAPE AND REEL BOX INFORMATION**

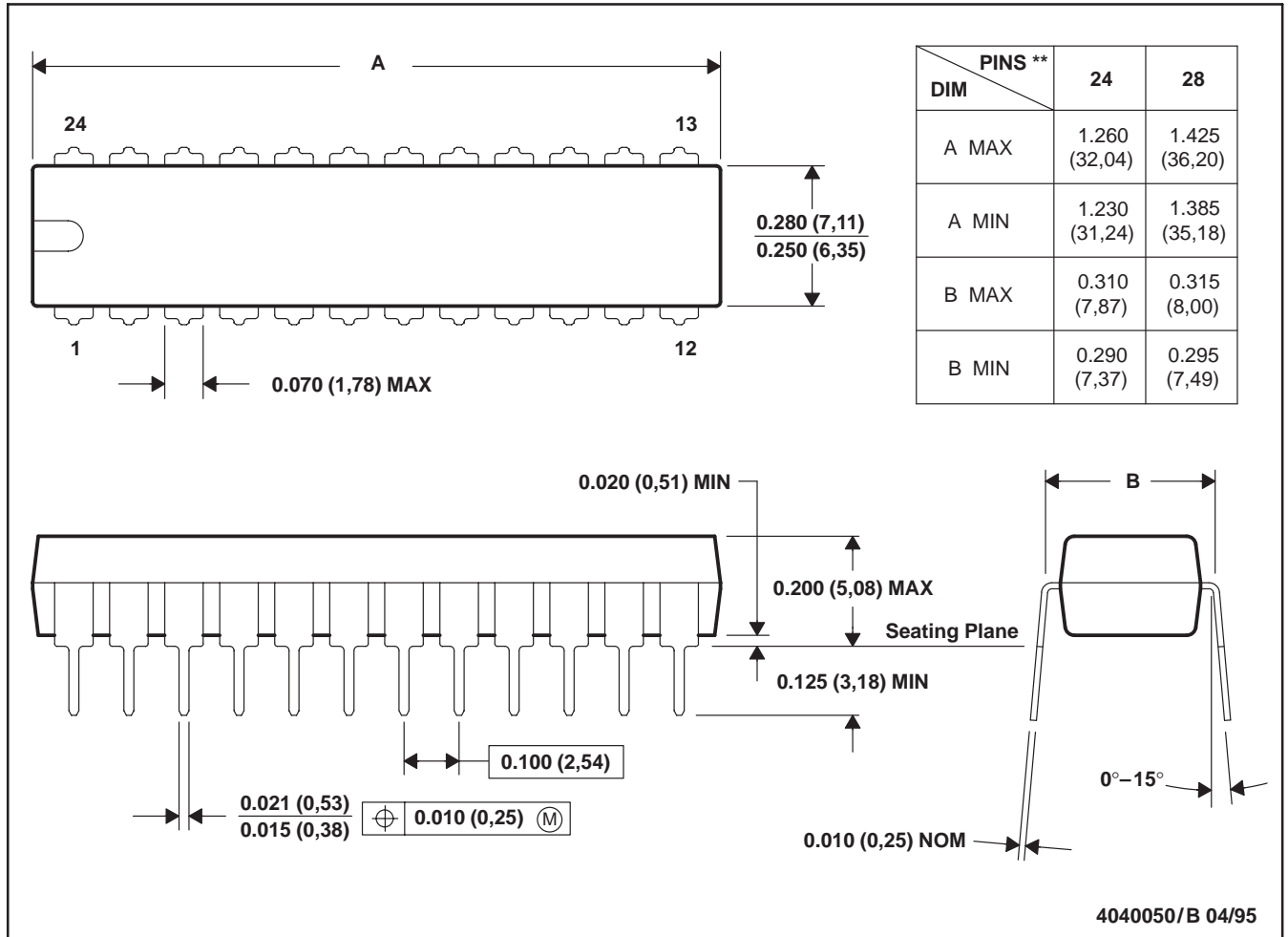
Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74ALS870DWR	DW	24	TAI	346.0	346.0	41.0
SN74ALS870NSR	NS	24	MLA	346.0	346.0	41.0



NT (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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