



**THE DATASHEET OF
SN74LVTH2952DWRG4**

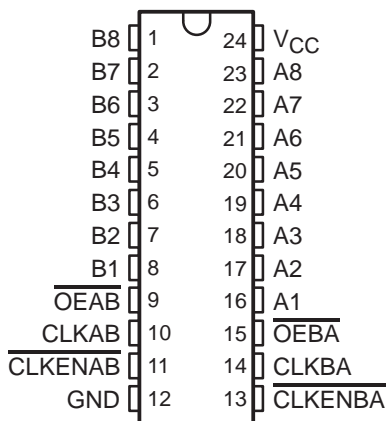


SN54LVTH2952, SN74LVTH2952 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

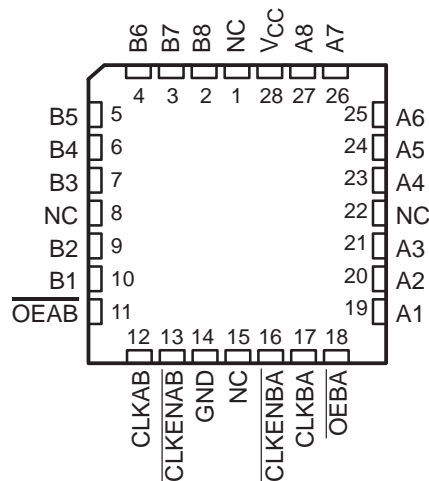
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- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus-Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

SN54LVTH2952 . . . JT PACKAGE
SN74LVTH2952 . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LVTH2952 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These octal bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – DW	Tube	SN74LVTH2952DW	LVTH2952
		Tape and reel	SN74LVTH2952DWR	
	SOP – NS	Tape and reel	SN74LVTH2952NSR	LVTH2952
	SSOP – DB	Tape and reel	SN74LVTH2952DBR	LK952
		Tube	SN74LVTH2952PW	
	TVSOP – DGV	Tape and reel	SN74LVTH2952DGV	LK952
Tape and reel		SN74LVTH2952PWR		
-55°C to 125°C	CDIP – JT	Tube	SNJ54LVTH2952JT	SNJ54LVTH2952JT
	LCCC – FK	Tube	SNJ54LVTH2952FK	SNJ54LVTH2952FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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SN54LVTH2952, SN74LVTH2952

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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description/ordering information

The LVTH2952 devices consist of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input, provided that the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low. Taking the output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE†

INPUTS				OUTPUT
$\overline{\text{CLKENAB}}$	CLKAB	$\overline{\text{OEAB}}$	A	B
H	X	L	X	B_0^\ddagger
X	H or L	L	X	B_0^\ddagger
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar, but uses $\overline{\text{CLKENBA}}$, CLKBA, and $\overline{\text{OEBA}}$.

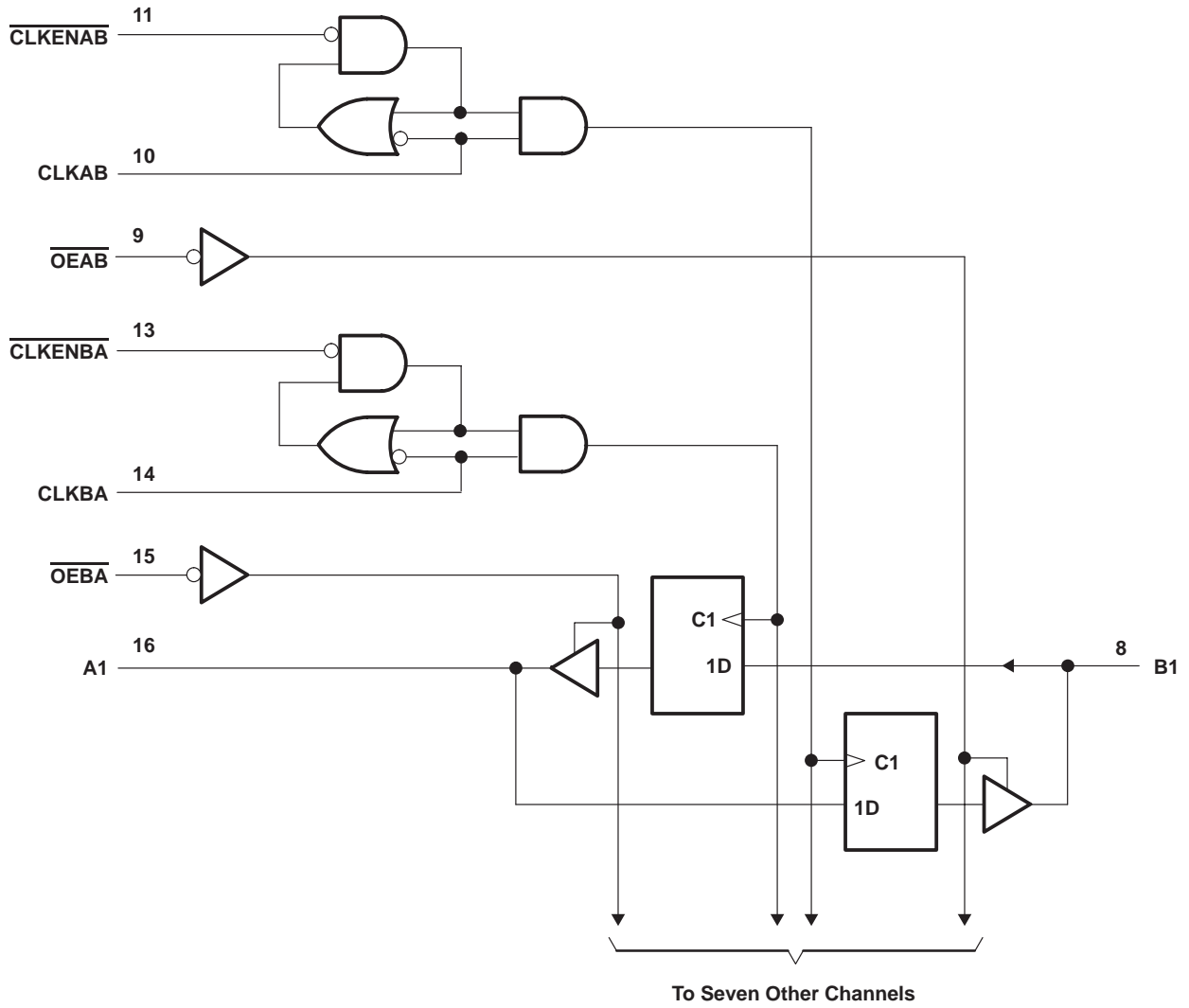
‡ Level of B before the indicated steady-state input conditions were established



SN54LVTH2952, SN74LVTH2952 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, JT, NS, and PW packages.

SN54LVTH2952, SN74LVTH2952

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH2952	96 mA
SN74LVTH2952	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH2952	48 mA
SN74LVTH2952	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	63°C/W
DGV package	86°C/W
DW package	46°C/W
NS package	65°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

	SN54LVTH2952		SN74LVTH2952		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage		5.5		5.5	V
I_{OH} High-level output current		–24		–32	mA
I_{OL} Low-level output current		48		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$ Power-up ramp rate			200	200	μs/V
T_A Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LVTH2952, SN74LVTH2952 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH2952		SN74LVTH2952		UNIT		
				MIN	TYP†	MAX	MIN		TYP†	MAX
V_{IK}		$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$		-1.2		-1.2		V		
V_{OH}		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$		$V_{CC}-0.2$		V		
		$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4		2.4				
		$V_{CC} = 3\text{ V}$		$I_{OH} = -24\text{ mA}$		2			$I_{OH} = -32\text{ mA}$	
V_{OL}		$V_{CC} = 2.7\text{ V}$		$I_{OL} = 100\text{ }\mu\text{A}$		0.2		0.2		
				$I_{OL} = 24\text{ mA}$		0.5		0.5		
		$V_{CC} = 3\text{ V}$		$I_{OL} = 16\text{ mA}$		0.4		0.4		
				$I_{OL} = 32\text{ mA}$		0.5		0.5		
				$I_{OL} = 48\text{ mA}$		0.55				
				$I_{OL} = 64\text{ mA}$				0.55		
I_I		Control inputs $V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND $V_{CC} = 0$ or 3.6 V , $V_I = 5.5\text{ V}$		± 1		± 1		μA		
				10		10				
		A or B ports‡ $V_{CC} = 3.6\text{ V}$		$V_I = 5.5\text{ V}$		20			20	
				$V_I = V_{CC}$		1			1	
		$V_I = 0$		-5		-5				
I_{off}		$V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V				± 100		μA		
$I_{I(hold)}$		A or B ports $V_{CC} = 3\text{ V}$		$V_I = 0.8\text{ V}$		75		75		
				$V_I = 2\text{ V}$		-75		-75		
		$V_{CC} = 3.6\text{ V}\S$, $V_I = 0$ to 3.6 V				± 500		μA		
I_{OZPU}		$V_{CC} = 0$ to 1.5 V , $V_O = 0.5\text{ V}$ to 3 V , $OE = \text{don't care}$		$\pm 100^*$		± 100		μA		
I_{OZPD}		$V_{CC} = 1.5\text{ V}$ to 0 , $V_O = 0.5\text{ V}$ to 3 V , $OE = \text{don't care}$		$\pm 100^*$		± 100		μA		
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND		Outputs high		0.19		0.19		
				Outputs low		5		5		
				Outputs disabled		0.19		0.19		
$\Delta I_{CC}\P$		$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND		0.2		0.2		mA		
C_i		$V_I = 3\text{ V}$ or 0		4		4		pF		
C_{io}		$V_O = 3\text{ V}$ or 0		9		9		pF		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused terminals at V_{CC} or GND

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

P This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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SN54LVTH2952, SN74LVTH2952

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timing requirement over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVTH2952				SN74LVTH2952				UNIT
		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	150		150		150		150		MHz
t _w	Pulse duration	CLK high	3.3	3.3	3.3	3.3	3.3	3.3	3.3	ns
		CLK low	3.3	3.3	3.3	3.3	3.3	3.3	3.3	
t _{su}	Setup time	A or B before CLK↑	Data high	1.6	2.2	1.5	2.1	1.5	2.1	ns
			Data low	1.6	2.2	1.5	2.1	1.5	2.1	
		CE̅ before CLK↑	Data high	1.6	1.9	1.5	1.8	1.5	1.8	
			Data low	2	2.6	1.9	2.5	1.9	2.5	
t _h	Hold time	A or B after CLK↑	1	0.2	1	0.2	1	0.2	ns	
		CE̅ after CLK↑	1.2	0.2	1.2	0.2	1.2	0.2		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

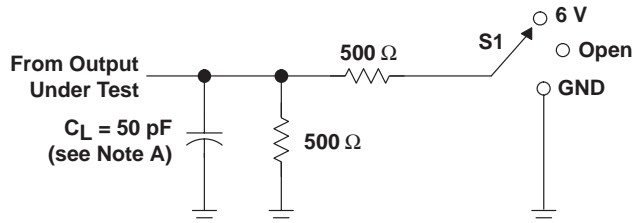
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH2952				SN74LVTH2952				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f _{max}			150		150		150		150		MHz	
t _{PLH}	CLKBA or CLKAB	A or B	1.2	4.8	5.5		1.3	2.9	4.6	5.3		ns
t _{PHL}			1.2	4.8	5.5		1.3	3.1	4.6	5.3		
t _{PZH}	OEBA or OEAB	A or B	1	4.8	5.9		1.1	2.6	4.6	5.8		ns
t _{PZL}			1	4.8	5.9		1.1	3	4.6	5.8		
t _{PHZ}	OEBA or OEAB	A or B	1.2	5.6	6		1.3	3.6	5.4	5.9		ns
t _{PLZ}			1.5	5.4	5.6		1.6	3.6	5.1	5.3		

† All typical values are at T_A = 25°C.

SN54LVTH2952, SN74LVTH2952 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

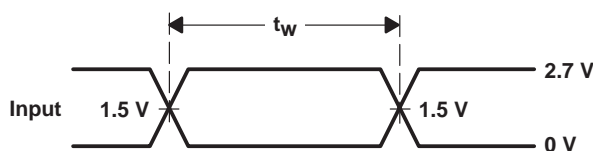
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PARAMETER MEASUREMENT INFORMATION

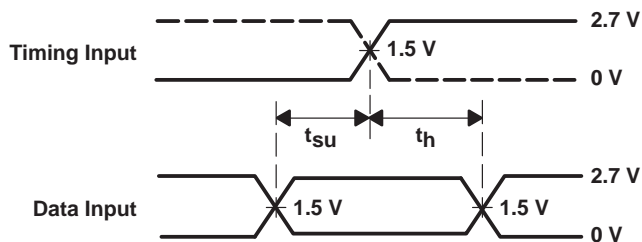


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

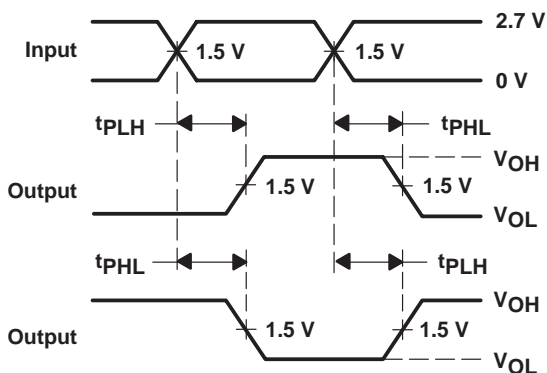
LOAD CIRCUIT FOR OUTPUTS



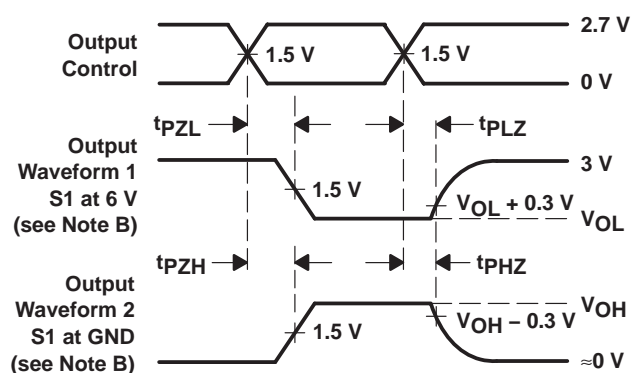
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVTH2952DW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH2952	Samples
SN74LVTH2952PW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LK952	Samples
SN74LVTH2952PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LK952	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH2952PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH2952PWR	TSSOP	PW	24	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVTH2952DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVTH2952PW	PW	TSSOP	24	60	530	10.2	3600	3.5

DW (R-PDSO-G24)

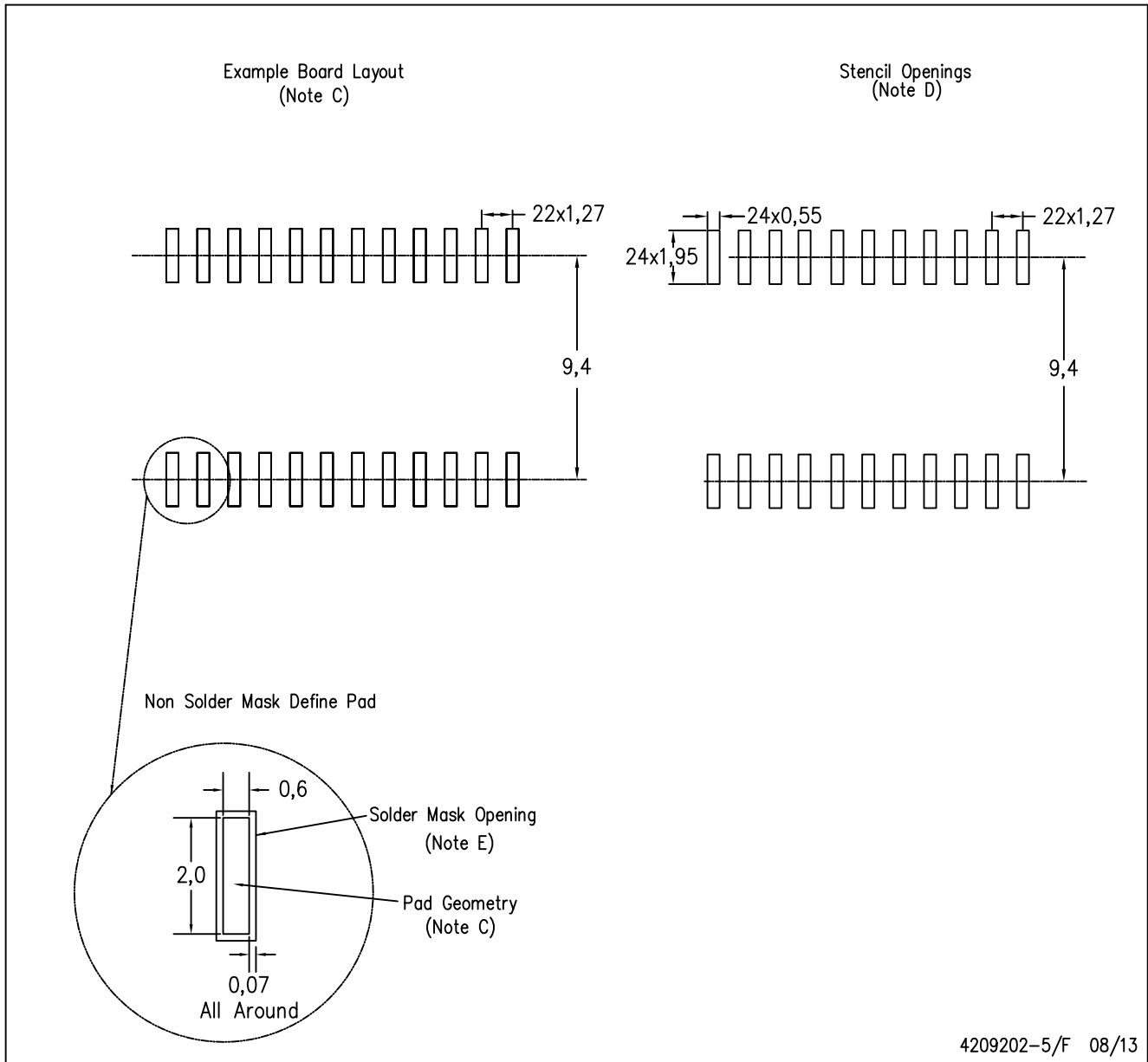
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



4209202-5/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

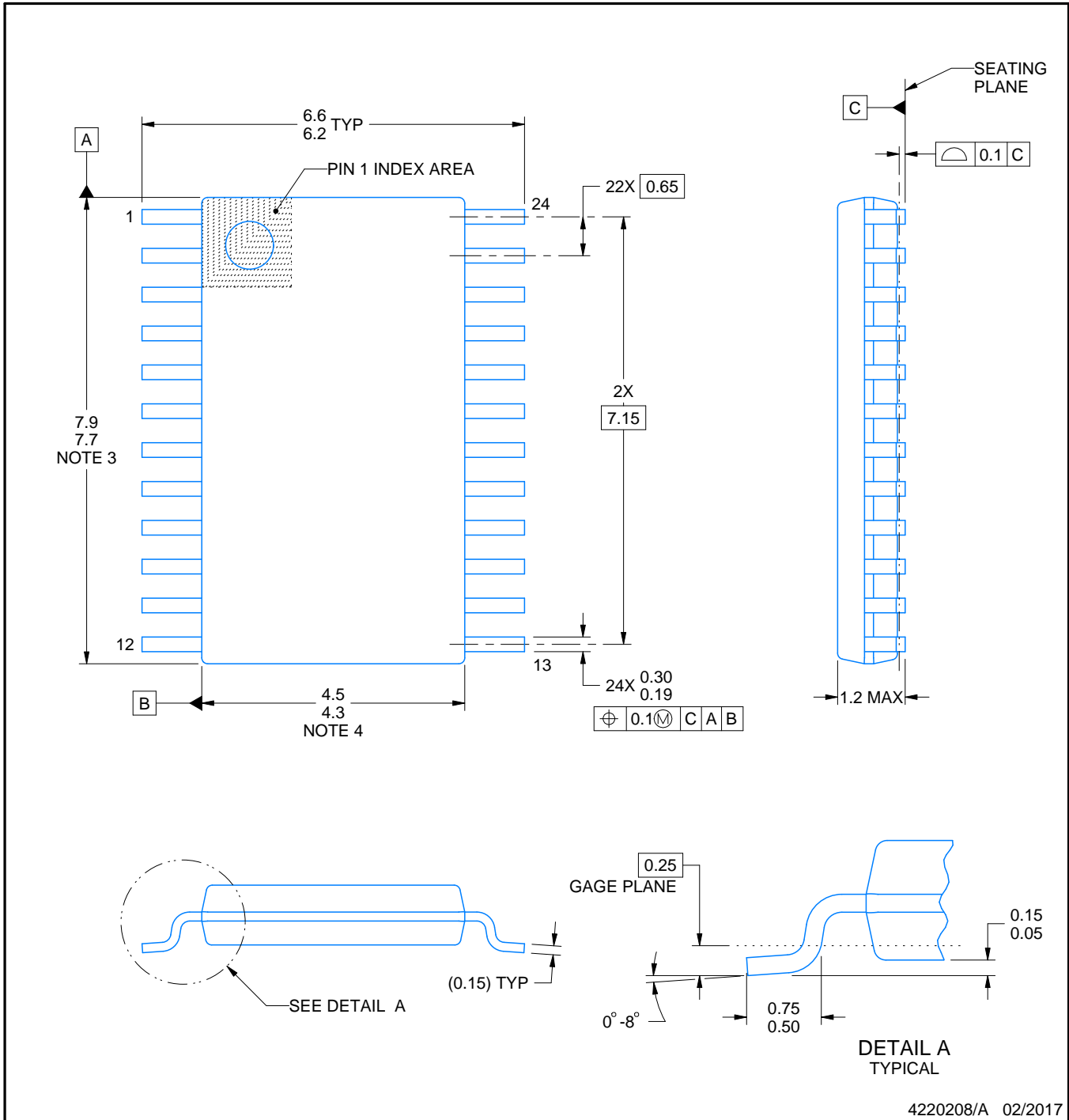
PW0024A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

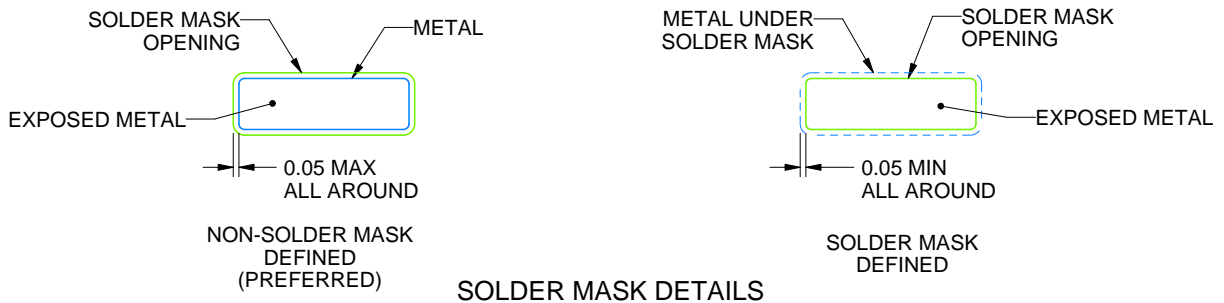
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

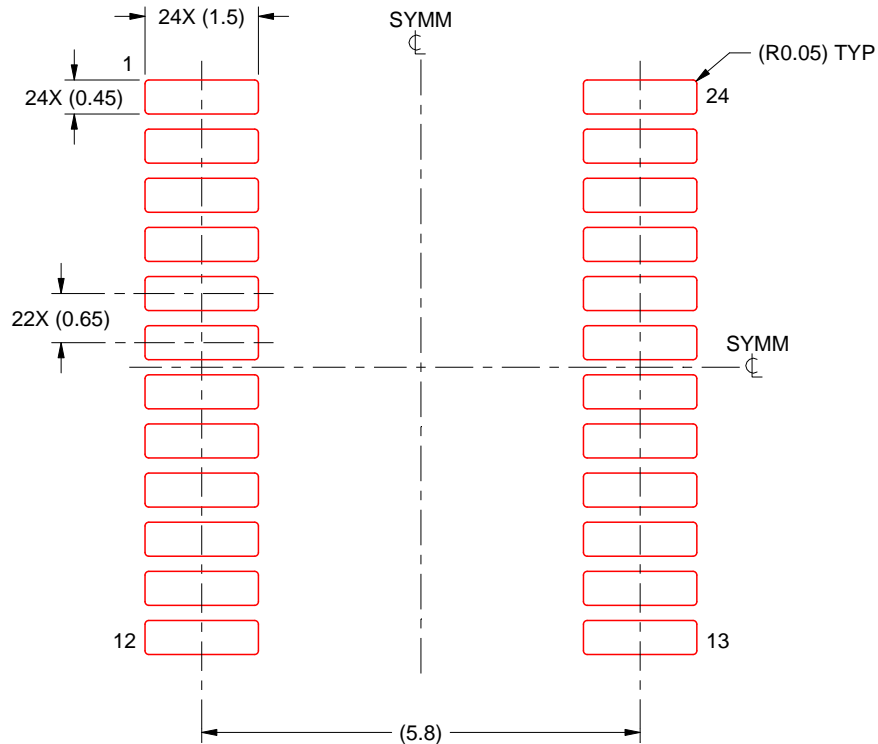
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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