



**THE DATASHEET OF  
SN74LVC8T245MDWREP**



# Logic Guide



**Logic Products**



# Logic Guide

## Introduction and Contents

### Introduction

As the world leader in logic, Texas Instruments (TI) offers a full spectrum of logic functions and technologies that range from the mature bipolar and bipolar complementary metal-oxide semiconductor (BiCMOS) families to the latest advanced-CMOS families. TI offers process technologies with the logic performance and features needed in today's electronic markets while maintaining support for traditional logic products.

TI's product offerings include the following process technologies or device families:

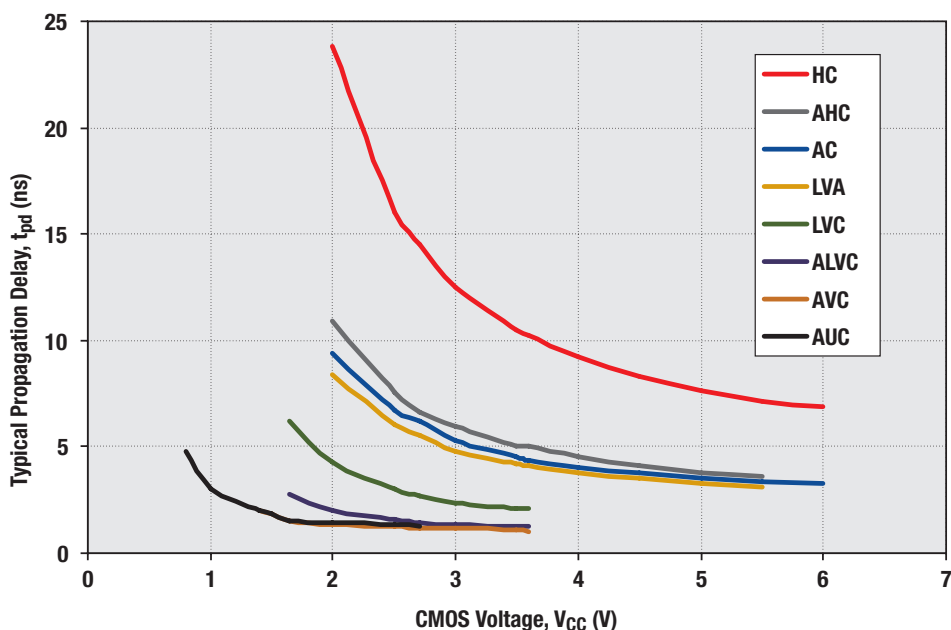
- AC, ACT, AHC, AHCT, ALVC, AUC, AUP, AVC, FCT, HC, HCT, LV-A, LV-AT, LVC, TVC
- ABT, ABTE, ALB, ALVT, BCT, HSTL, LVT, LV1T, LV4T
- FB, VME
- ALS, AS, F, LS, S, TTL

Today's applications are evolving with greater functionality and smaller size. TI's goal is to help designers easily find the ideal logic technology or function they need. Logic families are offered at every price/performance node along with benchmark delivery, reliability, and worldwide support. TI maintains a firm commitment to remain in the market with both leading-edge and mature logic lines.

Logic suppliers have historically focused on speed and low power as the priorities for product family improvement. As shown below, improved performance is offered by many new TI product technologies such as AUC (1.8 V) and ALVC (3.3 V) depending on operating voltage requirements. Other technologies such as AUP focus on delivering "best-in-class" low-power performance.

Data sheets can be downloaded from the TI Web site at [www.ti.com](http://www.ti.com) or ordered through your local sales office or TI authorized distributor. (See back cover.)

### CMOS Voltage vs. Speed



### Table of Contents

#### Logic Guide 2017

2 Introduction and Contents

#### Logic Overview

3 World of TI Logic  
 4 IC Basics  
 5 Automotive Logic  
 6 Introducing the Next Generation QFN packaging  
 7 Technology Functions Matrix

#### Logic Families

8 AUC  
 8 AUP  
 9 ALVC  
 9 AUP1T  
 9 AVC  
 10 LV1T/LV4T  
 10 LVC/LVC1G  
 11 AC/ACT  
 11 AHC/AHCT  
 11 HC/HCT  
 12 LV-A/LV-AT  
 12 ALB  
 12 ALVT  
 13 LVT  
 13 ABT/ABTE  
 13 ALS/AS/S/LS  
 14 BCT  
 14 F  
 15 FCT  
 15 TTL  
 15 CD4000

#### Resources

16 Package Options  
 17 Related Logic Resources  
 19 TI Worldwide Technical Support

# Logic Overview

## World of TI Logic

Some logic families have been in the marketplace for years, the oldest is well into its fifth decade. The following section gives the logic user a visual guide to the technology families that are available and their optimal voltage levels.

### 0.8-V Logic

AUC, AUP

### 1.2-V Logic

AUC, AUP, AVC

### 1.5-V Logic

AUC, AUP, AVC

### 1.8-V Logic

ALVC, AUC, AUP, AVC, LVC, LV1T

### 2.5-V Logic

ALVC, ALVT, AUC, AUP, AVC,  
LV, LV1T, LV-A, LVC

### 3.3-V Logic

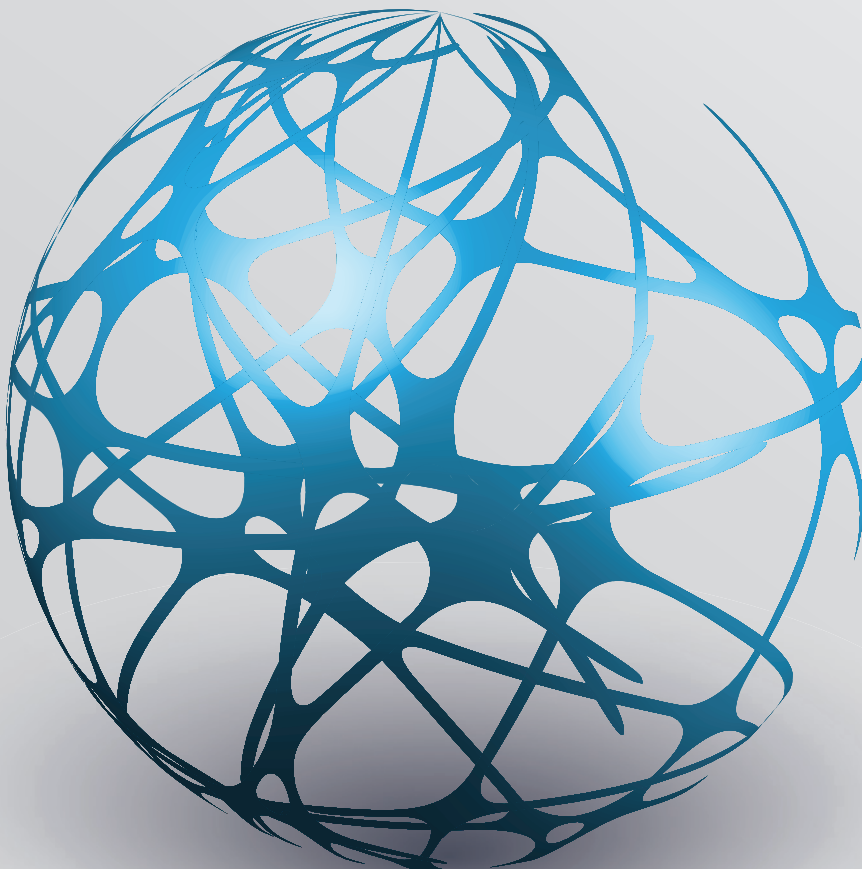
AC, AHC, ALB, ALVC, ALVT,  
AUP, AVC, LV, LV-A,  
LVC, LVT, LV1T, AUP1T

### 5-V Logic

ABT, AC/ACT, AHC, AHCT, ALS,  
AS, BCT, F, LV, LV1T, LV-A,  
LS, S, TTL, CD4000, FCT2

### 5-V+ Logic

CD4000

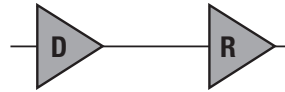


# Logic Overview

## IC Basics: Comparison of Switching Standards

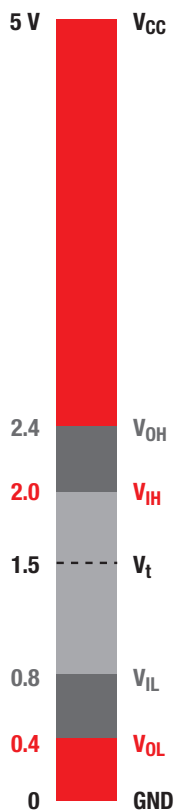
Shown below are the switching input/output comparison table and graphic that illustrate  $V_{IH}$  and  $V_{IL}$ , which are the minimum switching levels for guaranteed operation.  $V_t$  is the approximate switching level and the  $V_{OH}$  and  $V_{OL}$  levels are the guaranteed outputs for the  $V_{CC}$  specified.

Is  $V_{OH}$  higher than  $V_{IH}$ ?  
Is  $V_{OL}$  less than  $V_{IL}$ ?

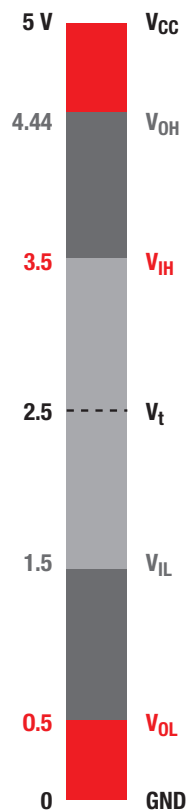


D \ R	5 TTL	5 CMOS	3 LVTTTL	2.5 CMOS	1.8 CMOS
5 TTL	Yes	No	Yes*	Yes*	Yes*
5 CMOS	Yes	Yes	Yes*	Yes*	Yes*
3 LVTTTL	Yes	No	Yes	Yes*	Yes*
2.5 CMOS	Yes	No	Yes	Yes	Yes*
1.8 CMOS	No	No	No	No	Yes*

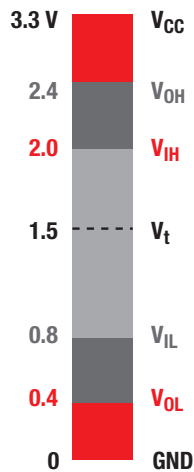
\* Requires  $V_{IH}$  Tolerance



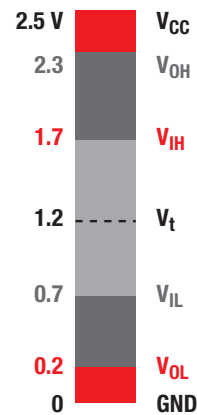
**5-V TTL**  
Standard TTL: ABT, AHCT, HCT, ACT, bipolar, LV1T, LV4T



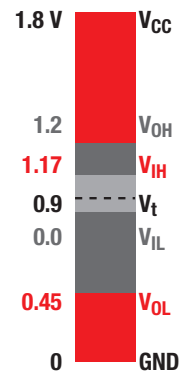
**5-V CMOS**  
Rail-to-Rail 5 V HC, AHC, AC, LV-A, LV1T, LV4T



**3.3-V LVTTTL**  
LVT, LV1T, LV4T, LVC, ALVC, AUP, LV-A, ALVT



**2.5-V CMOS**  
AUC, AUP, AVC, ALVC, LVC, ALVT, LV1T, LV4T



**1.8-V CMOS**  
AUC, AUP, AVC, ALVC, LVC, LV1T, LV4T

# Logic Overview

## Automotive Logic

Texas Instruments (TI) offers a vast portfolio of automotive logic products that are compliant to the AEC-Q100 standard. These devices are applicable for automotive, industrial, and high-reliability systems and come with world-class support.

### Breadth of Product Functions

TI's automotive logic products include a wide range in functionality in both standard logic and little logic functions such as single-, dual- and triple-gates. With more than 125 different standard gate functions and close to 40 little logic functions, TI has one of the most comprehensive portfolios for automotive logic in the industry. This gives automotive system designers the flexibility to choose the functions they need for their target systems.

### Package Offerings

TI's packaging options for logic products range from standard SOIC and TSSOP packages to small-form-factor SC70 and SOT-23 packages. These logic products are suitable for a wide spectrum of automotive applications.

### Benchmark Lead Times

With a vast network of worldwide wafer fabs and assembly/test sites, TI supports automotive customers with benchmark product lead times. Most TI automotive logic product lead times are six weeks or less.

### Quality Control

All logic products go through a tightly controlled manufacturing process that

includes quality-control checks geared to achieve the zero-DPPM requirements of automotive OEMs.

### Reliability

TI's design-flow checks ensure that all automotive logic products meet or exceed long-term reliability expectations.

### Supply Continuity

TI has a solid track record of supply continuity. TI's first logic products were introduced in 1964 and are still in production and supported. Automotive grade products have been in production and supported since 1984.

For the full list of TI's automotive logic products, please visit [www.ti.com/logic](http://www.ti.com/logic)

## Start Your Future Automotive Designs with TI Logic



# Logic Overview

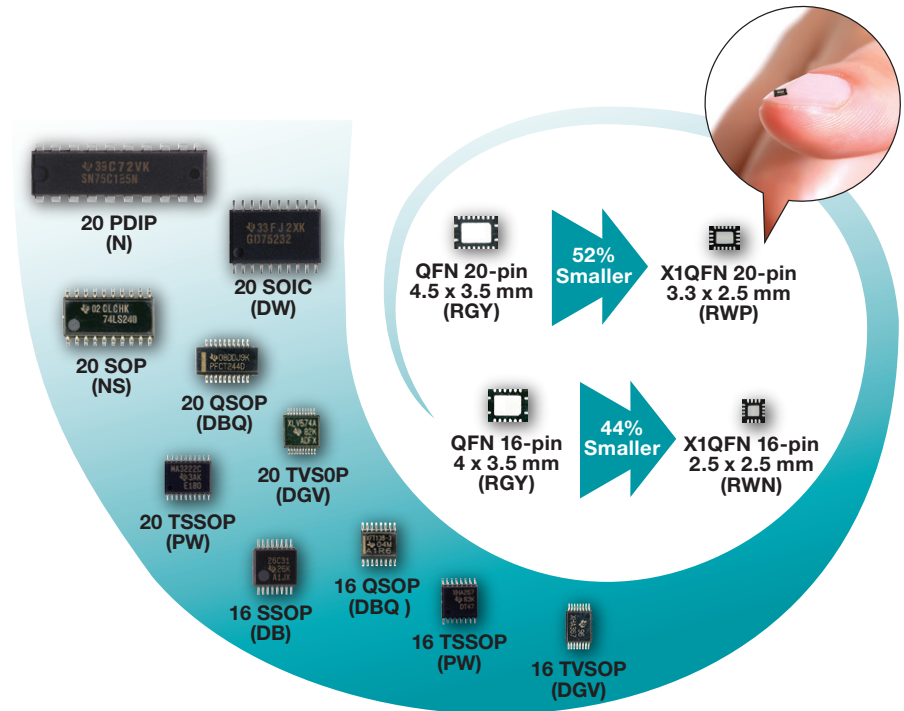
## Introducing the Next Generation QFN Packaging

### New Packaging for Space-Constrained Applications

TI's premier packaging portfolio allows for logic devices to be incorporated into small form factors such as the ever-shrinking wearables, mobile devices, home automation, as well as healthcare and fitness devices. Any customer planning to fit advanced logic functions into space constrained applications will find the X1QFN and X2SON packages to be a valuable resource for new designs.

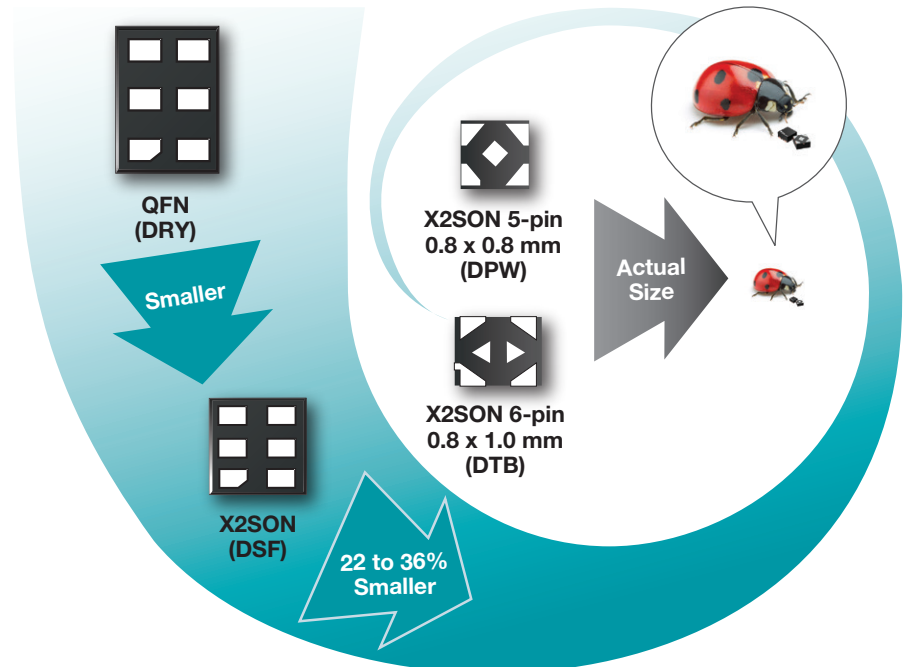
#### X1QFN NEW

X1QFN is a new advanced packaging series available for 14-, 16-, and 20-pin devices offered by Texas Instruments (TI) with a lower propagation delay and wider operating temperature than any other QFN package. The 14-pin X1QFN is just 2.5 x 2.1 x 0.5 mm with 0.4-mm pitch, a major revolution in the industry for small-scale packages. Such small package sizes were previously only offered for little logic functions such as single-, dual- and triple-gates, but with aggressive die shrinking, TI has brought multi-gate functions to this advanced small-scale package.



#### X2SON NEW

TI is not only investing in standard logic space, but also in popular little logic functions. TI has released the newest and smallest next generation X2SON package (a.k.a. X2QFN) for 5-pin and 6-pin devices. The 5-pin DPW package is just 0.8 x 0.8 x 0.4 mm (0.5-mm pitch), whereas the 6-pin DTB package is only 0.8 x 1.0 x 0.4 mm (0.4-mm pitch).



# Logic Overview

## Technology Function Matrix

Families	Voltage	Functions												Special Features						Process		
		Buffers/Line Drivers	Configurable Logic	Flip-Flops	Combination Logic	Counters	Shift Registers	Encoders/Decoders	Digital Comp/Parity Gen.	Gates	Transceivers	Level Translators	Phase Lock Loops	Bus-Hold	Series Damping Resistors	I <sub>prf</sub> (Partial Power Down)	Schmitt Triggers	Overvoltage-tolerant Inputs	Power-off Output Disable	Power-up 3-State	Bipolar	CMOS
AUC	0.8, 1.8, 2.5	✓		✓				✓	✓	✓	✓				✓	✓	✓	✓			✓	
AUP	0.8, 1.8, 3.3	✓	✓	✓					✓ <sup>1</sup>	✓					✓	✓	✓ <sup>1</sup>	✓ <sup>1</sup>			✓ <sup>1</sup>	
ALVC	1.8, 3.3	✓		✓					✓	✓	✓		✓	✓	✓	✓					✓	
AUP1T	1.8, 3.3	✓							✓		✓ <sup>1</sup>				✓	✓	✓ <sup>1</sup>	✓ <sup>1</sup>			✓ <sup>1</sup>	
AVC	1.8, 3.3	✓		✓						✓	✓ <sup>1</sup>		✓	✓	✓		✓ <sup>1</sup>	✓ <sup>1</sup>			✓ <sup>1</sup>	
LV1T	1.8, 3.3, 5	✓							✓		✓				✓		✓				✓	
LVC	1.8, 3.3, 5	✓ <sup>1</sup>	✓ <sup>1</sup>	✓ <sup>1</sup>	✓ <sup>1</sup>			✓ <sup>1</sup>	✓	✓	✓ <sup>1</sup>		✓	✓	✓	✓ <sup>1</sup>	✓ <sup>1</sup>	✓ <sup>1</sup>	✓		✓ <sup>1</sup>	
AC	3.3, 5	✓ <sup>1</sup>		✓		✓	✓	✓	✓ <sup>1</sup>	✓	✓						✓				✓ <sup>1</sup>	
AHC	3.3, 5	✓ <sup>1</sup>		✓ <sup>1</sup>			✓ <sup>1</sup>	✓	✓ <sup>1</sup>	✓ <sup>1</sup>	✓					✓	✓ <sup>1</sup>				✓ <sup>1</sup>	
HC	3.3, 5	✓ <sup>1</sup>		✓ <sup>1</sup>		✓ <sup>1</sup>	✓ <sup>1</sup>	✓ <sup>1</sup>	✓	✓ <sup>1</sup>	✓	✓				✓					✓ <sup>1</sup>	
LV-A	3.3, 5	✓ <sup>1</sup>		✓ <sup>1</sup>		✓ <sup>1</sup>	✓ <sup>1</sup>	✓	✓	✓	✓	✓			✓	✓	✓ <sup>1</sup>	✓ <sup>1</sup>			✓ <sup>1</sup>	
ALB	3.3	✓								✓												✓
ALVT	3.3	✓		✓						✓			✓	✓	✓			✓	✓			✓
GTL	3.3									✓	✓						✓	✓	✓			✓
GTLP	3.3									✓	✓		✓		✓		✓	✓	✓			✓
LVT	3.3	✓ <sup>1</sup>		✓						✓ <sup>1</sup>			✓ <sup>1</sup>	✓	✓			✓ <sup>1</sup>	✓			✓ <sup>1</sup>
VME	3.3									✓			✓		✓			✓	✓			✓
ABT	5	✓ <sup>1</sup>		✓				✓		✓			✓	✓				✓ <sup>1</sup>	✓ <sup>1</sup>			✓ <sup>1</sup>
ABTE	5									✓												✓
ACT	5	✓ <sup>1</sup>		✓ <sup>1</sup>		✓	✓	✓	✓	✓ <sup>1</sup>	✓	✓	✓				✓				✓ <sup>1</sup>	
AHCT	5	✓ <sup>1</sup>		✓ <sup>1</sup>			✓	✓ <sup>1</sup>		✓ <sup>1</sup>	✓	✓				✓	✓ <sup>1</sup>				✓ <sup>1</sup>	
ALS	5	✓		✓		✓	✓	✓	✓	✓	✓									✓		
AS	5	✓		✓		✓	✓	✓	✓	✓	✓									✓		
BCT	5	✓		✓				✓		✓				✓						✓		✓
F	5	✓		✓		✓	✓	✓	✓	✓				✓						✓		
FB	5									✓					✓							✓
FCT	5	✓		✓		✓	✓	✓	✓	✓			✓								✓	
HCT	5	✓ <sup>1</sup>		✓ <sup>1</sup>		✓	✓	✓	✓	✓	✓	✓									✓ <sup>1</sup>	
LS	5	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓								✓		
LV-AT	5	✓		✓				✓		✓					✓		✓				✓	
S	5	✓		✓	✓	✓	✓	✓	✓	✓		✓				✓				✓		
TTL	5	✓		✓	✓		✓	✓	✓	✓						✓				✓		
CD4000	5, 10, 12 to 18	✓ <sup>1</sup>	✓	✓	✓	✓	✓ <sup>1</sup>	✓	✓	✓ <sup>1</sup>		✓ <sup>1</sup>	✓			✓					✓ <sup>1</sup>	

<sup>1</sup>Also available in automotive grade

For product details, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

# Logic Families

## AUC and AUP1G

### Advanced Ultra-Low-Voltage CMOS

#### AUC

##### Key Features

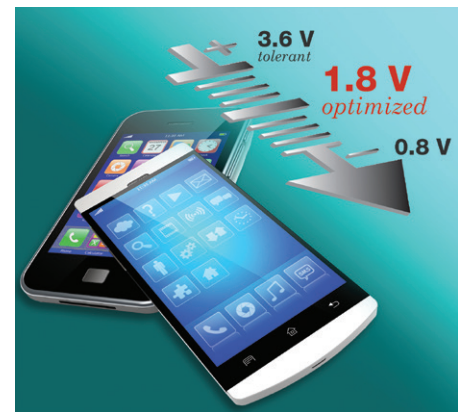
- 1.8-V optimized performance
- $V_{CC}$  specified at 2.5 V, 1.8 V, and 1.2 V
- 3.6-V I/O tolerance
- $I_{off}$  spec for partial power down
- ESD protection
- Low noise

##### Applications

- Telecommunications equipment
- High-performance workstations
- PCs and networking servers
- Portable consumer electronics

##### Packaging Options

- BGA MicroStar Junior™
- DSBGA
- LFBGA
- SC70
- SM8
- SON
- SOT-23
- SOT
- TSSOP
- TVSOP
- UQFN
- US8
- VQFN



##### AUC Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 1.8 V
SN74AUC1G125	2.7	-9/9	1.5
SN74AUC1G32	2.7	-9/9	1.5
SN74AUC245	2.7	-9/9	1.7
SN74AUC1G04	2.7	-9/9	1.2
SN74AUC1G17	2.7	-9/9	1.9

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

### Advanced Ultra-Low-Power

#### AUP

##### Key Features

- Low static-/dynamic-power consumption
- Wide  $V_{CC}$  operating range: 0.8 to 3.6 V
- Input hysteresis allows for slow input transition
- Best in class for speed-power optimization
- $I_{off}$  spec for partial power down
- ESD protection

##### Applications

- Mobile phones
- PDAs
- Digital and video cameras
- Digital photo frames
- Embedded PC
- Video communications system

##### Packaging Options

- DSBGA
- SC70
- SM8
- SON
- SOT-23
- SOT
- UQFN
- US8
- X2SON **NEW**



##### AUP Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 3.3 V	$I_{CC}$ ( $\mu$ A)
SN74AUP1G07	3.6	-4/4	3.3	0.9
SN74AUP1G34	3.6	-4/4	4.1	0.9
SN74AUP1G08	3.6	-4/4	4.3	0.9
SN74AUP1G32	3.6	-4/4	4.6	0.9
SN74AUP1G00	3.6	-4/4	4.8	0.9

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

# Logic Families

## ALVC, AUP1T and AVC

### Advanced Low-Voltage CMOS

#### ALVC

##### Key Features

- $V_{CC}$  specified at 3.3 V, 2.5 V, and 1.8 V
- Balanced drive
- Bus-hold option
- Low noise
- Damping resistor options
- ESD protection

##### Applications

- Automotive
- Memory Interfaces
- Datapath communication

##### Packaging Options

- BGA MicroStar Junior™
- LFBGA
- PDIP
- SO
- SOIC
- SSOP
- TSSOP
- TVSOP
- VQFN

##### ALVC Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 3.3 V
SN74ALVC125	3.6	-24/24	2.8
SN74ALVCH16373	3.6	-24/24	3.6
SN74ALVC164245	6	-24/24	5.8

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

### Advanced Ultra-Low-Power

#### AUP1T

##### Key Features

- Low voltage input switching levels of 1.8 V and 2.5 V allows for low threshold level
- Accepts 1.8-V to 2.5-V logic level for high or low
- Only requires a single voltage to achieve level shifting function
- $V_{CC}$  of either 2.5 V or 3.3 V

##### Applications

- Portable electronics
- Automotive
- Signal conditioning

##### Packaging Options

- DSBGA
- SON
- SC70
- SOT-23
- X2SON **NEW**



##### AUP1T Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 1.8 V	$I_{CC}$ ( $\mu$ A)
SN74AUP1T17	3.6	-4/4	10	0.9
SN74AUP1T08	3.6	-4/4	10.8	0.9
SN74AUP1T32	3.6	-4/4	10.8	0.9

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

### Advanced Very-Low-Voltage CMOS

#### AVC

##### Key Features

- $V_{CC}$  specified at 3.3 V, 2.5 V, and 1.8 V
- 3.3-V I/O tolerance
- Sub-2.0-ns max  $t_{pd}$  at 2.5 V
- Bus-hold option
- $I_{off}$  for partial power down
- Dynamic output control

##### Packaging Options

- BGA MicroStar Junior™
- DSBGA
- SC70
- SM8
- SOT-23
- SOT
- TSSOP
- TVSOP
- UQFN
- US8



##### AVC Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 3.3 V
SN74AVC16245	3.6	-12/12	1.7
SN74AVC16373	3.6	-12/12	2.8
SN74AVC16244	3.6	-12/12	3.5

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

# Logic Families

## LV1T/LV4T and LVC/LVCxG

### Low-Voltage CMOS Technology

#### LV1T/LV4T

##### Key Features

- Up/down translation with a single power rail
- Down translation from up to 5.5-V to  $V_{CC}$  level
- Optimized and balanced output drive (7 mA at 3.3-V  $V_{CC}$ )
- No need for damping resistor
- Lowered switching threshold

##### Applications

- Computing
- Wearables
- Personal electronics
- Automotive and industrial
- Notebook

##### Packaging Options

- SC70
- SOT-23
- TSSOP
- VQFN



#### LV1T/LV4T Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 3.3 V
SN74LV1T34	5.0	-8/8	8.0
SN74LV4T125	5.0	-16/16	5.5
SN74LV1T08	5.5	-8/8	5.5

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

### Low-Voltage CMOS

#### LVC/LVC1G

##### Key Features

- $V_{CC}$  specified at 5.5 V, 3.3 V, 2.5 V, and 1.8 V
- 5-V I/O tolerance
- Series damping resistor option
- $I_{off}$  spec for partial power down
- ESD protection

##### Applications

- Portable electronics
- Telecommunications equipment
- Networking servers
- Routing, clock buffering, and muxing
- Personal computing

##### Packaging Options

- BGA MicroStar Junior™
- CDIP
- CFP
- DSBGA
- LCCC
- LFBGA
- PDIP
- SC70
- SM8
- SO
- VQFN
- SOIC
- SON
- SOT/SOT-23
- X1QFN **NEW**
- SSOP
- TSSOP
- TVSOP
- UQFN
- US8
- USON
- X2SON **NEW**

#### LVC/LVC1xG Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 3.3 V
SN74LVC1G125	5.5	-32/32	4.5
SN74LVC245A	3.6	-24/24	6.3
SN74LVC14A	3.6	-24/24	6.4
SN74LVC1G08	5.5	-32/32	3.6

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

# Logic Families

## AC/ACT, AHC/AHCT and HC/HCT

### Advanced CMOS

#### AC/ACT

##### Key Features

- Balanced propagation delay
- Inputs are TTL-voltage compatible (ACT)
- Low power consumption
- ESD protection
- Center  $V_{CC}$  pin and GND configurations minimize high-speed switching noise

##### Applications

- Buffer registers
- Defense, aerospace
- Working registers
- I/O ports

##### Packaging Options

- CDIP
- CFP
- CPGA
- LCCC
- SO
- SOIC
- SSOP
- TSSOP
- PDIP

##### AC/ACT Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 5 V
SN74ACT245	5.5	-24/24	9.0
SN74AC373	6.0	-24/24	10.5
SN74ACT08	5.5	-24/24	10

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

### Advanced High-Speed CMOS

#### AHC/AHCT

##### Key Features

- Low noise without characteristic overshoot/undershoot
- Low power consumption
- Small propagation delay (5.5 ns)
- 5 V and input tolerance at 3.3 V
- Pin-for-pin compatibility

##### Applications

- Industrial
- Defense, aerospace
- Medical

##### Packaging Options

- CDIP
- CFP
- LCCC
- PDIP
- SC70
- SO
- SOIC
- SOT-23
- SOT
- SSOP
- TSSOP
- TVSOP
- VQFN

##### AHC/AHCT Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 5 V
SN74AHC245	5.5	-8/8	6.5
SN74AHC123A	5.5	-8/8	14
SN74AHC1G08	5.5	-8/8	7

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

### High-Speed CMOS

#### HC/HCT

##### Key Features

- Low noise without characteristic overshoot/undershoot
- Low power consumption
- Small propagation delay (5.5 ns)
- TTL voltage-compatible inputs (HCT)
- Balanced propagation delay and transition times
- Wide operating temperature

##### Applications

- Automotive
- Buffer/storage registers
- Frequency synthesis and multiplication
- Shift registers
- Pattern generators

##### Packaging Options

- CDIP
- CFP
- TSSOP
- TVSOP
- SO
- SOIC
- SSOP
- LCCC
- PDIP
- X1QFN **NEW**

##### HC/HCT Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 6 V
SN74HC245	6.0	-7.8/7.8	22
CD74HC123	6.0	-5.2/5.2	68
CD74HC164	6.0	-5.2/5.2	38

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

# Logic Families

## LV-A/LV-AT, ALB and ALVT

### Low Voltage

#### LV-A/LV-AT

##### Key Features

- $V_{CC}$  specified at 5.0 V, 3.3 V, and 2.5 V
- Inputs are TTL voltage compatible (LV-AT)
- 5-V I/O tolerance
- $I_{off}$  spec for partial power down
- ESD protection
- Low noise

##### Applications

- Portable electronics
- Buffer memory address registers
- Bidirectional bus drivers
- I/O ports

##### Packaging Options

- BGA MicroStar Junior™
- PDIP
- SO
- SOIC
- SSOP
- TSSOP
- TVSOP
- VQFN

#### LV-A/LV-AT Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 5 V
SN74LV245A	5.5	-16/16	8.5
SN74LV123A	5.5	-12/12	15
SN74LV244AT	5.5	-16/16	9.5

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

### Advanced Low-Voltage BiCMOS

#### ALB

##### Key Features

- State-of-the-art, advanced low-voltage BiCMOS technology design for 3.3-V operation
- Schottky diodes on all inputs to eliminate overshoot and undershoot
- Small high-speed switching noise
- Flow-through architecture that optimizes PCB layout

##### Applications

- Workstations
- Telecommunications equipment
- Advanced peripherals

##### Packaging Options

- SSOP
- TSSOP
- TVSOP



#### ALB Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 3.3 V
SN74ALB16244	3.6	-25/25	2.0
SN74ALB16245	3.6	-25/25	2.0

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

### Advanced Low-Voltage CMOS Technology

#### ALVT

##### Key Features

- $V_{CC}$  specified at 3.3 V and 2.5 V
- High-drive output: up to 64 mA
- 5-V I/O tolerance
- Power-up 3 state
- Partial power down ( $I_{off}$ )
- Hot insertion
- Bus hold

##### Applications

- Backplane
- Bus-driving
- Digital logic systems

##### Packaging Options

- BGA MicroStar Junior™
- LFBGA
- SSOP
- TSSOP
- TVSOP

#### ALVT Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 2.5 V
SN74ALVTHR16245	3.6	-12/12	4.3
SN74ALVTH16374	3.6	-32/64	3.8
SN74ALVTH162244	3.6	-12/12	4.2
SN74ALVTH16373	3.6	-32/64	4.2

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

# Logic Families

## LVT, ABT/ABTE and ALS/AS/S/LS

### Low-Voltage BiCMOS Technology

#### LVT

##### Key Features

- 5.5-V maximum input voltage
- Specified 2.7-V to 3.6-V supply voltage
- I/O structures support live insertion
- Rail-to-rail switching for driving CMOS
- $t_{pd} < 4.6$  ns
- Allows mixed-signal operation
- Low-input leakage current

##### Applications

- Computing
- Wearables
- Personal electronics
- Automotive and industrial

##### Packaging Options

- MicroStar BGA™
- BGA MicroStar Junior™
- CDIP
- CFP
- LCCC
- LFBGA
- LQFP
- SO
- SOIC
- SSOP
- TSSOP
- TVSOP
- VQFN

##### LVT Device Examples

Device	V <sub>CC</sub> (V)	Drive (mA)	t <sub>pd(MAX)</sub> (ns) at 3.3 V
SN74LVTH16245A	3.6	-32/64	3.3
SN74LVTH245A	3.6	-32/64	3.5
SN74LVTH16244A	3.6	-32/64	4.1
SN74LVTH125	3.6	-32/64	3.5

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

### Advanced BiCMOS Technology

#### ABT/ABTE

##### Key Features

- Low power dissipation
- ESD protection
- Distributed V<sub>CC</sub> and GND pin configuration minimizes high-speed noise
- Bus hold on data inputs eliminates the need for external pullup/pulldown resistors

##### Applications

- Buffer registers
- I/O ports
- Working registers

##### Packaging Options

- CDIP
- CFP
- LCCC
- LQFP
- PDIP
- SO
- SOIC
- SSOP
- TSSOP
- TVSOP
- QFN

##### ABT/ABTE Device Examples

Device	V <sub>CC</sub> (V)	Drive (mA)	t <sub>pd(MAX)</sub> (ns) at 5 V
SN74ABT245B	5.5	-32/64	3.9
SN74ABT125	5.5	-32/64	4.9
SN74ABT244A	5.5	-32/64	4.6

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

### Schottky Logic

#### ALS/AS/S/LS

##### Key Features

- PNP inputs reduce DC loading
- Hysteresis at inputs improves noise margins
- Low power consumption
- Short propagation delays and high clock frequencies
- Fully compatible with most TTL circuits
- Wide operating temperature

##### Applications

- Test and measurement
- Three-state memory address drivers
- Bus-oriented receivers/transceivers
- Balanced transmission lines

##### Packaging Options

- CDIP
- CFP
- LCCC
- PDIP
- SO
- SOIC
- SSOP
- TSSOP

##### ALS/AS/S/LS Device Examples

Device	V <sub>CC</sub> (V)	Drive (mA)	t <sub>pd(MAX)</sub> (ns) at 5 V
SN54ALS245A	5.5	-12/12	10
SN74ALS1034	5.5	-15/24	8.0
SN74AS373	5.5	-12/32	6.0
SN74LS07	5.5	40	30

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

# Logic Families

## BCT and F

### BiCMOS Technology

#### BCT

##### Key Features

- Low power consumption
- ESD protection
- Distributed  $V_{CC}$  and GND pins minimize noise generated by simultaneous switching of outputs
- Designed to facilitate incident-wave switching for line impedances of 25  $\Omega$  or greater
- Controlled baseline

##### Applications

- Asynchronous data bus communication
- 3-state memory address drivers
- Clock drivers
- Bus-oriented receivers and transmitters

##### Packaging Options

- CDIP
- CFP
- LCCC
- PDIP
- SO
- SOIC
- SSOP
- TSSOP

##### BCT Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 5 V
SN74BCT125A	5.5	-15/64	7.7
SN74BCT2245	5.5	-12/12	7.8
SN74BCT245	5.5	-15/64	7

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

### Fast Logic

#### F

##### Key Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Operational over the full military temperature range
- Fully synchronous operation for counting
- Fully independent clock circuit

##### Applications

- Stacked or pushdown registers
- Buffer storage
- Accumulator registers
- Asynchronous data bus communication

##### Packaging Options

- CDIP
- CFP
- LCCC
- PDIP
- SO
- SOIC
- SSOP

##### F Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 5 V
SN74F245	5.5	-15/64	7.0
SN74F373	5.5	-3/24	13
SN74F04	5.5	-1/20	6

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

# Logic Families

## FCT, TTL and CD4000

### Fast CMOS Technology

#### FCT

##### Key Features

- Edge-rate control circuitry for significantly improved noise characteristics
- $I_{off}$  supports partial-power-down mode operation
- ESD protection
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels

##### Applications

- Programmable dividers
- Transmission lines
- High-speed, low-power bus
- Bus interface

##### Packaging Options

- CDIP
- CFP
- LCC
- PDIP
- SOIC
- SSOP
- TSSOP

##### FCT Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 5 V
CD74FCT273	5.25	-15/48	13
CD74FCT245	5.25	-15/64	7.0

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

### Transistor-Transistor Logic

#### TTL

##### Key Features

- Synchronous operation
- Individual preset to each flip-flop
- Fully independent clear input
- Gated output-control lines for enabling or disabling the outputs
- Load control line
- Diode-clamped inputs
- High noise immunity
- Wide operating temperature

##### Applications

- High-speed counting designs
- Bus buffer register
- Interfacing with high-level circuits
- Driving high-current loads

##### Packaging Options

- CDIP
- CFP
- LCCC
- PDIP
- SO
- SOIC

##### TTL Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns) at 5 V
SN7407	5.25	40	30
SN7400	5.25	-0.4/16	5.0

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

### CMOS Logic

#### CD4000

##### Key Features

- Medium-speed operation:  $t_{PLH} = 60$  ns at  $V_{DD} = 10$  V
- Standardized, symmetrical output characteristics
- Separate serial outputs synchronous to both positive and negative clock edges for cascading

##### Applications

- Logical comparators
- Adders/subtractors
- Parity generators and checkers
- Serial-to-parallel data conversion
- Remote control holding register

##### Packaging Options

- CDIP
- CDIP SB
- CFP
- PDIP
- SO
- SOIC
- TSSOP












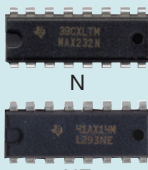





























##### CD4000 Device Examples

Device	$V_{CC}$ (V)	Drive (mA)	$t_{pd(MAX)}$ (ns)
CD4069UB	18	-6.8/6.8	60
CD40106B	18	-6.8/6.8	140
CD4011B	18	-6.8/6.8	120

For full product matrix, click this link for *Quick search* tab at [www.ti.com/logic](http://www.ti.com/logic)

# Resources

## Package Options

Pins	PDIP	SOIC	SOP	SSOP	QSOP	TSSOP	VSSOP
8	 P	 D	 PS	 DCT		 PW	
10							 DGS
14		 D	 NS	 DB		 PW	
16	 N NE	 D DW	 NS	 DB	 DBQ	 PW	
18	 N	 DW					
20	 N	 DW	 NS	 DB	 DBQ	 PW	
24	 NT	 DW	 NS	 DB	 DBQ	 PW	
28		 DW		 DB	 DL	 PW	
38						 DBT	
48				 DL		 DGG	
56				 DL		 DGG	
64						 DGG	

# Resources

## Package Options

Pins	TVSOP	SOT	QFN	MicroQFN (UQFN)	WCSP	XLGA	Pins	BGA
3		DBZ PK					8	YFP
4		DCY DZD			YFP YZV	YFM	12	ZXU
5		DBV DCK DRL DRT		<b>NEW</b> DPW	YZP YEA/YZA		20	ZXY VFBGA GQN/ZQN
6		DCK DBV DRL DRT DCQ	DRS	DRY DSF <b>NEW</b> DTB	YZP YFP YEA/YZA YFC		24	ZQS VFBGA GQL/ZQL
8		DCN	DRG DRJ	DQE RSE	YFP YZP YEA/YZA		48	ZAH ZQC
9					YFP		54	ZRD
10			DRC	RSE	YZP		56	VFBGA GQL/ZQL
12			RSF	RUE	YFC YZT		72	ZST
14	DGV		RGY	RUC			83	ZRG
16	DGV		RGT RGY RWN RTE	<b>NEW</b> RSV	YFP		96	VFBGA GKE/ZKE ZRL
20	DGV		RGW RGY RWP	<b>NEW</b> RUC	YFP		114	VFBGA GKF/ZKF
24	DGV		RTW RGE RHL RGE					
25					YFP			
30					YFC			
32			RGJ RSM RHB					
36			RHH					
42			RVA					
48	DGV							
56	DGV		RHU RGQ					
80	DBB							

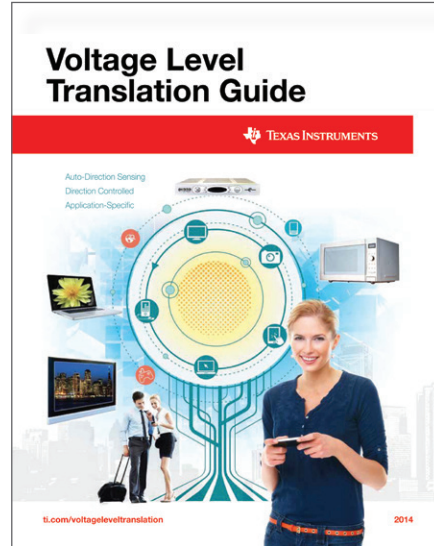
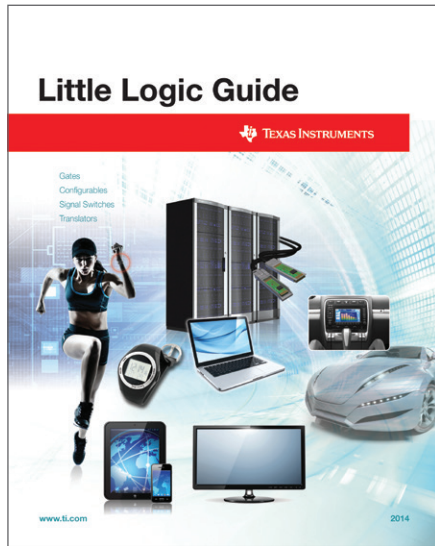
# Resources

## Related Logic Resources

**Little Logic Guide**  
[www.ti.com/lit/scyt129](http://www.ti.com/lit/scyt129)

**Voltage Translation Guide**  
[www.ti.com/lit/scyb018](http://www.ti.com/lit/scyb018)



**TI Logic and Linear Products**  
[www.ti.com/lit/slyc125](http://www.ti.com/lit/slyc125)



## Jump start your design process

- Comprehensive reference designs
- Complete schematics/block diagrams
- BOMs
- Design files and test reports

▶ Search by product type, application or keyword to find inspiration for your next design  
[www.ti.com/tidesigns](http://www.ti.com/tidesigns)



**TI E2E™**  
**Community**  
**engineer.to.engineer,**  
**solving problems**  
**e2e.ti.com**

## ***TI Worldwide Technical Support***

---

### **TI Support**

Thank you for your business. Find the answer to your support need or get in touch with our support center at

[www.ti.com/support](http://www.ti.com/support)

China: <http://www.ti.com.cn/guidedsupport/cn/docs/supporthome.tsp>

Japan: <http://www.tij.co.jp/guidedsupport/jp/docs/supporthome.tsp>

### **Technical support forums**

Search through millions of technical questions and answers at TI's E2E™ Community (engineer-to-engineer) at

[e2e.ti.com](http://e2e.ti.com)

China: <http://www.deyisupport.com/>

Japan: <http://e2e.ti.com/group/jp/>

### **TI Training**

From technology fundamentals to advanced implementation, we offer on-demand and live training to help bring your next-generation designs to life. Get started now at

[training.ti.com](http://training.ti.com)

China: <http://www.ti.com.cn/general/cn/docs/gencontent.tsp?contentId=71968>

Japan: <https://training.ti.com/jp>

**Important Notice:** The products and services of Texas Instruments Incorporated and its subsidiaries described herein are sold subject to TI's standard terms and conditions of sale. Customers are advised to obtain the most current and complete information about TI products and services before placing orders. TI assumes no liability for applications assistance, customer's applications or product designs, software performance, or infringement of patents. The publication of information regarding any other company's products or services does not constitute TI's approval, warranty or endorsement thereof.

**A011617**

The platform bar, E2E, MicroStar BGA, MicroStar Junior and NanoStar are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

## IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2017, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View SN74LVC8T245MDWREP](#) on WIN SOURCE

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management