



**THE DATASHEET OF
SN74BCT126AD**



SN54BCT126A, SN74BCT126A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCBS252A – SEPTEMBER 1988 – REVISED APRIL 1994

- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK) and Flatpacks (W), and Standard Plastic and Ceramic 300-mil DIPs (J, N)

description

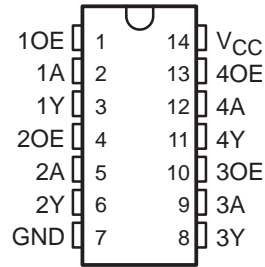
The 'BCT126A bus buffer features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

The SN54BCT126A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74BCT126A is characterized for operation from 0°C to 70°C .

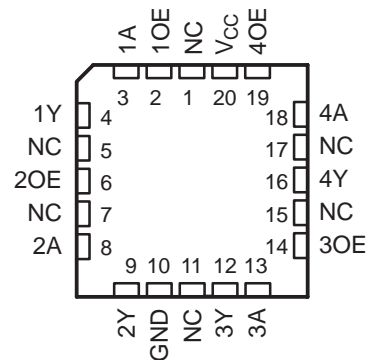
FUNCTION TABLE
(each buffer)

| INPUTS | | OUTPUT |
|--------|---|--------|
| OE | A | Y |
| H | H | H |
| H | L | L |
| L | X | Z |

SN54BCT126A . . . J OR W PACKAGE
SN74BCT126A . . . D OR N PACKAGE
(TOP VIEW)



SN54BCT126A . . . FK PACKAGE
(TOP VIEW)

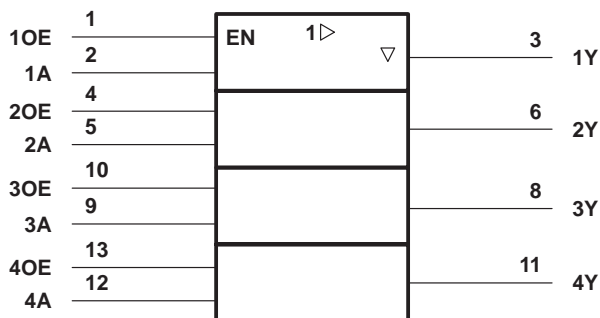


NC – No internal connection

SN54BCT126A, SN74BCT126A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

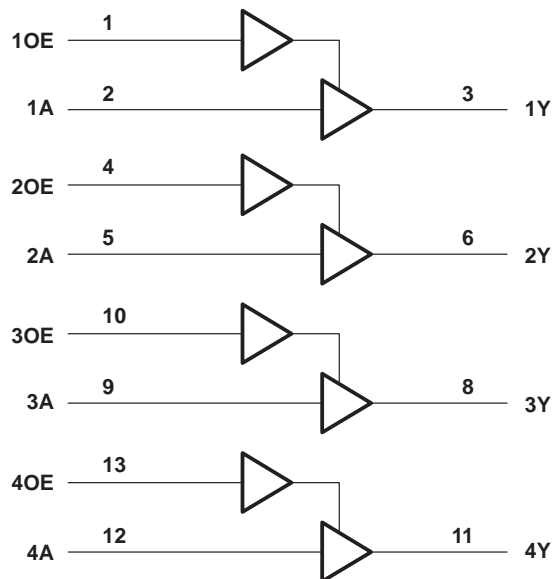
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|---------------------|
| Supply voltage range, V_{CC} | - 0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | - 0.5 V to 7 V |
| Voltage range applied to any output in the disabled or power-off state, V_O | - 0.5 V to 5.5 V |
| Voltage range applied to any output in the high state, V_O | - 0.5 V to V_{CC} |
| Current into any output in the low state: SN54BCT126A | 96 mA |
| SN74BCT126A | 128 mA |
| Operating free-air temperature range: SN54BCT126A | - 55°C to 125°C |
| SN74BCT126A | 0°C to 70°C |
| Storage temperature range | - 65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

| | SN54BCT126A | | | SN74BCT126A | | | UNIT |
|--------------------------------------|-------------|-----|-----|-------------|-----|-----|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I_{IK} Input clamp current | | | -18 | | | -18 | mA |
| I_{OH} High-level output current | | | -12 | | | -15 | mA |
| I_{OL} Low-level output current | | | 48 | | | 64 | mA |
| T_A Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

SN54BCT126A, SN74BCT126A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCBS252A – SEPTEMBER 1988 – REVISED APRIL 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54BCT126A | | | SN74BCT126A | | | UNIT |
|-----------|--------------------|--------------------------|-------------|------|------|-------------|------|------|---------|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| V_{IK} | $V_{CC} = 4.5 V$, | $I_I = -18 mA$ | | | -1.2 | | | -1.2 | V |
| V_{OH} | $V_{CC} = 4.5 V$ | $I_{OH} = -3 mA$ | 2.4 | 3.3 | | 2.4 | 3.3 | | V |
| | | $I_{OH} = -12 mA$ | 2 | 3.2 | | | | | |
| | | $I_{OH} = -15 mA$ | | | | 2 | 3.1 | | |
| V_{OL} | $V_{CC} = 4.5 V$ | $I_{OL} = 48 mA$ | | 0.38 | 0.55 | | | | V |
| | | $I_{OL} = 64 mA$ | | | | 0.42 | 0.55 | | |
| I_I | $V_{CC} = 0$, | $V_I = 7 V$ | | | 0.1 | | | 0.1 | mA |
| I_{IH} | $V_{CC} = 5.5 V$, | $V_I = 2.7 V$ | | | 35 | | | 25 | μA |
| I_{IL} | $V_{CC} = 5.5 V$, | $V_I = 0.5 V$ | | | -20 | | | -20 | μA |
| I_{OZH} | $V_{CC} = 5.5 V$, | $V_O = 2.7 V$ | | | 50 | | | 50 | μA |
| I_{OZL} | $V_{CC} = 5.5 V$, | $V_O = 0.5 V$ | | | -50 | | | -50 | μA |
| $I_{OS}‡$ | $V_{CC} = 5.5 V$, | $V_O = 0$ | -100 | | -225 | -100 | | -225 | mA |
| I_{CCH} | $V_{CC} = 5.5 V$, | Outputs open | | 21 | 33 | | 21 | 33 | mA |
| I_{CCL} | $V_{CC} = 5.5 V$, | Outputs open | | 35 | 51 | | 35 | 51 | mA |
| I_{CCZ} | $V_{CC} = 5.5 V$, | Outputs open | | 5 | 10 | | 5 | 10 | mA |
| C_i | $V_{CC} = 5 V$, | $V_I = 2.5 V$ or $0.5 V$ | | 4 | | | 4 | | pF |
| C_o | $V_{CC} = 5 V$, | $V_O = 2.5 V$ or $0.5 V$ | | 9 | | | 9 | | pF |

† All typical values are at $V_{CC} = 5 V$.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 5 V$, $C_L = 50 pF$, $R_1 = 500 \Omega$, $R_2 = 500 \Omega$, $T_A = 25^\circ C$ | | | $V_{CC} = 4.5 V$ to $5.5 V$, $C_L = 50 pF$, $R_1 = 500 \Omega$, $R_2 = 500 \Omega$, $T_A = MIN$ to MAX § | | | | UNIT |
|-----------|--------------|-------------|---|-----|-----|--|------|-------------|------|------|
| | | | BCT126A | | | SN54BCT126A | | SN74BCT126A | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | Y | 1.5 | 3.6 | 4.9 | 1.5 | 5.6 | 1.5 | 6.3 | ns |
| t_{PHL} | | | 2.7 | 5.3 | 6.9 | 2.7 | 7.7 | 2.7 | 7.4 | |
| t_{PZH} | OE | Y | 2.6 | 4.8 | 6.4 | 2.6 | 7.2 | 2.6 | 7.9 | ns |
| t_{PZL} | | | 3.7 | 6.4 | 8.3 | 3.7 | 10.5 | 3.7 | 10 | |
| t_{PHZ} | OE | Y | 3.2 | 6.6 | 8.2 | 3.2 | 9.6 | 3.2 | 10 | ns |
| t_{PLZ} | | | 3.4 | 6.5 | 8 | 3.4 | 12.3 | 3.4 | 10.7 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



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PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-9088901M2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-9088901MCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| 5962-9088901MDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SN54BCT126AJ | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SN74BCT126AD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT126ADE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT126ADG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT126ADR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT126ADRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT126ADRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74BCT126AN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74BCT126ANE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SNJ54BCT126AFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54BCT126AJ | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SNJ54BCT126AW | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74BCT126ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74BCT126ADR | SOIC | D | 14 | 2500 | 346.0 | 346.0 | 33.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE

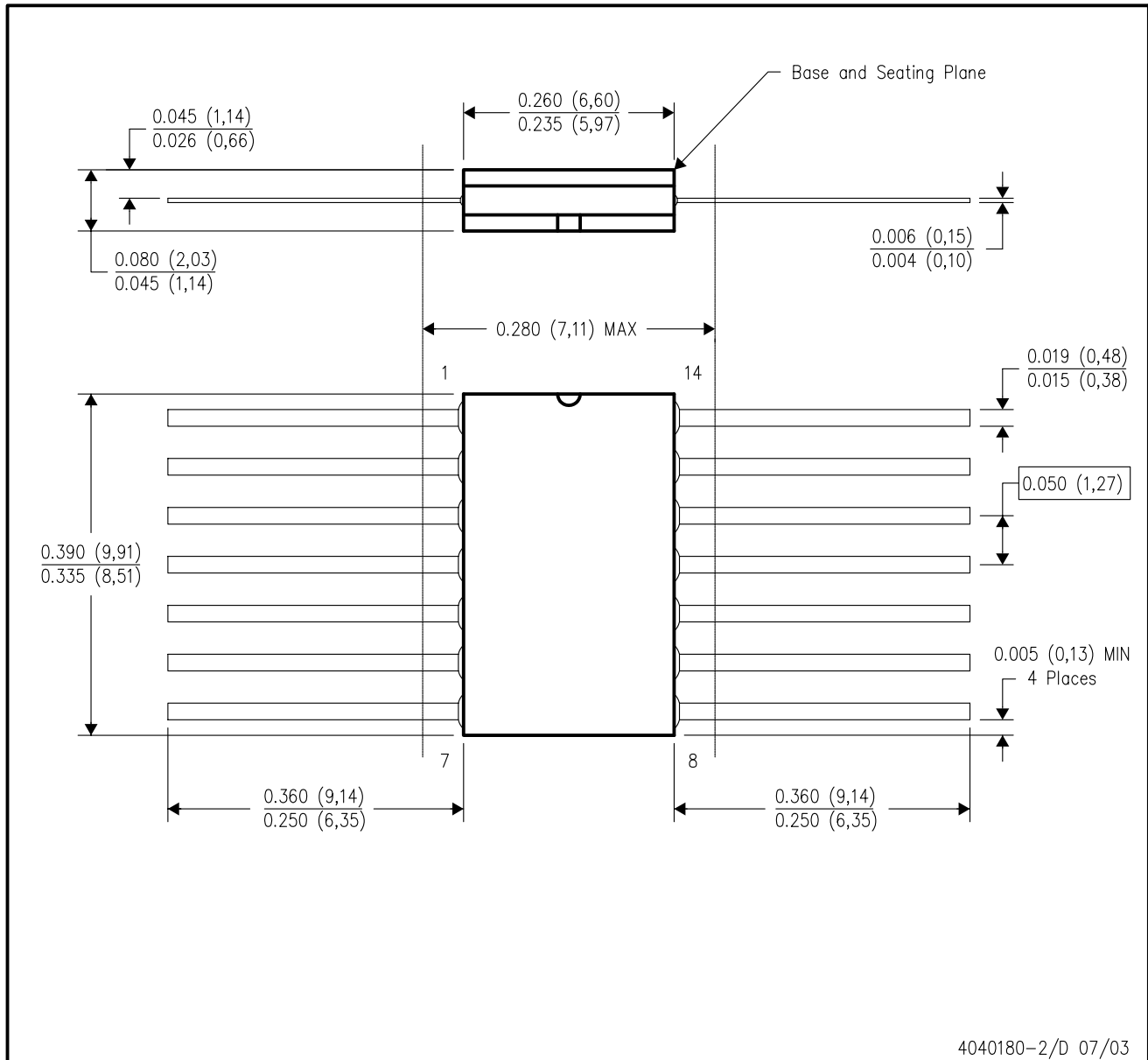


4040047-3/H 11/2006

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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